SYSTEM SUPPORT DIRECTIVE

ASR9 SSM-ASR9-012

6310

System Support Modification

WEATHER SYSTEMS PROCESSOR INTERFACE TO THE ASR-9

Highlights

- AP Suppressed 6LVWX
- +MICROBURST
- +GUST FRONT

06/19/2003

1. PURPOSE. This System Support Modification (SSM) provides authorization to the installation of backplane wiring to the Airport Surveillance Radar-9 (ASR9) to accommodate Lincoln Lab's new Weather Systems Processor (WSP). The Sensitivity Time Control Current Altitude-Low (STC/CAL) Generator Circuit Card Assembly (CCA) must be replaced to accommodate the backplane wiring changes. It authorizes the changes to the ASR9 waveguide hardware components. This modification encompasses changes necessary for the standard WSP hardware interface in the ASR-9 radar.

2. DISTRIBUTION.

a. This SSM is distributed to selected offices and services within Washington headquarters, the William J. Hughes Technical Center, the Mike Monroney Aeronautical Center, regional Airway Facilities divisions, and Airway Facilities field offices having the following facilities/equipment: ASR-9.

b. An electronic version and distribution report of this SSM is available on an Intranet site located at **http://aos-ext.amc.faa.gov/** under the "Technical Documentation" heading.

c. To obtain additional hard copies of this publication, contact Printing & Distribution Team, AMI-700B, at (405) 954-3771.

3. WITHDRAWALS. None.

4. REFERENCES.

a. 6310.19 ASR-9 Maintenance Handbook

b. TI 6310.24 ASR-9 System Field Maintenance

c. TI 6310.25 Transmitter Channel A/B (Unit 16)

d. TI 6310.26 Radar Receiver/Processor Channel A (Unit 2) and Radar Receiver/Processor Channel B (Unit 5)

e. TI 6310.27 ASR-9 Remote Monitoring Subsystem (Unit Three)

DISTRIBUTION: Selected Airway Facilities Field and Regional Offices, ZAF-605

INITIATED BY: AOS-270

f. TI 6310.28 ASR-9 Weather Receiver/SCIP (Unit Four)

g. TI 6310.36 Standard Local Site Wiring Diagram and Lists

h. Configuration Control Decision (CCD) No. N22950 ASR-9 Maintenance Technical Handbook Update, 6310.19A.

5. BACKGROUND. The WSP is an enhancement for the Federal Aviation Administration's (FAA) Airport Surveillance Radar-9 (ASR-9). It provides Doppler estimates of low-altitude winds that are used to automatically alert controllers and pilots to the presence of microburst and gust front wind shear phenomena. The WSP also generates six-level weather reflectivity maps that suppress ground clutter breakthrough induced by Anomalous Propagation (AP). Scan-to-scan tracking of storm cells and gust fronts provides estimates of their velocity, as well as 10- and 20-minute predictions of future gust front positions. The output of the WSP is presented on a Graphics Situation Display (GSD) for Terminal Radar Approach Control (TRACON) and Air Traffic Control Tower (ATCT) supervisors. Tower local controllers are provided wind shear alert messages on alphanumeric "ribbon" displays, for relay to pilots verbatim. These displays are similar to those used to depict Terminal Doppler Weather Radar (TDWR) output. Thus, the WSP provides comparable tactical information on microburst activity and strategic information for managing airspace and runway configurations at medium-density airports. This modification provides a standard hardware interface in the ASR-9 for the WSP equipment.

6. APPLICATION. Prior to the installation of the WSP equipment, a pre-installation kit, Part Number (P/N) 7D11412G01, must be installed to provide the necessary interfaces for the WSP equipment. This document contains reference data and instructions for the installation of the WSP pre-installation kit at a standard ASR-9 facility.

Prior to downtime, the installation will require a 20 hour block of time for a two person team to pre-assemble the Intermediate Frequency (IF) and Radio Frequency (RF) modification kits, and install waveguide components in both (Standby) Radar Receiver channels. Trained ASR-9 technicians and a basic knowledge of the ASR-9's architecture is assumed for all modifications to this operational National Airspace System (NAS). The installation of this kit will require approximately 21 hours of system down time with a two-person team. The downtime shall be divided into three 7-hour sessions. One session is allocated for the RIM and IF Receiver (RCVR) kit installation that should be completed prior to backplane wiring. The last two sessions are required for back plane wiring and the weather modification kit installation. Radar and Beacon operation cannot be restored during the installation of this kit. For additional information, refer to the ASR-9 Technical Instruction (TI) Manuals, series 6310.24 through 6310.39. Prior to commencing installation of the pre-installation kit, the ASR-9 system should be fully configured with all previously released EEM chapters installed.

a. Introduction.

The WSP Pre-installation Kit provides for the hardware modifications required for the interface between the WSP radar data processor and the ASR-9. The following subparagraphs identify the subassemblies affected by the modifications in this kit and provide a brief description of the modification.

The WSP utilizes ASR-9 RF signals, timing, triggers, control signals, STC, and target In-phase and Quadrature (I&Q) data to generate its weather product. Radio frequency signals are gathered from the target channel, high and low beam paths (when operating in Linear Polarization (LP) and the weather channel cross-polarized receive path (when in Circular Polarization (CP). The RF signals are then sent to the ASR-9 weather channel receive chain via coaxial RF switches. A

spare IF output on the ASR-9 weather RF receiver (4A3A1) sends data to an outboard Commercial-Off-The-Shelf (COTS) receiver. Here, the IF is digitized and separated into its I&Q components. I&Q data, header information, and timing are output to the WSP radar data processor.

b. Target Channel Waveguide Modifications.

The WSP requires near-simultaneous access to high and low beam receive signals. Therefore, WSP exploits the high/low beam switching mechanism already in place in the ASR-9 to access these receive signals. Modifications to the high and low beam target channel RF receive paths are necessary to accomplish this, as well as monitoring of existing ASR-9 beam switch operation and subsequent slaved control of WSP beam switches.

The microwave waveguide components are augmented to allow high and low beam target channel data to be used by WSP without affecting target channel surveillance. In the low beam, a second Range-Azimuth Gated (RAG) beam switch is installed, that is slaved to the existing ASR-9 low beam RAG beam switch (S2 in Channel A, S3 in Channel B). This low beam switch slaving is accomplished with a small, passive, switch control distribution box. In the high beam, a high-power 3 dB waveguide splitter is added. Appendix 2, paragraph 4 describes the steps to incorporate these modifications.

c. Antenna Waveguide Replacement.

The weather coax cable from the rotary joint to the radar equipment room is replaced with waveguide in order to reduce energy losses in the weather path and provide a higher quality signal for weather processing. Appendix 2, paragraph 10 describes the steps to incorporate these modifications.

d. Global Positioning System (GPS) Antenna Modification.

A GPS antenna is added to time/date stamp the WSP weather information. The antenna will be externally mounted to the radar equipment building. Appendix 2, paragraph 9 describes the steps to incorporate these modifications.

e. Sigmet Processor/RIM Modification.

In order for WSP to obtain the sensitivity required for detection of hazardous weather phenomena within the limitations of the ASR-9 antenna beam pattern and gain, a separate WSP receiver is employed. A COTS product manufactured by Sigmet Corporation, this receiver has the high dynamic range required to accommodate the near-range weather and clutter signal strengths that are encountered in WSP operation. The Sigmet receiver is composed of two parts: an IF receiver and Analog-to-Digital (A/D) portion that is synchronized to the ASR-9's Coherent Oscillator (COHO) frequency, and an outboard processor whose output is weather I&Q. The IF receiver and A/D portion are mounted in the rear of the Weather Receiver/Surveillance and Communication Interface Processor (SCIP) cabinet (Unit 4) and are incorporated as part of the IF modification kit (see Appendix 2, paragraph 6). The Sigmet processor/RIM unit is rack mounted in the Remote Monitoring Subsystem (RMS) cabinet (Unit 3). Cables are installed to complete the interface. Appendix 2, paragraph 7 describes the steps to incorporate these modifications.

f. Processor Modification.

To obtain additional sensitivity, WSP employs a different STC curve that is applied at all times when WSP is on-line. To accomplish this requirement, the Weather Receiver/SCIP cabinet (Unit 4) receives a new STC circuit card installed in place of the existing circuit card. In addition, the modification includes deletions and additions to the backplane wiring and interface cable additions. Appendix 2, paragraph 7 describes the steps to incorporate these modifications.

g. Weather Channel Modification.

Two RF coaxial switches are installed to make available the appropriate RF high beam, low beam, or CP receive signals to the weather receiver. The two switches are mounted on a plate, which is secured to the waveguide flanges of FL3 and FL4. Eight heliax cables are used to complete the interface. Appendix 2, paragraph 8 describes the steps to incorporate these modifications.

h. IF Modification.

This part of the modification installs the IF digitizer and interface cables employed by the Sigmet receiver discussed in paragraph 6(a). The IF digitizer assembly is installed within the Weather Receiver/SCIP cabinet (Unit 4). Appendix 2, paragraph 5 describes the steps to incorporate these modifications.

i. Pre-installation Cables.

A Pre-installation cable set is provided as part of the Pre-installation kit. This set consists of eight cable groups. Each of the modification sections discussed in paragraphs 6(a) through 6(i) are assigned one of the cable groups. The target channel waveguide modifications do not require a cable group.

7. MATERIALS REQUIRED. The equipment supplied with the WSP pre-installation kit are identified in Table 1, Equipment Supplied.

Table 1. Equipment Supplied

Quantity	Part Number	Nomenclature	Remarks
1	7A11790G01	Preinstallation Cables	(see appendix 3 for detailed parts list of this kit)
2	7D11431G01	ASR-9 RF Mod Kit, TGT	Same as above
1	7D11455G01	Ant. W/G Replacement Kit	Same as above
1	7A11741G01	GPS Antenna Mod Kit	Same as above
1	7D11434G01	ASR-9 Sigmet Processor/RIM Mod Kit	Same as above
1	7D11435G01	ASR-9 Processor Mod Kit	Same as above
1	7D11432G01	ASR-9 RF Mod Kit, WX	Same as above
1	7D11433G01	ASR-9 IF Mod Kit	Same as above

Quantity	Part Number	Nomenclature	Remarks
1	FTS Supplied Kit (Fesler Technical Services, Oklahoma City, Oklahoma)	This kit comes separately and must be present prior to installation)	Past supplied in this kit are listed below
4	VDS1706	Receiver Protector	Varian
3	1063863	Directional Coupler 7"	Continental Microwave MFR66544
100	MS16996-23	3/4" Length Cap Head Screws, Socket, 1/4x28 UNF-3A thread	
200	AN4C12A	1.25" Length Cap Head Screws, 1/4x28 UNF –3A thread	
300	MS35338-139	LOCK WASHERS	
600	AN960C416	FLAT WASHERS	
300	MS35650-3254	NUT, PLAIN, HEX(.250-28)	
1	645A753H06	WAVEGUIDE ASSEMBLY	
1	EFX2-50	W108 CABLE ASSEMBLY	

8. SOURCE OF MATERIALS. Requisition material through the Federal Aviation Administration (FAA) Logistics and Inventory System. KITS SHALL BE ORDERED AND USED ONLY FOR MODIFYING THE EQUIPMENT STATED IN PARAGRAPH 6 OF THIS CHAPTER. Do not order extra kits to ensure a plentiful supply of parts. However, if after receipt of the kits it becomes necessary to obtain certain parts, order the parts separately.

9. SPECIAL TOOLS AND TEST EQUIPMENT REQUIRED. Table 2, Special Installation Tools, lists the special tools needed for the installation, but are not supplied as part of the Pre-installation Kit. Common hand tools and common electrician, wireman, and mechanics tools are not listed. Test equipment is not required for the installation of the Pre-installation kit.

Table 2. Special Installation Tools

Qty	Name	Recommended Type/Model/Spec.	Manufacturer	Remarks
1	Wire Wrap/Unwrap Tool	10F7490 Type BW-928	Newark Electronics	Backplane wiring changes
1	Wire Wrap Bit, 30 awg wire	10F7518 Type SB30MSH-B	Newark Electronics	Backplane wiring changes
1	Wire Wrap Bit, 28 awg wire	10F7517 Type WB28SHM	Newark Electronics	Backplane wiring changes
1	Bit Sleeve	10F7522Type P3032	Newark Electronics	Use w/ wire wrap bits
1	28 awg wire strippers	ST 100-28	O.K. Industries,	Yonkers, N.Y.
1	30 awg wire strippers	ST 100-30	O.K. Industries,	Yonkers, N.Y.
1	Wire Wrap Tool	276-1570	Radio Shack	
1	Torque Wrench, 3/8-inch drive, 0-150 inch pounds	TE12A	Snap-On Tools	For waveguide flange bolts
1	Solder Iron, 25 watts	87F1636 Type 3125	Newark Electronics	IF Mod Kit dc power connections
1	Probe Set (dental picks)	50N045 Type SPC4793	Newark Electronics	For backplane wiring changes
1	Work Light, Fluorescent	50N524 Type 0221	Newark Electronics	
1	Tap (1/4 – 28)	4AHP3	Grainger	
1	Tap Handle	Model 93C Stk. No. 3X039	Starrett Grainger	
1	Bender, cable	2098-5286-54 Model T-1107	Omni Spectra	
1	3/16 Cut-off Allen Wrench			Cut short end to a ½ inch length.

10. PROCEDURE TO BE PERFORMED BY. This modification is to be performed by regional ANI personnel.

11. WHEN MODIFICATION IS TO BE PERFORMED.

a. As soon as practical after receipt of this modification.

b. The following list includes those ASR-9 sites that are scheduled to receive the WSP modification.

WSP Locations	State	LOCID	Region
FAA Academy	OK		
FAA Tech Center	NJ		
Albuquerque	NM	ABQ	ASW
Austin-Bergstrom	TX	BSM	ASW
Norfolk/Virginia Beach	VA	ORF	AEA
Program Support Facility AOS 25	OK		
Portland	OR	PDX	ANM*
Jacksonville	FL	JAX	ASO
Honolulu	HI	HNL	AWP
Buffalo/Niagra Falls	NY	BUF	AEA
Huntsville/Decatur	AL	HSV	ASO*
Grand Rapids	MI	GRR	AGL
San Antonio	TX	SAT	ASW
Syracuse	NY	SYR	AEA
Knoxville	TN	TYS	ASO
Islip/Long Island	NY	ISP	AEA*
Sarasota/Bradenton	FL	SRQ	ASO
Seattle	WA	SEA	ANM*
El Paso-Biggs	TX	ELP	ASW
Ontario	CA	ONT	AWP*
White Plains	NY	HPN	AEA
Madison	WI	MSN	AGL
Los Angeles (South)	CA	LAX	AWP
Birmingham	AL	BHM	ASO
Richmond	VA	RIC	AEA
Greensboro/High Point	NC	GSO	ASO
Harrisburg/Middleton	PA	MDT	AEA*
Des Moines	IA	DSM	ACE
Lubbock-Reese	TX	LBB	ASW
Ft. Wayne	IN	FWA	AGL
Charleston	SC	CHS	ASO
Tucson	AZ	TUS	AWP
Windsor Locks (Hartford)	CT	BDL	ANE
Albany	NY	ALB	AEA
Rochester	NY	ROC	AEA
Cedar Rapids	IA	CID	ACE
Toledo	OH	TOL	AGL

*Sites do not have LLWAS installed
**Production retrofits if necessary

***Northrop Crew with ANI TOR
NOTE: The program sponsor may revise Sites and priorities
12. ESTIMATED TIME REQUIRED. This procedure will require 2 technicians for eighty-two employee hours.

13. DISPOSITION OF SURPLUS PARTS.

a. Return the original ASR-9 STC/CAL/Generator board (P/N 1D21103) to the depot stock for the Non-WSP ASR9 sites.

b. Contact the local hazardous material personnel for disposition of the old receiver protectors. They contain tritium and promethium 147 gas plasma vials.

c. Other material such as the old helix weather cable, directional couplers, waveguide, etc. may be disposed of locally.

14. PROCEDURE. A detailed description of the procedure can be found in Appendix 2, Modification Procedures.

15. TEST AFTER MODIFICATION.

a. Refer to TI 6310.28, paragraph 6.5.1, to verify Cabinet Power Supply voltages are within specification.

b. Perform Fault Insertion Test (FIT) on all ASR-9 equipment using procedure in TI 6310.24, section 3 part 1, volume 1, paragraph 3.3.1.4.

16. RESULT OF MODIFICATION. The WSP modification to the ASR-9 provides the following benefits:

a. (Safety) To warn controllers and pilots of hazardous wind shear and microburst events near runways.

b. (Efficiency) To predict arrival of gust fronts and track storm motion giving a complete picture of current and future terminal area hazardous weather conditions which may impact runway usage.

17. CHANGES TO INSTRUCTION BOOKS. All holders of the Instruction Books are to update their books dated November 2001 with the attached change pages.

PAGE CONTROL CHART

Remove Pages	Dated	Insert Pages	Dated
		SSD TOC	
All Pages	All Dates	All Pages	06/19/2003
		TI 6310.25	
11-3/11-4	undated	11-3/11-4	06/19/2003
		TI 6310.28	
ix	03/26/2003	ix	03/26/2003
x	undated	x	06/19/2003

PAGE CONTROL CHART

Remove Pages	Dated	Insert Pages	Dated
		TI 6310.28 (Continued)	
2-1 through 2-4	undated	2-1 through 2-4	06/19/2003
2-9 through 2-12	undated	2-9 through 2-11	06/19/2003
		2-12	undated
2-15 through 2-22	undated	2-15	06/19/2003
		2-16 and 2-17	undated
	undated	2-18 through 2-21	06/19/2003
		2-22	undated
2-87 and 2-88	undated	2-87	undated
		2-88	06/19/2003
2-91 through 2-94	undated	2-91	06/19/2003
		2-92	undated
		2-93 through 2-93n	06/19/2003
		2-94	undated
2-99 and 2-100	undated	2-99	06/19/2003
		2-100	undated
2-121 and 2-122	undated	2-121	06/19/2003
		2-122	undated
2-129 through 2-132	undated	2-129 through 2-132	06/19/2003
2-135 through 2-138	undated	2-135	undated
		2-136 through 2-137b	06/19/2003
		2-138	undated
2-161 through 2-164	undated	2-161	undated
		2-162	06/19/2003
		2-163	undated
		2-164	06/19/2003
2-171 through 2-174	undated	2-171	undated
		2-172	06/19/2003
		2-173	undated
		2-174	06/19/2003
2-203 and 2-204	undated	2-203	undated
		2-204	06/19/2003
2-243 and 2-244	undated	2-243	undated
		2-244	06/19/2003
2-247 and 2-248	undated	2-247	06/19/2003
		2-248	undated
3-15 and 3-16	undated	3-15	undated
		3-16 through 3-24	06/19/2003
7-23 and 7-24	undated	7-23	undated
		7-24 through 7-24b	06/19/2003
8-13 and 8-14	undated	8-13 through 8-13b	06/19/2003
		8-14	undated
10-1 and 10-2	undated	10-1 through 10-22	06/19/2003

18. CHANGES TO INSTALLATION DRAWINGS. Installation Drawings referenced in this procedure are included in Appendix 3 of this document.

19. CHANGES TO RECORDED DATA. Enter this SSD number, date, chapter and change number on the appropriate FAA Form 6032-1, Airway Facilities Modification Record.

20. ADDRESS CHANGES. Submit facility address, copy count, and additions or deletions to Carrie Batty via email at Carrie.ctr.Batty@faa.gov.

21. CLARIFICATION OR COMMENTS. This chapter will be included in the next revision to the table of contents.

22. RISKS. If changes are not incorporated, unauthorized configuration may degrade the efficiency of the NAS and the ability to maintain operations.

23. FALLBACK PROCEDURES. If changes are not incorporated or unattainable by the installer, contact AOS-200 for field support assistance to clarify procedures and options.

24. STATUS ACCOUNTING. Providing your equipment is listed in the Facility/Service Equipment Profile (FSEP), the Maintenance Organization has opened a Log Equipment Modification (LEM) record in the Maintenance Management System (MMS). Upon completion of this modification, you are required to close the LEM record and change the Maintenance Action Code (MAC) to a "G" if the modification was completed or a "W" if the modification is not applicable. In the event that your equipment is not listed in the FSEP, it is your responsibility to open the LEM record upon receipt/completion of this Modification. Verify that an "N" is in the "REP COD" field to ensure that the log entry will be upwardly reportable to the national database for National MOD Tracking. The data is to be entered into the LEM as follows:

FAC/SERV:	ASR-9
LOC/IDENT:	53AC
SHORT NAME:	SYS
Order No:	SSM-ASR9
Chapter:	012
Change:	HW

25. RECOMMENDATIONS FOR CHANGES. Forward any recommendations for changes to this directive through normal channels to the National Airway Systems Engineering Division, AOS-200, Operational Support.

Richard A. Thoma
Program Director for Operational Support

LIST OF APPENDIXES AND ATTACHMENTS

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ATTACHMENT 2	INSTRUCTION BOOK CHANGES	1

APPENDIX 1. TEST AND EVALUATION GOLD STANDARD CONSIDERATIONS

1. Purpose - This appendix communicates the type of Gold Standard testing that was accomplished on this directive, SSM-ASR9-012. The scope of the testing conducted on this modification and test results are provided. Any additional unique testing or evaluation beyond the normal modification tests, that needs to be conducted during the field installation, is included in the Test Limitation paragraph.

2. Scope - This modification has completed development and systems testing. The system test was conducted at the facility with the system modification baseline at software and hardware modifications through SSM-ASR9-010. Key site testing of this modification was conducted at 2 other facilities with the same baseline as the system test.

3. Results - The system test was conducted at the Albuquerque, MN facility during periods of both peak and normal target load over a period of 24 months with customer representatives validating the user interfaces. All system specialist user screens on the MDTs were exercised and validated. The system test was successful and completed on March 19, 2001.

Key site testing of this modification was conducted at the Austin, TX and Norfolk, VA facilities. These 2 sites were selected to evaluate the modification at facilities that had varying weather conditions. Additionally, both WSP and non-WSP configurations were evaluated.

4. Test Limitations - This modification was tested and validated in all known configurations and no additional unique testing is required.

APPENDIX 2. MODIFICATION PROCEDURES

1. Overview.

NOTE: SSM-ASR9-011 must be completed before the ASR-9 system is placed back in service with the new hardware this kit installs.

The following subparagraphs describe how the WSP Pre-installation Modification Kit equipment is installed at a standard ASR-9 site. Beginning with a description of the installation drawings, work procedures, modification kit inventory, pre-installation coordination, and pre-installation checks, the description moves to the installation of the various modification kits that make up the Pre-installation Modification Kit. The descriptions are brief as it is assumed the work will be performed by skilled installation personnel familiar with the ASR-9 equipment operation. Furthermore, the necessary detail is contained in referenced drawings and documents.

2. Installation Drawings. The drawings listed in the Appendix 3 comprise the basic set of drawings required for installation. The Pre-installation Kit is comprised of a series of individual modification kits, each identified by a separate drawing.

3. General Work Procedures. The work should be performed in a logical sequence that was developed by ANI. The installation should proceed in a manner that permits the work to be completed within scheduled radar down time and not impact operational requirements.

Prior to performing any part of the installation, the operational condition of the radar should be ascertained and document any alarms reported by the RMS. This will ensure that after installation of the modification, any alarms reported and previously documented were not the result of the modification work.

The transmitters must be OFF during the installation of this kit. Place both transmitters OFF in accordance with the applicable Technical Instruction Book (TIB) procedures.

The power to cabinets Unit 3, RMS cabinet, and Unit 4, Weather Receiver/SCIP cabinet, must be OFF during the installation of this kit. Turn OFF ac power to Unit 3 and Unit 4 in accordance with the applicable TIB procedures.

CAUTION: To avoid damage to multivoltage power supply internal circuits, switch BATTERY ON/OFF toggle switch S2 to OFF position before switching MAIN POWER circuit breaker CB1 off.

Electrostatic Discharge Precautions (ESD)

The electronic equipment included in this modification kit and the circuit boards in the radar equipment contain semiconductor devices that can be damaged by electrostatic discharge. Refer to DOD-STD-1686 and DOD-HDBK-263 for proper ESD precautions to use when handling equipment. Failure to use proper ESD precautions could result in damage to ESD sensitive devices. To minimize the possibility of damage when handling the equipment or boards, a grounded wrist strap must be worn at all times when handling ESD sensitive equipment.

a. Configuration Control.
A configuration control list (attached) will be maintained for the installation at each site. The list will identify equipment removed, equipment installed, and if available, WSP site spares.

The components removed and no longer required shall be provided to the site manager for disposition.

b. Minimum Discernible Signal (MDS) Record.
A pre- and post-modification MDS record (attached) for each channel will be completed for each site installation.

c. Pre-installation Coordination.
Before installation begins, the shutdown of the radar equipment must be coordinated with the FAA site management. Twenty-one hours of downtime in three, seven hour blocks will be required during the installation.

Secondary Surveillance Radar (beacon) operation cannot be maintained during installation of this modification kit.

d. Pre-installation Checks.
Before the installation of the modification equipment begins, the following checks are required:

(1) Perform a complete inventory of the pre-installation kit material to ensure all material is available.

(2) Prior to installing the target channel waveguide modification (7D11431G01), record on lines 1-3 of the MDS data sheet (attached), the high beam, low beam, and weather channel Remote Monitoring Subsystem (RMS) Minimum Discernible Signal (MDS) measurement for each channel that is to be modified. Note that the measured channel must be online and stabilized for 15 minutes prior to recording the data. These numbers will be required below for MDS re-calibration following installation.

(3) At the local RMS terminal, access the ALARM REPORTS menu. Observe the ALARM Report's menu for the presence of any existing alarms.

(4) Record all pre-existing alarms on the Pre-installation System Status form (attached).

(5) Equipment failures that will have an impact on the installation or alignment and checkout of the Pre-installation kit must be corrected prior to proceeding with the installation.

4. Standby Radar Receiver Target Channel Waveguide Modifications (7D11431G01, RF Mod Kit, TGT).
Installation of the 3-dB waveguide power splitter, part number (p/n 7A11819H01) in the high beam causes an increase in the dimensions of the entire waveguide run. Portions of the overhead Unistrut™ channel structure may have to be moved to maintain proper support of the waveguide. Specific instructions cannot be provided, as overhead supports will vary slightly from site to site. However, extreme caution should be taken so no waveguide is left unsupported at any time. Because the changes in waveguide dimensions affect both the high and low beams, it is best to remove the existing pieces of waveguide as noted below first, reposition the remaining waveguide, then install the new waveguide sections. The modification should be performed one

channel at a time. All diagrams shown depict a channel A configuration. The channel B waveguide route mirrors that of channel A. Component reference designators refer to channel A, (channel B designators in parentheses).

The parts required for this modification are included in ASR-9 RF Mod Kit, Target, p/n 7D11431G01 and the WSP Supplied Kit from FTS corporation. Verify that all material required is available prior to starting the modification. Item numbers below refer to the Find Nos. in the 7D11431G01 parts list. Some ASR-9 fasteners such as the existing 1 inch 1/4x28 UNF thread (AN4C10A) bolts cannot be discarded, but will have to be recycled to complete this section.

Figure 1 and Figure 2 show the correct installation of the new waveguide components.

WARNING: Before proceeding with the waveguide section make certain the Standby transmitter power is OFF, and then secure the transmitter so it cannot generate microwave energy.

a. Low Beam RAG Switch XSW101 (XSW102) waveguide section:

(1) The strategy proposed in this section provides a method to complete the inside waveguide modifications without requesting downtime. This method uses the Waveguide Pressurization Manifold valves to bleed the Standby Channel's waveguide pressure down, while the Online channel is operating. This method also follows the procedures for waveguide removal and installation in TIB 6310.24 Figure 7.4.1.1 to depressurize and isolate the High Beam and Standby Transmitter channel waveguide. Because an outage will result if existing ASR-9 pressure windows leak, it may be preferable to request downtime to install the inside waveguide components. If downtime is requested for this section, the four waveguide sections shall be pre-assembled prior to the arranged downtime. The isolator HY1 is not available at this time, therefore the low beam sections cannot be completed until the original low beam waveguide section is removed.

First turn off the pressure by closing only the Standby Transmitter channel and High Beam Waveguide valves on the air manifold, then bleed the air from those sections using the needle valve on the manifold, while observing the manifold pressure gauge for any sign of a drop in pressure.

If a drop in manifold pressure is detected, stop the procedure because the air is leaking through a pressure window and this will cause the Online channel to fail. The operation is complete when both sections of waveguide are depressurized, and the manifold pressure is nominal. This action shall isolate the sections of waveguide in the Standby channel, but the Rotary Joint will remain completely pressurized.

(2) Ensure that all waveguide components from tunable filter FL2 (FL1) through LNA AR2 (AR1) are securely supported by Unistrut™ channel. Track the health of the new waveguide component by verifying the MDS readings recorded earlier in the Pre-installation checks (see attached data sheets – Pre-Modification column.) Wait until all the waveguide (High and Low beam) modifications are completed and recheck the MDS before proceeding past step b. Section Equipment Calibration, or installing new software. That is, if a problem originates from the new waveguide architecture, it will be easier to diagnose when only the waveguide components changed.

(3) Remove the section of waveguide between the low beam circulator HY2 (HY1) and the low beam STC unit A6 (A5). This section includes the following four components Directional

Coupler DC4 (DC3), Pressure Window, Isolator HY5 (HY4), Receiver Protector A8 (A7), and a 14" straight WR-284 waveguide section. Save the isolator HY5 (HY4) and Pressure Window for reuse.

> **NOTE: The Directional Coupler and the Isolator Input ports mate as illustrated in Figure 1.(2.). The orientation of the Directional Coupler, Isolator, and Receiver Protector are shown in the shaded regions of Figure 1. (2.). Therefore the orientation of these components does not change from the baseline ASR9 configuration.**

(4) Pre-assemble a replacement waveguide section using the components listed below in Table 1. and the hardware specified in Table 2. Install a parker gasket at each waveguide flange interface except for the flanges where the pressure window provides the mating surface. See Figure 1.(2.) for an assembly drawing of this new section of the low beam waveguide.

Table 1. Low Beam Components List

Item	**Part Number**
New Directional Coupler	1D19766H02
Reuse Pressure Window	645A895H02
Reuse Isolator HY5(HY6)	321R038H02
New Receiver Protector	VDS1706
New RAG ASR9/WSP Low Beam switch	EG0069
S Band Elbow	7A11819H01
New Waveguide Transition to type N coax	645A771H02

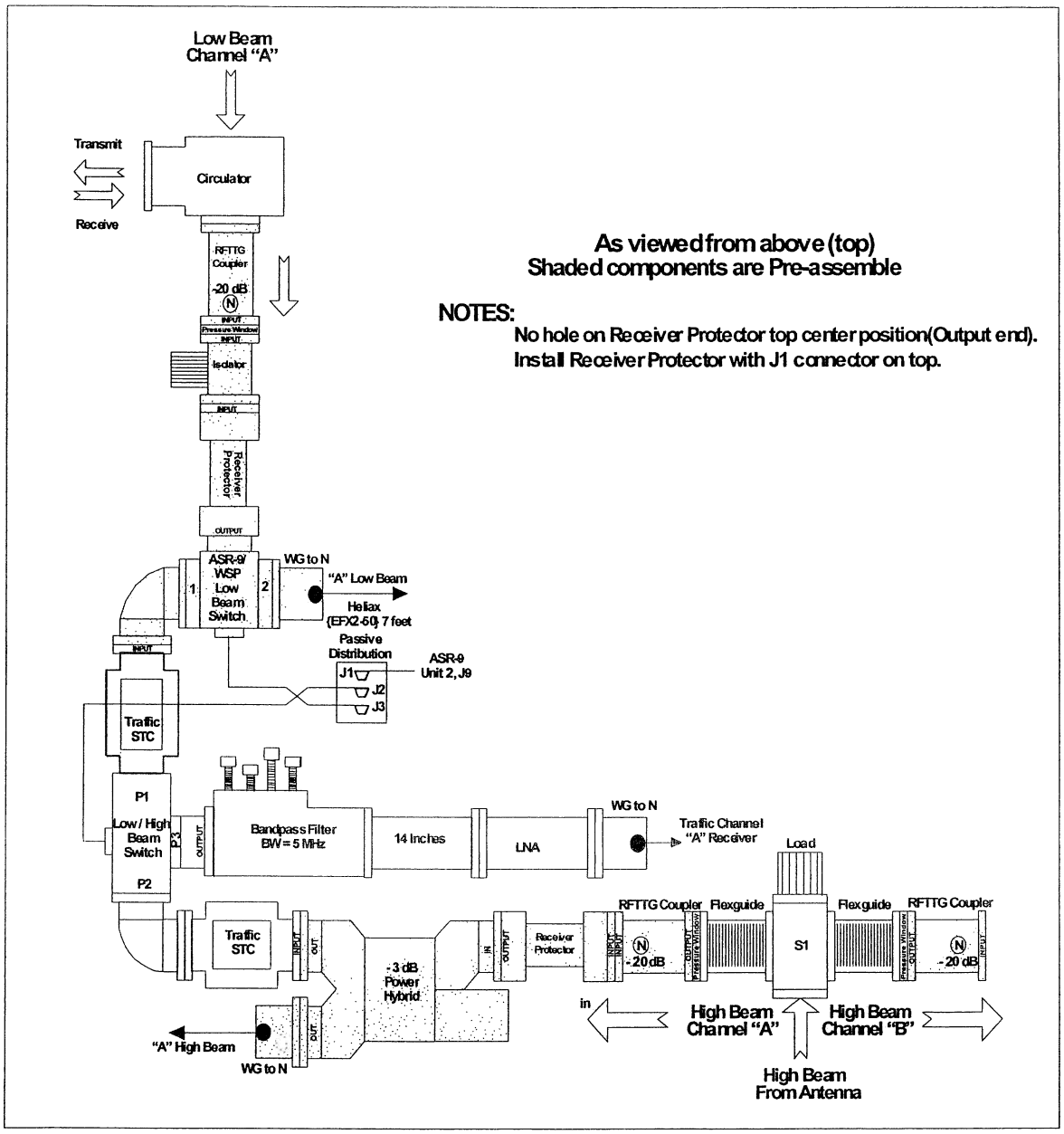
Use Flat Washers AN960C416 and Lock Washers MS35338-139 for all bolts. Follow Table 2. to assemble components with kit hardware.

Table 2. Low Beam Fastener List

Pre-Assemble Mating Flanges	Gasket	Bolts Recommended	Length
New Directional Coupler Input to Isolator HY5(HY6) In	Pressure Window	AN4C12A	1.25"
Isolator HY5(HY6) output to Receiver Protector in	Parker Seal	AN4C10A	1.0"
New Receiver Protector output to Rag Switch output	Parker Seal	AN4C10A	1.0"
New RAG Switch input 1 to S-Band Elbow	Parker Seal	MS16996-23	0.75"
New RAG Switch input 2 to WG Transition to coax	Parker Seal	MS16996-23	0.75"
Tie-In Flanges			
S Band Elbow to Traffic STC	Parker Seal	AN4C12A	1.25"
New Directional Coupler Output to Circulator HY1(HY2)	Parker Seal	AN4C12A	1.25"

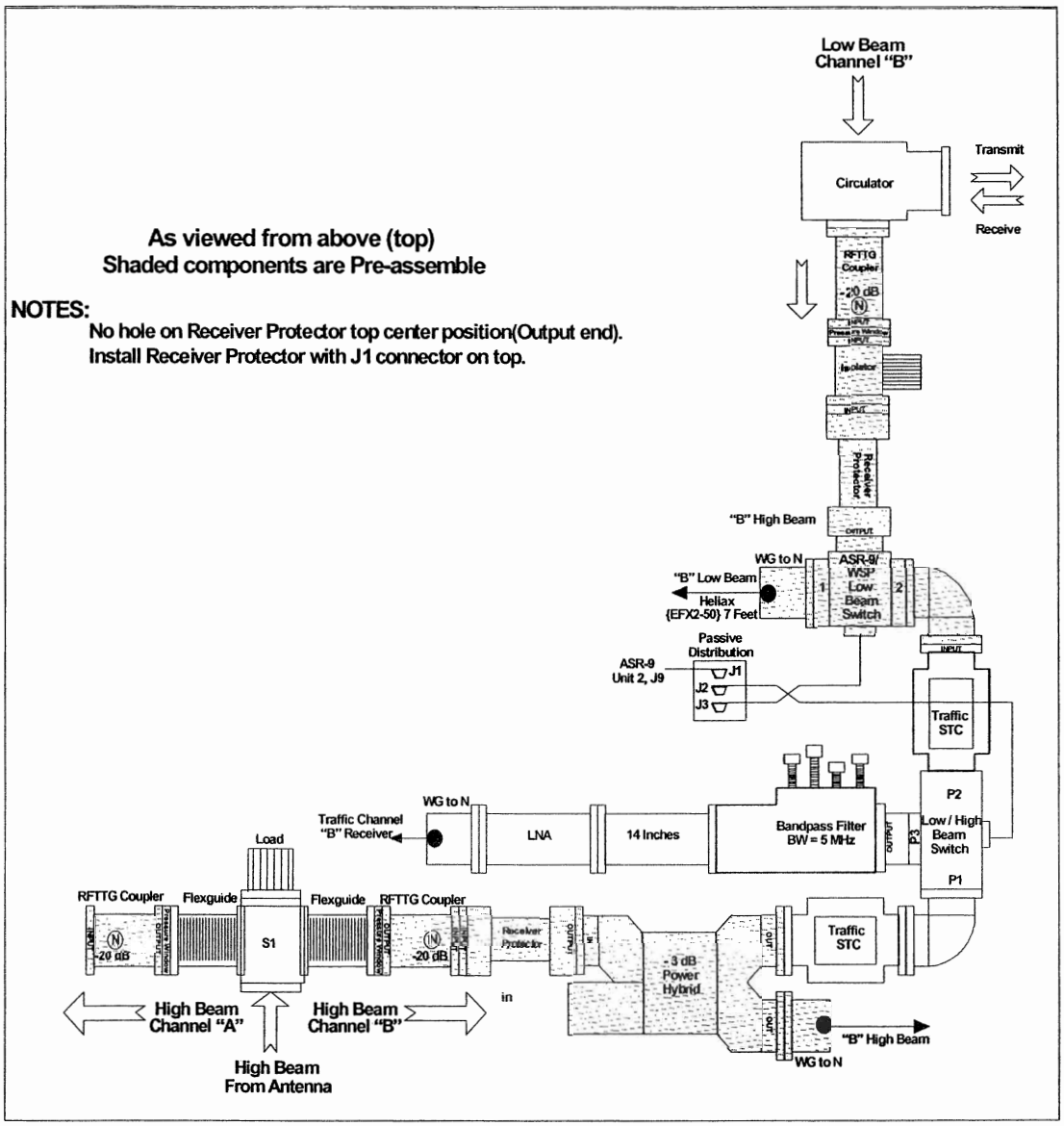
(5) The remainder of this paragraph requires that the waveguide removal and waveguide repositioning portions of the high beam 3-dB waveguide power splitter section installation in paragraph14.d. (2) be completed. Go to step 1 of Appendix 2, paragraph 4 (b) High Beam Replacement Section and continue with installation.

(6) Using ¼ 28 bolts, flat washers, and lock washers (AN4C12A, AN960C416 MS35338-139), attach the pre-assembled section directional coupler output end to the ASR9 waveguide structure at the Circulator HY1(HY2) as shown in Figure 1.(2.) (shaded). Install a gasket (Item 12, M24211/2-005) at this waveguide interface, Follow the waveguide flange bolt torquing sequence requirements outlined in the applicable section of TIB 6310.24.



ASR-9 TARGET CHANNEL A WAVEGUIDE WITH ADDED WSP HARDWARE

Figure 1. Target Channel A Waveguide Modifications



ASR-9 TARGET CHANNEL B WAVEGUIDE WITH ADDED WSP HARDWARE

Figure 2. Target Channel B Waveguide Modifications

(7) Using caps, flat washers, and lock washers (MS16996-23, AN960C416 MS35338-139), attach the pre-assembled section S Band Elbow end to the Traffic STC ASR9 waveguide structure as shown in Figure 1.(2.) (shaded). Install a gasket (item 12, M24211/2-005) at this waveguide interface. Follow the waveguide flange bolt torquing sequence requirements outlined in the applicable section of TIB 6310.24.

(8) Record the serial numbers for the installed H-bend, RAG beam switch, 4" straight waveguide, and the waveguide-to-coax transition on the configuration control form. Record the serial numbers of the on-site spares for these items on the configuration control form.

(9) Purge and pressurize the waveguide system in accordance with appropriate TIB procedures.

(10) Verify the waveguide is properly supported by the Unistrut™ channel, then remove the twine being used for temporary support. Go to Appendix 2, paragraph 4 (b) step 4 of the High Beam Waveguide Replacement section to complete the installation of the waveguide.

b. High Beam Waveguide Replacement Section:

Support high beam receiver protector A2 (A1) at its interface with the high beam test target coupler DC2 (DC1) using a piece of twine tied off securely to the overhead Unistrut™ channel. Assemble a replacement waveguide section with the following components as illustrated in Figure 1.(2.).

(1) Ensure that all waveguide components from tunable filters FL2 (FL1) through LNA AR2 (AR1) are securely supported by Unistrut™ channel. Support high beam receiver protector A2(A1) at its interface with the high beam test target coupler DC2(DC1) using a piece of twine tied off securely to the overhead Unistrut channel.

(2) Remove both the high beam receiver protector A2(A1) and the 14" straight waveguide section between the high beam directional coupler DC2 (DC1) and STC unit A4 (A3).

(3) Before proceeding further, go to section 14.d(1) **(2) Low Beam RAG Switch XSW101** (XSW102) and complete steps 6 through 10 for the waveguide replacement portion of the low beam RAG switch installation.

(4) Pre-assemble a replacement waveguide section using the components listed below in Table 1. and the hardware specified in Table 2. Both the Old and New style of directional couplers are listed in Table 3. and Table 4. because it is necessary to use an old style in one channel and a new style in the other channel. This is the only way to maintain a good waveguide fit given the asymmetry position of the high beam waveguide switch between the channels. See Figure 1.(2.) for detail assembly instructions of this low beam waveguide replacement section.

Table 3. High Beam Components List

Item	Part Number
New Directional Coupler (channel A) Old Directional Coupler (channel B)	1063863 (1D19766H02)
Old Pressure Window	645A895H02
New Receiver Protector	VDS1706
New 3-db. Splitter	1062891-2
S-Band (WG to N) Coax Transition	645A771H02

Table 4. High Beam Fastener List

Pre-Assemble Mating Flanges	Gasket	Bolts	*Length*
Directional Coupler Output to Receiver Protector Input	Parker Seal	AN4C10A	*1.0 "*
Receiver Protector output to 3db Splitter Input	Parker Seal	MS16996-24	*1.0 "*
3db Splitter to Transition (WG to N)	Parker Seal	AN4C12A	*1.25 "*
Tie-In Flanges			
Directional Coupler to Flexguide	Pressure Window	2" COTs Bolts	*≤ 2.0 "*
3db Splitter to STC unit	Parker Seal	AN4C12A	*1.25 "*

(5) Reposition the remaining waveguide assembly to accommodate the new section of waveguide.

(6) Using ¼-28 caps, nuts, flat washers, and lock washers (Items 8-11, MS35650-3254, AN960C416, AN4C12A, MS16996-3) attach the new 3-dB waveguide splitter XPS101 (XPS102) (Item 2, to the STC unit as shown in Figure 1.(2.) (shaded). Install a gasket (Item 12, M24211/2-005) at each waveguide interface. Follow the waveguide flange bolt torquing sequence requirements outlined in the applicable section of TIB 6310.24.

(7) Verify that the orientation of the input ports for both the new Receiver Protector and the new 3-db Waveguide Splitter will face the antenna (see Figure 1.(2.)). Because the MDS signal is injected into the waveguide, it is used as an injection port and not as a measuring device. Therefore, the coupler is used to direct the signal into the waveguide, so it must reverse direction and the waveguide input will face the 3-db splitter.

(8) Attach the output port of the directional coupler to the Flexguide as shown in Figure 1.(2.) (shaded). Using the ¼-28 bolts, nuts, flat washers, and lock washers (Item 8, MS35650-3254; Item 9, AN960C416; Item 11, IMS16996-23TEM 18.) Follow the waveguide flange bolt torquing sequence requirements outlined in the applicable section of TIB 6310.24.

(9) Record the serial numbers for the installed 3-dB waveguide splitter on the configuration control form. Record the serial numbers for the on-site spares for these items on the configuration control form.

c. Beam Switch Control Distribution Box XJB101 (XJB102):

(1) Using the hex cap screws, spring nut, flat washer, and lock washer (Items 14-17, MS35307-360, P1008, NAS1149C0663R, MS35338-141), secure the beam switch control distribution box XJB101 (XJB102) (Item 7, 7A11871H01) to the Unistrut™ channel above the left (right) side of the ASR-9 Radar Receiver/Processor Unit 2 (Unit 5).

(2) Disconnect the existing cable W506 (W520) from the low/high beam switch, S2J1 (S3J1). This is the switch control cable from target channel A, Unit 2 (target channel B, unit 5).

(3) Connect the cable into the input port XJB101J1 (XJB102J1) of the beam switch control distribution box.

(4) Apply new labels (provided) to both ends of the rerouted cable W1401 (W1402), formerly W506 (W520).

(5) Route cable W1403, p/n 7A11903G07, (W1404, p/n 7A11903G08) from XJB101J2 (XJB102J2) to S2J1 (S3J1).

(6) Route cable W1405, p/n 7A11903G09, (W1406, p/n 7A11903G10) from XJB101J3 (XJB102J3) to XSW101J1 (XSW102J1).

5. ASR-9 IF Modification Kit (7D11433G01).
The parts required for this modification are included in the ASR-9 IF Mod Kit, p/n 7D11433G01, with the exception of the IF digitizer (Item 2, 7A11800H03), which is shipped with the ASR-9 Sigmet Processor/RIM Modification kit, p/n 7D11434G01. Verify that all material required is available prior to starting the modification. Item numbers below refer to the Find Nos. in the 7D11433G01 parts list. The cables referenced below are in the Preinstallation Cable kits, p/n 7A11790G08 and p/n 7A11790G09 included in the 7D11433G01 kit.

NOTE: Refer to drawing 7D11433 while installing this kit. Some of the kit items may be installed on the ASR9-003.9.1 panel prior to delivery. Assemble as much of the kit as possible before installing the ASR9-003.9.1 panel in the ASR-9 Unit 4 cabinet. This includes most of the assembly shown on sheets 1 and 2 of the drawing. Install the default attenuator (AT1) as shown; it may change during the calibration process. This panel assembly is referenced as 4A12.

a. Refer to drawing 7D11433, sheet 1. Pre-assemble the A12 panel as shown prior to scheduled downtime.

b. Before proceeding, make certain the cabinet ac power and dc power has been turned OFF in accordance with applicable TIB procedures. To avoid damage to multivoltage power supply internal circuits, switch BATTERY ON/OFF toggle switch S2 to OFF position before switching MAIN POWER circuit breaker CB1 off.

c. Refer to drawing 7D11433, sheet 2, right-hand side. Install the 115 vac cover (Item 7, ASR9-003.9.2) over the ac voltage terminals of the IF digitizer (Item 2, 7A11800H03) as shown.

d. Install the power splitter bracket (Item 8, ASR9-003.9.3) and power divider 4A3A3 (Item 204, HJ-22010) to the 4A3 panel as shown on sheet 3 of the drawing.

e. Install the default attenuator as shown in the drawing. This attenuator may be replaced with another value during calibration.

f. Secure the 4A12 IF Receiver Assembly in ASR-9 Unit 4.

g. Make the +15V dc power connections to 4A12TB1 as shown on sheet 2.

h. Install the following semi-rigid coax cables from the 7A11790G09 Preinstallation Cable kit:

- ❑ W2707, p/n 7A11902H62
- ❑ W2709, p/n 7A11902H63
- ❑ W2710*, p/n 7A11902H64
- ❑ W2712, p/n 7A11902H65

*Attenuator A3AT1 must be removed from A3S1-J2 to permit connection of W2710 to A3S1. Discard A3AT1.

The WSP System Interconnect Schematic (7J10022) may be used for reference.

NOTE: The Sigmet IF digitizer connects to the Sigmet Processor/RIM, which has not been installed prior to this step. The coax cables and markers are in the 7A11790G08 Preinstallation Cable kit. The fiber optic cable is shipped with modification kit p/n 7D11434G01 (ASR-9 S igmet Processor/RIM Modification kit).

i. Install and terminate one end of the following cables to the IF digitizer and route the other end through the cutouts in the back of the cabinets into Unit 3. They will be connected after 7D11434G01, ASR-9 Sigmet Processor/RIM Modification kit is installed:

- ❑ W2706, p/n 7A11902H61
- ❑ W2201*, p/n 7A11902H68

*Cable is received with the Sigmet processor without cable markers. Apply cable markers included with cable group p/n 7A11790G08.

Refer to sheet 2 of drawing 7D11433. Connect the AC power cord into A19 J4 in the RMS cabinet (Unit 3). The power cord supplied will need to be stripped back and new lugs applied to the cable ends for the terminal connections. Note that turning off the cabinet breaker does not insure that power is off at A19 J4.

6. ASR-9 Sigmet Processor/RIM Modification Kit (7D11434G01).
The parts required for this modification are included in the ASR-9 Sigmet Processor/RIM Modification Kit, p/n 7D11434G01. Verify that all material required is available prior to starting the modification. Item numbers below refer to the Find Nos. in the 7D11434G01 parts list. The cables referenced below are in the 7A11790G04 and 7A11790G08 Preinstallation Cable kits included in 7D11434G01 and 7D11433G01, respectively.

NOTE: The Sigmet IF Digitizer and Processor/RIM (Item 2, 7A11800H01) are packed in the same box. The RIM and RVP7 Printed Wiring Assemblies (PWA) that go in the Processor/RIM chassis are removed for shipping. The PWAs will be installed in the Processor/RIM later in this procedure.

Refer to drawing 7D11434 while installing this kit. When installing cables, refer to drawing 7J10022, WSP System Interconnect Schematics.

a. Rotate Unit A20 in RMS cabinet, Unit 3, as shown on sheets 1 and 3 of the drawing. This may require moving existing cable bundles in the area to insure best routing, given limited cable length.

b. Install the filler panel (Item 4, ASR9-003.10.1) on the Processor/RIM as shown on sheet 2 of the drawing.

c. Install the Processor/RIM in RMS cabinet, Unit 3, as shown on sheets 1 and 3 of the drawing.

d. Remove the front cover of the Processor/RIM and install the RIM and RVP7 PWAs. Use care to line the PWAs up with the edge guides such that the PWA connectors mate properly with the chassis connectors. The boards and slots are labeled to indicate which board goes in which slot. Record the serial numbers of the PWAs and Processor/RIM chassis on the configuration control list.

e. Connect the fiber optic cable to the front of the RVP7 PWA.

f. Replace the front cover on the Processor/RIM.

g. Connect cables W2706, p/n 7A11902H61, and W2201, p/n 7A119902H68, to the connector panel on the rear of the Processor/RIM per the cable markers. If slide latches are installed on the cables connectors, they will have to be removed or the cable connectors will not mate properly. Roll up the extra length of these cables and tie off to the side of the cabinet.

h. Verify that the power switch on the Processor/RIM is in the OFF position. Plug the AC power cord provided with the Processor/RIM into power outlet A19.

i. The following cables, included in the 7A11790G04 Preinstallation Cable kit, provide the interface between the ASR-9 and the WSP RDP cabinet. Refer to system interconnect schematic, 7J10022:

- ❑ W3101 p/n 7A11902H50
- ❑ W3401 p/n 7A11902H51 **<u>Do not attach the ferrite core assembly until after the cable is installed</u>.**

j. Remove shell from P1 to permit the cables to pass through an opening (labeled J8) at the top of Unit 4 and connect to the rear of the Processor/RIM. The W3401 connector cover assembly and ferrite core assembly will need to be off for the connector to fit through the top of the cabinet. The other ends of these 2 cables will be connected when the WSP RDP cabinet is installed.

NOTE: Due to unique site requirements and local NCP's the opening (labeled J8) on the top of Unit 4 may have been used for other purposes. In this case see appendix for locating, drilling and punching a new hole on the top of Unit 4, the Weather/SCIP cabinet.

7. ASR-9 Processor Modification Kit (7D11435G01).
The parts required for this modification are included in ASR-9 Processor Modification Kit, p/n 7D11435G01. Verify that all material required is available prior to starting the modification. Item numbers below refer to the Find Nos. in the 7D11435G01 parts list. The cables referenced below are in the 7A11790G05 Preinstallation Cable kit included in 7D11435G01.

Wire wrap and unwrap tools are required for this part of the modification.

NOTE: Extreme care must be taken when deleting and adding wires in the backplane. Errors are extremely hard to find. Broken wire wrap pins are very difficult to replace.

a. Before proceeding, make certain the cabinet ac power and dc power has been turned OFF in accordance with applicable TIB procedures on the entire ASR-9 system. To avoid damage to multivoltage power supply internal circuits, switch BATTERY ON/OFF toggle switch S2 to OFF position before switching MAIN POWER circuit breaker CB1 OFF.

b. **Delete** the following wires identified in Table 5., from the ASR-9 Weather Receiver/SCIP Unit 4 A4 backplane. The connector interface at position **J125** must be removed in order to delete or add wires to the backplane pins.

Table 5. ASR-9 (Unit 4 A4) Backplane Wire Deletions

Deleted Wires				
FROM		TO		Name
Symbol	Pin	Symbol	Pin	
A123	B15	A120	B15	AIOWC
A123	C02	A123	C03	STCCALGNDC
A123	C02	A123	A01	STCCALGNDC
A120	A61	J125	09	BEAMSEL+
A120	A62	J125	10	BEAMSEL-
A215	A21	A217	A21	SDATOUT0A+
A215	A22	A217	A22	SDATOUT0A-
A215	A23	A217	A23	CLKOUT0A+
A215	A24	A217	A24	CLKOUT0A-
A215	A25	A217	A25	SDATOUT1A+
A215	A26	A217	A26	SDATOUT1A-
A215	A27	A217	A27	CLKOUT1A+
A215	A28	A217	A28	CLKOUT1A-

c. **Add** the wires shown in Table 6. to the ASR-9 Weather Receiver/SCIP 4A4 backplane.

NOTE: All additions are 30awg wire (Item 2, 10F7567) except the additional grounds (SWGND) and voltages (+15V), which are 28 AWG, wire (item 3, 10F7607).

Table 6. ASR-9 (Unit 4 A4) Backplane Wire Additions

ADDED WIRES				
FROM		TO		
Symbol	Pin	Symbol	Pin	Name
A123	B61	J125	09	BEAMSEL+
A123	B62	J125	10	BEAMSEL-
A123	A39	A123	B39	STCCALGNDC
A123	A40	A123	A39	STCCALGNDC
A123	B51	A120	A61	BEAMONHI+
A123	B52	A120	A62	BEAMONHI-
A123	B26	A120	B15	AIOWC-
A216	C06	A123	B55	RPGTXD+
A216	C07	A123	B56	RPGTXD-
A216	C08	A123	B57	2TESTDM+
A216	C09	A123	B58	2TESTDM-
A216	C91	A123	A73	WSP_EN
A216	A04	A216	B08	BAUDCLK+
A216	A05	A216	B09	BAUDCLK-
A123	A73	A119	C94	WSP_EN
A123	B63	A121	B85	CHA-/B+
A123	B64	A121	B86	CHA-/B-
A123	B65	A121	B87	SYSLP/CP-+
A123	B66	A121	B88	SYSLP/CP--
A123	B67	A121	B74	CHAANTBM+
A123	B68	A121	B75	CHAANTBM-
A123	B69	A121	C87	CHBANTBM+
A123	B70	A121	C88	CHBANTBM-
A123	C87	A124	C86	GDWDWA+
A123	C88	A124	C87	GDWDWA-
A123	C35	A124	C84	GDWDWB+
A123	C36	A124	C85	GDWDWB-
A123	C31	A217	A21	WSP_DATA+
A123	C32	A217	A22	WSP_DATA-
A123	C33	A217	A23	WSP_CLOCK+
A123	C34	A217	A24	WSP_CLOCK-
A217	A21	A217	A25	WSP_DATA+
A217	A22	A217	A26	WSP_DATA-
A217	A23	A217	A27	WSP_CLOCK+
A217	A24	A217	A28	WSP_CLOCK-

Table 6. ASR-9 (Unit 4 A4) Backplane Wire Additions (continued)

Added Wires				
FROM		TO		
Symbol	Pin	Symbol	Pin	Name
A123	C27	A125*	B11	SXSW104(0)_I+
A123	C28	A125*	C11	SXSW104(0)_I-
A123	B27	A125*	B12	SXSW104(1)_I+
A123	B28	A125*	C12	SXSW104(1)_I-
A123	A13	A125*	B01	XSW103(0)_O+
A123	A14	A125*	C01	XSW103(0)_O-
A123	A15	A125*	B02	XSW103(1)_O+
A123	A16	A125*	C02	XSW103(1)_O-
A123	A25	A125*	B03	SXSW103(0)_I+
A123	A26	A125*	C03	SXSW103(0)_I-
A123	A27	A125*	B04	SXSW103(1)_I+
A123	A28	A125*	C04	SXSW103(1)_I-
A123	A21	A125*	B09	XSW104(0)_O+
A123	A22	A125*	C09	XSW104(0)_O-
A123	A23	A125*	B10	XSW104(1)_O+
A123	A24	A125*	C10	XSW104(1)_O-
A114	A46	A125*	B06	+15V
A114	B46	A125*	C06	+15V
A114	C46	A125*	B14	+15V
A114	C46	A125*	C14	+15V
A114	A50	A125*	B08	-15V
A114	B50	A125*	B16	-15V
A125*	A01	A125*	B07	SWGND
A125*	A01	A125*	C07	SWGND
A125*	A10	A125*	B15	SWGND
A125*	A10	A125*	C15	SWGND

Tips

- Perform wire wraps over 2 nights. Turn off entire ASR-9 system before attempting wire wraps.
- The deletes and the first page of the adds shall be performed on the first night. U90 (see SSM011) in the LSCI-2 boards (A215 & A217), and the WX STC card (A123) must be changed on the first night with the first set of wire wraps. There is no quick restoration. The work must be finished to restore service.
- Perform wraps to A125, 2nd page of adds, on second night. Service can be restored in about 10 minutes.
- Use the transmitter extender board (will not work to check slot A123) and 4-bay extender board (place in slot A123) to check wire wrap connections. Remove cards from front insert extender and check for short.
- Check each wrap for correctness. **Redo if needed, there is always time to do it right**.
- Use dental pick to weave added wires under existing wires.

- When wiring to the bottom bucket to the top, start with A216 then weave the wire up to A123.
- When deleting wires, insert a piece of paper under the pin you're removing the wire from to keep broken wires from falling into the pins below.

On connector A125, make wire wraps as low as possible to permit the installation of connector P1 of cable W2401.

d. Install switch matrix control cable W2401, p/n 7A11903G12, between backplane connector 4A125 and cabinet connector 4A5J23 (remove slide lock hardware on cable connector). This 50-pin cable connects to the slot A125 of the Weather Receiver/SCIP backplane. Pin 1 (identified by a brown insulated wire) of W2401/P1 connector is attached (pushed on) to the backplane connector pins at pin C01 (see figure 4). Connector P2 of W2401 is connected to 4A5J23 (Unit 4 bulkhead connector J23 on panel A5). The ribbon cables follow the color code convention with pins 1,2,3... follows brown, red, orange ...etc.

e. Install cable W2403, p/n 7A11903G14, between backplane connector 4A123 and J1 of the Sigmet Processor/RIM in RMS cabinet, Unit 3 (remove slide lock hardware on cable connector J1). Notice, in Figure 4., the rectangle containing pins B1 thru B25 and pins C1 thru C25 of the backplane. This rectangle represents where the W2403/P1 connector is attached (pushed on) to the ASR-9 backplane at the STC card slot (A4A123). Pin 1 (identified by a brown insulated wire) of P1 should align with pin C01.

The cable should pass through the openings between Units 3 and 4, and connect W2403/P2 to 3A21J1 (Sigmet Processor/RIM in Unit 3).

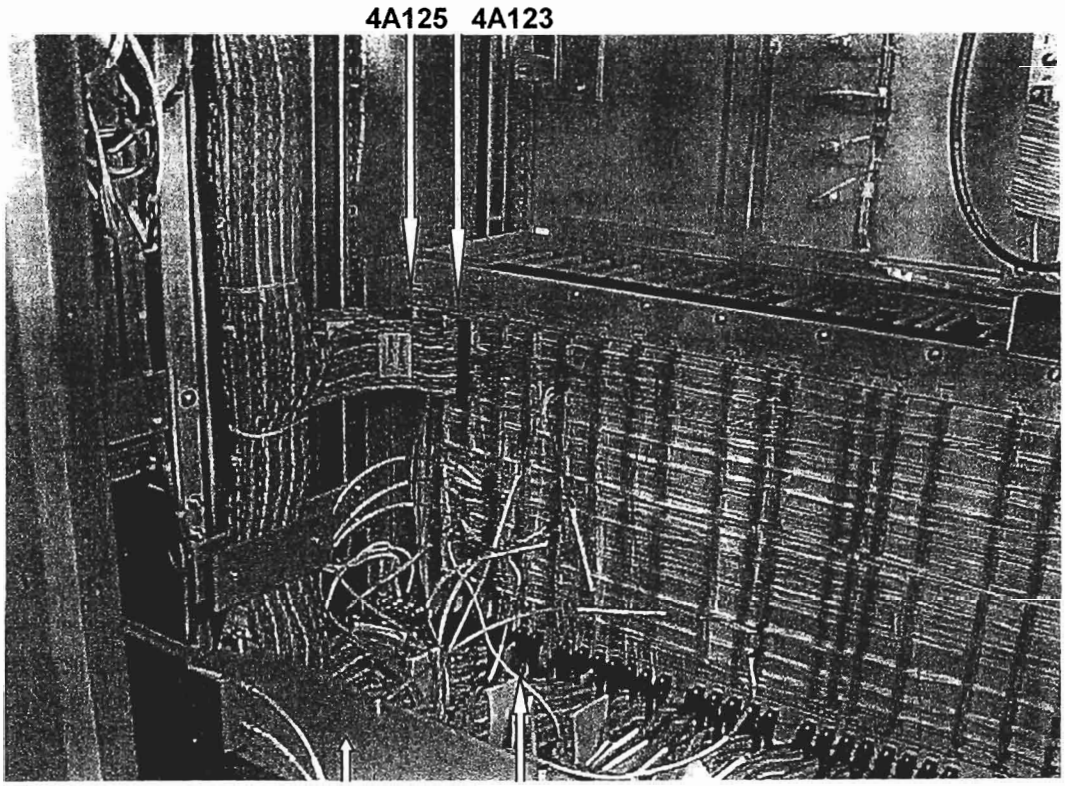


Figure 3. Photograph of Unit 4 A4 backplane

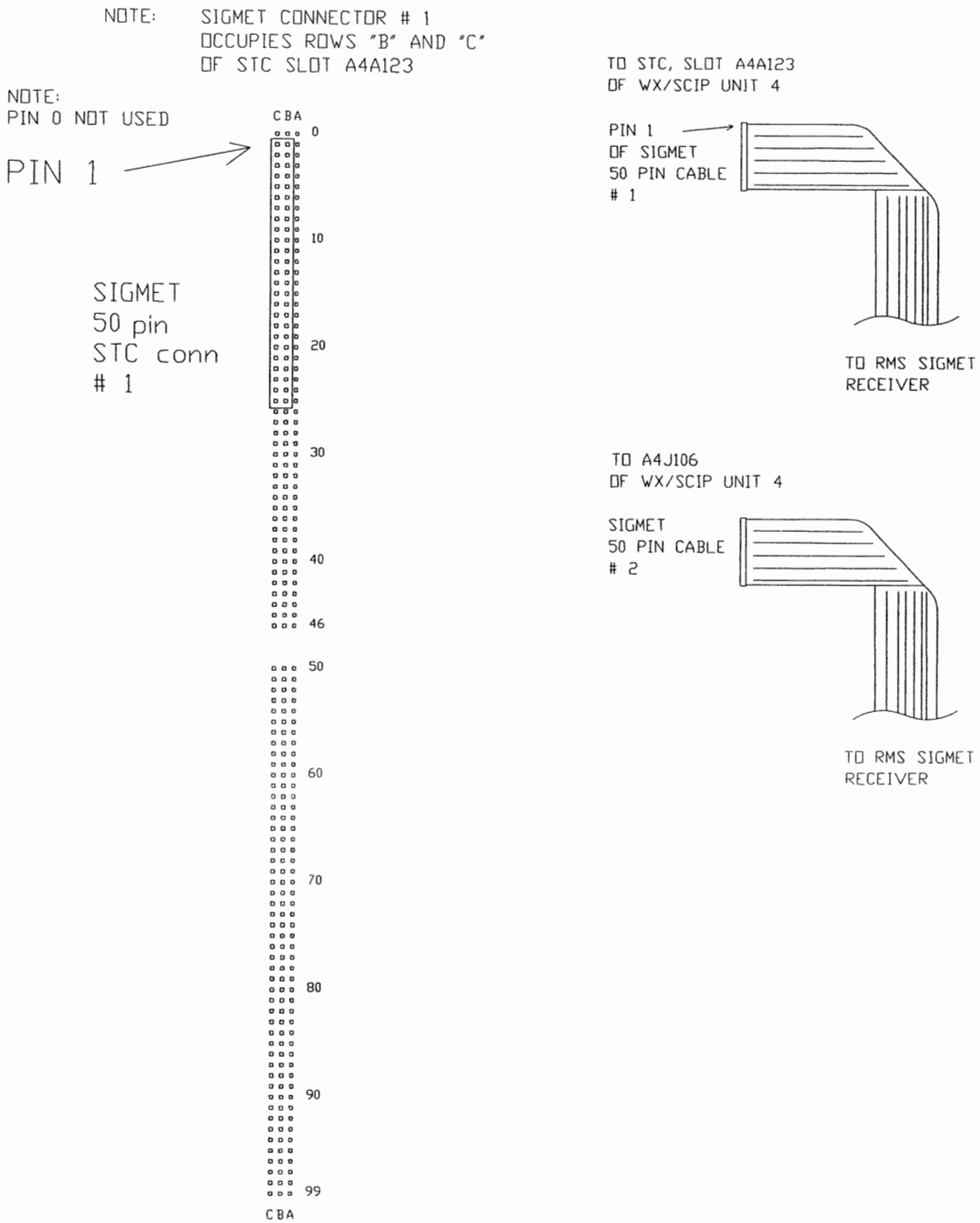


Figure 4. Backplane Card Slot Cable Connections

f. Connect cable W2402/P1, p/n 7A11903G13, to 4A4J106. Route the cable through the openings between Units 3 and 4, and connect W2402/P2 to 3A21J2 on the Processor/RIM.

g. Remove the STC circuit board, p/n 1D21103G01, in 4A4A123. Record the serial number on the configuration control form.

h. Install the new STC circuit board (Item 1, 7D11436G01) in slot 4A4A123. Record the serial number on the configuration control form

i. Load all VSP's to the 6 Lvl Wx channel so the E^2 PROM on this new board is configured properly.

8. Weather Channel Modification Kit (7D11432G01).
The parts required for this modification are included in the ASR-9 RF Mod Kit, WX, p/n 7D11432G01. Verify that all material required is available prior to starting the modification. Item numbers below refer to the Find Nos. in the 7D11432G01 parts list. The cables referenced below are in the Preinstallation Cable kit, p/n 7A11790G06, included in the 7D11432G01 kit.

NOTE: If the Antenna Waveguide Replacement Kit (7D11455G01) has been installed, the input to the bi-Directional coupler (DC7) must be removed and cable W1801 must be installed between the coupler (XCP105J1) at the end of the waveguide run and DC7.

a. Remove the cables between S6J1 and CP4J1 (Frequency A) and between S6J3 and CP3J1 (Frequency B).

b. Refer to drawing 7D11432 for installing the SP3T switches (XSW103, XSW104). Mount the switches (Item 3, MD013S015) on the WSP Switch Bracket (Item 4, ASR9-003.7.1) using number 6 screws, flat and lock washers provided (Items 10-12, MS51957-36, MS15795-806, MS35338-136).

c. Mount the assembled switch bracket on to FL3 and FL4 as shown in the drawing.

d. Refer to drawing 7D11432 for the installation of the WSP WX/SCIP electrical cover (Item 5, ASR9-003.7.5). Remove the original cover and install the new cover as shown in the drawing.

e. Install the RF Switch matrix control cable, W1410, p/n 7A11903G15, between 4A5J23 on the top of Unit 4 (through the cover just installed) and the switch inputs XSW103J5 and XSW104J5. The Military polarizing keys on the **topside** of A5J23 must be removed so the switch matrix control cable connector will mate properly.

f. Install the following 8 helix cables as shown in the WSP System Interconnect Schematic (7J10022):

- ❑ W1805, p/n 7A11902H53
- ❑ W1806, p/n 7A11902H54
- ❑ W1807, p/n 7A11902H55
- ❑ W1808, p/n 7A11902H56
- ❑ W1809, p/n 7A11902H57
- ❑ W1810, p/n 7A11902H58
- ❑ W1811, p/n 7A11902H59
- ❑ W1812, p/n 7A11902H60

g. Carefully check for +15/-15 vdc power supply voltages at the RF Switch Matrix control cable p/n 7A11903G15 connectors W1410P2 and W1410P3, immediately after the WX/SCIP is powered on. This will help verify the backplane power wiring and the connections on the backplane.

Pin 14 - ground
Pin 11 - +15vdc
Pin 12 - +15 vdc
Pin 15 - -15vdc

9. GPS Antenna Modification Kit (7A11741G01).
The parts required for this modification are included in GPS Antenna Modification Kit, p/n 7A11741G01. Verify that all material required is available prior to starting the modification. Item numbers below refer to the Find Nos. in the 7A11741G01 parts list. The cables referenced below are in the 7A11790G03 Preinstallation Cable kit included in 7A11741G01.

The GPS antenna installation is not directly related to the other ASR-9 modifications in the WSP Pre-installation kit. It is provided with the Pre-installation kit so that if lift equipment is required for the Antenna Waveguide installation, it can be used at the same time for the GPS antenna installation. The GPS antenna installation can be deferred to when the WSP RDP cabinet is installed.

The installation may need to be adjusted based on the specific radar building/shelter location. The following is provided as general guidelines for installing the antenna (Item 1, 7A11805H02), surge suppressor (Item 5, 7A11805H03), and cable (Item 4, 7A11790G03).

a. Material is provided in the GPS antenna kit for mounting the antenna to the outside of the radar equipment building. This material is identified on the parts list as items 18 through 33. The installation should be adapted to specific site requirements and conditions.

b. The maximum combined cable length from the RDP cabinet through the surge suppressor to the antenna is 75 feet. The GPS antenna should be located with a clear view of the sky and as isolated as possible from ASR-9 radiation.

c. The surge suppressor should be mounted on a grounded, bulkhead plate outside where the antenna cable will enter into the building.

d. Cut the cable supplied to fit between the antenna and surge suppressor. Terminate each end of the cable with the appropriate connector supplied with the antenna kit. Apply the appropriate sleeve markers on to the cable. Install the cable between the antenna and surge suppressor.

e. The cable used between the surge suppressor and RDP cabinet is not included in this kit, but is supplied with the WSP system. The cable must be 50-ohm type coax type such as the RG-58 type.

10. Antenna Waveguide Replacement Kit (7D11455G01).
The parts required for this modification are included in the Antenna Waveguide Replacement Modification Kit, p/n 7D11455G01. Verify that all material required is available prior to starting the modification. Item numbers below refer to the Find Nos. in the 7D11455G01 parts list. Refer to drawing 7D11455G01 during the installation of this kit. The cables referenced below are in the 7A11790G02 Preinstallation Cable kit included in 7D11455G01.

a. Assemble brackets (see drawing ASR9-003.12.1)

b. Mount brackets on Center Tower Pole according to drawing ASR9-003.12.1

c. Position Flex W/G (Item 8) such that the horizontal run lines up with the existing waveguide entering the building.

d. Assemble the vertical run up the center pole near the stairway (see drawing (ASR9-003.12).

e. Installer's preference to continue installation as deemed appropriate for facility. The final installation shall correspond with the drawings series in the SSM-012 Appendix 3 given by Northrup Grumman.

11. EQUIPMENT CALIBRATION.

a. Overview.

Installing the WSP Pre-installation kit causes a degradation in MDS measurements due to increased RF path loss. In the high beam, this is a 3-dB loss attributable to the waveguide power splitter. In the low beam, the additional loss is roughly 0.5-dB caused by the added RAG beam switch and S-band transitions. In the weather channel, the loss is about 0.7-dB as a result of the introduction of coaxial RF switches into the weather receive path. These additional path losses naturally change RMS MDS measurements, and with the existing computation algorithm can cause summary faults in any of the three paths. To compensate for these increased losses, the radar MDS must be re-calibrated.

In addition, the hard coded alarm threshold will be raised to roughly -103 dBm to accommodate the additional path losses introduced by WSP Pre-installation kit, and widening the Programmable Alarm Thresholds (PATs) to avoid soft failures.

The changes to the VSPs and PATs to account for the losses induced by the addition of waveguide components to the RF path must be verified by the FAA to insure acceptable radar coverage loss. The VSPs and PATs are baselined by AOS-270. The following VSP/PAT changes are specified in the Weather Systems Processor (WSP) to Airport Surveillance Radar (ASR-9) Interface Requirements Document (IRD) NAS-IR-31073403 (August 10, 1999).

Make the following changes to the VSP/PATs:

- ❑ Beam Select RAG – Adjacent Windows VSP: 1109 through 1116 (Range for Adjacent Beam Switch Window #1-#8). Change from 15 to 14.
- ❑ High Beam STC Reference Attenuation VSP: 1601. Change from 77 to 74.
- ❑ Low Beam STC Reference Attenuation VSP: 1501. Change from 85 to 82.
- ❑ MDS – Hi Beam PAT: 2C0. Change from –1120 and –1070 to –1090 and –1040.
- ❑ MDS – Lo Beam PAT: 2C1. Change from –1120 and –1070 to –1110 and –1060.
- ❑ Noise figure – Hi Beam PAT: 2C2. Change from 0 and 50 to 30 and 80.
- ❑ Noise figure – Lo Beam PAT: 2C3. Change from 0 and 50 to 0 and 56.
- ❑ MDS Hi Beam Fail - PAF: 213 Change from 2 of 3 to 4 of 4.
- ❑ Set VSP 1710 = 1: 3DB Beam Splitter Installed

b. Before proceeding with a new MDS re-calibration, verify that the new components have not changed the MDS more than anticipated when comparing the current MDS readings to those recorded earlier (see attached data sheet). The high beam MDS shall drop about 3.5-db (Power Splitter and SPDT waveguide switch) while the low beam MDS may drop by 0.5 db. If the readings drop significantly more than anticipated (>1 db), one of the new components may be bad. Troubleshoot the new waveguide section and locate the bad part before proceeding with a new calibration of the MDS if the readings are not reasonable. Re-calibrate the MDS measurement in all three paths following the procedures provided in ASR-9 TIB 6310.24. Complete an MDS calibration data sheet as shown in table 6-1 of the TIB.

c. After re-calibrating the MDS measurement, allow the system to stabilize with high voltage ON. Record on lines 4-6 of the MDS data sheet used previously in paragraph 3.3.4, step 3, the high beam, low beam, and weather channel RMS MDS measurements for each modified channel. On lines 7-9 for each MDS measurement (high beam, low beam, and weather), subtract the number recorded prior to modification (lines 1-3) from the number recorded after modification (lines 4-6). These numbers should all have a positive value (i.e. they should reflect some loss introduced by WSP), and should approximate the numbers in parentheses next to lines 7-9.

Assuming the changes to the MDS computational algorithms and PATs have been made, the new readings should not cause any summary faults or maintenance alerts. The site technicians will be able to track further front end degradations as usual.

d. Updating the Clear Day Map. This modification changes the receiver parameters allowing more severe ground clutter returns. The ground clutter returns may appear as false weather detections if the Clear Day Map is not adapted to the new baseline. To prevent these additional weather returns from appearing on ATC displays, the Clear Day Map must be updated using procedure 3.3.2.6.3.2 in T.I manual 6310.24. This procedure can only be run on a reasonably clear day so Air Traffic may have to work with the sub optimal system until the map can be updated.

At the discretion of the installation personnel, the Sigmet RxNet7 IF receiver calibration procedure can be completed at this time or can be performed later after the WSP equipment installation. The WSP IF receiver calibration procedure is included as an attachment to the WSP System Installation and Setup Instructions drawing, 7A11723.

This concludes the installation and checkout of the WSP Pre-installation Modification Kit. The ASR-9 radar system operation should be returned to normal site operation.

Verify the system is fully operational and no alarms are present except for those previously recorded in paragraph 3.3.4, step 3 and 4. If the presence of new alarms is determined to be the result of the installation of the modification kit, corrective action must be taken to eliminate the cause of the alarm.

PRE- AND POST-MODIFICATION MDS RECORD

SITE_____ DATE_____

Pre-Modification	Channel A	Channel B
1. High Beam MDS	-_____dBm	-_____dBm
2. Low Beam MDS	-_____dBm	-_____dBm
3. Weather MDS	-_____dBm	-_____dBm

Post-Modification	Channel A	Channel B
4. High Beam MDS	-_____dBm	-_____dBm
5. Low Beam MDS	-_____dBm	-_____dBm
6. Weather MDS	-_____dBm	-_____dBm

Additional WSP Path Losses	Channel A	Channel B
7. High Beam = Line 4 - Line 1 =	_____dB	_____dBm (approx. 3 dB)
8. Low Beam = Line 5 - Line 2 =	_____dB	_____dBm (approx. 0.5 dB)
9. Weather = Line 6 - Line 3 =	_____dB	_____dBm (approx. 1.5 dB)

PRE-INSTALLATION SYSTEM STATUS RECORD

SITE_____ DATE_____

Alarms:

Missing Parts:

Other Notes:

Configuration Control List

SITE_____ DATE_____

Record the Serial Number if available. Otherwise, check the box when installed or removed.

Part Number	Description	Channel A or RMS/WX	Channel B	Site Spares
645A863A01	W/G Beam Switch (XSW101/102)			
7A11819H01	W/G Splitter (XPS101/102)			N/A
7A11819H04	W/G, Elbow			N/A
7A11819H02	W/G, 5 inch			N/A
7A11819H03	W/G, 4 inch			N/A
645A771H02	Adapter, W/G to Coax (XCP101/102)			N/A
645A771H02	Adapter, W/G to Coax (XCP103/104)			N/A
7A11871H01	Beam Switch Control Box (XJB101/102)			N/A
XXXXXXX	Antenna W/G Replacement TBD		N/A	
MD-013S015	Microwave Switch SP3T (XSW103)		N/A	
MD-013S015	Microwave Switch SP3T (XSW104)		N/A	
7A11800H03	Sigmet IF Digitizer 4A12		N/A	
HJ-22010	Power Splitter (4A3A3)		N/A	
7A11820H01	Cascadable RF Amplifier (4A12A2)		N/A	
7A11800H02	Sigmet Processor/RIM (3A21)		N/A	
RIM	RIM PWA		N/A	
RVP7	RVP7 PWA		N/A	
ASR9_003.1	STC CCA 4A4A123		N/A	
	Unit 4 backplane wiring changes		N/A	N/A
	Remove High Beam 14" W/G			N/A
	Remove Low Beam 14" W/G			N/A
	Remove 3db attenuator 4A3S1J2		N/A	N/A
1D21103G01	Remove STC CCA 4A4A123		N/A	N/A

APPENDIX 3. INSTALLATION DRAWINGS

7D11431G01 Rev. D ASR-9 RF MOD KIT, TGT

Find	Part Number	Note	Part Name	Quantity
1	7A11822H01		WAVEGUIDE SWITCH	1 EA
1	7A11822H01		WAVEGUIDE SWITCH	1 EA
2	7A11819H01		W/G HYBRID POWER SPLITTER,	1 EA
2	7A11819H01		W/G HYBRID POWER SPLITTER,	1 EA
3	7A11819H04		WAVEGUIDE, RIGID H PLANE ELB	1 EA
3	7A11819H04		WAVEGUIDE, RIGID H PLANE ELB	1 EA
4	7A11819H02		W/G, 5 INCH	1 EA
4	7A11819H02		W/G, 5 INCH	1 EA
5	7A11819H03		W/G, 4 INCH	1 EA
5	7A11819H03		W/G, 4 INCH	1 EA
6	645A771H02		ADAPTER, WG TO COAX	4 EA
7	7A11871H01		SWITCH CONTROL BOX ASSY	1 EA
7	7A11871H01		SWITCH CONTROL BOX ASSY	1 EA
8	MS35650-3254		NUT,PLAIN,HEX (.250-28)	120 EA
9	AN960C416		WASHER, FLAT	320 EA
10	AN4C12A		BOLT,MACHINE	120 EA
11	MS35338-139		WASHER, LOCK-SPRING (.250 D	220 EA
12	M24211/2-005	2	GASKET	18 EA
13	MS16996-23		SCREW, CAP, SOCKET HD .250-28unf	60 EA
14	MS35307-360	3	SCREW,CAP,HEX	4 EA
15	P1008HG	3	NUT, UNISTRUT (3/8"-16)	4 EA
16	NAS1149C0663R	3	WASHER,FLAT,300 CRES, PASS,	4 EA
17	MS35338-141	3	WASHER, LOCK-SPRING, CRES	4 EA

Find	*Part Number*	*Note*	*Part Name*	*Quantity*
18	MS16996-24		SCREW, CAP, SOCKET HD, .250-	20 EA

NOTES FOR: *7D11431G01*

Note 2 Replace used seals with new seals supplied.

Note 3 Used for mounting 7A11871H01 to Unistrut.

WSP SHIPPING LIST
7D11432G01 Rev .C ASR-9 RF MOD KIT, WX

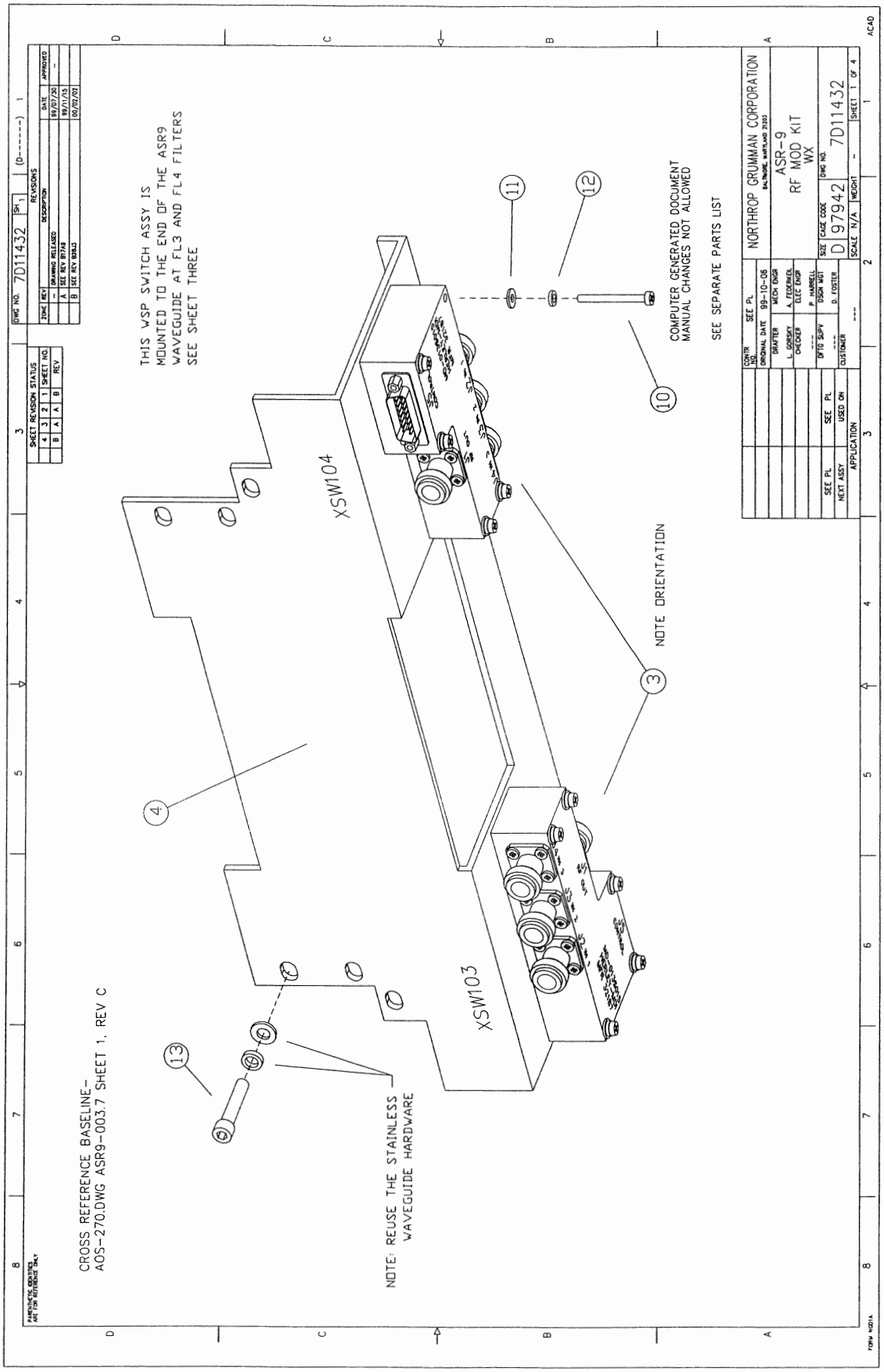
Find	Part Number	Note	Part Name	Quantity
2	7A11790G06		PREINSTALLATION CABLES, RF	1 EA
3	7A11823H01		SWITCH, MICROWAVE, SP3T	1 EA
3	7A11823H01		SWITCH, MICROWAVE, SP3T	1 EA
4	ASR9-003.7.1		WSP SWITCH BRACKET	1 EA
5	ASR9-003.7.5		WSP WX/SCIP ELECTRICAL COVER	1 EA
10	MS51957-36	2	SCREW	10 EA
11	MS15795-806	2	WASHER, FLAT, NO. 6	10 EA
12	MS35338-136	2	WASHER, LOCK-SPRING, CRES	10 EA
13	MS16998-46	3	SCREW,CAP,SOCKET HEAD, (.250	6 EA
14	MS3367-1-9		STRAP,TIEDOWN,ELECTRICAL COM	5 EA
15	582R688H04		MOUNT, CABLE STRAP	5 EA
100	83869NB/4		MARKING, INK AND LABEL	1 AR

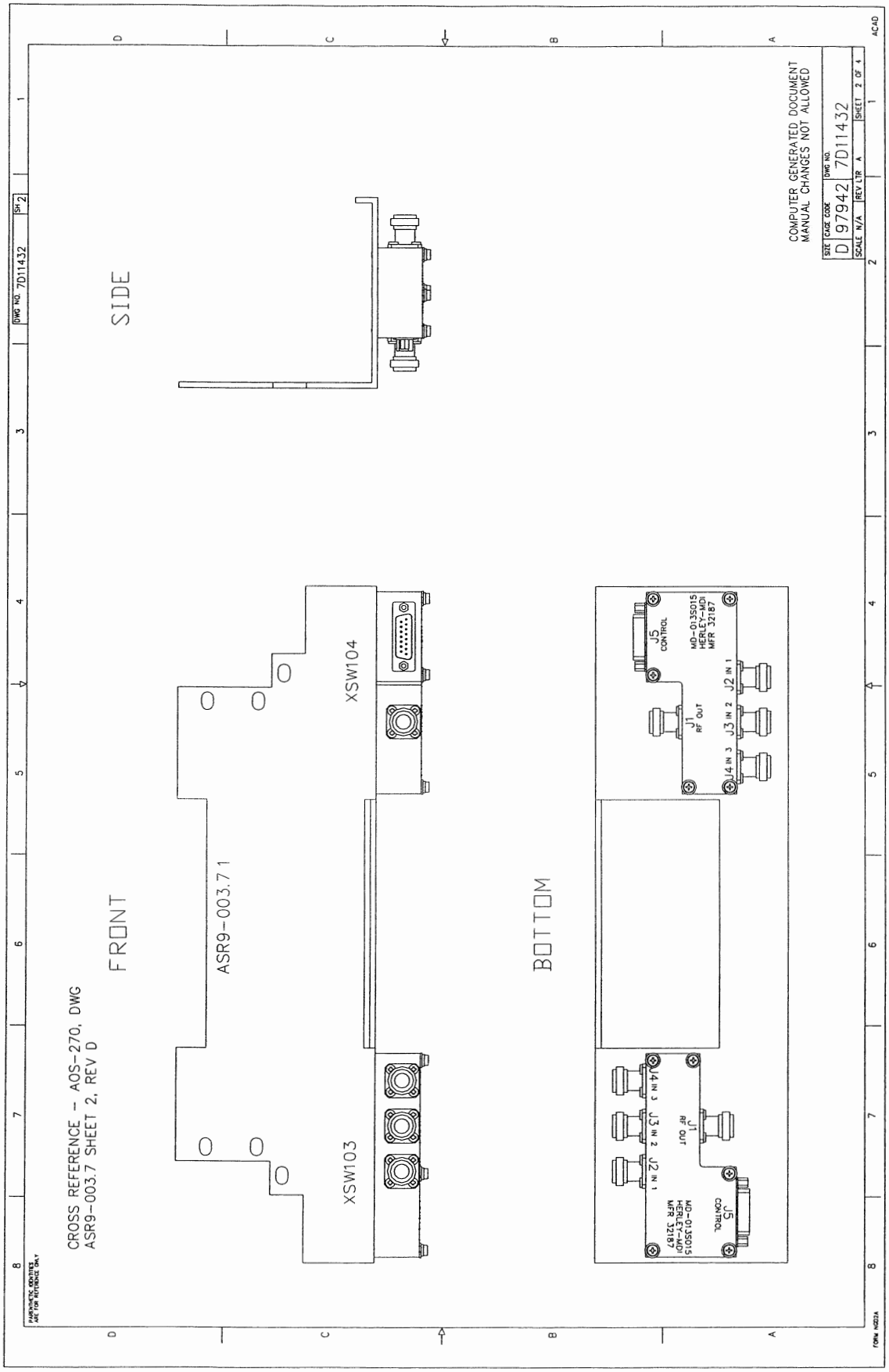
NOTES FOR: *7D11432G01*

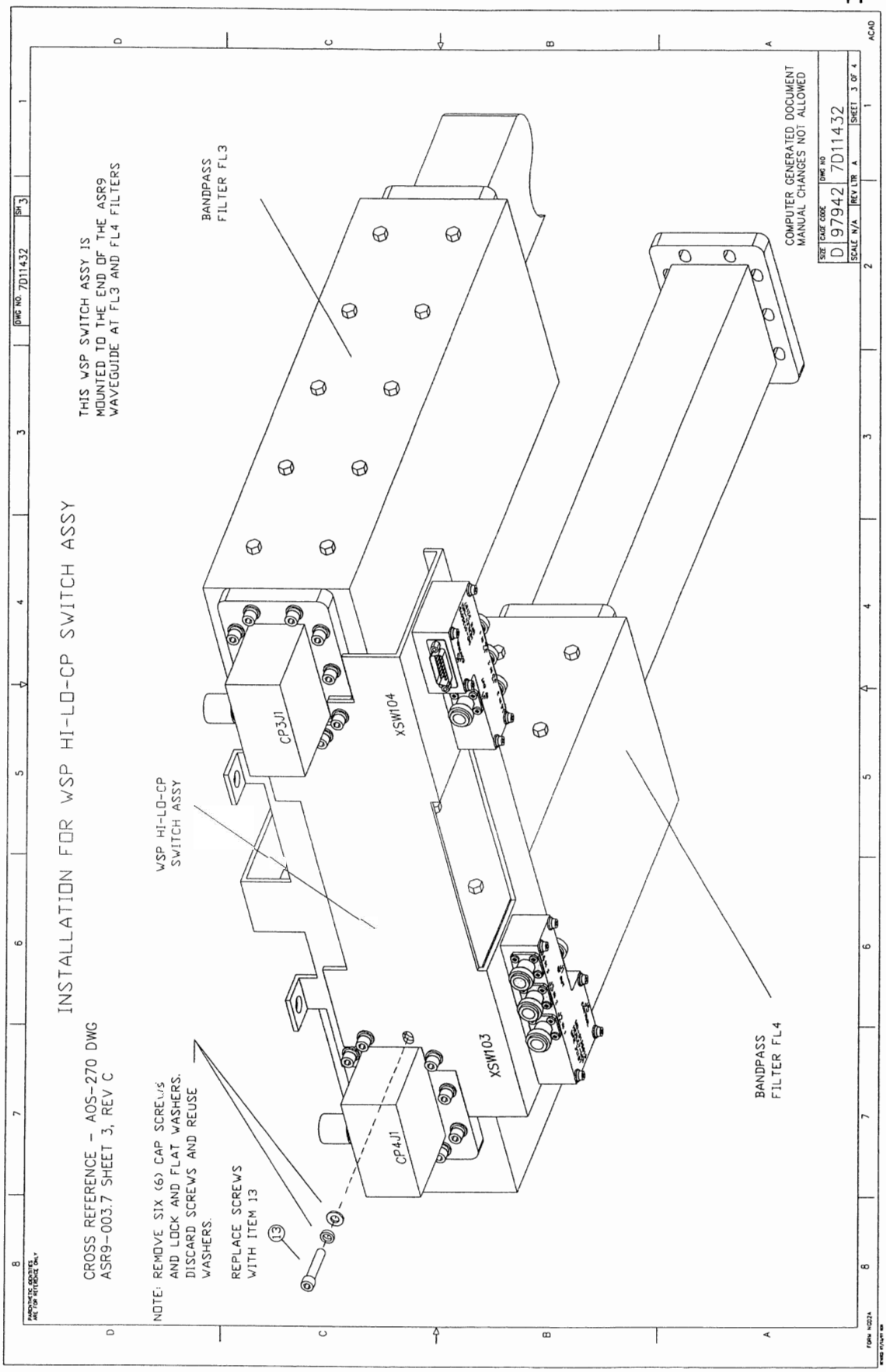
Note 2 Required to mount 7A11823H01.

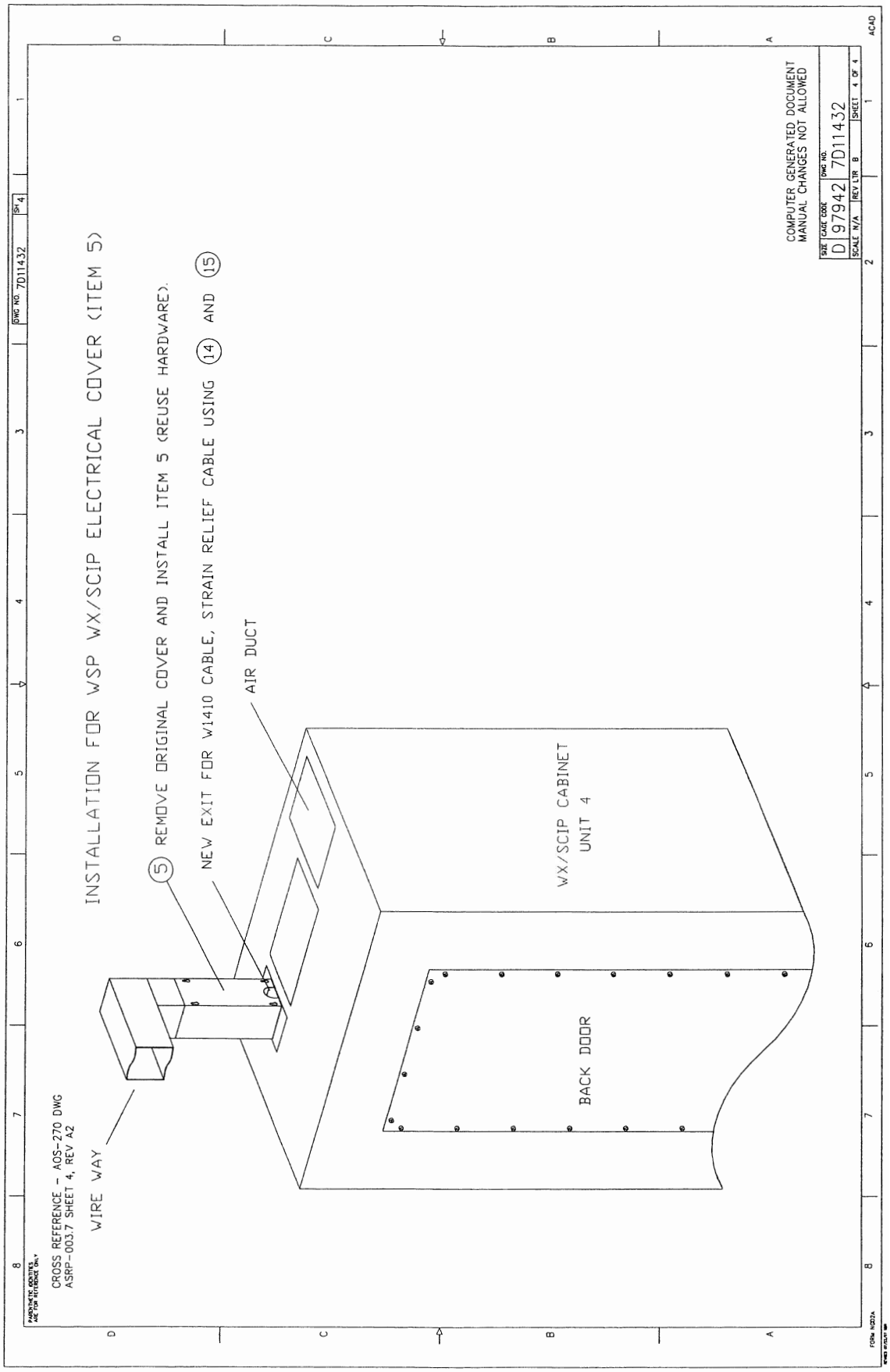
Note 3 Required to mount ASR9-003.7.1.

Preinstallation Kit - Page 5 of 18


THIS WSP SWITCH ASSY IS
MOUNTED TO THE END OF THE ASR9
WAVEGUIDE AT FL3 AND FL4 FILTERS
SEE SHEET THREE
COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
SEE SEPARATE PARTS LIST
NOTE ORIENTATION
XSW104
XSW103
CROSS REFERENCE BASELINE-
AOS-270.DWG ASR9-003.7 SHEET 1, REV C
NOTE: REUSE THE STAINLESS
WAVEGUIDE HARDWARE
NORTHROP GRUMMAN CORPORATION
ASR-9
RF MOD KIT
WX
D 97942
7D11432
SHEET 1 OF 4
SCALE N/A
WEIGHT -
SEE PL
ORIGINAL DATE 99-10-06
DRAFTER L. GORSKY
CHECKER
MECH ENGR A. FEDERKEL
ELEC ENGR P. HARRELL
DFTG SUPV
DSGN MGT D. FOSTER
CUSTOMER
SEE PL
NEXT ASSY
USED ON
APPLICATION
DWG NO. 7D11432
SHEET REVISION STATUS
REVISIONS
DRAWING RELEASED
SEE REV 97A9
SEE REV 92B13
99/07/30
99/11/15
00/02/02
ACAD


COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
SIZE D
CAGE CODE 97942
DWG NO. 7D11432
SCALE N/A
REV LTR A
SHEET 2 OF 4
DWG NO. 7D11432
SH 2
SIDE
FRONT
BOTTOM
ASR9-003.71
XSW104
XSW103
J5 CONTROL
MD-013S015
HERLEY-MDI
MFR 32187
J1 RF OUT
J2 IN 1
J3 IN 2
J4 IN 3
CROSS REFERENCE - AOS-270, DWG
ASR9-003.7 SHEET 2, REV D
PARENTHETIC IDENTITIES ARE FOR REFERENCE ONLY
FORM NO22A


INSTALLATION FOR WSP HI-LO-CP SWITCH ASSY
CROSS REFERENCE - AOS-270 DWG
ASR9-003.7 SHEET 3, REV C
NOTE: REMOVE SIX (6) CAP SCREWS
AND LOCK AND FLAT WASHERS.
DISCARD SCREWS AND REUSE
WASHERS.
REPLACE SCREWS
WITH ITEM 13
13
THIS WSP SWITCH ASSY IS
MOUNTED TO THE END OF THE ASR9
WAVEGUIDE AT FL3 AND FL4 FILTERS
BANDPASS
FILTER FL3
WSP HI-LO-CP
SWITCH ASSY
CP3J1
XSW104
XSW103
CP4J1
BANDPASS
FILTER FL4
COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
SIZE D
CAGE CODE 97942
DWG NO 7D11432
SCALE N/A
REV LTR A
SHEET 3 OF 4
DWG NO. 7D11432
SH 3
ACAD


INSTALLATION FOR WSP WX/SCIP ELECTRICAL COVER (ITEM 5)
5 REMOVE ORIGINAL COVER AND INSTALL ITEM 5 (REUSE HARDWARE).
NEW EXIT FOR W1410 CABLE, STRAIN RELIEF CABLE USING 14 AND 15
AIR DUCT
WX/SCIP CABINET
UNIT 4
BACK DOOR
WIRE WAY
CROSS REFERENCE - AOS-270 DWG
ASRP-003.7 SHEET 4, REV A2
DWG NO. 7D11432
SH 4
COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
SIZE
CAGE CODE
D 97942
DWG NO.
7D11432
SCALE N/A
REV LTR B
SHEET 4 OF 4
ACAD

7D11433G01 Rev. E ASR-9 IF MOD KIT

Find	Part Number	Note	Part Name	Quantity
2	7A11800H03	2	SIGMET IF DIGITIZER	1 EA
3	7A11790G08		PREINSTALLATION CABLES, SIGMET	1 EA
4	7A11790G09		PREINSTALLATION CABLES, IF	1 EA
5	7A11725		PRE-INSTALLATION INSTRUCTION	1 EA
6	ASR9-003.9.1		SIGMET IF RCVR PANEL	1 EA
7	ASR9-003.9.2		SIGMET IF RCVR, 115VAC COVER	1 EA
8	ASR9-003.9.3		43A3 POWER SPLITTER BRACKET	1 EA
9	ASR9-003.9.5		AMPLIFIER BRACKET	1 EA
10	2098-5286-54		RG141 BENDING TOOL	1 EA
200	MS51958-69		SCREW,PAN HEAD (.190-32)	4 EA
204	HJ-22010		POWER SPLITTER	1 EA
205	7A11820H01		CASCADABLE RF AMPLIFIER	1 EA
206	MS51957-3		SCREW, PAN HD (2-56UNC-2A TH	4 EA
207	NAS620C2		WASHER, FLAT NO. 2, .089 ID,	4 EA
208	MS35338-134		WASHER, LOCK-SPRING, CRES	4 EA
209	77002-49 13150		TERMINAL STRIP, 2 POSITION	1 EA
210	MS51957-30		SCREW,PAN HD, .138-32 X .500	2EA
211	MS35338-136		WASHER, LOCK-SPRING, CRES	2 EA
212	MS15795-805		WASHER, FLAT, NO. 6, (.156 D	2 EA
213	9912-5		HOOK-UP WIRE, PVC INSUL AWG	4 IN
215	17650		CABLE, POWER	1 EA
217	CCS31-S8-C		CLAMP,CABLE, NYLON	1 EA
218	MS51957-43		SCREW,PAN HEAD (.164-32)	5 EA
219	MS15795-841		WASHER,FLAT	7 EA

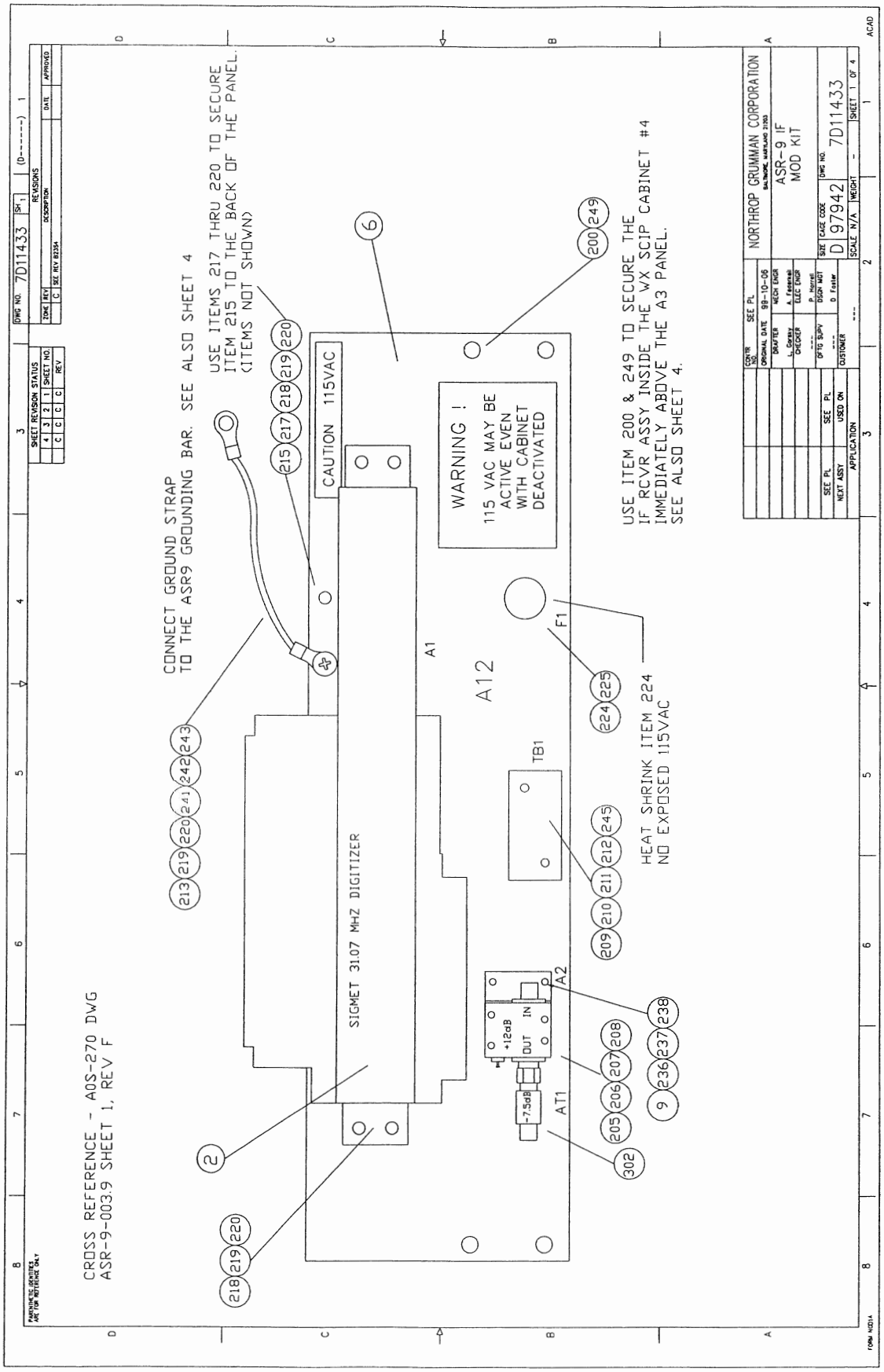
Find	Part Number	Note	Part Name	Quantity
220	MS35338-137		WASHER, LOCK-SPRING, CRES	6 EA
224	344125A		FUSEHOLDER, INDICATING, 125V	1 EA
225	312001		5FUSE, 1A, 3AG (LITTLEFUSE)	1 EA
226	MS51957-36		SCREW	2 EA
227	MS35649-264		NUT, PLAIN, HEX (.138-32)	4 EA
228	MS15795-806		WASHER, FLAT, NO. 6	2 EA
229	MS51859-15		WASHER, PLASTIC (.149 DIA)	2 EA
230	9921-2		HOOK-UP WIRE, PVC INSUL AWG	6 IN
231	9921-10		HOOK-UP WIRE, PVC INSUL AWG	6 IN
232	9918-10		HOOK-UP WIRE, PVC INSUL AWG	8 IN
236	MS51957-15		SCREW,PAN HD (.112-40)	4 EA
237	MS35338-135		WASHER, LOCK-SPRING, CRES	4 EA
238	NAS620C4		WASHER,FLAT,.115 ID X .209	4 EA
241	MS35649-284 9		NUT, PLAIN HEX (#8-32)	1 EA
242	MS51957-45		SCREW, PAN HD (.164-32)	1 EA
243	MS25036-153		TERMINAL LUG	1 EA
244	MS51958-63		SCREW, PAN HD (.190)	1 EA
245	MS25036-101		TERMINAL LUG	7 EA
246	MS25036-108		TERMINAL, LUG	1 EA
247	MS15795-842		WASHER, FL, (.219 DIA)	1 EA
248	MS35338-138		WASHER, LOCK-SPRING, CRES	1 EA
249	1225-10-N		SPACER, NYLON, #10 X .75	4 EA
300	18AH-06	3	ATTENUATOR, FIXED,6DB,SMA	2 EA
301	18AH-07	3	ATTENUATOR, FIXED,7DB,SMA	2 EA

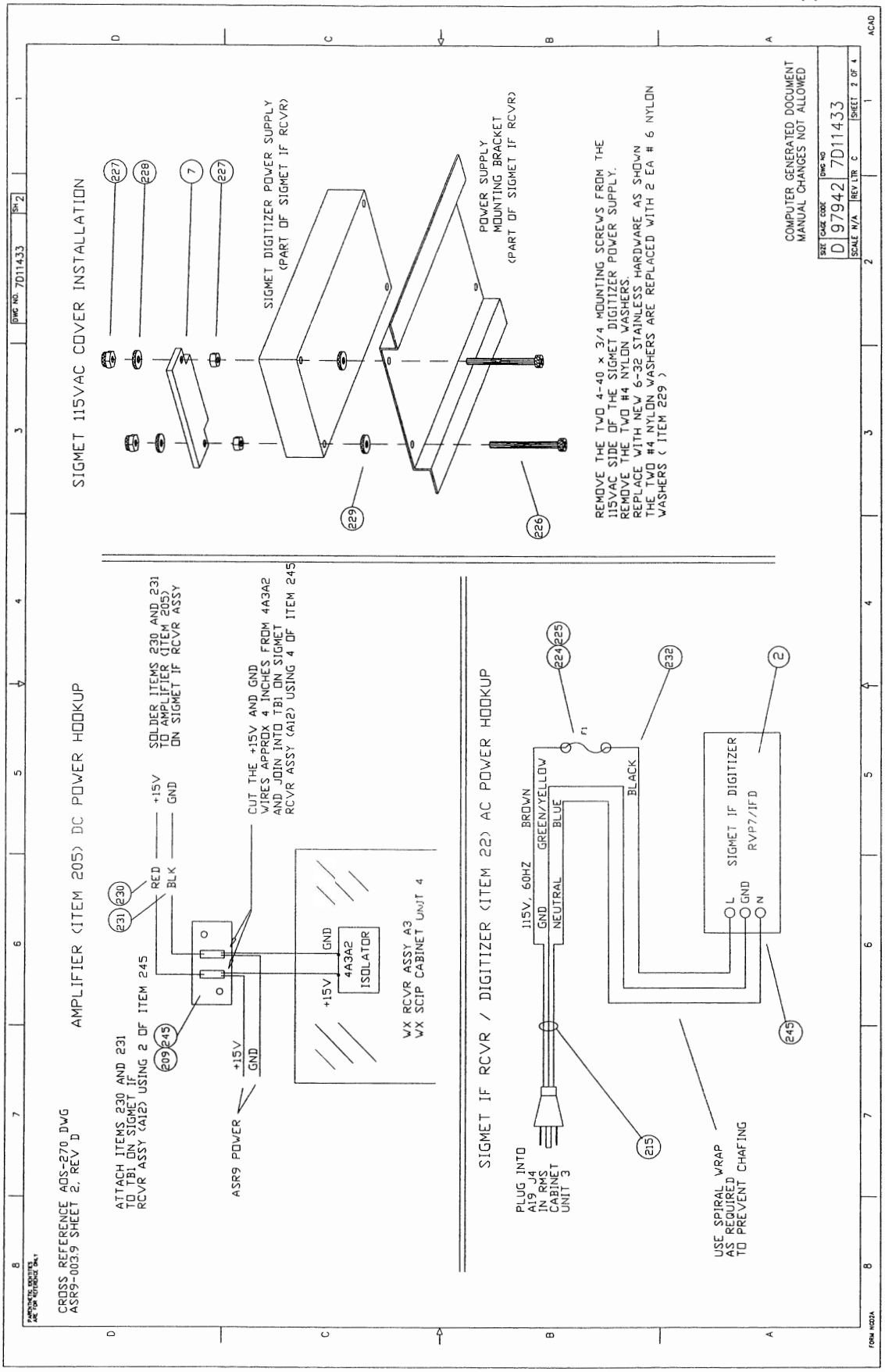
Find	*Part Number*	*Note*	*Part Name*	*Quantity*
302	18AH-08	3	ATTENUATOR, FIXED,8DB,SMA	2 EA
303	18AH-09	3	ATTENUATOR, FIXED,9DB,SMA	2 EA
304	18AH-10	3	ATTENUATOR, FIXED,10DB,SMA	2 EA
305	18AH-11	3	ATTENUATOR, FIXED,11DB,SMA	2 EA

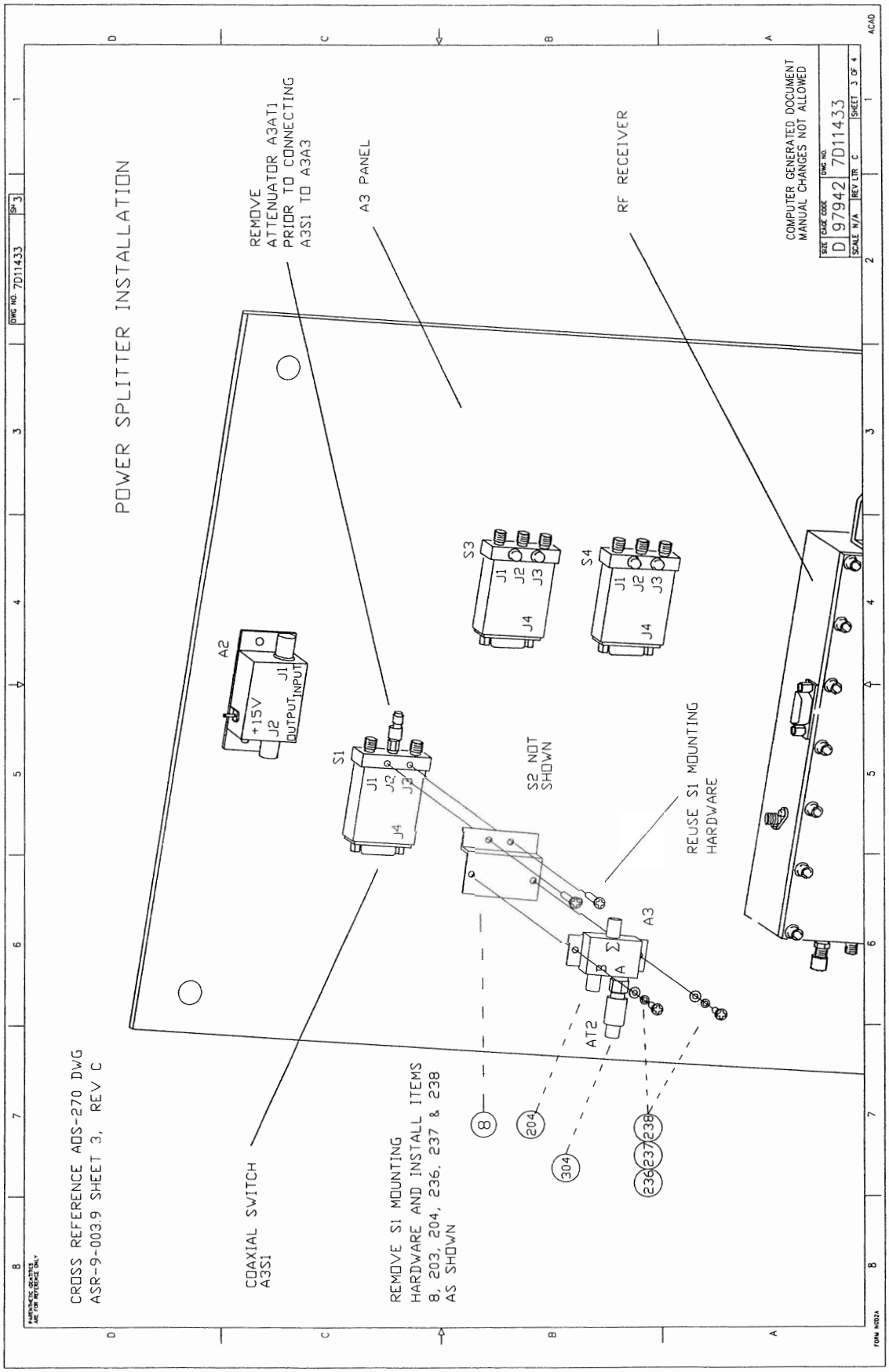
NOTES FOR: *7D11433G01*

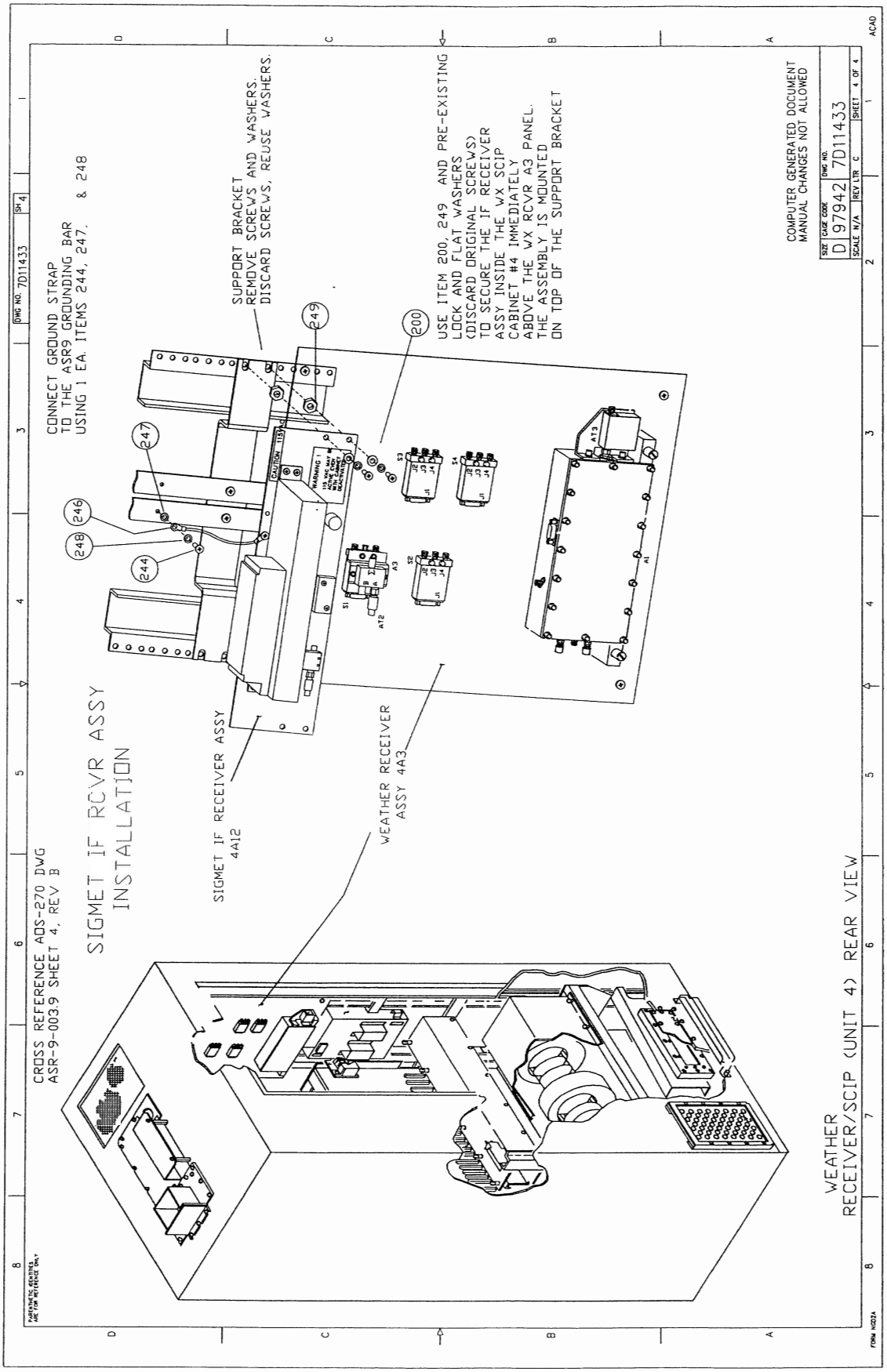
Note 2 7A11800H03 is part of 7A11800H01. 7A11800H02 is a positive quantity on 7D11434G01. 7A11800H03 will be installed as part of 7D11433 using preinstallation instructions 7A11725.

Note 3 Baseline attenuator for 4A12At1 is 18AH-08. Baseline attenuator for 4A3AT2 is 18AH-10. Remaining attenuators should be kept at the site for calibration of replacement unit.


CONNECT GROUND STRAP
TO THE ASR9 GROUNDING BAR. SEE ALSO SHEET 4
USE ITEMS 217 THRU 220 TO SECURE
ITEM 215 TO THE BACK OF THE PANEL.
(ITEMS NOT SHOWN)
CAUTION 115VAC
WARNING !
115 VAC MAY BE
ACTIVE EVEN
WITH CABINET
DEACTIVATED
USE ITEM 200 & 249 TO SECURE THE
IF RCVR ASSY INSIDE THE WX SCIP CABINET #4
IMMEDIATELY ABOVE THE A3 PANEL.
SEE ALSO SHEET 4.
HEAT SHRINK ITEM 224
NO EXPOSED 115VAC
A1
A12
F1
TB1
A2
AT1
SIGMET 31.07 MHZ DIGITIZER
+12dB
DUT
IN
-7.5dB
CROSS REFERENCE - AOS-270 DWG
ASR-9-003.9 SHEET 1, REV F
NORTHROP GRUMMAN CORPORATION
ASR-9 IF
MOD KIT
7D11433
D 97942
SHEET 1 OF 4


SIGMET 115VAC COVER INSTALLATION
SIGMET DIGITIZER POWER SUPPLY (PART OF SIGMET IF RCVR)
POWER SUPPLY MOUNTING BRACKET (PART OF SIGMET IF RCVR)
REMOVE THE TWO 4-40 x 3/4 MOUNTING SCREWS FROM THE 115VAC SIDE OF THE SIGMET DIGITIZER POWER SUPPLY. REMOVE THE TWO #4 NYLON WASHERS. REPLACE WITH NEW 6-32 STAINLESS HARDWARE AS SHOWN THE TWO #4 NYLON WASHERS ARE REPLACED WITH 2 EA # 6 NYLON WASHERS (ITEM 229)
AMPLIFIER (ITEM 205) DC POWER HOOKUP
SOLDER ITEMS 230 AND 231 TO AMPLIFIER (ITEM 205) ON SIGMET IF RCVR ASSY
CUT THE +15V AND GND WIRES APPROX 4 INCHES FROM 4A3A2 AND JOIN INTO TB1 ON SIGMET RCVR ASSY (A12) USING 4 OF ITEM 245
ATTACH ITEMS 230 AND 231 TO TB1 ON SIGMET IF RCVR ASSY (A12) USING 2 OF ITEM 245
ASR9 POWER
WX RCVR ASSY A3
WX SCIP CABINET UNIT 4
4A3A2 ISOLATOR
SIGMET IF RCVR / DIGITIZER (ITEM 22) AC POWER HOOKUP
115V, 60HZ
SIGMET IF DIGITIZER RVP7/IFD
PLUG INTO A19 J4 IN RMS CABINET UNIT 3
USE SPIRAL WRAP AS REQUIRED TO PREVENT CHAFING
CROSS REFERENCE ADS-270 DWG ASR9-003.9 SHEET 2, REV D
COMPUTER GENERATED DOCUMENT MANUAL CHANGES NOT ALLOWED
DWG NO. 7D11433
SIZE D CAGE CODE 97942 DWG NO 7D11433
SCALE N/A REV LTR C SHEET 2 OF 4


POWER SPLITTER INSTALLATION
REMOVE
ATTENUATOR A3AT1
PRIOR TO CONNECTING
A3S1 TO A3A3
A3 PANEL
RF RECEIVER
COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
SIZE D CAGE CODE 97942 DWG NO. 7D11433
SCALE N/A REV LTR C SHEET 3 OF 4
DWG NO. 7D11433 SH 3
A2
+15V
J2
OUTPUT
J1
INPUT
S1
J1
J2
J3
J4
S2 NOT
SHOWN
S3
J1
J2
J3
J4
S4
J1
J2
J3
J4
REUSE S1 MOUNTING
HARDWARE
A3
Σ
A
AT2
COAXIAL SWITCH
A3S1
REMOVE S1 MOUNTING
HARDWARE AND INSTALL ITEMS
8, 203, 204, 236, 237 & 238
AS SHOWN
8
204
304
236
237
238
CROSS REFERENCE ADS-270 DWG
ASR-9-003.9 SHEET 3, REV C
DIMENSIONS ARE FOR REFERENCE ONLY
ACAD

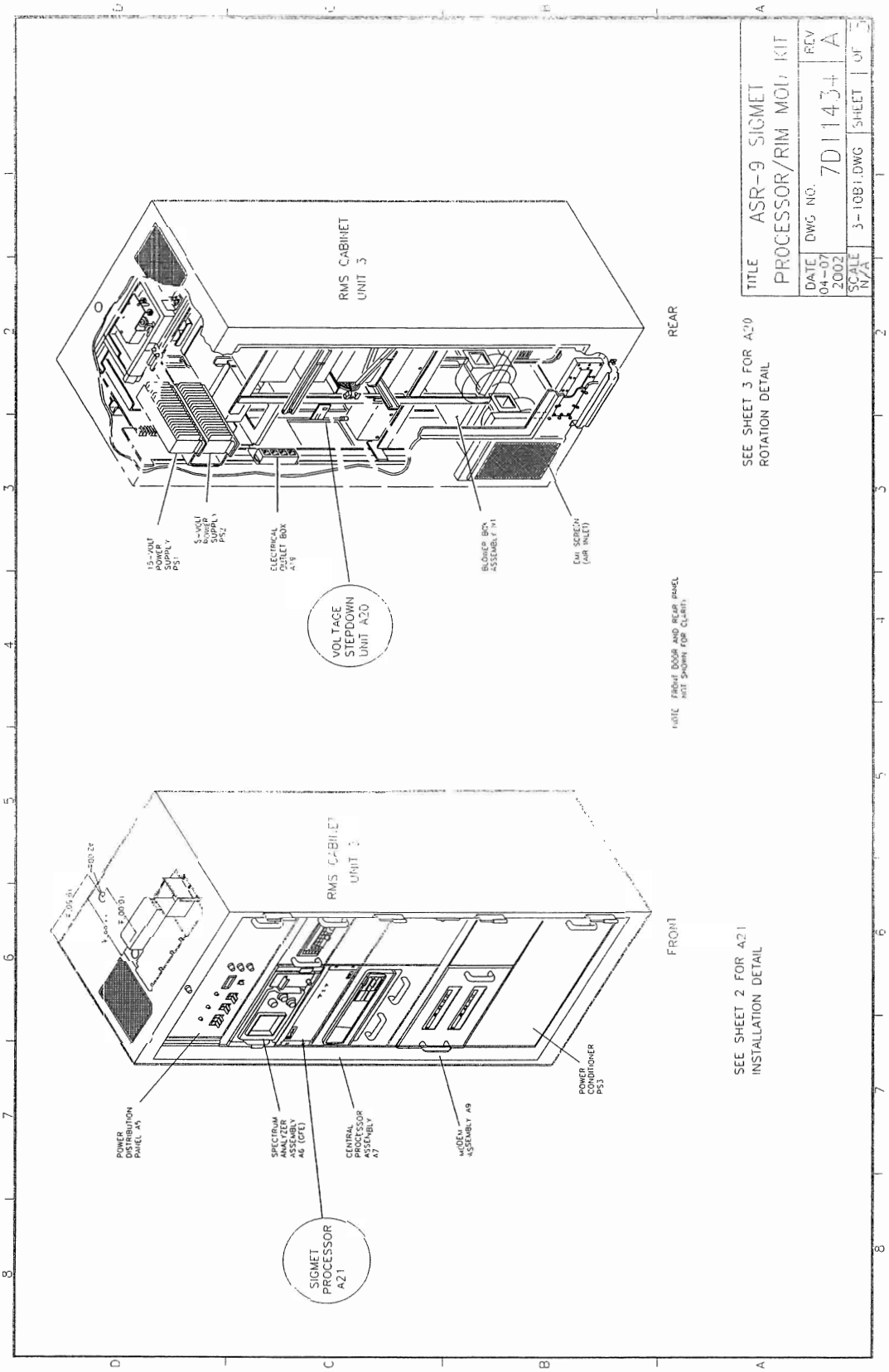

CONNECT GROUND STRAP
TO THE ASR9 GROUNDING BAR
USING 1 EA. ITEMS 244, 247, & 248
SUPPORT BRACKET
REMOVE SCREWS AND WASHERS.
DISCARD SCREWS, REUSE WASHERS.
USE ITEM 200, 249 AND PRE-EXISTING
LOCK AND FLAT WASHERS
(DISCARD ORIGINAL SCREWS)
TO SECURE THE IF RECEIVER
ASSY INSIDE THE WX SCIP
CABINET #4 IMMEDIATELY
ABOVE THE WX RCVR A3 PANEL.
THE ASSEMBLY IS MOUNTED
ON TOP OF THE SUPPORT BRACKET
SIGMET IF RCVR ASSY
INSTALLATION
SIGMET IF RECEIVER ASSY
4A12
WEATHER RECEIVER
ASSY 4A3
CROSS REFERENCE ADS-270 DWG
ASR-9-003.9 SHEET 4, REV B
WEATHER
RECEIVER/SCIP (UNIT 4) REAR VIEW
COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
SIZE CAGE CODE DWG NO.
D 97942 7D11433
SCALE N/A REV LTR C SHEET 4 OF 4
DWG NO. 7D11433 SH 4
ACAD

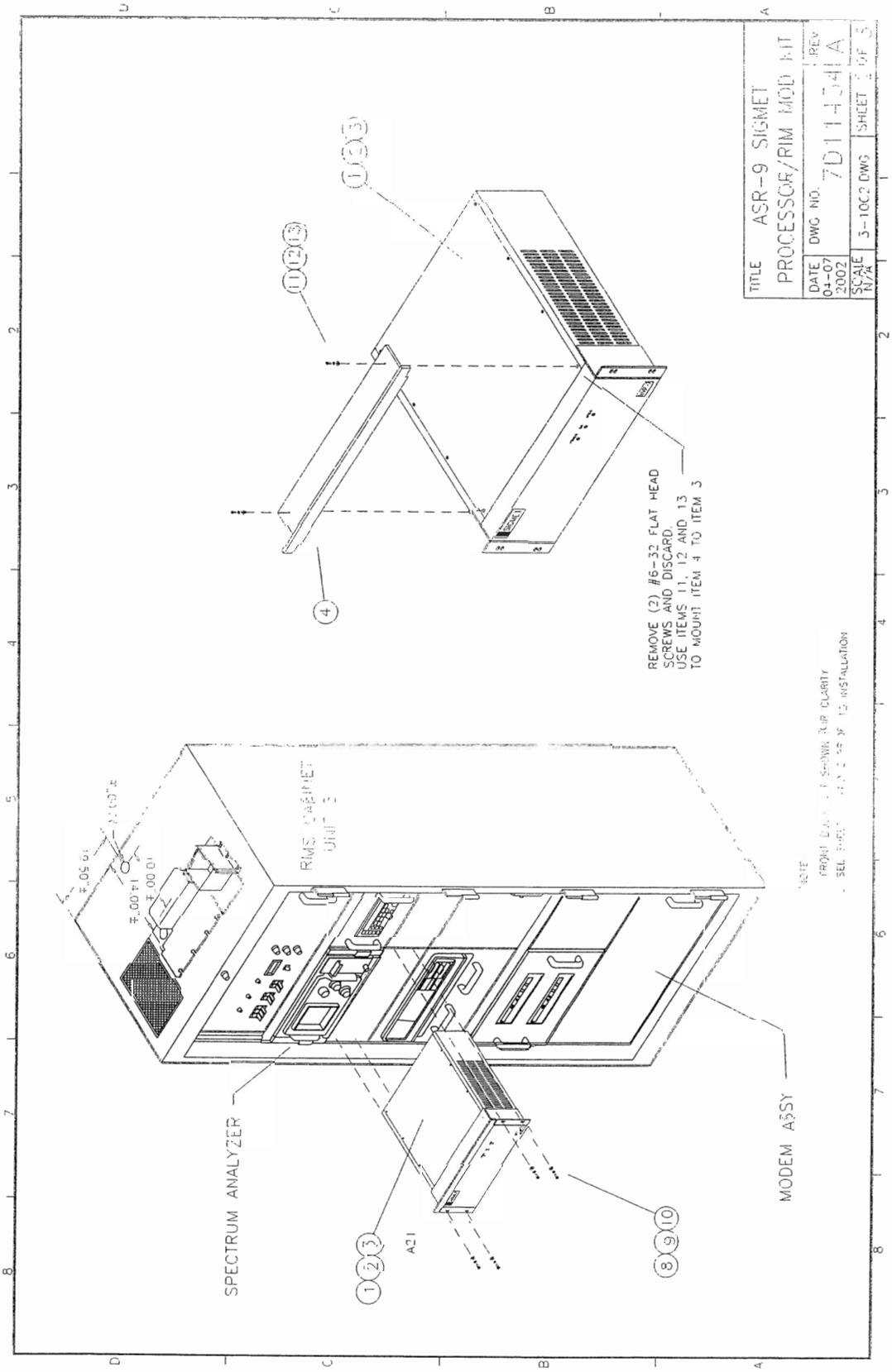
7D11434G01 Rev. A ASR-9 SIGMET PROCESSOR/RIM

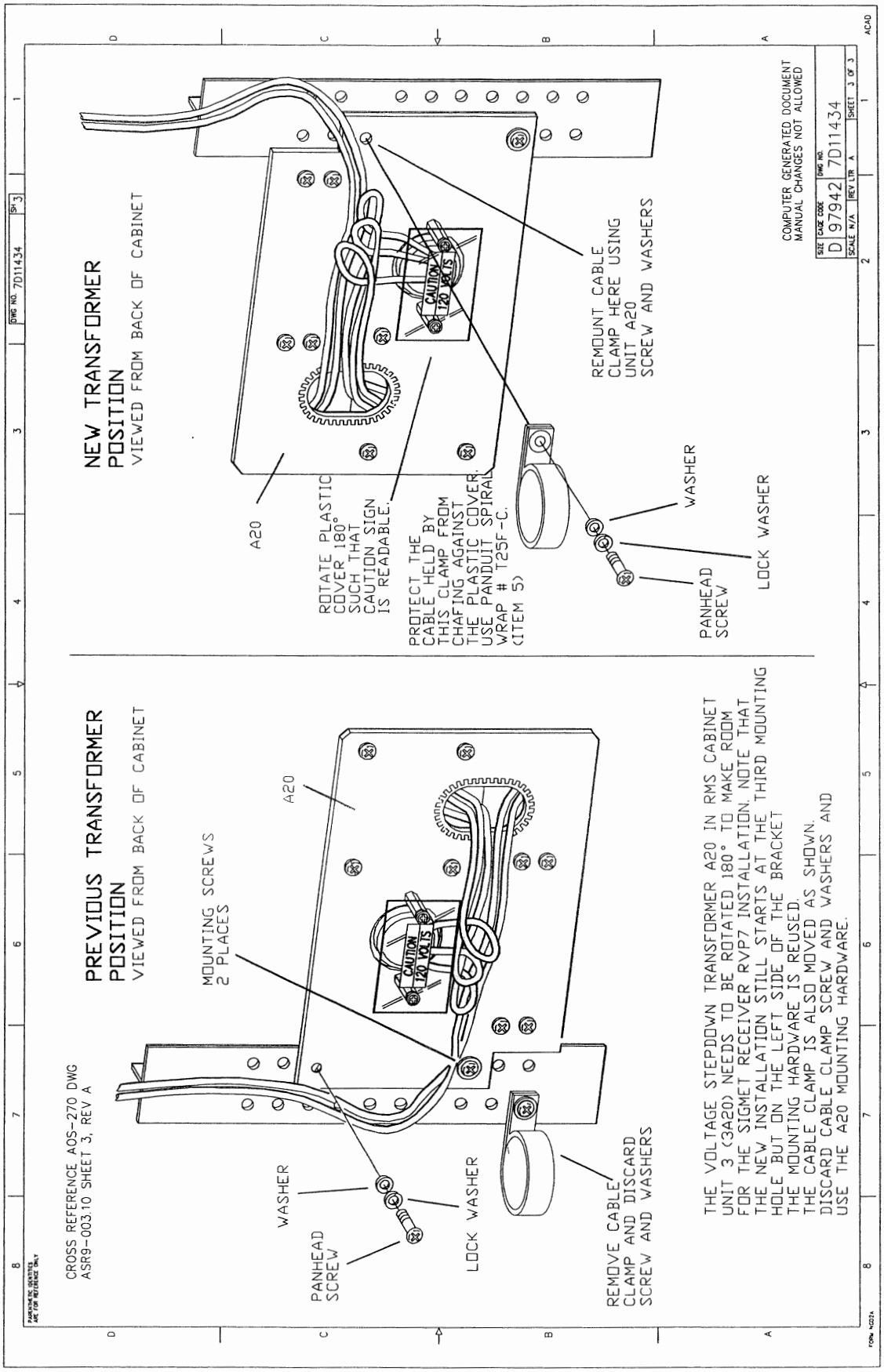
Find	Part Number	Note	Part Name	Quantity
1	7A11790G04		PREINSTALLATION CABLES, SIGMET	1 EA
2	7A11800H01	2	SIGMET PROCESSOR/RIM AND IF	1 EA
3	7A11800H02		CHASSIS BOX	1 EA
3	7A11800H02		MAIN PC BOARD	1 EA
3	7A11800H02		SIGMET PROCESSOR/RIM	1 EA
4	ASR9-003.10.1		FILLER PANEL, SIGMET SIGNAL	1 EA
5	T25F-C		SPIRAL WRAPPING, PANDUIT	1 FT
8	MS51958-63		SCREW, PAN HD (.190)	4 EA
9	MS35338-138		WASHER, LOCK-SPRING, CRES	4 EA
10	MS15795-842		WASHER, FL, (.219 DIA)	4 EA
11	MS51957-30		SCREW,PAN HD, .138-32 X .500	2 EA
12	MS35338-136		WASHER, LOCK-SPRING, CRES 3	2 EA
13	MS15795-806		WASHER, FLAT, NO. 6	2 EA

NOTES FOR: *7D11434G01*

Note 2 7A11800H01 consists of 2 parts, 7A11800H02 and 7A11800H03. 7A11800H02 will be installed at 7D11434. 7A11800H03 will be installed at 7D11433.


RMS CABINET
UNIT 3
REAR
15-VOLT POWER SUPPLY PS1
5-VOLT POWER SUPPLY PS2
ELECTRICAL OUTLET BOX A19
VOLTAGE STEPDOWN UNIT A20
BLOWER BOX ASSEMBLY A1
EMI SCREEN (AIR INLET)
NOTE: FRONT DOOR AND REAR PANEL NOT SHOWN FOR CLARITY
SEE SHEET 3 FOR A20 ROTATION DETAIL
RMS CABINET
UNIT 3
FRONT
POWER DISTRIBUTION PANEL A5
SPECTRUM ANALYZER ASSEMBLY A6 (OPT)
CENTRAL PROCESSOR ASSEMBLY A7
MODEM ASSEMBLY A9
SIGMET PROCESSOR A21
POWER CONDITIONER PS3
SEE SHEET 2 FOR A21 INSTALLATION DETAIL
TITLE ASR-9 SIGMET PROCESSOR/RIM MOD KIT
DATE 04-07-2002
DWG NO. 7D11434
REV A
SCALE N/A
3-1081.DWG
SHEET


TITLE ASR-9 SIGMET
PROCESSOR/RIM MOD KIT
DATE 04-07 2002
DWG NO. 7D114734
REV A
SCALE N/A
3-1002 DWG
SHEET 2 OF 3
REMOVE (2) #6-32 FLAT HEAD
SCREWS AND DISCARD.
USE ITEMS 11, 12 AND 13
TO MOUNT ITEM 4 TO ITEM 3
SPECTRUM ANALYZER
MODEM ASSY
A21


NEW TRANSFORMER POSITION
VIEWED FROM BACK OF CABINET
A20
ROTATE PLASTIC COVER 180° SUCH THAT CAUTION SIGN IS READABLE.
PROTECT THE CABLE HELD BY THIS CLAMP FROM CHAFING AGAINST THE PLASTIC COVER. USE PANDUIT SPIRAL WRAP # T25F-C. (ITEM 5)
CAUTION 120 VOLTS
REMOUNT CABLE CLAMP HERE USING UNIT A20 SCREW AND WASHERS
WASHER
LOCK WASHER
PANHEAD SCREW
PREVIOUS TRANSFORMER POSITION
VIEWED FROM BACK OF CABINET
MOUNTING SCREWS 2 PLACES
A20
CAUTION 120 VOLTS
WASHER
PANHEAD SCREW
LOCK WASHER
REMOVE CABLE CLAMP AND DISCARD SCREW AND WASHERS
CROSS REFERENCE AOS-270 DWG ASR9-003.10 SHEET 3, REV A
THE VOLTAGE STEPDOWN TRANSFORMER A20 IN RMS CABINET UNIT 3 (3A20) NEEDS TO BE ROTATED 180° TO MAKE ROOM FOR THE SIGMET RECEIVER RVP7 INSTALLATION. NOTE THAT THE NEW INSTALLATION STILL STARTS AT THE THIRD MOUNTING HOLE BUT ON THE LEFT SIDE OF THE BRACKET
THE MOUNTING HARDWARE IS REUSED.
THE CABLE CLAMP IS ALSO MOVED AS SHOWN.
DISCARD CABLE CLAMP SCREW AND WASHERS AND USE THE A20 MOUNTING HARDWARE.
COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
SIZE CAGE CODE DWG NO.
D 97942 7D11434
SCALE N/A REV LTR A SHEET 3 OF 3
DWG NO. 7D11434 SH 3
ACAD

7D11435G01 Rev. A ASR-9 PROC. MOD KIT

Find	*Part Number*	*Note*	*Part Name*	*Quantity*
1	7D11436G01		CCA, STC	1 EA
2	10F7567		WIRE WRAP, WIRE 30 AWG BLUE,	1 EA
3	10F7607		WIRE WRAP, WIRE 28 AWG BLUE,	1 EA
5	7A11790G05		PREINSTALLATION CABLES, ASR-9	1 EA
	(7A11903G12, G13, G14)			
6	7A11795H31		MARKER	1 EA
7	7A11745H01		LENS, WSP	4 EA
8	7A11745H02		LENS, 6WX AL/WSP AL	4 EA

NOTES FOR: *7D11435G01*

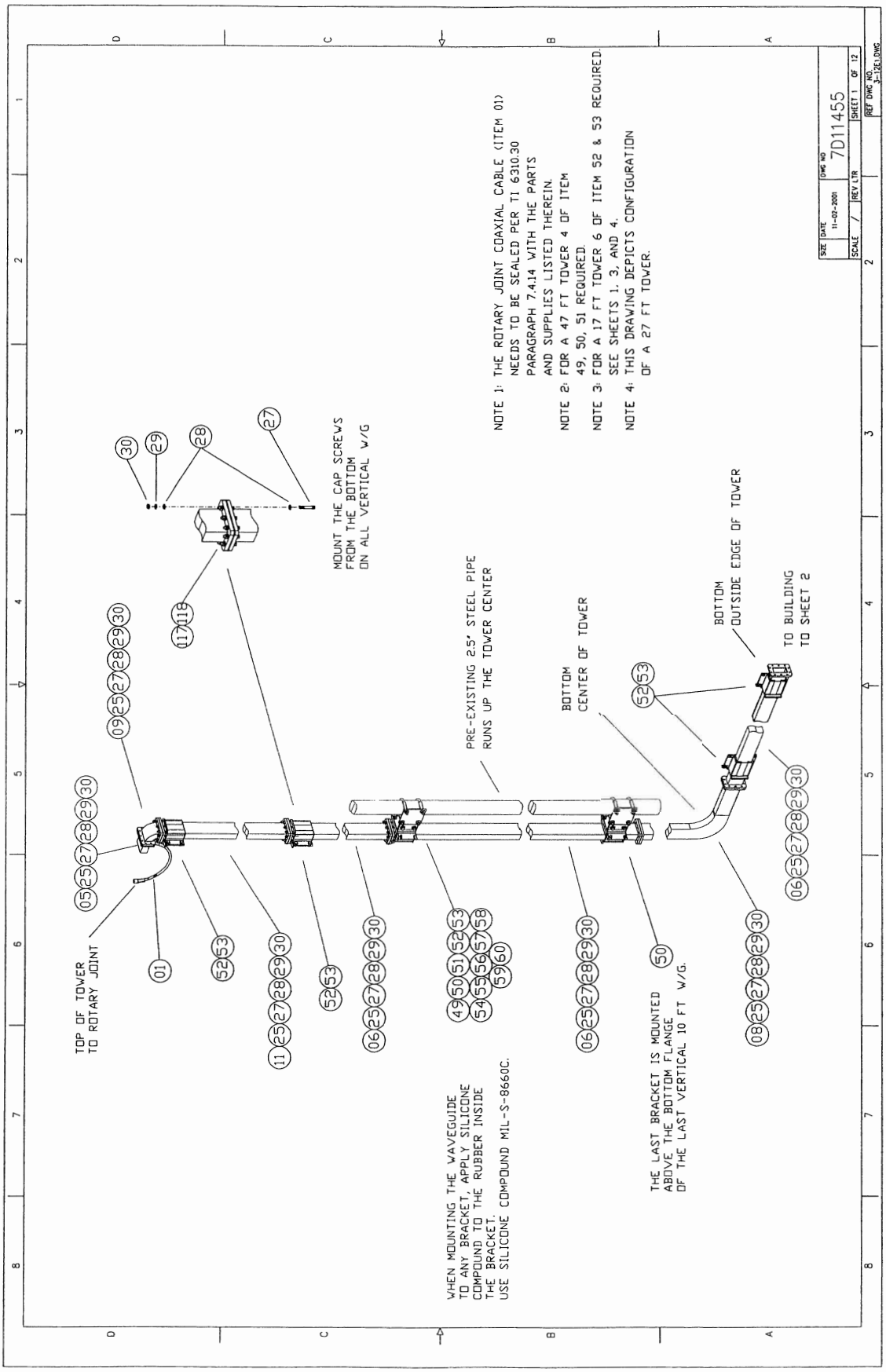
All material in this parts list will be installed using 7A11725 preinstallation instructions.

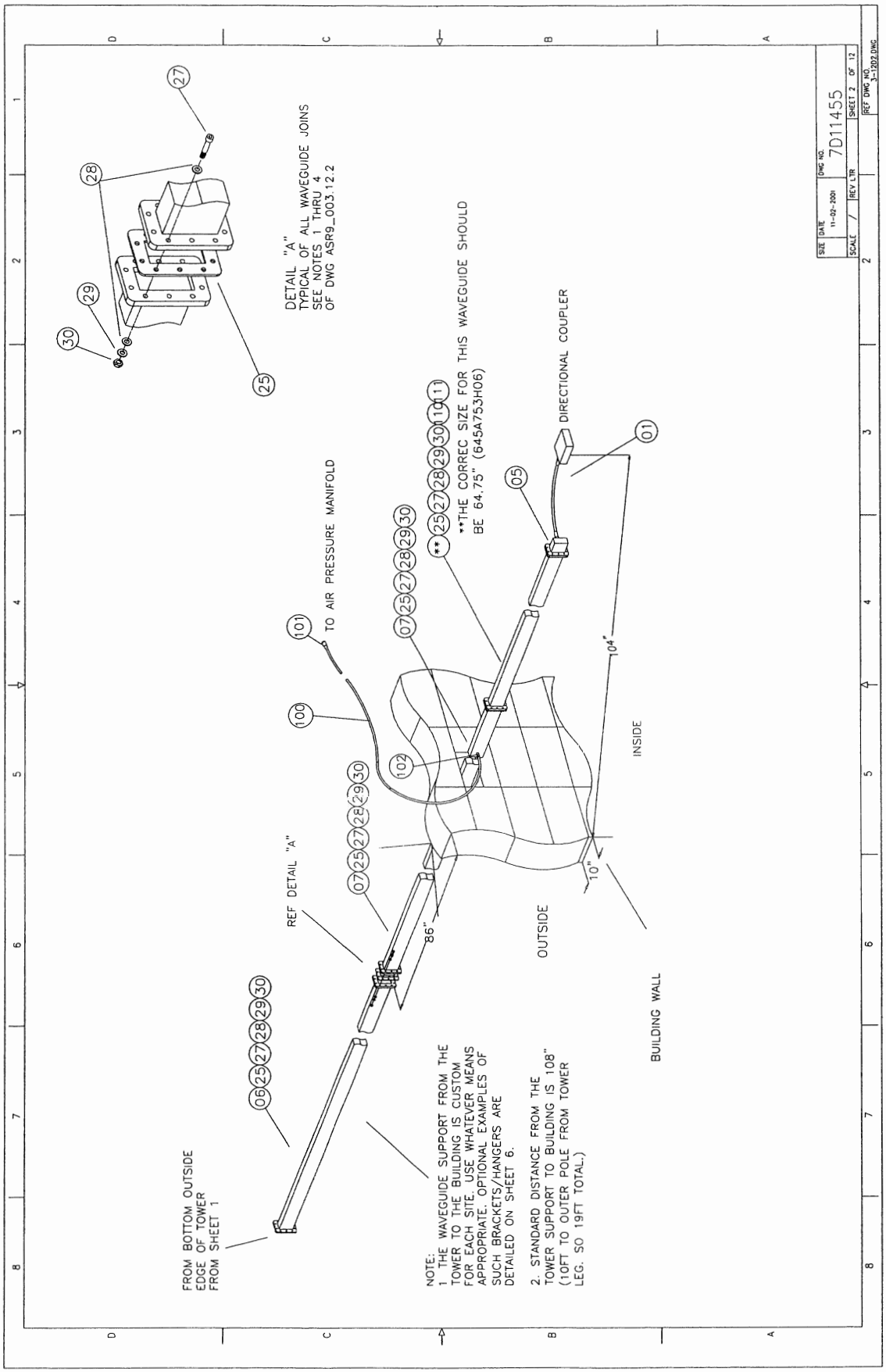
7D11455G01 Rev. E ANTENNA W/G REPLACEMENT KIT

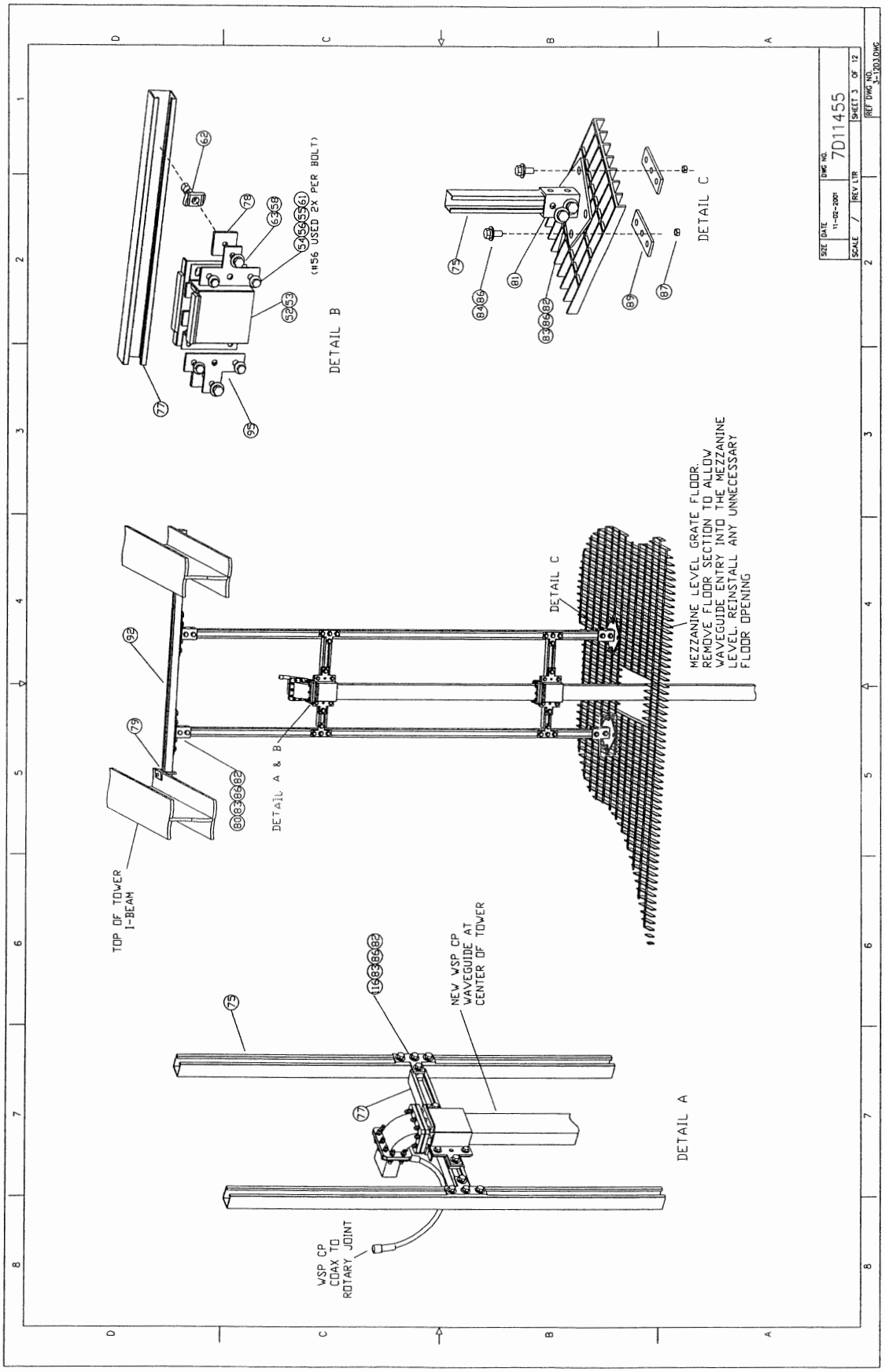
Find	Part Number	Note	Part Name	Quantity
1	7A11790G02		PREINSTALLATION CABLES, ANT	1 EA
2	221213		CONNECTOR/SPLICE WEATHERPROOF	1 EA
3	53351GK		SEALANT, ELECTRICAL, RUBBER	1 AR
5	645A771H01		ADAPTER,WG TO COAX	2 EA
6	645A753H03		WAVEGUIDE,RIGID	2 EA
7	645A753H01		W/G,RIGID	1 EA
8	7A11819H05		FLEXIBLE WAVEGUIDE	1 EA
9	645A752H01		W/G,ELBOW	1 EA
10	645A753H04		WAVEGUIDE	1 EA
11	645A753H13		WAVEGUIDE, RIGID	1 EA
14	645A753H14		WAVEGUIDE,RIGID	1 EA
14	645A753H14		WAVEGUIDE,RIGID	1 EA
25	M24211/2-005		GASKET	9 EA
27	MS16996-26		SCREW,CAP,SOCKET HD, .250-2811	6 EA
28	AN960C416		WASHER, FLAT	260 EA
29	MS35338-139		WASHER, LOCK-SPRING (.250 D	116 EA
30	MS35650-3254		NUT,PLAIN,HEX (.250-28)	110 EA
49	ASR9-003.12.1.4		BRACKET, ASR9 WAVEGUIDE, WS	1 EA
50	ASR9-003.12.1.1		PLATE, ASR9 WAVEGUIDE, WSP	1 EA
51	ASR9-003.12.1.3		BRACKET, ASR9 WAVEGUIDE, WS	1 EA
52	ASR9-003.12.1.5.1		PLATE ASS'Y, ASR9 WAVEGUIDE	6 EA
53	ASR9-003.12.1.5.2		BRACKET ASS'Y, ASR9 WAVEGUIDE	6 EA
54	MS35307-336		SCREW,CAP HEX HD .312-18 X 1	28 EA

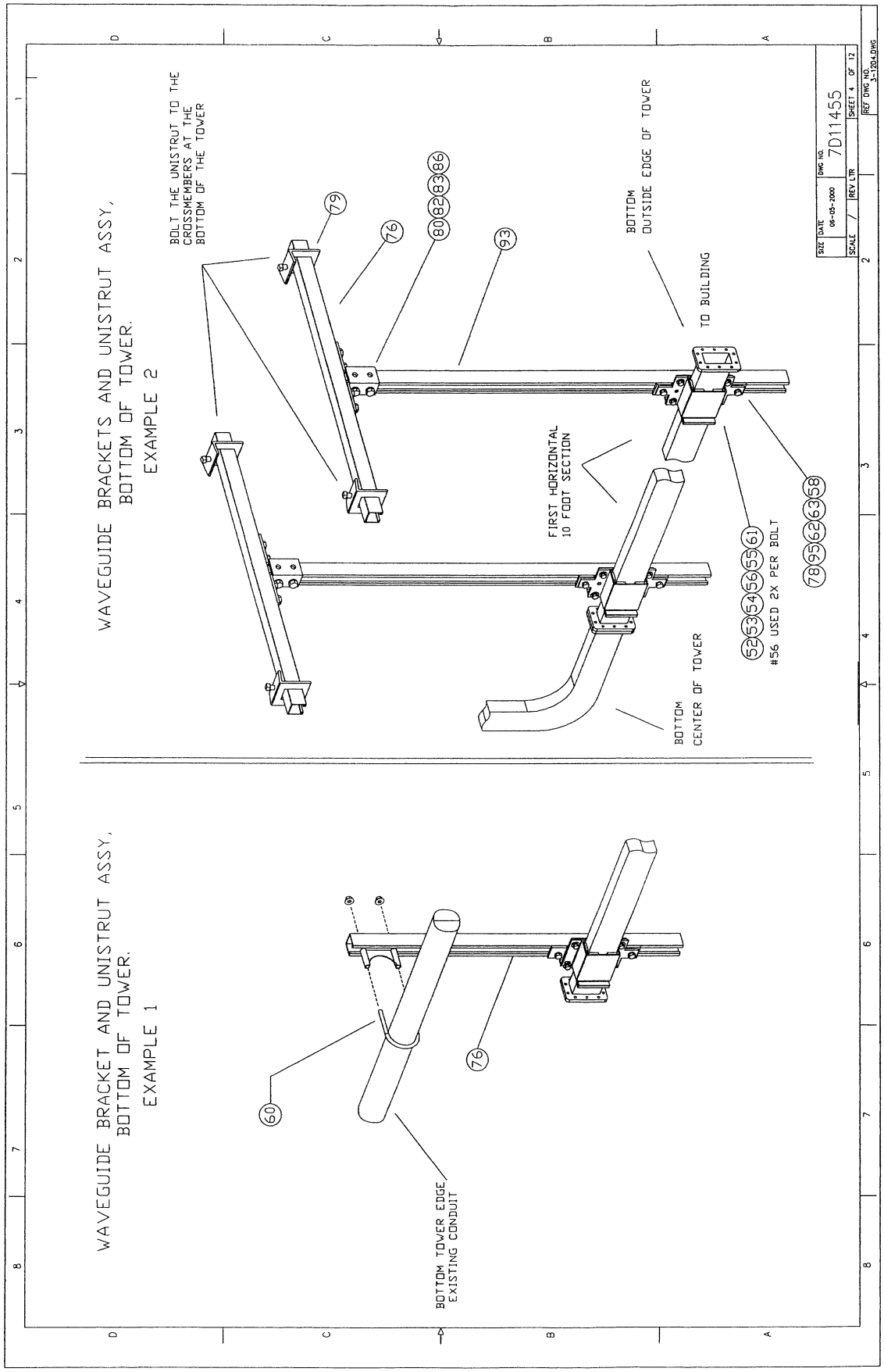
Find	Part Number	Note	Part Name	Quantity
55	MS35338-140		WASHER, LOCK-SPRING, CRES 3	28 EA
56	NAS1149C0563R		WASHER,FLAT,300 CRES, PASS,	48 EA
57	MS35307-360		SCREW,CAP,HEX	4 EA
58	MS35338-141		WASHER, LOCK-SPRING, CRES	14 EA
59	NAS1149C0663R		WASHER,FLAT,300 CRES, PASS,	4 EA
60	3042T58		U-BOLT, 2.75 IN PIPE, 3/8-1	4 EA
61	MS35649-2314		NUT,HEX	20 EA
62	P1008HG		NUT, UNISTRUT (3/8"-16)	10 EA
63	MS35307-364		BOLT, MODIFIED	10 EA
75	7D11455H01		UNISTRUT, 96.0 INCH	4 EA
76	7D11455H02		UNISTRUT, 36.0 INCH	2 EA
77	7D11455H03		UNISTRUT, 24.0 INCH	3 EA
78	P1063HG		FLAT SQUARE 1.625 IN WASHER	10 EA
79	P1796SHG		BEAM HANGER, UNISTRUT	10 EA
80	P2347HG		WING SHAPED FITTING, JOINER,	6 EA
81	P2072AHG		POST BASE. UNISTRUT	2 EA
82	P1010		UNISTRUT,NUT	80 EA
83	MS35307-411		BOLT,HEX HD,.500-13UNC X1.25	80 EA
84	MS35307-417		SCREW,CAP,HEX HD	16 EA
86	MS35338-143		WASHER, LOCK-SPRING, CRES	96 EA
87	MS35691-35		NUT, JAM HEX	16 EA
88	7D11455H04		UNISTRUT, 14.0 INCHL	1 EA
89	P1925HG		PLATE, FLAT FITTING, 3 X 1.	4 EA
91	P1359HG		ANGLE FITTING, 90	1 EA
92	D11455H05		UNISTRUT, 78.0 INCH	3 EA

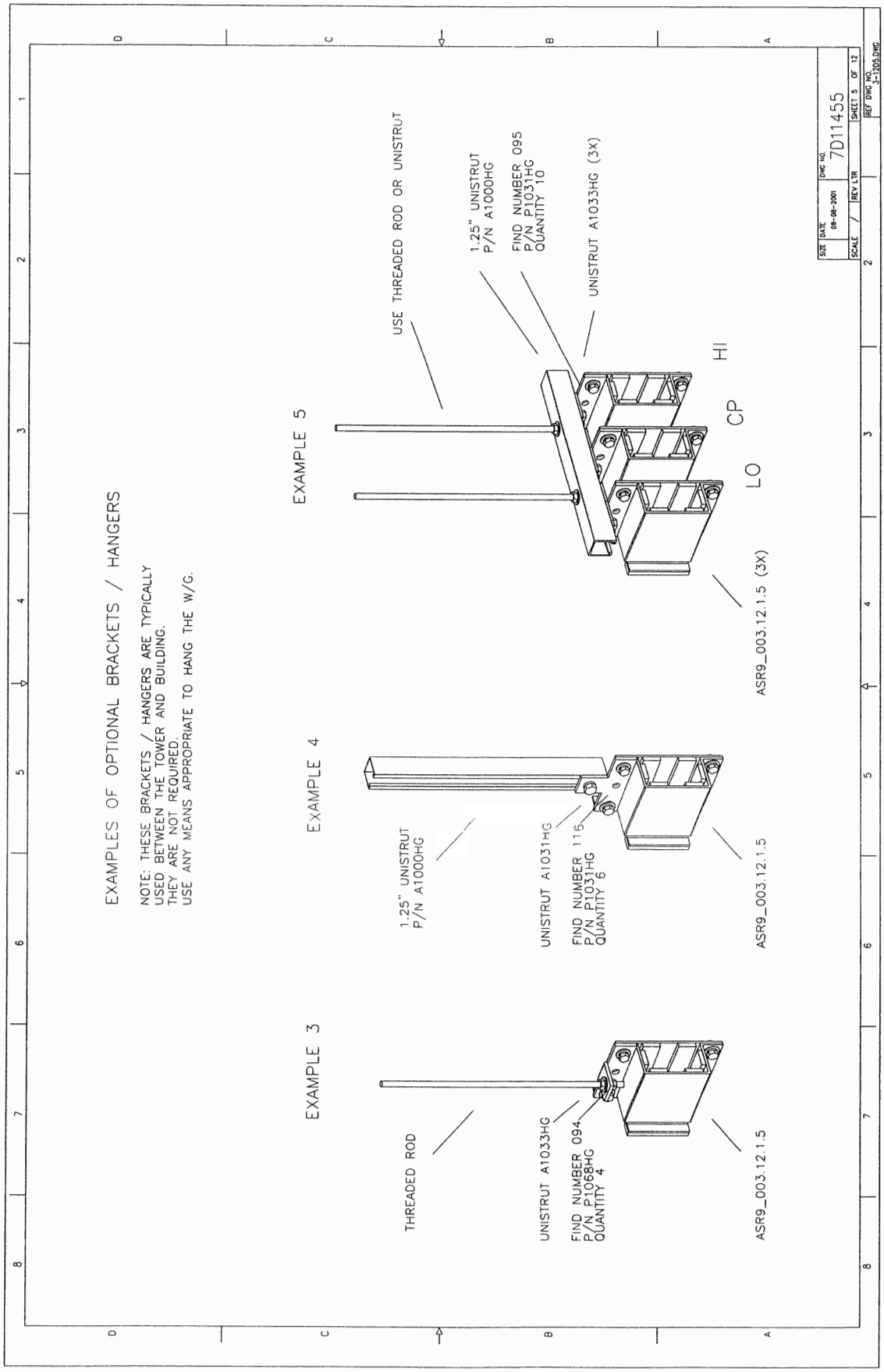
Find	Part Number	Note	Part Name	Quantity
93	7D11455H06		UNISTRUT, 48.0 INCH	2 EA
94	P1068HG		ANGLE FITTING, 90 DEGREE	4 EA
95	A1031HG		PLATE, FLAT FITTING, TEE	10 EA
100	66PPBK		TUBING, IMPOLENE	600 IN
101	268PF-6A		FITTING, 1/8 NPT TO 3/8 TUBE	1 EA
102	269P06X02		FITTING, 90 DEG, 1/8NPT TO	1 EA
110	156C337G01		HANGER,W/G,NO 1	2 EA
111	156C339G02		BRACKET	2 EA
112	90034A029		THREADED ROD, STEEL, .250-20	2 EA
113	MS35649-2254		NUT,PLAIN,HEX (.250-20)	6 EA
115	7D11455H07		UNISTRUT, 9.5 INCH	1 EA
116	P1031HG		PLATE, FLAT FITTING, TEE, 1.	6 EA
118	32240DH		PRIMER, ZINC CHROMATE	1 GA
900	7D11455		KIT, ANT WG REPLACEMENT, 17	1 DOC
901	ASR9-003.12		ASSEMBLY, ASR9 WAVEGUIDE, WS	1 DOC
902	ASR9-003.12.1		BRACKET ASSY, ASR9 WAVEGUIDE	1 DOC
903	ASR9-003.12.2		HARDWARE ASSY, ASR9 WAVEGUIDE	1 DOC

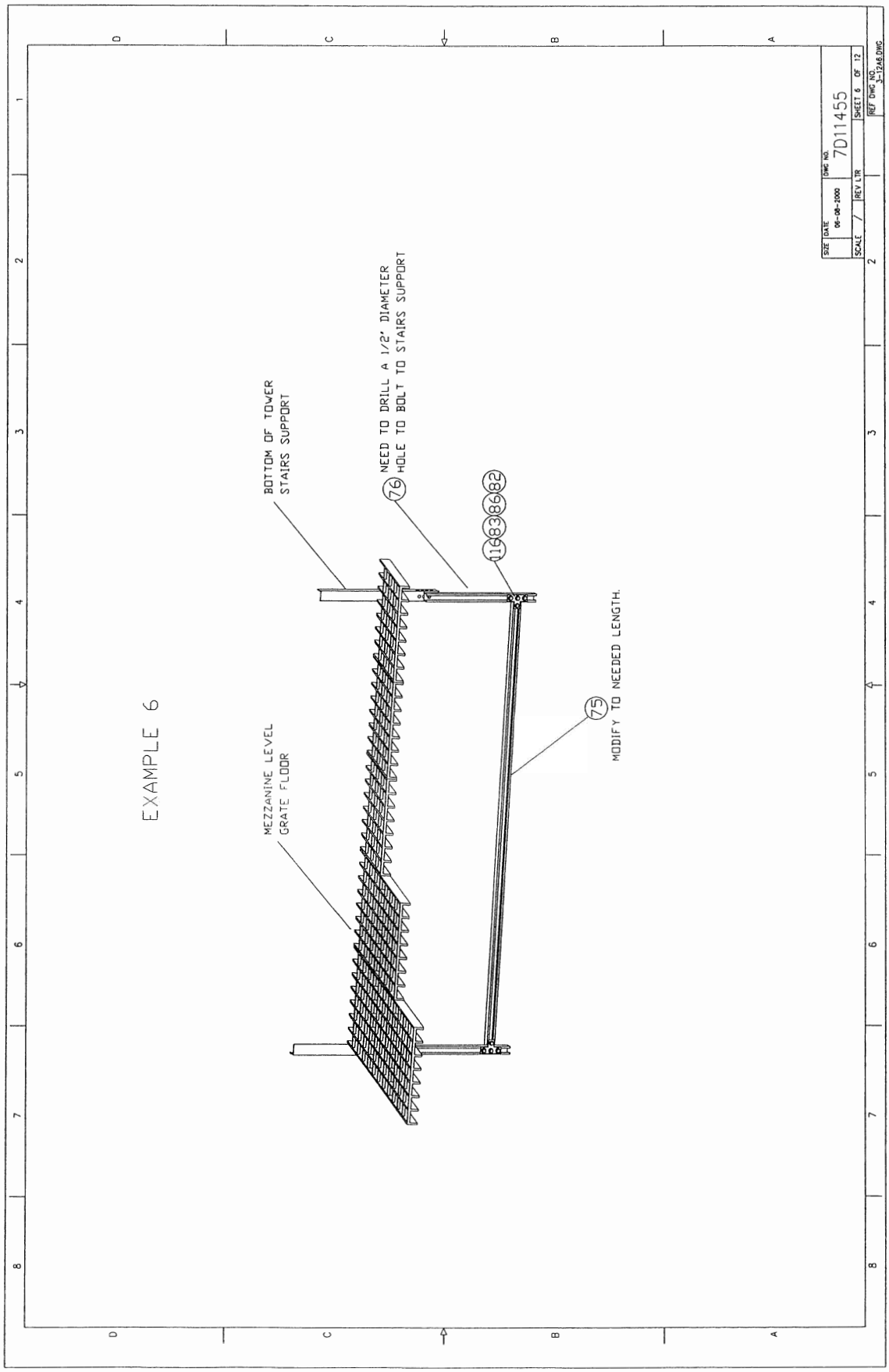

NOTE 1: THE ROTARY JOINT COAXIAL CABLE (ITEM 01) NEEDS TO BE SEALED PER TI 6310.30 PARAGRAPH 7.4.14 WITH THE PARTS AND SUPPLIES LISTED THEREIN.
NOTE 2: FOR A 47 FT TOWER 4 OF ITEM 49, 50, 51 REQUIRED.
NOTE 3: FOR A 17 FT TOWER 6 OF ITEM 52 & 53 REQUIRED. SEE SHEETS 1, 3, AND 4.
NOTE 4: THIS DRAWING DEPICTS CONFIGURATION OF A 27 FT TOWER.
MOUNT THE CAP SCREWS FROM THE BOTTOM ON ALL VERTICAL W/G
PRE-EXISTING 2.5" STEEL PIPE RUNS UP THE TOWER CENTER
BOTTOM CENTER OF TOWER
BOTTOM OUTSIDE EDGE OF TOWER
TO BUILDING TO SHEET 2
TOP OF TOWER TO ROTARY JOINT
WHEN MOUNTING THE WAVEGUIDE TO ANY BRACKET, APPLY SILICONE COMPOUND TO THE RUBBER INSIDE THE BRACKET. USE SILICONE COMPOUND MIL-S-8660C.
THE LAST BRACKET IS MOUNTED ABOVE THE BOTTOM FLANGE OF THE LAST VERTICAL 10 FT W/G.
SIZE
DATE 11-02-2001
DWG NO 7D11455
SCALE /
REV LTR
SHEET 1 OF 12
REF DWG NO. 3-12E1.DWG

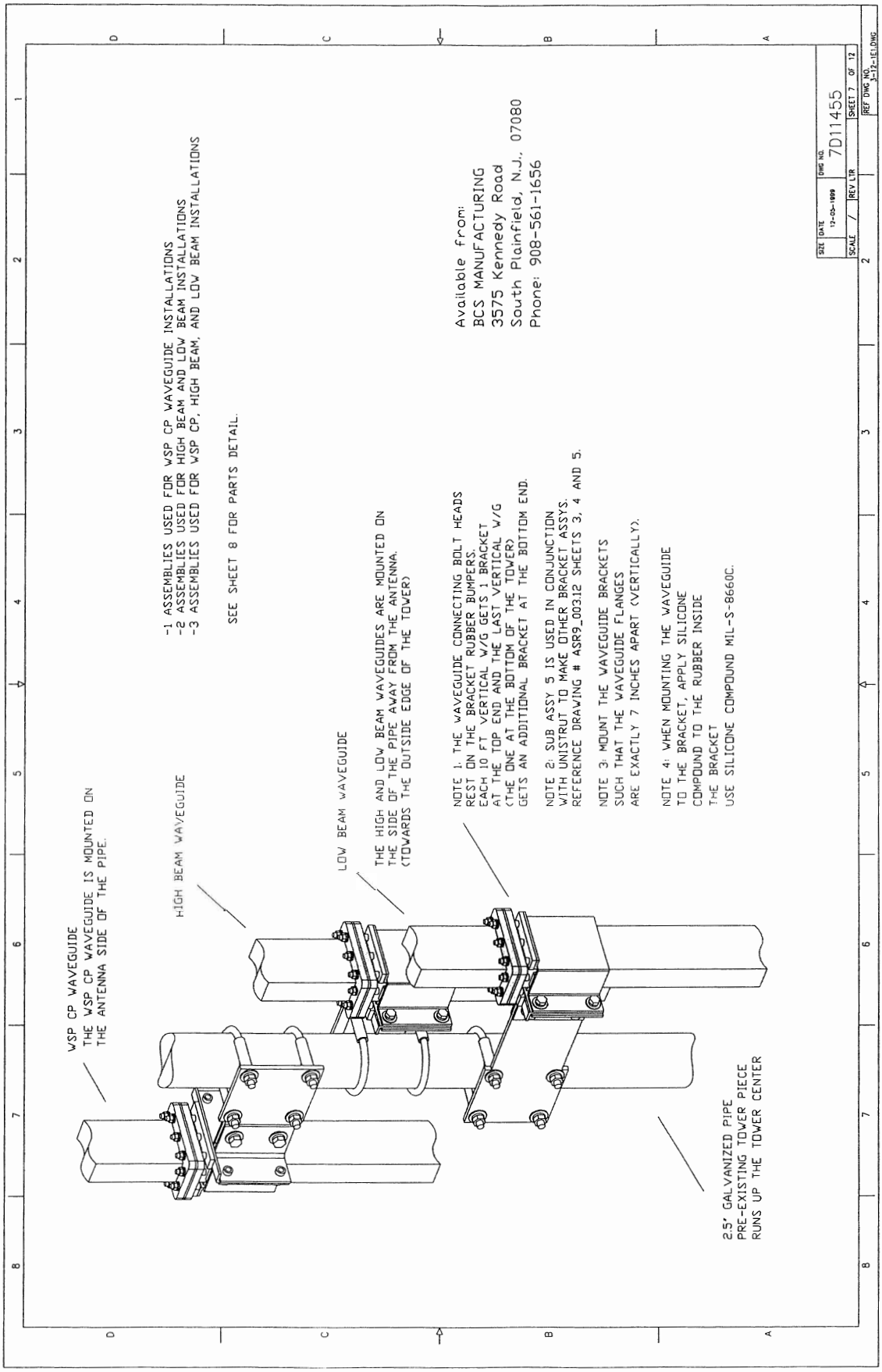

DETAIL "A"
TYPICAL OF ALL WAVEGUIDE JOINS
SEE NOTES 1 THRU 4
OF DWG ASR9_003.12.2
TO AIR PRESSURE MANIFOLD
**THE CORREC SIZE FOR THIS WAVEGUIDE SHOULD
BE 64.75" (645A753H06)
DIRECTIONAL COUPLER
REF DETAIL "A"
86"
104"
10"
OUTSIDE
INSIDE
BUILDING WALL
FROM BOTTOM OUTSIDE
EDGE OF TOWER
FROM SHEET 1
NOTE:
1 THE WAVEGUIDE SUPPORT FROM THE
TOWER TO THE BUILDING IS CUSTOM
FOR EACH SITE. USE WHATEVER MEANS
APPROPRIATE. OPTIONAL EXAMPLES OF
SUCH BRACKETS/HANGERS ARE
DETAILED ON SHEET 6.
2. STANDARD DISTANCE FROM THE
TOWER SUPPORT TO BUILDING IS 108"
(10FT TO OUTER POLE FROM TOWER
LEG. SO 19FT TOTAL.)
SIZE
DATE
11-02-2001
DWG NO
7D11455
SCALE
REV LTR
SHEET 2 OF 12
REF DWG NO
3-1202.DWG

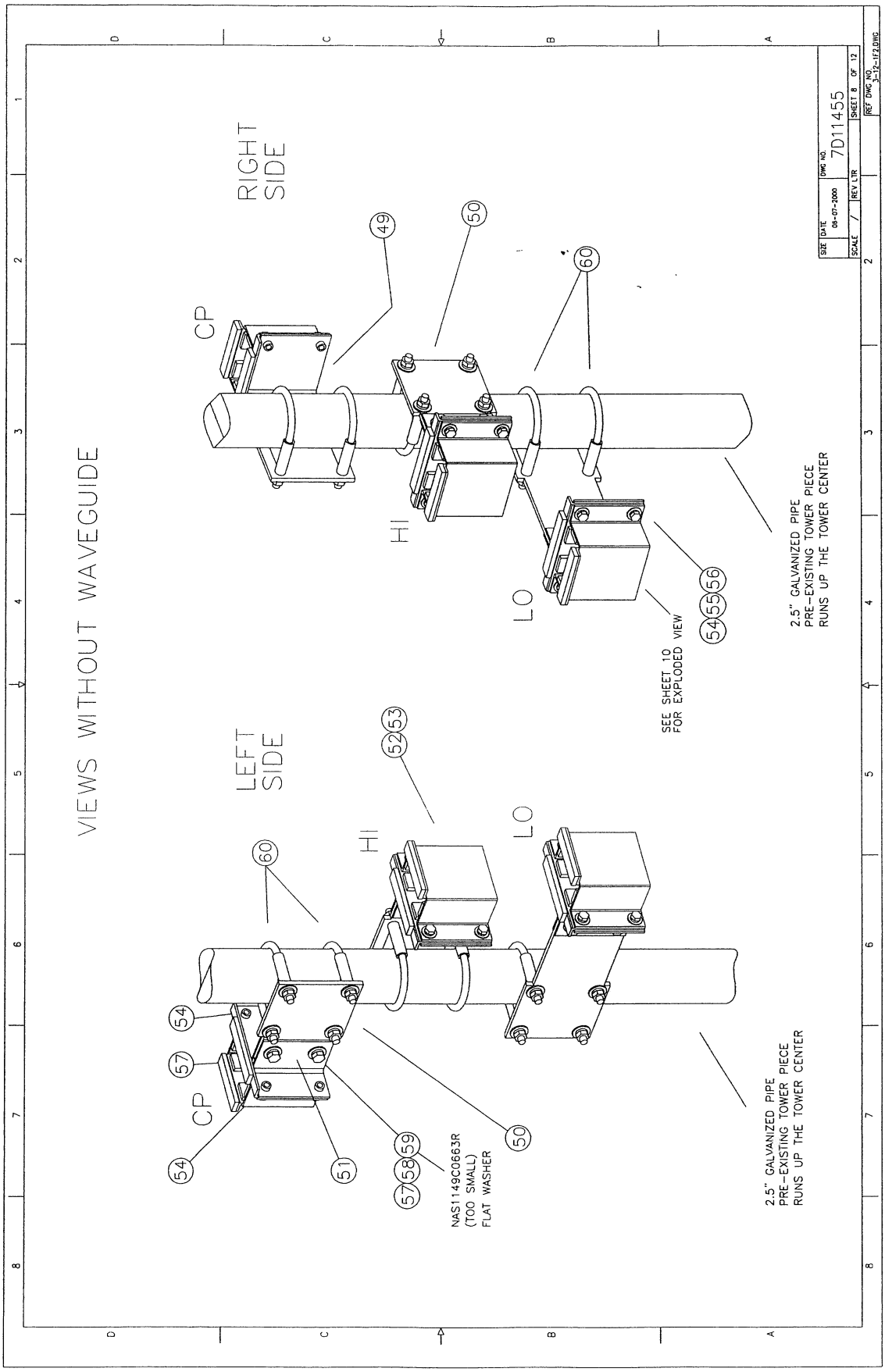

DETAIL B
(#56 USED 2X PER BOLT)
DETAIL C
DETAIL A & B
DETAIL C
MEZZANINE LEVEL GRATE FLOOR.
REMOVE FLOOR SECTION TO ALLOW
WAVEGUIDE ENTRY INTO THE MEZZANINE
LEVEL. REINSTALL ANY UNNECESSARY
FLOOR OPENING
TOP OF TOWER
I-BEAM
NEW WSP CP
WAVEGUIDE AT
CENTER OF TOWER
DETAIL A
WSP CP
COAX TO
ROTARY JOINT
SIZE
DATE
11-02-2001
DWG NO.
7D11455
SHEET 3 OF 12
SCALE
REV LTR
REF DWG NO.
J-1203.DWG

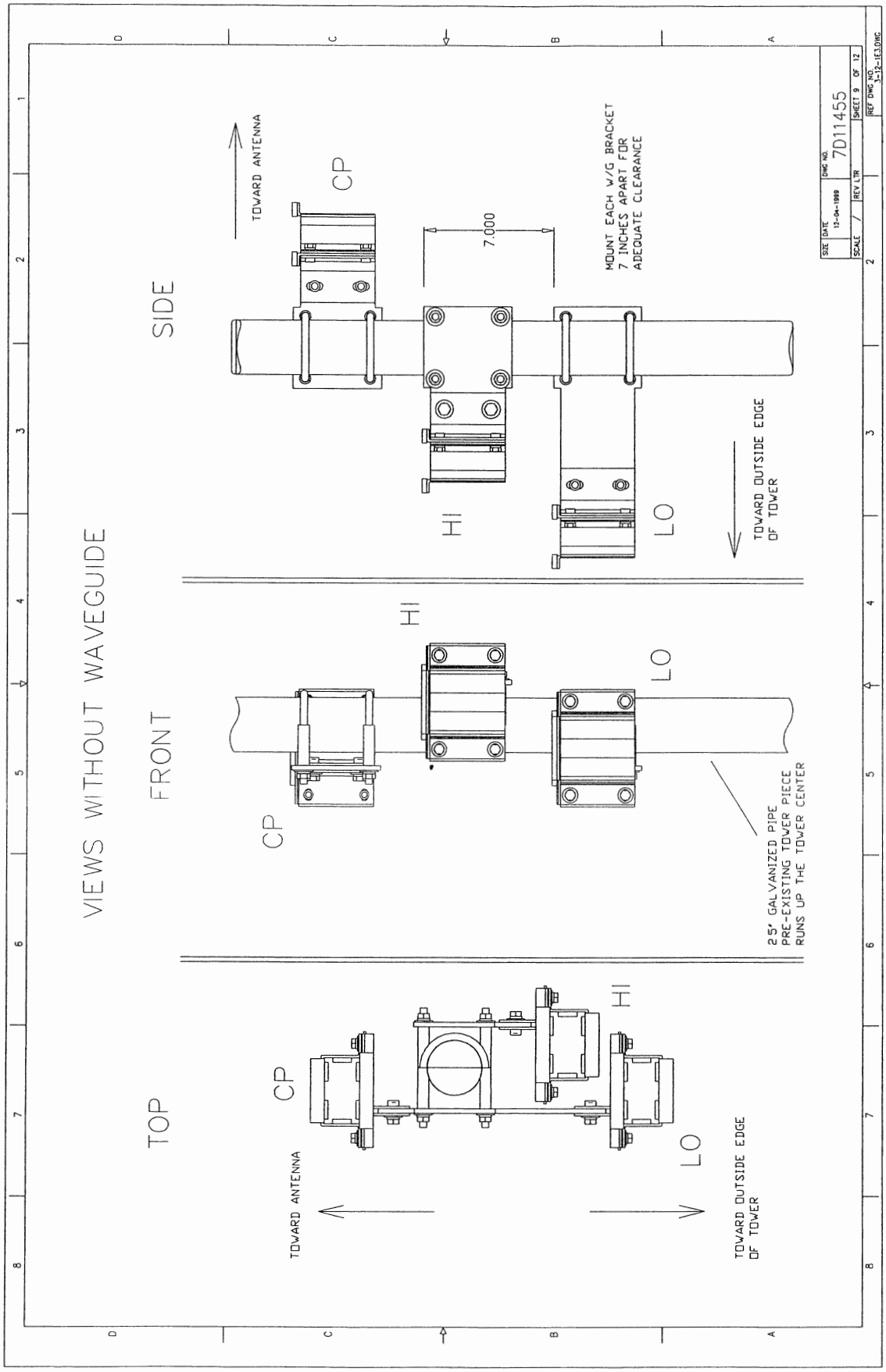

WAVEGUIDE BRACKETS AND UNISTRUT ASSY,
BOTTOM OF TOWER.
EXAMPLE 2
BOLT THE UNISTRUT TO THE
CROSSMEMBERS AT THE
BOTTOM OF THE TOWER
79
76
80 82 83 86
93
BOTTOM
OUTSIDE EDGE OF TOWER
TO BUILDING
FIRST HORIZONTAL
10 FOOT SECTION
78 95 62 63 58
52 53 54 56 55 61
#56 USED 2X PER BOLT
BOTTOM
CENTER OF TOWER
WAVEGUIDE BRACKET AND UNISTRUT ASSY,
BOTTOM OF TOWER.
EXAMPLE 1
60
76
BOTTOM TOWER EDGE
EXISTING CONDUIT
SIZE
DATE
06-05-2000
DWG NO.
7D11455
SCALE
REV LTR
SHEET 4 OF 12
REF DWG NO.
SP-3924.DWG

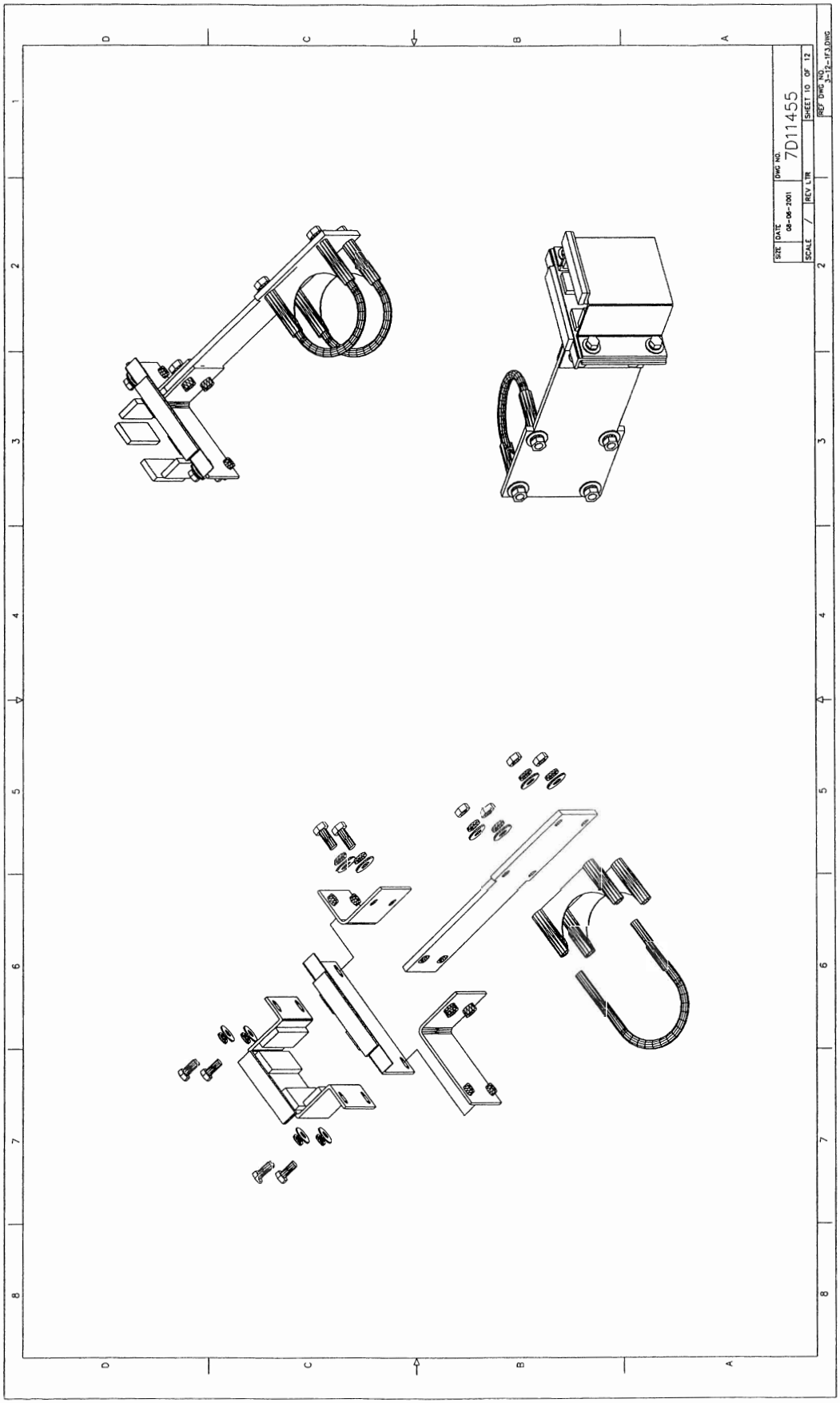

EXAMPLES OF OPTIONAL BRACKETS / HANGERS
NOTE: THESE BRACKETS / HANGERS ARE TYPICALLY USED BETWEEN THE TOWER AND BUILDING. THEY ARE NOT REQUIRED. USE ANY MEANS APPROPRIATE TO HANG THE W/G.
EXAMPLE 3
THREADED ROD
UNISTRUT A1033HG
FIND NUMBER 094
P/N P1068HG
QUANTITY 4
ASR9_003.12.1.5
EXAMPLE 4
1.25" UNISTRUT
P/N A1000HG
UNISTRUT A1031HG
FIND NUMBER 115
P/N P1031HG
QUANTITY 6
ASR9_003.12.1.5
EXAMPLE 5
USE THREADED ROD OR UNISTRUT
1.25" UNISTRUT
P/N A1000HG
FIND NUMBER 095
P/N P1031HG
QUANTITY 10
UNISTRUT A1033HG (3X)
ASR9_003.12.1.5 (3X)
HI
CP
LO
SIZE
DATE
06-06-2001
DWG NO.
7D11455
SCALE
REV LTR
SHEET 5 OF 12
REF DWG NO.
5-1205.DWG

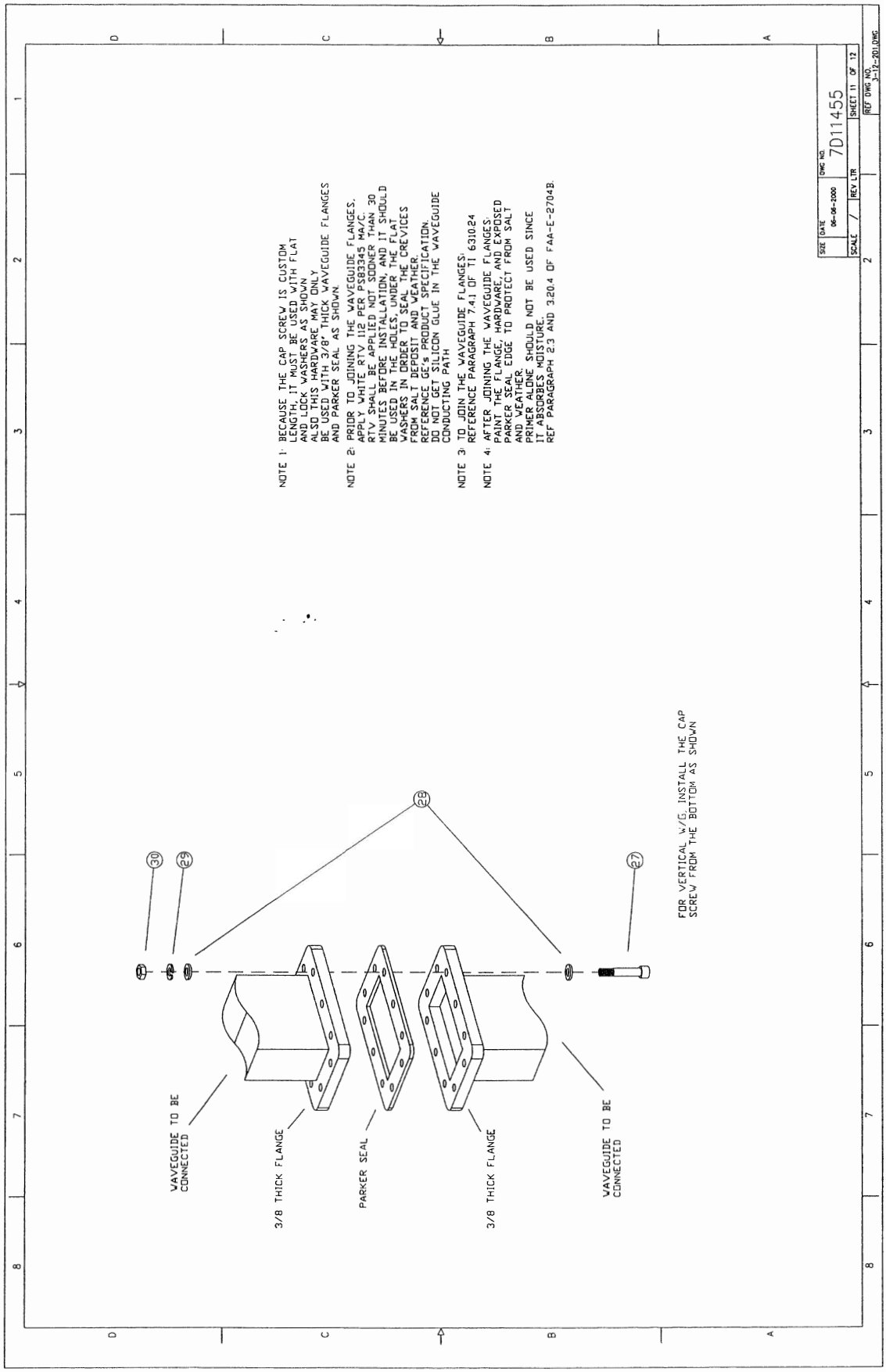

EXAMPLE 6
MEZZANINE LEVEL
GRATE FLOOR
BOTTOM OF TOWER
STAIRS SUPPORT
NEED TO DRILL A 1/2" DIAMETER
HOLE TO BOLT TO STAIRS SUPPORT
76
1
83
86
82
75
MODIFY TO NEEDED LENGTH.
SIZE
DATE
06-08-2000
DWG NO.
7D11455
SCALE
/
REV LTR
SHEET 6 OF 12
REF DWG NO.
2-1246.DWG

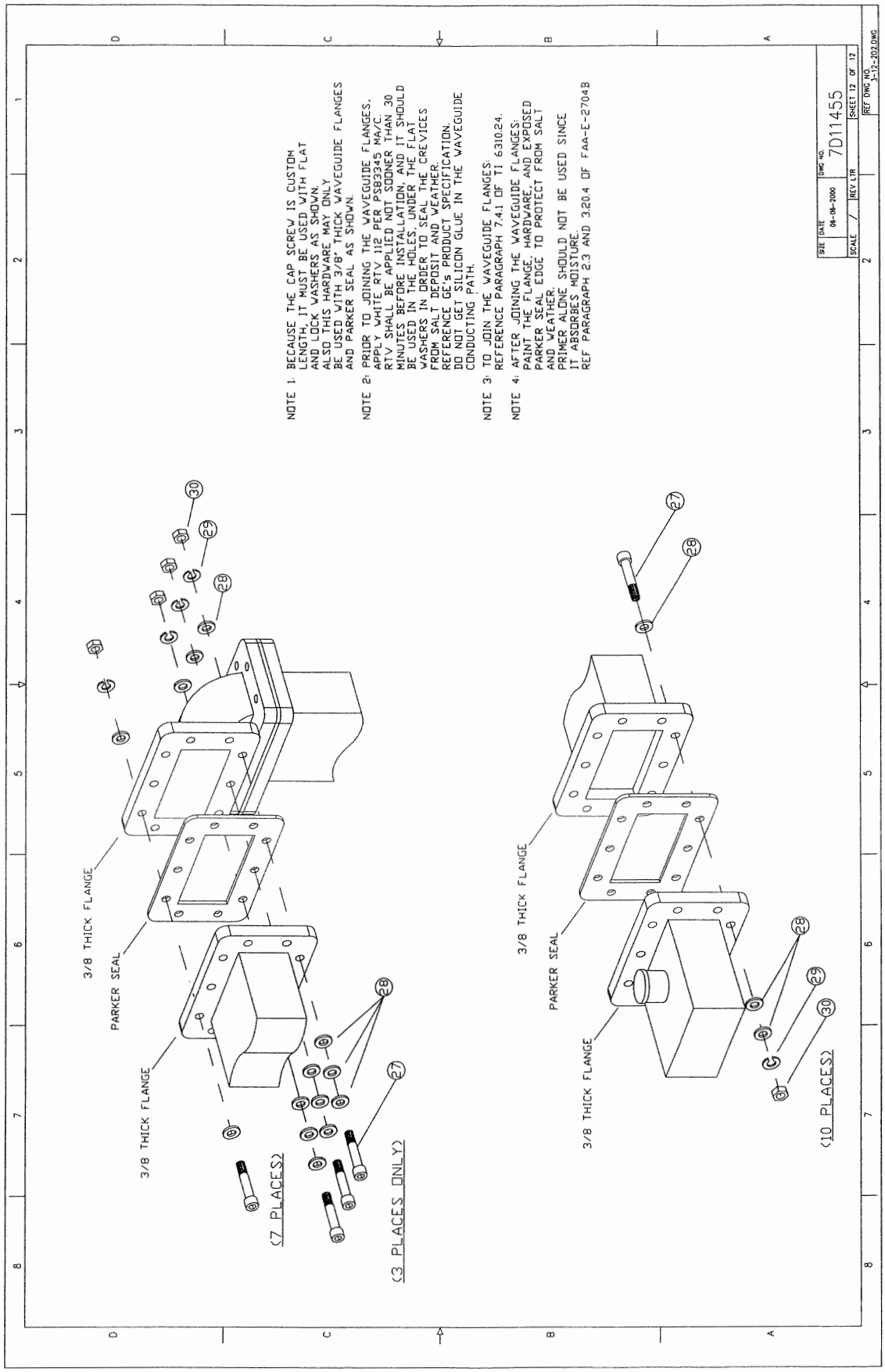

WSP CP WAVEGUIDE
THE WSP CP WAVEGUIDE IS MOUNTED ON
THE ANTENNA SIDE OF THE PIPE.
HIGH BEAM WAVEGUIDE
LOW BEAM WAVEGUIDE
THE HIGH AND LOW BEAM WAVEGUIDES ARE MOUNTED ON
THE SIDE OF THE PIPE AWAY FROM THE ANTENNA.
(TOWARDS THE OUTSIDE EDGE OF THE TOWER)
-1 ASSEMBLIES USED FOR WSP CP WAVEGUIDE INSTALLATIONS
-2 ASSEMBLIES USED FOR HIGH BEAM AND LOW BEAM INSTALLATIONS
-3 ASSEMBLIES USED FOR WSP CP, HIGH BEAM, AND LOW BEAM INSTALLATIONS
SEE SHEET 8 FOR PARTS DETAIL.
NOTE 1: THE WAVEGUIDE CONNECTING BOLT HEADS
REST ON THE BRACKET RUBBER BUMPERS.
EACH 10 FT VERTICAL W/G GETS 1 BRACKET
AT THE TOP END AND THE LAST VERTICAL W/G
(THE ONE AT THE BOTTOM OF THE TOWER)
GETS AN ADDITIONAL BRACKET AT THE BOTTOM END.
NOTE 2: SUB ASSY 5 IS USED IN CONJUNCTION
WITH UNISTRUT TO MAKE OTHER BRACKET ASSYS.
REFERENCE DRAWING # ASR9_00312 SHEETS 3, 4 AND 5.
NOTE 3: MOUNT THE WAVEGUIDE BRACKETS
SUCH THAT THE WAVEGUIDE FLANGES
ARE EXACTLY 7 INCHES APART (VERTICALLY).
NOTE 4: WHEN MOUNTING THE WAVEGUIDE
TO THE BRACKET, APPLY SILICONE
COMPOUND TO THE RUBBER INSIDE
THE BRACKET
USE SILICONE COMPOUND MIL-S-8660C.
Available from:
BCS MANUFACTURING
3575 Kennedy Road
South Plainfield, N.J., 07080
Phone: 908-561-1656
2.5" GALVANIZED PIPE
PRE-EXISTING TOWER PIECE
RUNS UP THE TOWER CENTER
SIZE
DATE 12-05-1999
DWG NO. 7D11455
SCALE /
REV LTR
SHEET 7 OF 12
REF DWG NO. X-12-1E1.DWG


VIEWS WITHOUT WAVEGUIDE
RIGHT SIDE
LEFT SIDE
CP
HI
LO
49
50
60
52
53
54
55
56
57
58
59
51
SEE SHEET 10 FOR EXPLODED VIEW
2.5" GALVANIZED PIPE PRE-EXISTING TOWER PIECE RUNS UP THE TOWER CENTER
NAS1149C0663R (TOO SMALL) FLAT WASHER
SIZE
DATE 08-07-2003
DWG NO. 7D11455
SCALE /
REV LTR
SHEET 8 OF 12
REF DWG NO. 3-12-IF2.DWG


VIEWS WITHOUT WAVEGUIDE
SIDE
TOWARD ANTENNA
CP
7.000
MOUNT EACH W/G BRACKET
7 INCHES APART FOR
ADEQUATE CLEARANCE
HI
LO
TOWARD OUTSIDE EDGE
OF TOWER
FRONT
CP
HI
LO
25' GALVANIZED PIPE
PRE-EXISTING TOWER PIECE
RUNS UP THE TOWER CENTER
TOP
CP
HI
LO
TOWARD ANTENNA
TOWARD OUTSIDE EDGE
OF TOWER
SIZE
DATE
12-04-1999
DWG NO.
7D11455
SCALE
REV LTR
SHEET 9 OF 12
REF DWG NO.
3-12-1E3.DWG


SIZE
DATE
08-06-2001
DWG NO
7D11455
SHEET 10 OF 12
SCALE
/
REV LTR
REF DWG NO
3-12-1F3.DWG


NOTE 1: BECAUSE THE CAP SCREW IS CUSTOM LENGTH, IT MUST BE USED WITH FLAT AND LOCK WASHERS AS SHOWN ALSO THIS HARDWARE MAY ONLY BE USED WITH 3/8" THICK WAVEGUIDE FLANGES AND PARKER SEAL AS SHOWN.
NOTE 2: PRIOR TO JOINING THE WAVEGUIDE FLANGES, APPLY WHITE RTV 112 PER FS83345 MA/C. RTV SHALL BE APPLIED NOT SOONER THAN 30 MINUTES BEFORE INSTALLATION, AND IT SHOULD BE USED IN THE HOLES UNDER THE FLAT WASHERS IN ORDER TO SEAL THE CREVICES FROM SALT DEPOSIT AND WEATHER. REFERENCE GE's PRODUCT SPECIFICATION. DO NOT GET SILICON GLUE IN THE WAVEGUIDE CONDUCTING PATH
NOTE 3: TO JOIN THE WAVEGUIDE FLANGES: REFERENCE PARAGRAPH 7.4.1 OF TI 6310.24
NOTE 4: AFTER JOINING THE WAVEGUIDE FLANGES: PAINT THE FLANGE, HARDWARE, AND EXPOSED PARKER SEAL EDGE TO PROTECT FROM SALT AND WEATHER. PRIMER ALONE SHOULD NOT BE USED SINCE IT ABSORBES MOISTURE. REF PARAGRAPH 2.3 AND 3.20.4 OF FAA-E-2704B.
30
29
28
27
FOR VERTICAL W/G, INSTALL THE CAP SCREW FROM THE BOTTOM AS SHOWN
WAVEGUIDE TO BE CONNECTED
3/8 THICK FLANGE
PARKER SEAL
3/8 THICK FLANGE
WAVEGUIDE TO BE CONNECTED
SIZE DATE
06-06-2000
DWG NO.
7D11455
SCALE
REV LTR
SHEET 11 OF 12
REF DWG NO.
3-72-201.DWG


NOTE 1: BECAUSE THE CAP SCREW IS CUSTOM LENGTH, IT MUST BE USED WITH FLAT AND LOCK WASHERS AS SHOWN. ALSO THIS HARDWARE MAY ONLY BE USED WITH 3/8" THICK WAVEGUIDE FLANGES AND PARKER SEAL AS SHOWN.
NOTE 2: PRIOR TO JOINING THE WAVEGUIDE FLANGES, APPLY WHITE RTV 112 PER PS83345 MA/C. RTV SHALL BE APPLIED NOT SOONER THAN 30 MINUTES BEFORE INSTALLATION, AND IT SHOULD BE USED IN THE HOLES, UNDER THE FLAT WASHERS IN ORDER TO SEAL THE CREVICES FROM SALT DEPOSIT AND WEATHER. REFERENCE GE's PRODUCT SPECIFICATION. DO NOT GET SILICON GLUE IN THE WAVEGUIDE CONDUCTING PATH.
NOTE 3: TO JOIN THE WAVEGUIDE FLANGES: REFERENCE PARAGRAPH 7.4.1 OF TI 6310.24.
NOTE 4: AFTER JOINING THE WAVEGUIDE FLANGES: PAINT THE FLANGE, HARDWARE, AND EXPOSED PARKER SEAL EDGE TO PROTECT FROM SALT AND WEATHER. PRIMER ALONE SHOULD NOT BE USED SINCE IT ABSORBES MOISTURE. REF PARAGRAPH 2.3 AND 3.20.4 OF FAA-E-2704B
3/8 THICK FLANGE
PARKER SEAL
3/8 THICK FLANGE
(7 PLACES)
(3 PLACES ONLY)
3/8 THICK FLANGE
PARKER SEAL
3/8 THICK FLANGE
(10 PLACES)
SIZE
DATE 06-06-2000
DWG NO. 7D11455
SCALE
REV LTR
SHEET 12 OF 12
REF DWG NO. 3-12-202.DWG

7A11741G01 Rev. C GPS ANTENNA MOD KIT

Find	*Part Number*	*Note*	*Part Name*	*Quantity*
1	7A11805H02		GPS BOARD,ANTENNA	1 EA
4	7A11790G03		PREINSTALLATION CABLES, GPS	1 EA
5	7A11805H03		GPS BOARD,SURGE SUPRESSOR	1 EA
9	7A11795H55		MARKER	1 EA
10	7A11795H59		MARKER	1 EA
18	5038K2		PIPE, AL, 6061-T6, 3/4 X 72	1 EA
19	98841A031		ROD, THREADED, 3/8-16, 3 FT	1 EA
20	3023T24		HANGER, PIPE, SPLIT-RING	1 EA
22	4549K597		NIPPLE, GALVANIZED, 3/4 X 4	2 EA
23	90161A651		ANCHOR, MASONRY, TAPCON	10 EA
24	7599K71		CLAMP, GND, 3/4 IN PIPE	1 EA
25	7512K612		WIRE, GND, 7-STRAND	600 IN
26	7153K45		TEE BOX, GALVANIZED, 3/4 IN	2 EA
27	11445T1		PLATE, WALL, IRON, 3/8 X 16	1 EA
28	4589K53		COUPLING, THREADED, CPVC, 3/	1 EA
29	6810K33		NIPPLE, THREADED, CPVC, 3/4	1 EA
30	4549K606		NIPPLE, GALVANIZED, 3/4 X 12	1 EA
31	7153K78		COVER AND GASKET, CONDUIT BO	1 EA
32	6P892		NIPPLE, GALVANIZED, 3/4 X 18	2 EA
33	5P968		FLANGE, FLOOR, GALVANIZED,	2 EA
34	221213		CONNECTOR/SPLICE WEATHERPROOF	1 EA

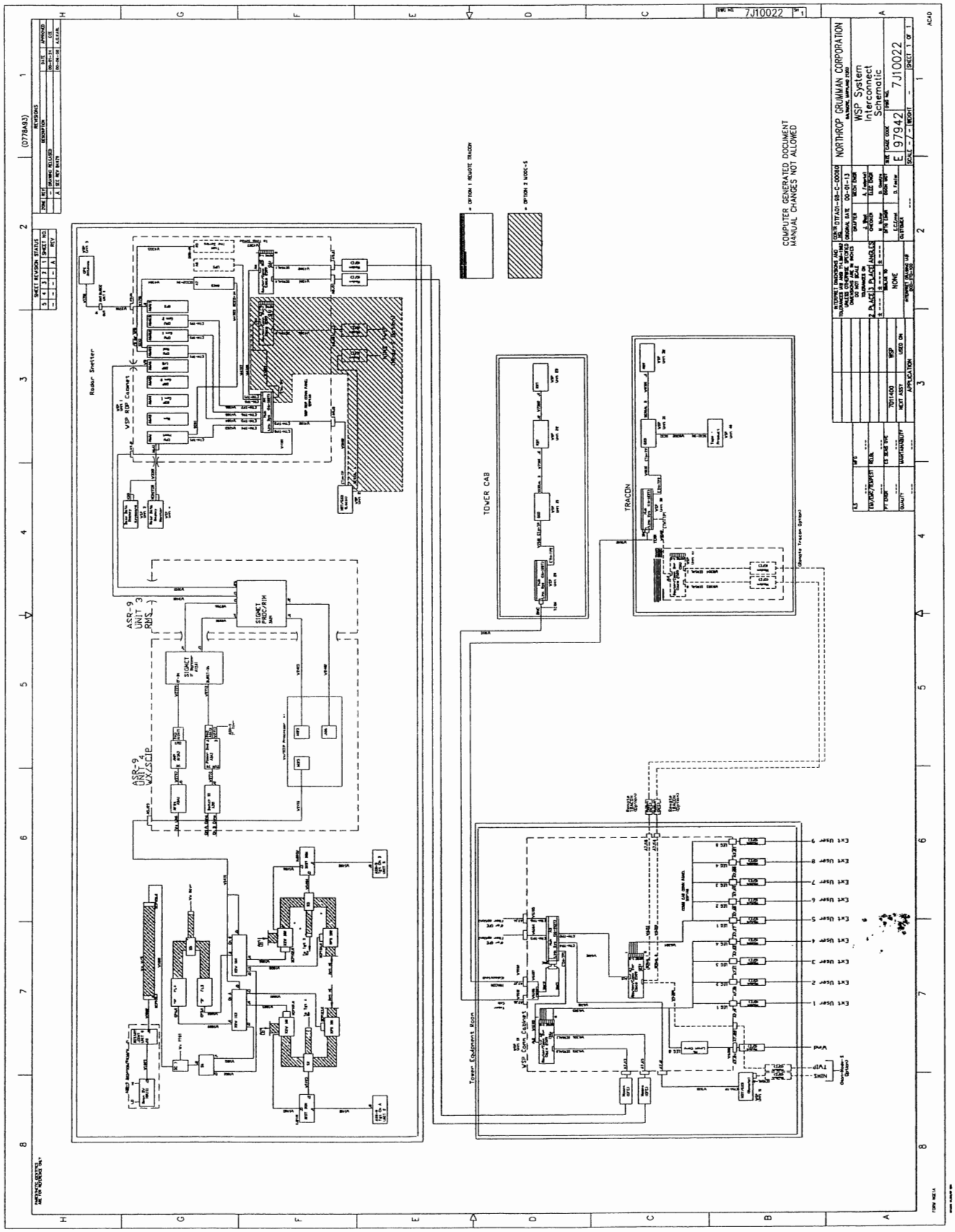
7A11790G01 Rev. A PREINSTALLATION CABLES, TGT CHAN BEAM SWITCHES

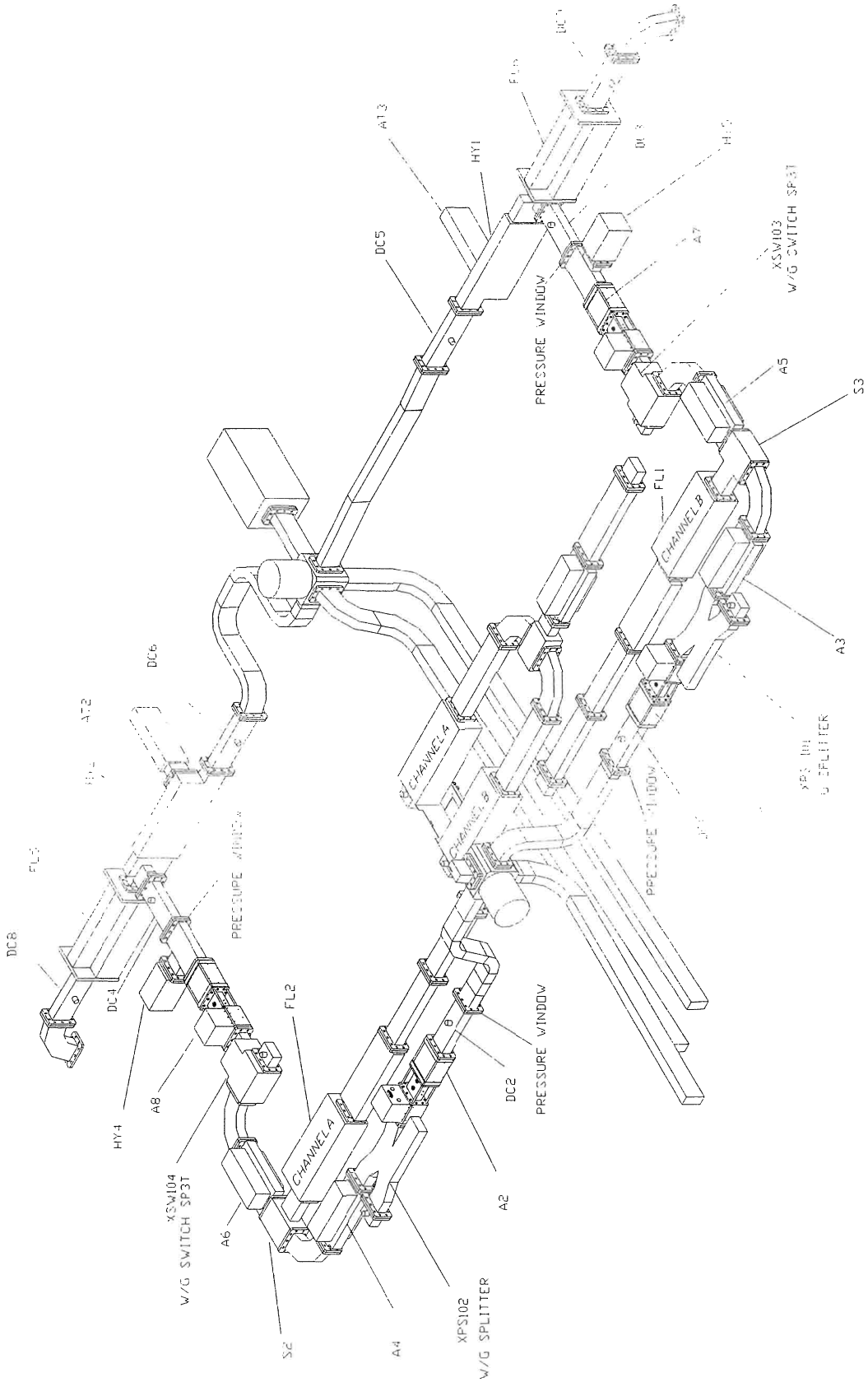
Find	*Part Number*	*Note*	*Part Name*	*Quantity*
1	7A11902H66	**6**	CABLE MAKE FROM, W1401	1 EA
2	7A11902H67	**7**	CABLE MAKE FROM, W1402	1 EA
50	7A11903G07		CABLE ASSEMBLY, W1403	1 EA
51	7A11903G08		CABLE ASSEMBLY, W1404	1 EA
52	7A11903G09		CABLE ASSEMBLY, W1405	1 EA
53	7A11903G10		CABLE ASSEMBLY, W1406	1 EA
72	7A11795H05		MARKER	1 EA
73	7A11795H06		MARKER	1 EA
74	7A11795H07		MARKER	1 EA
75	7A11795H08		MARKER	1 EA
100	7A11794		WIRELIST AND MARKERS, WSP	1 DOC

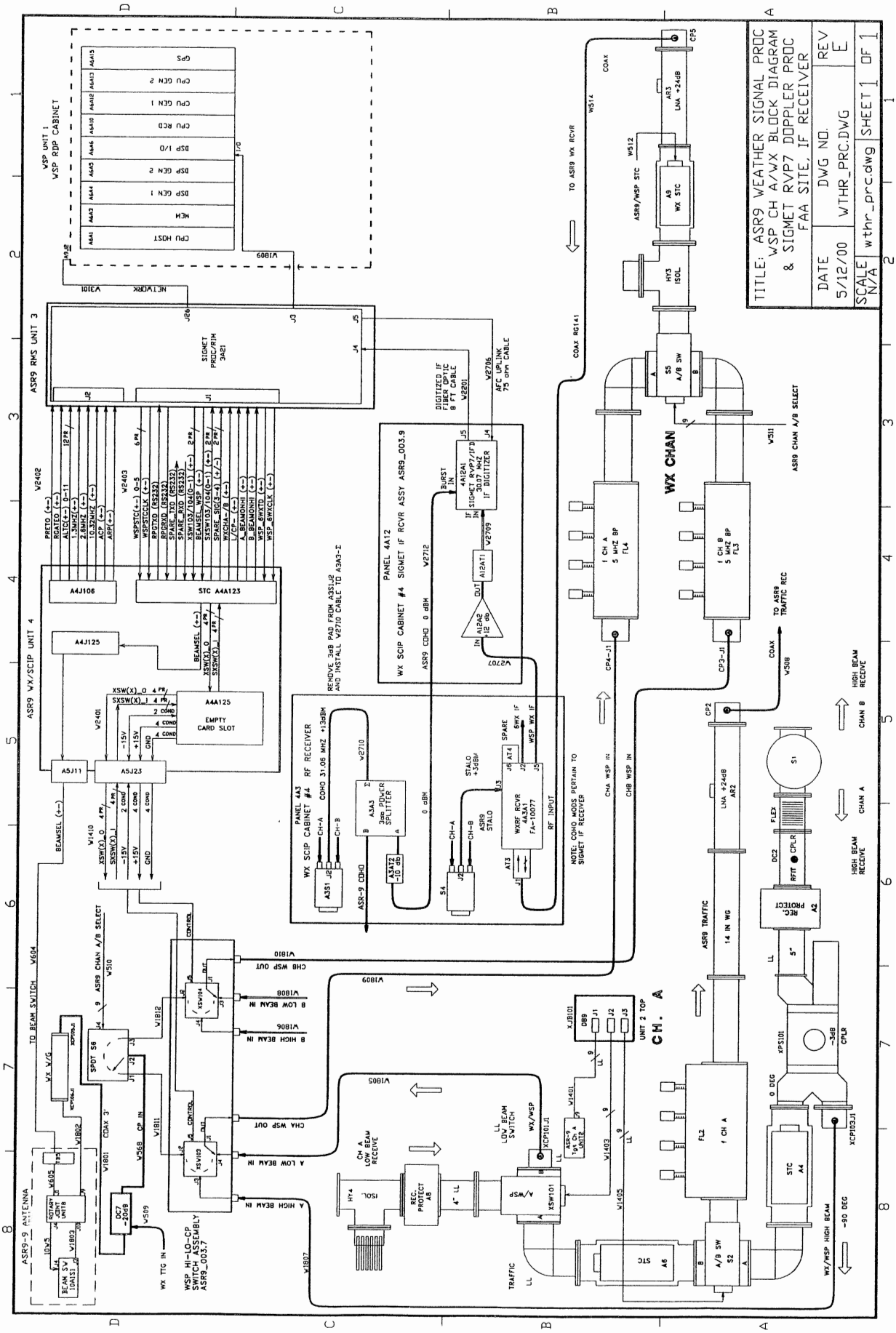
NOTES FOR: *7A11790G01*

Note 6 This cable is identical to cable 646A939G01 with unique WSP markers. Find nos. 072 and 073 installed per find no. 100. 646A939G01 is ASR-9 cable W506.

Note 7 This cable is identical to cable 646A939G03 with unique WSP markers. Find nos. 074 and 075 installed per find no. 100. 646A939G03 is ASR-9 cable W520.


NORTHROP GRUMMAN CORPORATION
WSP System
Interconnect
Schematic
7J10022
E 97942
COMPUTER GENERATED DOCUMENT
MANUAL CHANGES NOT ALLOWED
TOWER CAB
TRACON
Radar Shelter
ASR-9
UNIT 3
RMS
ASR-9
UNIT 4
WX/SCIP
SIGMET
PROC/RIM
Tower Equipment Room
Ext User 1
Ext User 2
Ext User 3
Ext User 4
Ext User 5
Ext User 6
Ext User 7
Ext User 8
Ext User 9
NONE
APPLICATION
SHEET 1 OF 1


A13
HY1
DC5
PRESSURE WINDOW
XSW103
W/G SWITCH SP3T
A7
A5
S3
FL1
CHANNEL B
A3
DC6
CHANNEL A
CHANNEL B
PRESSURE WINDOW
DC8
DC4
FL2
PRESSURE WINDOW
DC2
A8
HY4
XSW104
W/G SWITCH SP3T
CHANNEL A
A2
A6
S2
A4
XPS102
W/G SPLITTER


TITLE: ASR9 WEATHER SIGNAL PROC
WSP CH A/WX BLOCK DIAGRAM
& SIGMET RVP7 DOPPLER PROC
FAA SITE, IF RECEIVER
DATE 5/12/00
DWG NO. WTHR_PRC.DWG
REV E
SCALE N/A
wthr_prc.dwg
SHEET 1 OF 1
WX CHAN
CH. A
ASR9 RMS UNIT 3
ASR9 VX/SCIP UNIT 4
ASR9-9 ANTENNA
WSP HI-LO-CP SWITCH ASSEMBLY ASR9_003.7
PANEL 4A12
WX SCIP CABINET #4 SIGMET IF RCVR ASSY ASR9_003.9
PANEL 4A3
WX SCIP CABINET #4 RF RECEIVER
VSP UNIT 1
WSP RDP CABINET
STC A4A123
EMPTY CARD SLOT
SIGMET PROC/RIM 3A21
A/B SW S5
A/B SW S2
STC A4
STC A6
REC. PROTECT A2
REC. PROTECT A8
LNA +24dB AR2
LNA +24dB AR3
WX STC
HY3 ISOL
HY4 ISOL
SPDT S6
DC2 -20dB
BEAM SW 10A1S1
ROTARY JOINT UNIT 8
A/WSP XSW101
LL LOW BEAM SWITCH
CH A LOW BEAM RECEIVE
HIGH BEAM RECEIVE
CHAN A
CHAN B
ASR9 TRAFFIC 14 IN WG
TRAFFIC
WX/WSP HIGH BEAM
-90 DEG
0 DEG
CPLR
FLEX
RFIT
COAX
ASR9 CHAN A/B SELECT
TO ASR9 WX RCVR
TO ASR9 TRAFFIC REC
ASR9/WSP STC
WX TTG IN
TO BEAM SWITCH
NETWORK
REMOVE 3dB PAD FROM A3S1J2 AND INSTALL V2710 CABLE TO A3A3-Σ
NOTE: COHO MODS PERTAIN TO SIGMET IF RECEIVER
DIGITIZED IF FIBER OPTIC 8 FT CABLE
AFC UPLINK 75 ohm CABLE
CHA WSP IN
CHB WSP IN
CHA WSP OUT
CHB WSP OUT
A LOW BEAM IN
A HIGH BEAM IN
B LOW BEAM IN
B HIGH BEAM IN
CONTROL
WX V/G
CP IN
CDAX 3"

SYSTEM SUPPORT DIRECTIVE (SSD)

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SYSTEM SUPPORT MODIFICATIONS (SSM)

Document Number	Date Issued	Title
SSM-ASR9-001	04/23/99	ARSR-9 SERIAL INTERFACE SYSTEM
SSM-ASR9-002	02/06/98	TRANSMITTER POWER INTERUPT AND BLOWER MOTOR FUSE
SSM-ASR9-003	10/19/99	REMOVAL OF CIRCUIT BREAKERS FROM MODEM RACK
SSM-ASR9-004	03/13/98	UPGRADE MODE-S INTERFACE SUPPORT
SSM-ASR9-005	04/01/99	PROCESSOR AUGMENTATION CARD PHASE I
SSM-ASR9-006	04/29/98	ASR-9 REMOTE SCIP CIRCUIT BREAKER WIRING CONNECTION
SSM-ASR9-007	06/07/99	ALTERNATE DUAL REDUNDANT MODIFICATION
SSM-ASR9-008	08/02/99	MUFFIN FAN REPLACEMENT
SSM-ASR9-009	TBD	PROCESSOR AUGMENTATION CARD PHASE II
SSM-ASR9-010	CANCELLED	ASR-9 UPDATES
SSM-ASR9-011	03/26/03	SOFTWARE SUPPORT FOR THE WEATHER SYSTEMS PROCESSOR
SSM-ASR9-012	06/19/03	WEATHER SYSTEMS PROCESSOR INTERFACE TO THE ASR-9
SSM-ASR9-013	06/05/01	ASR-9 SERIAL INTERFACE SYSTEM (ASIS) PHASE II
SSM-ASR9-014	TBD	ANOMALOUS PROPAGATION (AP) FILTER
SSM-ASR9-015	TBD	UPDATE PROCOMM PLUS SCRIPTS
SSM-ASR9-016	07/14/03	ASR-9 SERIAL INTERFACE SYSTEM (ASIS) PHASE II DUAL BOARD

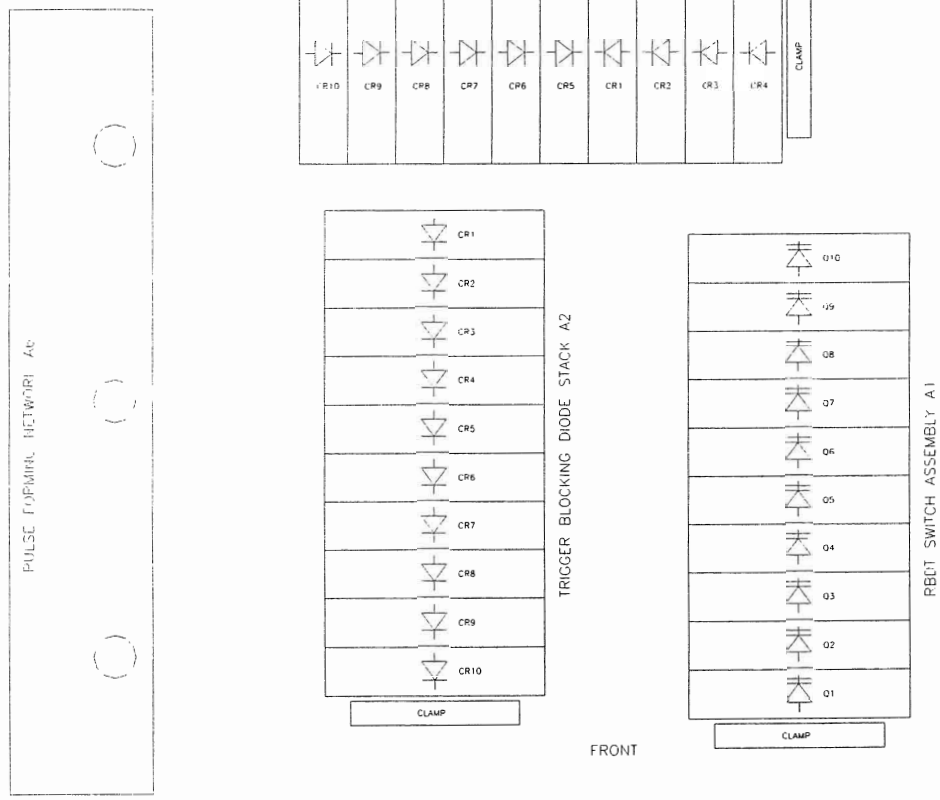
SYSTEM TECHNICAL RELEASES (STR)

Document Number	Date Issued	Title
STR-ASR9-001	02/06/98	DELIVERY OF AIRPORT SURVEILLANCE RADAR-9 PROCOMM SOFTWARE UPDATE
STR-ASR9-002	12/29/98	DELIVERY OF AIRPORT SURVEILLANCE RADAR-9 PROCOMM SOFTWARE UPDATE VERSION 5.0
STR-ASR9-003	11/29/99	DELIVERY OF AIRPORT SURVEILLANCE RADAR-9 SOFTWARE UPDATE VERSION 6.0
STR-ASR-9-004	12/15/99	ASR-9 VARIABLE SITE PARAMETERS AND PROGRAMMABLE ALARM THRESHOLD/FILTER BASELINE
STR-ASR9-004A	06/20/01	ASR-9 VARIABLE SITE PARAMETERS AND PROGRAMMABLE ALARM THRESHOLD BASELINE UPDATES

SYSTEM DOCUMENTATION RELEASES (SDR)

Document Number	Date Issued	Title
SDR-ASR9-001	CANCELLED	BY SDR-ASR9-002
SDR-ASR9-002	CANCELLED	BY SDR-ASR9-003
SDR-ASR9-003	05/09/02	ASR-9 TECHNICAL INSTRUCTION BOOKS UPDATE AND REISSUE OF ASR-9 TI CD ROM
SDR-ASR9-004	TBD	DELIVERY OF THE AIRPORT SURVEILLANCE RADAR-9 OPTIMIZATION PROCEDURES

ATTACHMENT 2. INSTRUCTION BOOK CHANGES



A1 RBDT DIODES Q1–Q10 ARE 835A716H01 AND 589R131H01

A2 TRIGGER BLOCKING DIODES CR1–CR10ARE 1420890H01

A3 BACKSWING DIODES CR1–CR4 ARE 1420559H01

A3 INVERSE DIODES CR5–CR10 ARE 845A684H01

PRESSURE STACK COMPONENT CONFIGURATIONS (VIEWED LOOKING DOWN INTO MODULATOR PULSE ASSEMBLY A12)

FIGURE 11-17 MODULATOR PULSE ASSEMBLY A12 MAJOR COMPONENTS (SHEET 3-END)

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2.0 TECHNICAL DESCRIPTION

2.1 INTRODUCTION

This section contains a functional description of the ASR-9 System Weather Receiver/SCIP equipment. * This manual incorporates the WSP interface modification, and will be distributed to only those sites that require the WSP (Weather Systems Processor ASR9 Modification developed by Lincoln Labs, Northrup Grumman for the FAA). The description is divided into two major subsections, one containing an * overview description and the other containing a detailed functional description. The overall description defines the equipment functions and describes their basic operations. In the detailed description, each function defined in the overview is described in greater detail with reference to actual hardware. The descriptions in this section are written with the assumption that the reader is familiar with the overall operation of the ASR-9 System, as described in section 2 of the top–level system field maintenance book, TI 6310.24.

2.2 OVERVIEW DESCRIPTION

An overview block diagram that defines the major equipment functions is shown in figure 11-1. Refer to that diagram during the following discussion.

2.2.1 Introduction

The Weather Receiver/SCIP (Unit 4) receives digitized radar return data from Radar Receiver/Processor Channel A (Unit 2) and Radar Receiver/Processor Channel B (Unit 5). It also receives radar return signals directly from the antenna feedhorns. The weather receiver/SCIP resolves the radar returns into six levels of weather intensity. The subsystems of the weather receiver/SCIP are * the weather receiver/processor, WSP interface, system control panel, local system control, local display processor and multivoltage power supply. The WSP interface adds new functions to Unit 4 that does not exist in the original ASR-9 architecture. The weather receiver/SCIP is the most significant point of * data correlation at the local site. The six levels of weather intensity from the weather receiver/processor subsystem and the surveillance channel status from the receiver/processor are processed by the local system control subsystem to output a target report to the modems which transfer the data to the remote site. The local system control subsystem also provides termination points (RS449 interface generator) for unused modem lines. The local display processor provides video for the Maintenance Display (Unit 7) plan position indicator (PPI), which provides video at the local site for maintenance purposes.

2.2.2 Power and Alternate Power Input Subsystem

The units of the ASR-9 receive facility power from a prime commercial source of 60-Hz, 208 V ac, four–wire, three–phase, alternating current. The weather receiver/SCIP multivoltage power supply is located at the bottom of the weather receiver/SCIP cabinet and provides power for the subsystems and environment. If commercial power fails, an auxiliary engine generator automatically switches over in less than 15 seconds. A backup battery is included with the weather receiver/SCIP power supply. The battery immediately supplies direct current to the regulators of four of the nine multivoltage modules and maintains input power to the modules during line power switchover to the auxiliary engine generator.

2.2.3 Weather Receiver/Processor Subsystem

See figure 11-1. The weather receiver/processor subsystem receives radar return weather data from the low noise amplifier (LNA), critical timing signals and digital radar return data from

receiver/processor channel A and B, diagnostics and variable site parameters (VSPs) from the Remote Monitoring Subsystem (RMS) (Unit 3), and azimuth change pulse (ACP) and azimuth reference pulse (ARP) azimuth data from the antenna. The radar return weather data from the LNA passes through the radio frequency/intermediate frequency (rf/i–f) receiver function, the filtering and magnitude function, and the six–level weather detector function. The digital data from both receiver/processors bypasses the weather rf/i–f receiver function and is input to the six–level weather filtering and magnitude function. The data input to the filtering and magnitude function is either circular polarized I/Q data from the rf/i–f * receiver or linear polarized I/Q data from the receiver/processors. The digital receiver/processor I/Q data is also sent by the WSP via backplane ribbon cable connector 4AJ106. Batch data is output to the six–level weather detector which classifies the data into six levels of intensity for input to the local * system control subsystem. The monitoring and control function distributes VSPs to the synchronizer, filtering and magnitude and six–level weather detector functions. The synchronizer, which is similar to that of the receiver/processor, generates system and batch timing for the weather receiver/processor subsystem.

2.2.3.1 Rf/I–f Receiver Basic Signal Flow. The rf/i–f signals through the weather rf/i–f receiver originate at the antenna feedhorns (high beam and low beam). They are transmitted along a path separate from the radar target data for channel A and channel B. These weather signals are amplified by a LNA and applied to the rf/i–f receiver input. The input signals from the LNA are amplified, converted to an i–f signal, amplified again, and detected to produce phase–referenced video signals. These signals are then converted to digital values for further processing of radar weather information. The receiver includes a test and calibration control system which tests or adjusts receiver parameters under the control of the RMS/CMT processor.

2.2.3.1.1 Use of Weather Rf/I–f Signals. See figure 11-2, sheet 1. The weather rf/i–f receiver supplies the weather digital video signals to the weather processor when circular antenna polarization is * selected. In circular polarization the WSP taps the 6Lvl-Wx if signal using a more advanced if receiver (with a dynamic range exceeding 80 dbm or comparable to the dynamic range of the ASR9's LNA) to synthesize the digital I/Q data for it's processor. When linear antenna polarization is selected the weather digital video signals are supplied to both the 6-WX processor and the WSP, by the on–line * target receiver/processor channel (A or B) rf/i–f receiver. Circular polarization is used when a heavy precipitation condition exists. In heavy precipitation the nearly spherical raindrops are passed by the weather rf/i–f receiver because of the receivers opposite sense receive polarization characteristics. Conversely, the antenna/waveguide system of the target channel attenuates these type of returns making detection of target signals easier. In clear or light precipitation conditions, linear polarization is generally selected and video to the weather processor is provided by the online target receiver/processor channel.

2.2.3.1.2 Rf/I–f Signal Flow. See figure 11-2, sheet 1. The rf signal from the weather LNA is applied * through an input driver amplifier to the i–f mixer circuit. This signal is in the S–band section of the * microwave spectrum. The received signal is heterodyned in the mixer with a stable local oscillator (stalo) frequency (f2) and filtered to produce an i–f frequency (f1) of 31.07 MHz. This stalo signal is generated in a crystal–controlled oscillator in the frequency generator assembly of the online target * channel. The i–f signal is applied through a variable gain amplifier circuit to a limit circuit in the ASR9; but in the WSP-if receiver, it is immediately digitized (A/D @ 35.9571 MHZ.), filtered and synthesized I/Q data is produced on a serial fiber optic link. The limit circuit is not used in the weather channel, since it would reduce the intensity of severe storm returns that the weather channel is to process. The * i–f signal from the limiter is applied through several stages of amplification and filtering to the I and Q phase detector. The I & Q phase detector generates in–phase and quadrature video signals which are referenced to the coherent oscillator (coho) signal from the frequency generator in the online target channel. The I and Q video signals are applied through amplifiers to the analog to digital (a/d) converter. The a/d converter converts each of the video signals (I and Q) into a series of 12–bit digital values. These values are transmitted to the six–level weather detector as alternating I and Q values on a 12–bit parallel bus.

* The WSP-digital IF receiver is different than the ASR9-IF receiver because it employs DSP techniques to produce the I/Q data stream that were not available when the ASR9 design occurred. Many techniques to produce the ASR9 I/Q data such as analog calibration servo loops, phase detectors, and limiters are not needed any more. Therefore, the following discussion regarding Test and Calibration is not altered by the WSP, because it does not need to use these techniques to produce reliable I/Q data. *

* **2.2.3.1.2.1 WSP Flow.** See Figure 11-7 sheet 6. The WSP is a place Online from the WSP control terminal, the ASR9 system control panels indicate the status of the WSP but is not allowed to put the WSP online. This method of selecting the WSP service only at the WSP consoles and not the ASR9 control panels is instituted to prevent control panel ambiguities contributing to the confusion during an outage. Simply put, the WSP is placed Online when the ASR9 system control receives a message (via USART on LSCI-1 board) that it is ready and commanded to go Online from a WSP master control console. The WSP will be taken offline if the ASR9 receives a message (via USART on LSCI-1 board) from the WSP requesting a return to the normal ASR9 6 LVL Weather channel. The WSP will be forced offline after 3 to 5 seconds if no messages are received from the WSP. In the case when the WSP is Offline and the system is in Linear Polarization, the WSP is in control of the ASR9 Weather channel rf/if components. This provides a means to troubeshoot the WSP using live data while it is offline, it does not interfere with the ASR9 6 LVL Weather data because it is using target channel data in this mode. *

2.2.3.1.3 Test and Calibration. Certain circuits in the rf/i–f receiver are used to provide test signals for the receiver or to control adjustments of various parameters in the receiver. These signals or adjustments are controlled by signals from the weather synchronizer (figure 11-2, sheet 2) which are sent on the RX calibration bus. The RX calibration control bus is programmed with a simultaneous value which specifies the function of the accompanying value on the calibration bus. Test and calibration sequences are controlled by the RMS/CMT single board computer (SBC) which programs circuits in the synchronizer to initiate the test and calibration signals. The i–f signal from the amplifier and filtering network is applied to an amplitude detector which produces a video signal for maintenance.

2.2.3.1.3.1 Test Input Signals. See figure 11-2, sheet 1. A test signal (zero dBm reference) used to test the a/d converter is generated by the test/calibration control circuit under the control of signals from the RX calibration bus. This signal is a fixed analog level proportional to the digital word (12 bits) received on the bus. This test value, which is applied to the video input of the a/d converter, can be changed periodically by programming another value through the RX calibration bus. Another test signal is generated by the test frequency generation circuits in the online channel (A or B). This signal (test tone), which is an ac signal in the i–f band, is connected to the weather receiver at the limiter output. An rf test target signal is generated in the online channel target frequency generator. This signal is coupled into the weather receiving channel before the LNA for use in testing rf portions of the weather receiver channel. The signal is generated by mixing the stalo frequency and the coho frequency in the online target channel and tuning on the output to obtain the sum frequency (f1 + f2). This frequency is used as the radar transmit frequency as well as the test target frequency.

2.2.3.1.3.2 Calibration. See figure 11-2, sheets 1 and 2. As was previously stated (paragraph 2.2.3.1.2) the i–f signal from the mixer is sent through a variable gain amplifier. This allows the amplitude of the signal to be adjusted by an automatic gain control (agc) circuit. This agc signal is developed in the test/calibration control circuit based on signals received from the weather synchronizer on the RX calibration bus. These signals are initiated and controlled by the RMS/CMT processor which periodically samples digitized video from six–level weather filtering and magnitude signal processor (sheet 2) and adjusts the variable gain amplifier (sheet 1) to keep the overall gain of the receiver to the desired level. Samples of receiver noise serve as the reference signal for this adjustment. The phase

and gain balance of the I and Q phase detector and the dc offset on the I and Q amplifiers driving the a/d converter are all adjusted by the RMS/CMT processor in a manner similar to the agc calibration. For the I/Q phase and gain cases, however, the test signal (test tone), generated by the online target channel, is applied to the receiver at the limiter output. This signal is used as a standard for adjustment of the I/Q gain and phase parameters. Samples of receiver noise are used to minimize dc offset for the I
* and Q channels. The WSP-IF does not employ AGC, it relies on its 80 db+ dynamic range to pass all weather return signals without distortion. *

2.2.3.2 Weather Filter and Magnitude Processing. See figure 11-2, sheet 2. Received digital data is selected from one of three sources for processing in the filter and magnitude processor. The three sources of digital data are the weather receiver/processor rf/i–f receiver, target channel A filtering and magnitude processor and target channel B filtering and magnitude processor. The selected data words are stored in blocks of memory in the order in which they are received and read out in a differently arranged order for further processing. Each word group read from the memory block is analyzed for doppler frequency content. The amplitude values resulting from this analysis are then converted to equivalent logarithmic values as a convenience in subsequent processing in the six–level weather detector.

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2.2.3.2.1 Input Digital Data Timing. See figure 11-3. Timing for the video a/d conversion in any channel (A, B, or weather) rf/i–f receiver is such that each analog video signal (I and Q) is sampled once every 1/16 of a mile of radar range during each range sweep time period. The time period (distance) slot in which each pair of data words (I/Q) is produced by the a–d converter is called a range cell. Range cells are numbered as shown, from 1 to 973. Range cell 960 marks the maximum (60–mile) range point (16 x 60 = 960). The additional 13 range cells are not used in weather processing. The I and Q digital values in each range cell are, of course, proportional to the analog level applied to the converter during that particular range cell period. The values in the majority of range cells represent the background noise or distributed clutter (including weather returns) being received at the time. High level return pulses (targets point clutter or highly reflective weather conditions) generate larger digital values in those cells in which they occur. The number of a particular cell is, of course, representative of range (i.e., sweep time since the transmitted pulse). The transmitted pulse width is such that return pulses are approximately 50 percent wider in time than a range cell. This enables detection of a target point source appearing in adjacent range cells.

2.2.3.2.2 Input Data Control and Limiting. See figure 11-2, sheets 1 and 2. The alternating digital I and Q data words from the weather a/d converter are clocked through the input control/buffer circuit by input timing signals generated in the weather channel synchronizer. This timing is based on the 31.07-MHz coho signal from the online frequency generator (sheet 1), which is applied to the clock generator (sheet 2) to control generation of the 1.3-MHz clock. The 1.3-MHz clock is sent to the trigger pulse generator to produce the input timing triggers. The input timing triggers clock a pair of I and Q data words through the input control/buffer circuit at a rate proportional to the radar range of 1/16–mile range cell. This, of course, is the rate at which the pair of values is generated in the a/d converter (figure 11-3). Each of these data words is compared to maximum limit values hard–wired in the limiter (figure 11-2, sheet 2), and the limit value is substituted for the input data value if the input word exceeds the limit value. Operation of the limit circuit is controlled by receiver data select from the input source select circuit.

2.2.3.2.3 Input Data Word Selection. See figure 11-2, sheet 2. Digitized video data words from the weather receiver are stepped through the input control/buffer by the input timing (paragraph 2.2.3.2.1). Each of these data words is then limited in amplitude to a fixed maximum value (paragraph 2.2.3.2.2). The digital video data words from the online target channel (A or B) are timed and amplitude limited in the same manner, by a circuit on the online target channel filtering and magnitude signal processor. The weather channel source control signal, from the data source channel status circuit in the weather channel synchronizer, controls the selection of the source of weather digital video data. Data on the polarization of the antenna beam is received on the configuration, monitor, and test (cmt) data bus. If the beam is linearly polarized, the weather channel source control signal sets the input source select circuit to apply I/Q video data from the online target channel (A or B) to the bulk (X and Y) memory inputs. At the same time, the input source select circuit sets receiver data select inactive to inhibit limiter operation and block data from the weather receiver. If the antenna is circularly polarized, the weather channel source signal blocks the input from the target channels and sets receiver data select to activate the limiter and send the weather receiver data to the bulk memory (X and Y) inputs. If the antenna is
* circularly polarized and the WSP is online, the weather channel source reverts back and blocks the weather receiver data because it selects the online target channel data. That is, the WSP is already receiving the weather channel returns via its own IF receiver so the target channel data provides a source of co-polarized data to the WSP processor on this path. The selected data is stored in the bulk memories for reformatting prior to further processing. *

2.2.3.2.4 Radar Return Data Formatting. See figure 11-4. In understanding the arrangement of data for processing in the weather channel the arrangement of the data as received from the antenna by the receiver must first be considered. In establishing the format of received data, the

of the low velocity (zero–doppler) return from fixed objects, the clear day map is used to provide a censor bit for the weather cell. This censor bit disables weather detection in the weather cell and is also used in further processing.

2.2.3.3.6.1 Filter Selection. See figure 11-2, sheets 2 and 3. The clear day map memory is addressed by the sector count and the mile count (sheet 3). These address values cause a value to be read from the memory which represents the weather filter selection for the area defined by the sector and mile counts. These values specify the weather filter to be used in the two weather cells (one mile range by 1.4–degree scan) from which signals are about to be received and filtered. When a low level of ground clutter is to be expected, the filter select signal selects the all–pass filter which passes weather signals across the full range of doppler frequencies including those frequencies at or around zero (i.e., from fixed or very low velocity targets). When one of three higher levels of ground clutter is to be expected, the filter select signal selects one of three filters, each having a zero doppler notch of a different width. The higher the expected clutter, the wider the zero frequency notch to prevent spillover of the expected clutter return signal into the weather detection signals.

2.2.3.3.6.2 Censor Data. See figure 11-2, sheet 3. The map decode circuit also generates censor data word that indicates the highest level of weather that is caused by ground clutter and cannot be rejected by filtering. This censor value is compared to the weather detection level data from the threshold comparator. If the censor value (indicative of the expected clutter level) equals or exceeds the weather detection level (i.e., the intensity actually received), a censor bit is set. This bit is associated with the data in subsequent processing to indicate that the weather level is not detectable due to ground clutter.

2.2.3.3.7 Smoothing and Contour Processing. See figure 11-2, sheet 3. At the end of weather cell processing for a scan sector the data storage circuit memory contains the weather level value and the associated censor bits for each weather cell in the scan sector. This data is transmitted in sequence from weather cell 1 at the start of high–beam sweep no. 1 in the scan sector to weather cell 120 (maximum range) in low–beam sweep no. 8. The transmission of the last value is followed by the transmission of two test words generated in the test word generator. These two words mark the end of the block of weather data and also identify the scan sector number as being odd or even. Smoothing and contour processing is accomplished in a single board computer (SBC) which is programmed to generate general levels of weather background data for the radar scan area. The SBC compares the data for each weather cell over six antenna scans and selects a median level for the group as the interim level for that weather cell. This level is further smoothed by setting a value for each weather cell which is determined from that cell and the eight cells adjacent (four above and four below) to it. The level that is declared is the highest level for which M–out–of–9 (M is a VSP) detections occur. The contour processing operations set each weather cell in the nine–cell group to the highest declared weather level in the group. Cells with the censor bit set are not used in the smoothing process. The weather level in censored cells is set equal to those levels in adjacent uncensored cells in the contouring process.

2.2.3.3.8 Weather Map Data Transmission. See figure 11-2, sheet 3. The weather map display data is transmitted from storage in the smoothing and contour processor to the interface circuit. The interface circuit serves as a buffer to control the transmission of this data to the local control circuits.
* When the WSP is online, the WSP 6LVL Weather Map Data replaces the ASR 6-Lvl Weather map data on the LSCI #2 boards, for the Weather Map Data Transmission from the ASR9. *

2.2.4 Local System Control Subsystem

The local system control subsystem distributes the data that is output by the weather receiver/SCIP to other ASR-9 units, with the exception of the test/fault line that is output from unit 4 by the weather receiver/processor subsystem. The local system control receives six–level weather data or two–level weather data (depending upon manual selection), system timing from the synchronizer, and surveillance (target) data and status and timing signals from the active channel of the receiver/processor. The local system control also receives channel and weather–levels selection from the Maintenance Display (Unit 7), feedback control/status signals from the local modems, and control signals from the RMS. The local system control also provides two– or six–level weather data to the local display processor.

2.2.4.1 Local System Control Circuits. See figure 11-2, sheet 4. The local system control circuits process input/output data for both of the surveillance (target and two–level weather) channels and also the six–level weather channel. The local system control circuits consist of microcomputer–controlled processing and interface circuits. These circuits provide a communication link between corresponding remote system control panels and the Remote Monitoring Subsystem (RMS) to set up the operating configuration of the entire ASR-9 System. The local system control circuits also select the following data and transmit it to the local data communication system for transmission to the remote display system:

1. Target receiver/processor channel A or B as the source of surveillance data and two–level weather data.
2. * Weather receiver/processor or WSP as the source of six–level weather data. *
3. Control of the ASR-9 System by the local system control panel, remote system control panel, or RMS.

2.2.4.1.1 Display Data Interfaces. See figure 11-2, sheet 4. SCIP data is received from the radar receiver/processors (A or B) and applied to interface circuits in both system control interface assemblies no. 2 (A215 and A217). SCIP data is the processed target, beacon, and two–level weather information that is used to produce displays of target, beacon, and weather data. Selection of the online channel is controlled by the operator at the local or remote system control panel. Weather display data from the six–level weather receiver/processor is likewise applied to both interface circuits.

2.2.4.1.1.1 Target Data Formats. See figure 11-2, sheet 4. Three independent serial streams of beacon/target data are received from the online target receiver/processor. The received data is organized into word fields and messages. A word field is composed of up to 12 data bits plus one odd parity bit, for a total of 13 bits. The parity bit is the last bit transmitted in each word field. A message is a combination of serially transmitted word fields. Depending on the type of message, there can be 4, 7, 10, or 32 word fields in a message. Beacon/target messages are received from the online channel only when the appropriate return signals have been received. Idle characters are transmitted from the receiver/processor at least once between each message and, in the absence of messages, are sent continuously. Idle characters consist of three binary 0's followed by 10 binary 1's. The idle characters employ even parity to distinguish them from word fields. The local system control looks for idle characters to establish word and message synchronization.

2.2.4.1.1.2 Weather Data Format. See figure 11-2, sheet 4. Three two–level weather serial data streams are received from the online target receiver/processor as part of the SCIP data.

One six–level weather serial data stream is received from the weather receiver/processor. A weather message consists of 32 13–bit word fields. The receiver/processor transmits at least one idle pattern between each message.

2.2.4.1.1.3 Display Data Transmission. See figure 11-2, sheet 4. Target and display data messages are transmitted to the local data communications modems via system control interface no. 2 A215 and A217. Two identical data transmission interfaces are provided. There are two reasons for providing two identical interfaces. One reason is to provide a fail–safe redundant path for transmission/reception of system control data (which is multiplexed with the two/six–level weather data). If either A4A215 or A4A217 fails, the remaining operative board is automatically switched to become the active transmission interface. The second reason for providing two identical configurations is that they are needed at dual–redundant configuration sites to feed parallel streams of surveillance data to separate modems. The data messages are forwarded from modems in the local data communications units through transmission lines to the display system at the remote site. The transmissions are controlled by clear–to–send signals from local data communications modems. The clear–to–send signals are sent as part of the control data from the local data communications modems. The signals are forwarded to the online channel as part of the target channel (A or B) control data and to the six–level weather detector.

2.2.4.2 Control/Status Interface. See figure 11-2, sheet 4. The control/status interface circuit in system control interface no. 1 receives status messages from both target receiver/processors and the weather receiver processor. This interface is controlled by the local control processor and by control data from the remote site through the local data communication system when initiating control signals from the target and weather receiver/processor channels. Status messages are received periodically and whenever a change in status occurs. These messages provide system configuration and summary fault alarms from the ASR-9 System to the local system control. The local system control converts the status messages into signals which control the flow of surveillance and weather messages to the local data communications facility. The control/status interface also initiates the control signals which configure the receiver/processor channels in response to local control selections or control data received from the remote site.

2.2.5 System Control Panel Subsystem

See figure 11-36. A system control panel is located above the dual card rack in the weather receiver/SCIP cabinet. Fifteen select switches with 30 indicators and 21 alarm indicators at the front of the system control panel are accessible to the local site operator. The system control panel, in conjunction with the local system control, selects two– or six–level weather, the active receiver/processor channel, and either local or remote site control. The system control indicators display the switch selections and the status of various functions of ASR-9 system processors.

2.2.6 Local Display Processor

The local display processor receives target and two–level weather data from both target receiver/processor channels (A and B), WSP weather, and six–level weather data from the local system control circuits. The local display processor uses this data to generate video signals and triggers for the maintenance display. Channel select signals from the maintenance display system select the input data to be used. A single board computer (SBC) processor identifies the types of incoming data messages and stores this data in the SBC data memory in the order necessary for proper generation of display video signals. The output control SBC processor reads the stored data from the SBC data memory and transfers it to the target and weather video generators to generate the video signals used in forming the local display.

2.2.6.1 Local Display Processor Initialization. See figure 11-2, sheet 5. Two SBC's are used in local display processing. The operating programs for these SBC's are stored in a program storage ROM when the system is not in use. These programs are downloaded and stored in RAM within each SBC processor at the start of operation. The incoming SBC processor (no. 1) addresses the program storage ROM in the map and storage circuit through the programmable interface multibus and the associated bus transceiver. The program instruction values are read from the ROM through the transceiver and the programmable interface multibus and stored in RAM in the incoming data SBC processor (no. 1). In a similar manner, the output control SBC processor (no. 2) uses the data memory multibus to download its program from the program storage through the associated bus transceiver.

2.2.6.2 Input Formatting and Control. See figure 11-2, sheet 5. The channel select signals activate the appropriate serial–to–parallel conversion circuits to pass data from the selected source. Each conversion circuit steps messages in from the serial input and outputs them as parallel data words to temporary RAM storage in the associated storage and bus control circuit. The incoming data SBC processor (no. 1) controls the transfer of data messages from the storage and bus control circuits by addressing storage readout through the programmable interface multibus. The programmable interface multibus is a multi–use time–shared bus which, during local display generation, transmits address values and data words between storage and bus control circuits, the incoming data SBC processor (no. 1), and the SBC data memory. The incoming data is read out of the temporary storage and transferred through the programmable interface multibus to the incoming data SBC processor. The processor identifies each type of data and sends the data word through the programmable interface multibus for storage in the SBC data memory. The incoming data SBC processor controls the sequence of data storage in the SBC data memory so that the data is arranged in blocks by azimuth scan sectors. This keeps the data available in the order required for the generation of display video signals.

2.2.6.3 Azimuth Pulse Generation. See figure 11-2, sheet 5. The azimuth pulse generator receives azimuth data messages through the bus transceiver from the input data SBC processor. This data is used to generate the azimuth reference pulse (ARP), the azimuth change pulse (ACP), and the sweep pretrigger, which are used in display generation. The pre–trigger signal pulse marks the start of each display sweep. The ARP marks the zero degree point in the azimuth display scan, and the ACP marks the start of each of the 256 1.4–degree scan sectors within a full 360–degree display scan. These pulses control the generation of display video from the stored target messages so as to produce a correct data display on the maintenance display indicator.

2.2.6.4 Output Video Generation. See figure 11-2, sheet 5. Data read from the SBC data memory after storage by the incoming SBC data processor is used in generating target video, weather video, and beacon codes. Transfer of data from the memory is made through the data memory multibus and the appropriate bus transceiver.

2.2.6.4.1 Display Video. See figure 11-2, sheet 5. Target surveillance data is sent to the target video generator by output SBC processor (no. 3) every time a video pre–trigger is generated in the azimuth pulse generator. The target video generator generates correlated, uncorrelated, beacon response and mapped video for one scan sector sweep based on the data words read from the SBC data memory during the 18 video pre–trigger periods in a scan sector. The video select signal from the maintenance display selects one of the types of video for transmission to the maintenance display. Data is also transmitted from the SBC data memory through another bus transceiver to the beacon code generator. The beacon code generator generates the beacon interrogation and

2.3.1.1.1.1.2 Staggered Gate Generation. See figure 11-7, sheet 1. The system timing unit A A4A120 staggered gate generation function uses the 10.35-, 5.18-, and 2.6-MHz basic clock pulses from the basic clock generation function to produce a series of staggered gate pulses. The staggered gate generation function outputs the staggered gate pulses, at frequencies of 0.65, 1.3, 2.6, and 5.18 MHz, for distribution throughout the weather channel and to be used as clock gates and synchronous enable signals. The channel A or channel B staggered gate reset signal, selected by the online channel input select signal, initiates the staggered gate generation function. The online channel input select signal, from the channel status interface, is low if the online target channel is channel A or high if the online target channel is channel B. The selected channel A or channel B staggered gate reset signal synchronizes weather channel staggered gate generation to the operation of the online target channel synchronizer.

2.3.1.1.1.2 Antenna Position Logic. See figure 11-7, sheets 1, 2, and 3. As the weather data flows through the weather channel processing circuits, the antenna position logic on RAG generator A4A122 provides antenna position pulses and data that are used to correlate azimuth with weather data returns. The antenna position logic inputs raw azimuth reference and change pulses from the online target channel, receiver/processor A or B. The online channel input select signal from the channel status interface (sheet 3) selects the channel A or B raw azimuth reference and raw azimuth change pulses from azimuth pulse generator no. 1 (APG1). Raw azimuth data generated in azimuth pulse generator no. 2 (APG2) is used in channel A or B if an error is detected in the raw azimuth data from APG1 or if APG2 input is remote monitoring subsystem–selected. The online channel input select signal is low when receiver/processor A is online or high when receiver/processor B is online. The raw azimuth reference pulses occur when the antenna is at the zero–degree (north) position, and the raw azimuth change pulses occur at each 0.088–degree increment of antenna rotation. There are 4096 azimuth change pulses and one azimuth reference pulse in a 360–degree antenna rotation. The antenna position logic synchronizes the azimuth position pulses with the 1.3-MHz target processing clock rate, and outputs the synchronized azimuth reference and azimuth change pulses to the weather channel * and WSP. The coherent processing interval pair (cpip) generation and batch time signals * synchronization (sheet 2) functions use the synchronized azimuth reference pulse as an antenna scan start (zero–degree) reference point. The cpip generation function (sheet 1) uses the synchronized azimuth change pulse to generate the 1.4–degree cpip. The monitoring and control processor monitors and schedules tests for the azimuth reference and change pulses via the BIT/FIT logic analyzer interrupt function (sheet 3).

2.3.1.1.1.3 Cpip Generation. See figure 11-7, sheets 1, 2, and 4. The cpip generation function on RAG generator A4A122 uses the synchronized azimuth reference and change pulses to establish the cpip. The cpip is the fundamental target data processing time interval and is based on the time interval required for the antenna to rotate 1.4 degrees. This time interval is established by a count of 16 ACP. The cpip generation function outputs a 16th ACP gate trigger that defines 16 ACP (or one cpip), and a digital cpip count that is a binary count of the 256 cpip in a 360–degree antenna rotation. The 16th ACP gate trigger is the timing signal used by the trigger pulse generation function (sheet 2) to develop trigger pulses that initiate events within the time interval of the cpip. The antenna high/low beam select function (sheet 1), and the weather test target control and data generation function (sheet 4) use the digital cpip count as a real–time cpip reference.

2.3.1.1.1.4 Trigger Pulse Generation. See figure 11-7, sheets 1 and 2, and timing diagram, figure 11-9. The trigger pulse generation function (sheet 2) consists of a circuit centered around preprogrammed memory on RAG generator A4A122, and a stabilization circuit on system timing unit B A4A121. Weather test target generator A4A124 provides the interface for the channel A

and B high voltage off signals from receiver/processors A and B. The 16th ACP gate trigger from the cpip generation function (sheet 1) initiates the generation of a sequence of trigger pulses that:

1. Define the cpip and the time intervals within the cpip, and

2. Start receiver events that occur within the cpip.

Trigger pulse timing is determined by site prf set number, which is a variable site parameter (VSP) selected at installation. For a particular prf set number selection, the timing can be fixed or can automatically vary to compensate for antenna speed variations. Timing control is a function of the monitoring and control processor via the multibus. The fixed rate timing parameters for the trigger pulses are programmed into RAG generator board memory; the variable timing mode is implemented by adding a delay factor to the memory addressing. The RAG generator board memory generates all of the trigger pulses except those that must always be maintained at a fixed rate relative to the start of receiver live time. These fixed–rate (stabilized) trigger pulses are generated by system timing unit B. The multibus provides address and control signals (from the monitoring and control processor) required to access the RAG generator memory to output the trigger pulses. The 16th ACP gate trigger synchronizes the trigger pulse outputs to the real–time azimuth position of the antenna. The trigger pulse generation function also outputs a digital, real–time binary count of the range cells that occur within each prt. There are 18 or more prts in a cpip, depending on antenna speed. The length of time it takes the antenna to rotate 1.4 degrees (16 ACPs) determines the number of prts. Within each prt, the weather channel processes weather data in 1/16–nautical mile increments known as range cells (973 range cells equal 60– and 13/16–nautical miles; one range cell is equivalent to one 1.3-MHz clock).

2.3.1.1.1.4.1 Cpip, Cpi, and Prt Start Triggers. See figure 11-7, sheets 2 and 3. The cpip, cpi, and prt start triggers define the start of the cpip, cpi, and prt processing intervals, respectively. The cpip start trigger is a cpip reference signal for the filter and magnitude processor and the monitoring and control processor. The prt start trigger is a prt reference trigger for the filter and magnitude processor. The monitoring and control processor uses the cpip and prt start triggers in monitoring and control processing functions via the cpip start trigger and prt start trigger interrupt logic functions (sheet 3). The monitoring and control processor tests the cpip, cpi, and prt start triggers via the BIT/FIT logic analyzer interrupt function (sheet 3). The weather channel synchronizer normally uses the prt and cpip start triggers generated in the online target channel, receiver/processor A or B. The online channel input select signal from the channel status interface (sheet 3) is low to select the online target channel inputs, channel A prt and cpip start triggers, or high to select the channel B prt and cpip start triggers. The online channel input select signal is low when receiver/processor A is online, or high when receiver/processor B is online.

2.3.1.1.1.4.2 Receiver Event Triggers. See figure 11-7, sheets 1, 2, 3, and 4. The remaining triggers from the trigger pulse generation function are timing signals for receiver events that occur within the prt. The range zero trigger indicates the start of target data detection. The end–of–range trigger indicates the end of the radar range (60 nautical miles), and the CFAR end trigger indicates the end of the range used for CFAR calculations (60– and 13/16–nautical miles). (The target and two–level weather detector, in the target channel, control the CFAR by averaging the echo return power from a range of 13/16 nautical miles on either side of each 1/16–nautical mile range cell. The average power calculation sets the threshold level for target detections. The CFAR range extends 13 range cells beyond the 60–nautical mile radar range to allow the average power calculation

for the furthest range cell.) The calibration trigger initiates the calibration and test of rf/i–f receiver servo loops via the receiver calibration and test control function (sheet 4). The single gate pulse signal is a clock enable for the I/Q d/a conversion function (sheet 3) that provides I/Q video for viewing at test points. The 0.5–nautical mile trigger is used internally by the trigger pulse generation function (sheet 2) for establishing a window during which the timing of the prts within a cpip can be varied by VSP delay factors. All receiver event triggers are tested by the system timing unit A BIT/FIT logic analyzer interrupt function (sheet 3).

2.3.1.1.1.5 A/d Interrogate Pulse Generation. See figure 11-7, sheet 2. The a/d interrogate pulse generation function on system timing unit B A4A121 outputs the interrogate pulse, used on the a/d converter board of the rf/i–f receiver for a/d interrogations. The prt start trigger enables the output of the interrogate signal.

2.3.1.1.1.6 Batch Control Sequence Generation. See figure 11-7, sheets 2 and 3. The batch control sequence generation function on batch control sequencer A4A117 (sheet 2) generates a series of batch control signals that sequentially order the flow of weather data, starting at the filter and magnitude processor and proceeding through all the six–level weather detector/processor functions. The batch control signals not only control the data flow but also initiate the processing functions that occur at various stages in the data path. Each batch control sequence controls the data flow for one "batch" of data. A batch of data includes the weather, test, and calibration data processed during one cpip. The batch control signals that control the flow of data are stored in preprogrammed memory in the batch control sequencer. The memory access is started by the cpip start trigger from the trigger pulse generation function. The batch control signals go to the filter and magnitude processor and to the six–level weather detector/processor. The monitoring and control processor schedules tests and monitors the batch control signals via the BIT/FIT logic analyzer interrupt function (sheet 3). This function sends a batch control sequence test control code to select one of the batch control signals to test, and the batch control sequence generation returns the selected batch control test signal to the BIT/FIT logic analyzer interrupt function. Under control of the monitoring and control processor, the BIT/FIT logic analyzer interrupt function tests the signal and generates interrupt request RUINT04- when the test is completed. The monitoring and control processor services the interrupt request by reading the test results.

2.3.1.1.1.7 Batch Time Signals Synchronization. See figure 11-7, sheet 2. The batch time signals synchronization function on system timing unit B A4A121 sends three batch time signals to the six–level weather detector/processor: the antenna polarization flag (circular or linear), the north indicator (antenna at zero degrees), and the level–of–weather flag (toggles on alternate scans). The six–level weather detector/processor uses the batch time signals to select preprogrammed VSPs that define weather detection threshold values. The batch time cpip clock, enabled by the cpip start trigger from the trigger pulse generation function, synchronizes the batch time signals to batch processing time.

2.3.1.1.1.8 Antenna High/Low Beam Select Signals. See figure 11-7, sheets 1 and 4. The antenna high/low beam select function on system timing unit A A4A120 (sheet 1) outputs the high/low beam select signal (during live and calibration times) based on the VSP parameters selected by the remote monitoring system operator (for live time only). The monitoring and control processor programs and stores the selected VSP parameters in memory on system timing unit A. The high/low beam select signal controls whether the high or low beam (located in the antenna feedhorn) is used during the reception of the target data. The high/low antenna beam select signal from the online target channel, receiver/processor A or B, is used by the weather channel when operating

in linear polarization. (The weather channel uses the online target channel live time receiver data during
* linear polarization.) If the WSP is installed this is no longer the case, that is, when the ASR9 is online LP, the WSP assumes control of the 10A1S1 switch. That is, the WSP 10A1S1 control signals are mixed in and replace the ASR9 control signals. When the antenna is operating in circular polarization, * the weather channel generates its own receiver data, and the antenna high/low beam select function generates the high/low beam select signal. This function also generates a high/low beam select signal that is used during some of the BIT/FIT calibration tests (mds, stc, and a/d 3–point) that test the operation of the receiver servo loops. The calibration tests, initiated by the calibration trigger, occur during dead time in the second cpi in a cpip (cpi B, the low prf transmission cpi). The calibration trigger initiates generation of the calibration test high/low beam select signal, which is generated in both circular and linear modes.

* **2.3.1.1.1.8.1 Automatic vs. Manual Linear Polarization Beam Select.** See figure 11-7, sheets 1 * and 3. The antenna high/low beam select function (sheet 1) receives the antenna polarization flag from system control. The flag is set when the antenna polarization is switched manually by the operator at
* the local RMS terminal or when switched automatically by the weather processor. The automatic switch from CP to LP is made based on the percent of weather cell set below a predetermined threshold (Weather VSP). The flag is high to select linear polarization mode. A high level antenna * polarization flag enables the online channel input select signal from the channel status interface (sheet 3) to select the high/low beam select signal from the online target channel, receiver/processor A or B. The online channel input select signal is low when receiver/processor A is online, or high when receiver/processor B is online. A low level online channel input select signal transfers the channel A beam select signal to the high/low beam select line. A high level online channel input select signal transfers the channel B beam select signal to the high/low beam select line. During calibration tests, the calibration trigger from the trigger pulse generation function on the RAG generator initiates the
* generation of the high/low beam select signal. The polarization is also set to circular during calibration time so the Weather rf/if components can be tested. *

* **2.3.1.1.1.8.2 Automatic vs. Manual Circular Polarization Beam Select.** See figure 11-7, sheet 1. The antenna polarization flag from system control is low to select the circular polarization mode. The automatic switch from LP to CP is made based on the percent of weather cell (above level one) set above a predetermined threshold (Weather VSP). See TI Manual 6310.24 paragraph 2.3.4. The WSP reads these ASR9 VSPs to determine when to switch polarizations based on the percent of cells above level 2 that are filled. If the WSP is online and the polarization switch is in Auto, then the WSP will send a message via the RPG control link (see Figure 11-7 sheet 6) to switch polarization. A low level * antenna polarization flag enables a memory in the antenna high/low beam select function to output a programmed high/low beam select signal. The monitoring and control processor, via the multibus, programs the memory with VSP selected by the remote monitoring subsystem operator. The VSP define range and azimuth windows. The memory map for antenna high/low beam selection covers the entire 360–degree, 60–nautical mile radius of the antenna scan. As each programmed range and azimuth interval occurs in real time, the memory outputs the preprogrammed beam select signal (high for high beam, low for low beam). The real time azimuth reference is the digital cpip count from the cpip generation function. The real time range reference is the digital range cell count from the trigger pulse generation function (sheet 2). The calibration trigger, from the trigger pulse generation function on the RAG generator A4A122, initiates the generation of the high/low beam select signal during calibration tests.

2.3.1.1.1.9 Data Path Select Interface. See figure 11-7, sheet 3. The data path select interface function on system timing unit A A4A120 transfers a data path select code from the monitoring and
* control processor to the filter and magnitude processor. The WSP configuration alters this control when it is online in circular polarization it will select the online target channel I/Q data because it already has *

* the CP returns from its own if receiver. The filter and magnitude processor uses the data path select code to choose the weather data input path to the a/d interface board. *

* **2.3.1.1.1.10 Channel Status Interface and the WSP Online/Maintenance command.** See figure 11-7, sheets 3 and 4. The channel status interface function on system timing unit B A4A121 (sheet 3) transfers the channel unavailable signal from the monitoring and control processor, via the multibus, to the local system control processor. The channel unavailable signal (active high) indicates that the weather channel is in maintenance mode. When the weather channel is in maintenance mode, the channel unavailable signal goes to the sensitivity time control function (sheet 4) to turn off the weather channel sensitivity *

time control attenuation. The channel status interface function also outputs the online channel input select signal which is a select signal for all weather channel synchronizer functions that use inputs from the online target channel, receiver/processor A or B. The level of this signal is established by the online channel A/B select signal from the local system control processor. The A/B select signal reflects the position of the ONLINE/STANDBY switch on the system control panels located in the weather receiver/SCIP cabinet, in the remote monitoring subsystem menus, and in the remote SCIP. The system operator uses the online/standby switch on the weather receive/SCIP system control panel to select the online or standby status of target channels A and B. The online target channel provides the weather channel with frequency generator signals and with synchronizer timing signals. It is not possible to put the WSP online or offline from the ASR9 panels. The WSP must be commanded online or into maintenance mode from its own terminals. The only caveat to this is to force the WSP offline by changing the WSP exist VSP, this VSP will force the ASR9 software to ignore the WSP interface. *

2.3.1.1.1.11 Frequency Generator Control Signals Interface. See figure 11-7, sheet 3. The frequency generator control signals interface on weather test target generator A4A124 generates seven control signals used to enable the weather channel's rf/i–f receiver function to use the online target channel's frequency generator STALO, rf test target generator, and COHO input signals, and two signals used to control the weather channel's filter input/output signals.

2.3.1.1.1.11.1 Frequency Generator Control Signals. See figure 11-7, sheet 3. The frequency generator control signals control flow of COHO, STALO, doppler tone, and rf test target signals from the online target channel to the weather channel. The online channel A/B select signal from the local system control processor is low when receiver/processor A is online or high when receiver/processor B is online. The online channel A/B select signal is tied to seven line drivers in the rf/i–f control signal interface. The line drivers output seven switch control signals. Four electro–mechanical switches (COHO 4A3S1, DOPPLER 4A3S2, STALO 4A3S4, and RFTTG 4A3S2) are located in the weather channel. The COHO, doppler, STALO, and rf test target switch controls from the control signals interface go to these four switches to enable signal flow from the online channel to the weather channel rf/i–f receiver, and to disable signal leakage from the standby channel. The channel A and channel B rf test target switch control signals go to the up–converter module in frequency generator in channel A and channel B, respectively. These signals enable rf test target signal input from the online channel and disable rf test target signal input from the standby channel. The filter select 1 control signal enables the rf test target signal input through filter switch 4A3S6 into one of two tunable filters in the weather channel. The two tunable filters correspond to the operating frequency of target channels A and B. The filter switch passes the rf test target signal to the filter tuned to the frequency of the online target channel.

2.3.1.1.1.11.2 Filter/Blanking Control Signals. See figure 11-7, sheet 3. The channel A and channel B filter on/off control signals go to the filter switch in the weather channel's waveguide to enable the filter output signal from the online target channel and to disable the filter output signal from the standby target channel. The control signals disable both output paths during transmission to prevent energy leakage from damaging the weather rf/i–f receiver. The rf/i–f control signal interface receives GUARD WINDOW CHA and CHB signals from receiver/processors A and B. The guard window signals define the channel A and channel B transmission windows. A guard window signal is high when the respective channel transmitter is on. The online channel A/B select signal from system control, low when receiver/processor A is online or high when receiver/processor B is online, selects the guard window signal from the online channel to produce the channel filter A or B on/off switch control signal.

2.3.1.1.1.12 Sensitivity Time Control. See figure 11-7, sheets 3 and 4. The stc function on STC/calibration generator A4A123 (sheet 4) provides clock and attenuation data to the stc

attenuator during the processing of high level (levels 2 through 6) weather rf energy from the antenna. During low level (level 1) weather data processing, no stc attenuation is used. The stc function regulates the weather rf energy inputs to protect the rf/i–f receiver from saturation. The attenuation data is stored in memory that is accessed under control of the monitoring and control processor via the multibus. The stc clock, generated from the 5.1-MHz clock input, clocks the data into the stc attenuator. The stc function is reset under control of the prt start trigger, the channel unavailable signal, and the level–of–weather flag. The monitoring and control processor tests the stc reset signal and stc clock through the BIT/FIT logic analyzer interrupt function (sheet 3). The receiver calibration and test control function generates the calibration stc test data during receiver calibration time when selected online tests are interleaved with receiver calibration updates.

* (WSP-features) The new WSP interface required additional interface circuitry on the WSP STC/CAL/GEN board. The High Beam STC circuitry was removed to accommodate the new circuitry because only one STC unit is used for both high and low beams on the Weather channel. That is, in the weather channel high/low beam switching is performed at 10A1S1 on the antenna feed horn, before the Rotary Joint and STC unit. In the ASR9-CP mode the STC is determined by the WSP, and the high and low beam is switched on an alternate scan basis in the first 30 nmi.

(determined by VSP). *

2.3.1.1.1.13 Receiver Calibration and Test Control. See figure 11-7, sheets 2, 3, and 4. During dead time of a low prf transmission (cpi B), the receiver calibration and test control function on STC/calibration generator A4A123 (sheet 4) initiates four calibration events:

1. Calibration and update of rf/i–f receiver servos
2. A/d three–point testing
3. Stc testing, and
4. Mds testing.

The stc and mds tests require an rf test target, which is generated by the online target channel and input to the weather channel through RFTTG switch 4A3S3 (sheet 3). The online channel input is selected by the rf test target switch control signal generated in the frequency generator control signals interface, described in paragraph 2.3.1.1.1.11. The rf test target is injected into the weather channel waveguide filter for the online target channel. Filter select 1 signal from the frequency generator control signals interface is switched through the online filter to the weather rf/i–f receiver, by the filter A or B on/off control signal from the control signals interface. The a/d interrogate signal from the a/d interrogate pulse generation function on system timing unit B (sheet 2) goes to the a/d converter in the weather rf/i–f receiver where it controls the a/d input timing, for a/d conversion of rf test targets. This converted data goes to the monitoring and control processor via the filter and magnitude processor where test data calculations and conclusions are determined. The sample window enable initiates a window of time when the filter and magnitude processor monitors the data. An internal control sequence in the receiver calibration and test control function (sheet 4) outputs a control sequence for all calibration time events. This control sequence includes all control signals output by the receiver calibration and test control function. The monitoring and control processor schedules tests and monitors
* these signals via the BIT/FIT logic analyzer interrupt function (sheet 3). (WSP feature) When the WSP is online the Receiver Calibration and Test Control functions are maintained by switching XSW103/104 *

* back to the ASR9 mode during dead time. The idea is to revert all ASR9 signals back to the ASR9 Mode during dead time so that the system is fooled into thinking it is in normal ASR9 mode during dead time. *

2.3.1.1.1.13.1 Calibration and Update of Receiver Servos. See figure 11-7, sheets 2, 3, and 4. The calibration trigger from the trigger pulse generation function (sheet 2) initiates the calibration of the rf/i–f receiver servos once during each cpip. For each of the five servos (agc, phase, gain, I/Q, and bias), a desired state for a particular receiver parameter is computed by the monitoring and control processor, based on information retrieved from calibration data received from the rf/i–f receiver. During the following calibration, the monitoring and control processor sends the calculated parameter data to the receiver calibration and test control function (sheet 4) via the multibus. The data is stored in memory until the calibration update is initiated and is then output on the receiver calibration data lines. The calibration trigger starts the internal control sequence which outputs the control signals for all calibration events. These control signals include the test id code which tells the rf/i–f receiver which calibration event is to occur, and the receiver calibration clock which latches receiver calibration data into the rf/i–f receiver. The analog circuits in the rf/i–f receiver are set to the requested receiver calibration data values corresponding to the decoded test id code, and the servos are adjusted to the desired parameters. The a/d interrogate signal from the a/d interrogate pulse generation function on system timing unit B (sheet 2) goes to the a/d converter in the weather rf/i–f receiver where it controls the a/d input timing enabling correct a/d conversion of calibration test results. This converted data goes to the monitoring and control processor via the filter and magnitude processor where test data calculations and conclusions are determined. The sample window enable initiates a window of time
* during which the filter and magnitude processor monitors the data. (WSP features) No change here. *

2.3.1.1.1.13.2 A/d Converter Three–Point Test. See figure 11-7, sheet 4. The a/d three–point test is a calibration time event used to ensure that the a/d converter in the weather rf/i–f receiver is operating properly at three levels of input (+4, -4, and 0 dc voltages). The monitoring and control processor sends a/d converter three–point test data to the receiver calibration and test control function, and the test id code and receiver calibration clock are generated as described for the calibration and update of receiver servos in the preceding paragraph. The test data goes to the rf/i–f receiver on the receiver calibration data lines, the test id code is decoded, and the test data is converted to +4, -4, or 0 volts dc. The receiver a/d test enable signal from the internal sequence generator in the receiver calibration and test control function controls a multiplexer on the a/d converter board that selects the data processing path. The a/d three–point test results are converted to digital and sent to the monitoring and control processor via the filter and magnitude processor where test data calculations and conclusions are determined. The sample window enable initiates a window of time when the filter and magnitude processor verifies the output data is with +/-5% of the input test data. The a/d three–point test is repeated for each voltage level at one–second intervals. Additional a/d three–point test criteria is
* provided in paragraph 2.3.1.2.2.4.2. (WSP features) No change here. *

2.3.1.1.1.13.3 Stc Test. See figure 11-7, sheet 4. The stc test verifies that the weather channel's stc attenuator is functioning properly. The rf test target generated in the online target channel (refer to paragraph 2.3.1.1.1.13) is inserted into the weather channel waveguide. The selectable parameters for the test target include range and range extent, azimuth and azimuth extent, center doppler, and doppler width. The weather channel stc attenuator attenuates the test target based on the current stc curve parameters stored by the sensitivity time control function. The monitoring and control processor sends the weather channel's stc curve calibration data to memory in the receiver calibration and test control function via the multibus. During calibration, this data is placed in temporary storage in the sensitivity time control function, and is clocked into the stc attenuator by the stc clock signal. The control

sequence generator in the receiver calibration and test control function generates the select signal that places the attenuation data in the stc data path. The stc test results are converted to digital and sent to the monitoring and control processor via the filter and magnitude processor where test data calculations and conclusions are determined. The sample window enable initiates a window of time when the filter
* and magnitude processor monitors the data. (WSP features) When the WSP is online, this test is maintained by swapping back to the ASR9 mode for all the 9's control signals during calibration time. The data streams are reverted to the normal dead time scenario that the ASR9 employs to maintain BIT functionality. *

* **ASR-9/WSP Interface**

This section presents an overview of the ASR-9/WSP interface initiative as illustrated in Figure 11-1a. The majority of the interface functionality physically resides on the WSP/STC/CAL Generator board (4A123). This section addresses the calibration, synchronizer signals and other items that are used in extracting the radar's I/Q data for processing by the WSP. This description delineates the system control software requirements needed to implement the control and monitoring functions in the ASR9 equipment. Finally, it explains the switching mechanism employed to create the proper environment for WSP signal processing. The operational controls of the WSP are intrinsic to the ASR9 system controls. This paradigm shift results when both systems must share common ASR9 resources. This interdependency adds functionality to the ASR9 system specification that is not in its baseline configuration documentation.

WSP RF/IF Receiver Signals:

WSP High Beam

High beam return signals are provided to the WSP receiver by inserting a power divider in the ASR9 high beam waveguide path. When the high beam return signal path divides, it follows that the ASR9 calibration test target signals are also routed down the WSP path. The power divider takes half the signal power (3 decibels) away from both the radar return and the calibration test target signals and routes it to the WSP. The following internal calibration alarms result from the three decibel loss in the high beam path, shortly after the installation of this waveguide component.

- Alarm 212 ---- MDS HI Beam Degrade
- Alarm 225 ---- High Beam RFTTG Ref Degrade

The WSP power divider is located in the middle of the High Beam MDS calibration loop. To compensate for its effect on the MDS, a lowered alarm threshold window for the MDS is implemented in the SSM011 (WSP) ASR9 Receiver Monitor software. This solution to leave the calibration levels alone and expect the hardware to pass the certification tests at decreased signal levels will require a modification to the 6310.19 ASR9 handbook. The critics of this approach maintain that the classical method for measuring MDS at the 50% detection point is a daily check at the old radars, the ASR9 BIT test performs a continuous measurement. It may not be reasonable to expect the same variation for the MDS values, when they are operating at a reduced signal level close to the noise floor. Additionally, the loss associated with this power splitter represent an increase in the system noise, and this may effect the target detection capabilities, but reducing the STC attenuation curve 3 db., compensate for the power splitter loss.

The ASR9's MDS value is calculated from a table that converts the number of test target detections in 1024 tries to an MDS decibel value. The MDS is measured in the 50% detection region (-106.5 dbm.) because the variation of the signal to noise ratio is steeper in this region than at much higher or lower *

* detection values. To calibrate the MDS, a test target is inserted in the waveguide at the reference level of 106.5 dbm corresponding to the system's 50% detection requirement. This input is called the reference test target level. The second step is to increase the programmable attenuator 32db, and remove a fixed 32db attenuator. The third step completes a second MDS measurement, and is called the raw MDS. Finally, the raw MDS is subtracted from the reference measurement to get the MDS compensation value which is stored in non-volatile ram. The MDS compensation value is used to adjust the programmable attenuator so that calibrated MDS measurements are made in the future. The MDS Cal compensation value is added to the VSP screen read backs after SSM011 is installed.

Thus, the WSP modification is holding onto the MDS calibration procedure. We modified the software alarm threshold levels enough to extinguish these alarms on all the sites and leave the MDS procedure intact. This solution does not require changing any calibration baseline procedures that have been working reliably for many years at the ASR9 sites.

WSP Low Beam:

When the ASR9 selects the high beam receive signal returns, the Low Beam receive signal is routed to the WSP receiver by Waveguide Switch XSW101 (see Figure 11-1a). This WSP pin diode switch XSW101 is added to the low beam receive path. This switch is inserted in the waveguide after the low beam receiver protector; therefore, it is subjected to the residual energy leakage out of the receiver protector. Measured leakage out of the receiver protector varies between 120 and 140 watts peak. This new switch has a 300-watt peak power rating. A guard state signal is sent to this new switch which will forward bias the pin diodes in both paths, when the transmitter pulse is present. When the PIN diode is forward biased, it shorts a quarter wavelength stub creating the appearance of an open condition at the input to the switch, thus the transmitter pulse energy will be reflected back toward the receiver protector when the input to the switch appears open. In the Guard State, the isolation provided by the WSP beam switch will be greater than 40 decibels.

WSP RF Beam Switches XSW103/104

The WSP_STC/CAL/GEN board will relay the control signals from the RPG to the RF switches XSW103 and XSW104 (see Figure 11-1a). To control these switches from the RPG, the WSP must be Online. The control for the switches will be transferred to the ASR9 if Local System Control determines the WSP is not operational. In this case, the switches will be set to a mode where the ASR9 Weather Processor will use the return signals from the antenna. Switch state readback lines go from the switch, through the STC/CAL/GEN board, and back to the RPG for confirmation of the switch position. During radar dead time, the switches must direct the RF test target signals to the ASR9 Weather Processor. This requirement insures the RF switches, along with the existing microwave components in the ASR9 weather RF and IF paths, are subjected to the rigorous testing environment designed in the baseline configuration.

WSP Control and Monitoring:

WSP/ASR9 Switch. The control and monitoring scheme is illustrated in the Figure 11-7 sheet 6. Fundamental to this scheme is the ability to switch between the WSP online and the baseline ASR9 modes of operation. To implement this switch, the WSP communicates with the ASR9 Local System Control via the RS232 link between the WSP_RIM and the ASR9_LSC#1 board. This link was used for ANS-2 patch loop-back FIT test before the WSP modification, therefore, when this FIT test is in progress, it must use the ANS-1 link. The ASR-9 shall send the Control and Status messages to the WSP over this ASR9/WSP communications channel. The WSP shall extract information it requires *

* about the current state of the ASR-9 from these messages. These messages include information about:

Polarization	linear or circular
Polarization	auto or manual
Antenna Rotation	on or off
Online Channel	A or B
High Voltage A	on or off
High Voltage B	on or off

When the ASR9 System Control determines the WSP is degraded, it will change the state of a discrete line going to the WSP-STC/CAL/GEN board. This board will then switch all signals necessary to restore the ASR9 to its baseline ASR9 architecture.

WSP AP Free 6 Level Weather Serial Data:

The WSP shall also output a CD-2 format AP-free 6WX data stream. An entire weather map shall be transmitted every 6 scans. The duration for sending each map shall not exceed 3 scans. The WSP shall include each CPC (Control Panel Configuration) message it receives in the AP-free 6LVL WX data stream. The CPC message transmitted shall be identical to the CPC message received. The transmittal of these messages shall be done on a priority basis (minimal delay in WSP). The WSP CPC message and AP-free 6WX will replace the ASR9 6Lvl WX data stream and CPC message when it is switched in place of the ASR9 6WX on the LSCI2 board. This switching scheme is illustrated in Figure 11-7 sheet 7 where it outputs to modem #3. A read back of the multiplexer switch will indicate whether the ASR9 or the WSP weather map is selected, and will determine the state of a WSP system control panel light. The CPC message for the ASR9 will be embedded in the WSP weather map data. The SCIP shall receive this data and process it for display on the controllers screens, while Remote System Control extracts the CPC message for the ASR9 Control Panels.

The WSP shall send requests for polarization changes (LP/CP) to the ASR-9 using the RPG serial control path. The ASR-9 shall perform all valid polarization change requests received from the WSP as if it came from the in Control Panel. A WSP polarization change request is valid if all of the following conditions are true. Polarization is in auto mode and the WSP is the online weather source.

3.3 Radar Calibration Time. Also during radar calibration time (60nmi-0nmi), if the L/P mode is selected for the ASR9, the new hardware on the STC/CAL/GEN board associated with this modification will direct the WSP Switch Matrix to supply the WX C/P test targets to the ASR9 Receiver. The I/Q data multiplexer on the ADI board must follow the RF switch matrix and direct the Weather Channel A/D data to the ASR9 Weather Processor. This switch from the Co-Polarized CP I/Q data to the Weather channel CP data during dead time will be handled by the ADI board signal CALOL. This is necessary to satisfy the ASR9 BIT tests.

3.4 WSP/ASR9 Communication Channel. The WSP shall send status information to the ASR-9 using the ASR9/WSP communication channel. This data shall include, but not be limited to:

WSP	online or offline
WSP	summary alarm or normal
WSP	unavailable or available
WSP	performance data

*

* The ASR9/WSP communications path directs the CPC Control Panel Configuration message between the ASR9's System Control Unit and the WSP. This data path is physically located between the ASR9 LSCI1 board's USARTS and a WSP's serial port. The path routes the data from the System Control LSCI1 board through the WSP/STC/CAL Generator board through the Sigmet Chassis and finally it reaches its destination in the WSP-RDG chassis. All communications between the ASR9 and the WSP will be limited to this path. If the WSP is online, not summary alarmed and not unavailable, then the ASR-9 shall direct the WSP data to Modem #3. A multiplexer on the ASR9's LSCI#2 board will select the 6 level weather map either from the WSP or the ASR9 based on the control lines from system control via the STC/CAL board. *

*

Synchronizer Signal and Hardware Description

ASR-9 to WSP Interconnections
Comprehensive Listing

Bolded Signals are used in the existing system

ASR-9 Name	Function	Location	Pin Name	Signal Reference / Comments	Type
PRETO	A trigger that occurs prior to "Main Bang" every PRI.1 Bit TTL compatible. Occurs 5.4 us prior to every PRI. Synchronous with the range cell rate 1.3 MHZ. Active Low, Pulse width is 772 ns.	4A4A120	C72	TI 6310.28 Fig. 11-8, Sheet 6 of 17 From RAG Generator Trigger	Timing
RGRO-	Constitutes the beginning of "Livetime" (Range). 1 Bit. TTL Compatible. Occurs 1.5us after TO synchronous with the range cell rate (1.3 MHZ). Active low. Pulse Width is 772 ns. Single end TTL driver used.	4A4XA120	B75	TI 6310.28 Fig. 11-8, Sheet 8 of 17 From RAG Generator Trigger	Timing
ALTC100(+/-) ALTC111(+/-)	From Alternate Channel. I/Q Data, 12 Bits Two's Complement, Active High, Synchronized with 10.35 MHZ, Data rate period equal to 386ns. Balanced twisted pair.	4A4XA103	B13/B14 ..... B35/B36	TI 6310.28, Fig. 11-16, Sheet 1 of 9	Data
SA1.3TSTGTS(+/-)	Range Clock 1.3 MHz. A series of synchronous enable used for clock gating. TTL compatible. Active High. Pulse width is 96ns.	4A4AX120	A58/A59	TI 6310.28 Fig. 11-8, Sheet 2 of 17	Timing
PLL2.6MHZ2	2.6 MHz Phase-lock Clock. A series of synchronous enable used for clock gating. TTL compatible. Active high. Pulse width is 96ns.	4A4AX114	C26 (grd B26)	TI 6310.28 Fig. 11-8, Sheet 1 of 17	Timing

*

*

Synchronizer Signal and Hardware Description (Continued)

ASR-9 to WSP Interconnections
Comprehensive Listing

Bolded Signals are used in the existing system

ASR-9 Name	Function	Location	Pin Name	Signal Reference / Comments	Type
10.35MHZ(+/-)	10.35MHz Phase-lock Clock. Basic clock supplied to everyone. 1 Bit. TTL compatible. This is 10.35MHZ. Active in rising edge. Rising edge to rising edge is 96 ns. Single ended TTL drivers are used.	4A4XA114	A16/A17	TI 6310.28 TO A4J108 25/26 Test only. Digital Clock Buffer	Timing
RGCPIST-	Constitutes the beginning of a CPI. 1 Bit. TTL compatible. Occurs at To. Synchronous with the range cell rate 1.3 MHZ. Active Low, Pulse width is 772 ns.	4A4A120	B81	TI 6310.36 From Wiring Diagrams Sheet 55	Timing
BEAMONLO(+/-)	Select Beam SW Linear A Select Beam SW Linear B	2A4XA120 & 5A4XA120	A63/A64	TI 6310.26 Figure 11-8, Sheet 2 of 17	Control
LP/CP-	Selected LP/CP	4A4XA121	C27	TI 6310.28, Fig. 11-8, Sheet 8 of 17	Control
WXCHA-/B	Selected A/B	4A4XA121	C80	TI 6310.28, Fig. 11-8, Sheet 9 of 17	Control
BEAMONLOI(+/-)	CP High/Low beam switch (Scan X Scan Switching)	A4J125 4A5J11	9 & 10 2 & 20	TI 6310.28, Fig. 11-8, Sheet 4 of 17 Cable to top of equipment rack	Control
ACP(+-)	Azimuth Change Pulse used to control the azimuth counter. 1 Bit. 4096 per scan. Synchronous with the range cell rate (1.3 MHZ). Active high. Pulse width is 772 ns. Driver is RS-422 compatible.	4A5J2	W571 BNC	TI 6310.28, Fig. 11-8, Sheet 8 of 17	Data Video

*

Synchronizer Signal and Hardware Description (Continued)

*

ASR-9 to WSP Interconnections
Comprehensive Listing

Bolded Signals are used in the existing system

ASR-9 Name	Function	Location	Pin Name	Signal Reference / Comments	Type
(+-)ARP	Azimuth Reference Pulse (north mark) used to reload the azimuth counters. 1 Bit. TTL compatible. 1 per scan. Synchronous with the range cell rate (1.3 MHZ). Active high. Pulse width is 773 ns. Driver is RS-422 compatible.	4A5J2	W571 BNC	TI 6310.28 Fig. 11-8, Sheet 8 of 17	Data Video
SELAD101, 02	Channel A strobe (2:1 mux)	A4A103	A17 & A19	TI 6310.28 See Synchronizer (SELAD101, 02)	Timing
WSP_EN-	Selects WSP or ASR9 mode of operation. 1 Bit. TTL compatible. Software controlled from System Control Board #1	Card #216	A61 A62	TI 6310.26 Wiring List	Control
WSTSTC00 …….. WSPSTC05	Controls the sensitivity time control attenuator in the weather receiver channel. 6 Bits. TTL compatible. Programmable over full range (60 nm). Synchronous at half of the range cell rate (2.6 MHZ). Pulse width is determined by the STC curve. Active High (All "ONES" for maximum attenuation). RS-422.	P2/A4J1		TI 6310.26 WSP STC curve replaces ASR STC curve during WSP operations	Control & Data
WSPSTCCLK	The main clock for the receiver low beam STC functions. 1 Bit. TTL compatible. Synchronous with half of the range cell rate (2.6MHZ). Pulse width is 386ns. Active high. RS-422 compatible.	P2/S6J4	9 Pin "D" Connector	TI 6310.26 WSP failure mode. MUXed ASR-9 and WSP data to A9 STC unit	Control & Data

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*

Synchronizer Signal and Hardware Description (Continued)

ASR-9 to WSP Interconnections
Comprehensive Listing

Bolded Signals are used in the existing system

ASR-9 Name	Function	Location	Pin Name	Signal Reference / Comments	Type
RPGTXD	Data Transmission signal involved in the transfer of information between the ASR9 and WSP RPG. RS-232.			Signal also used in Modem Patch Panel Test	
RPGRXD	Data Receive signal involved in the transfer of information between the ASR9 and WSP RPG. RS-232.			Signal also used in Modem Patch Panel Test	
XSW103/104+/-	Controls RF switches XSW103 and XSW104, located in the WSP RF interface switch chassis. Possible inputs are high beam, low beam, or circular polarization signals from the antenna. RS-422.				
XSW105(0-1)+/-	Controls RF switch XSW106 selection of Online CP inputs to WSP XSW103 and XSW104. RS-422				
WSP_COM_EN	Provides a mechanism to switch between the ASR9 modem patch loop back test and WSP online operation				
RPGTXD	Status and Control data to RPG from ASR9. RS-232				
RPGRXD	Status and Control data from the RPG to ASR9. RS-232				
WSP_6WXTD+-	AP free 6 Level Weather Map from the WSP RPG. RS422				
WSP_6WXCLK+-	Clock for AP free 6 Level Weather Map from the WSP RPG. RS422				

*

* **All digital signals are either RS-422, RS232 or TTL logic levels.** Differential line drivers / receivers or TTL drivers / receivers to interface ASR-9 system.

Signals may appear in multiple locations on the ASR-9 backplane and interconnections.

	ASR-9 Source			**WSP**
	Function Name	**Signal Name**	**Part Name / Tie Point**	**Part Name / Tie Point**
51.	Break out "A" high beam target channel	WSP "A" high beam	XPS101 Cha. A Power Splitter	RF interface box: Cha. "A" high beam
52.	Break-out "B" high-beam target channel	WSP "B" high beam	XPS102 Cha. B Power Splitter	RF interface box: Cha. "B" high beam
53.	Break-out "A" low-beam target channel	WSP "B" low beam	XSW101 Cha. A Power Splitter	RF interface box: Cha. "A" low beam
54.	Break-out "B" low-beam target channel	WSP "B" low beam	XSW102 Cha. A Power SPlitter	RF interface box: Cha. "B" low beam
55.	Cp RF weather signal from antenna	CP Channel	CP high or low beam on alternate scans	RF interface box: CP high or low beam
56.	RF Test Target Generator	RF test target generator	Linear "A", "B", & CP	Used off-line as in ASR-9
57.	Selected COHO	COHO	Remove 3 dB pad and Add 3 dB IF power splitter	WSP Receiver & timing
59.				

*

2.3.1.1.1.13.4 Mds Test. See figure 11-7, sheets 2 and 4. The mds test verifies that the weather channel's rf/i–f receiver can detect a target at the minimum discernible signal level. Just as in the stc test, the rf test target is injected into the waveguide. The stc attenuation values are set to zero. The mds test results are converted to digital and sent to the monitoring and control processor via the filter and magnitude processor where test data calculations and conclusions

are determined. The sample window enable initiates a window of time when the filter and magnitude processor monitors the data.

2.3.1.1.1.14 Test Target Generation. See figure 11-7, sheets 1 through 4. The weather test target control and data generation function on weather test target generator A4A124 (sheet 4) provides target channel A and B two–level weather test target data that is used for the generation of two–level weather test targets in receiver/processors A and B. It also provides six–level weather test target data which is used to generate six–level weather test targets in the weather channel. The weather test targets, used in off–line testing, provide simulated rain clutter. The weather test target data is stored in memory that is accessed by control signals from the monitoring and control processor (via the multibus). They are correlated to real time by the cpip start trigger and digital range cell count from the trigger pulse generation function (sheet 2), by the digital cpip count from the cpip generation function (sheet 1), and by the synchronized antenna reference pulse from the antenna position logic. The monitoring and control processor programs the weather test target data memory on weather test target generator A4A124 with weather test target data based on remote monitoring subsystem menu selections. The remote monitoring subsystem operator selects which channel (A, B, or weather) will run weather test targets, and defines the range/azimuth parameters of the targets. When the remote monitoring subsystem operator also enables rf (population) test targets in channel A or B, the rf test target enable signal from channel A or B is high. The two–level weather test targets, providing up to two levels of simulated rain clutter, are developed in synchronization with the channel A or channel B rf test targets. (The rf test targets are injected into the target data processing path, and the weather test targets are injected into the two–level weather data processing path.) The weather test target range/azimuth gate signals output by the weather test target control and data generation function define the time interval during which weather test targets are enabled. These gate signals are used internally by the weather test target control and data generation function, and are tested via the BIT/FIT logic analyzer interrupt function (sheet 3).

2.3.1.1.1.15 RAG Video Select. See figure 11-7, sheets 1 and 3. The RAG video select function on system timing unit A A4A120 (sheet 3) outputs a RAG video signal that goes to jack J10 on the weather i–f panel assembly A2. The RAG video signal is the high/low beam select signal from the antenna high/low beam select function (sheet 1). The monitoring and control processor, via the multibus, controls the output of the RAG video signal from the RAG video select function.

2.3.1.1.1.16 I/Q D/a Conversion. See figure 11-7, sheets 2 and 3. The I/Q d/a conversion function on PLL channel sync A4A114 (sheet 3) receives digital I and Q weather data components from the filter and magnitude processor, and converts the data to analog signals that go to test points on PLL channel sync A4A114. The single gate pulse signal from the trigger pulse generation function (sheet 2) provides a real time range gate reference to enable the clocking of the data into the d/a conversion circuits.

2.3.1.1.1.17 Interrupt Request Logic Functions. See figure 11-7, sheet 3. The interrupt request logic functions report rf/i–f receiver and synchronizer faults to the monitoring and control processor in the form of an interrupt. The interrupt logic functions are located on system timing unit A A4A120 and system timing unit B A4A121.

2.3.1.1.1.17.1 System Timing Unit B Interrupts. See figure 11-7, sheets 1 and 3. The system timing unit B A4A121 interrupt logic functions (sheet 3) are used during receiver live time. The occurrence of the antenna reference pulse, cpip start trigger, or prt start trigger, causes an interrupt

2.3.1.1.3.6.3.1 EEPROM Write Enables and Addressing. See figure 11-8, sheet 2. The azimuth/range window EEPROM address lines come from the monitoring and control processor via the multibus address lines ADR00- through ADR11-. The multibus interface buffers the address lines, and routes them to the EEPROM 12–bit address select multiplexer as BADR01 through BADR12. The SELMUXANT- signal (active low when the monitoring and control processor is loading the EEPROM) selects BADR01 through BADR12 to form EEPROM address lines A00 through A11. Address lines A04 through A11 are azimuth data addresses, and A00 through A03 are range data addresses. When the EEPROM is addressed, AWRITE- enables the EEPROM I/O ports to input the ANTBS and DRNG04 through DRNG09 data, and WRITEABS- enables the data transfer (write) to the addressed memory location. AWRITE- is active low configuring the EEPROM data ports for input when the monitoring and control processor IOWC- signal is active low and ANTBM- is active low. ANTBM- is decoded from three bits of monitoring and control processor address data (ADR13- through ADR15-) in the multibus interface. (Refer to paragraph 2.3.1.1.2 for a general discussion of board multibus interfaces and the address decode process.)

2.3.1.1.3.6.3.2 EEPROM Data Output. See figure 11-8, sheet 2. The WRITEABS and AWRITE signals are high to enable the azimuth/range window EEPROM to read (output) data. AWRITE- is high when IORC- and ANTBM- are active low, configuring the EEPROM data ports for output. WRITEABS is high after the write operation ends, when the monitoring and control processor raises the level of the IOWC- write enable. When IOWC- goes high, SELMUXANT- also goes high, disabling the data flow control function and selecting the read address in the EEPROM 12–bit address select multiplexer.

2.3.1.1.3.6.3.3 EEPROM Addressing (Read). The azimuth/range window EEPROM read address is derived from CPIADR00 through CPIADR03 from the nautical mile range counter, and RGCIPR00 through RGCIPR07 from the RAG generator board. RGCIPR00 through RGCIPR07 are the AD04 through AD11 address bits. RGCPIPR00 through RGCPIPR07 are a binary count of the cpi pairs in an antenna scan. (The cpip counter and generation of RGCPIPR00 through RGCPIPR07 are described in paragraph 2.3.1.1.3.2.5.2.)

2.3.1.1.3.6.3.4 Nautical Mile Range Counter. The nautical mile range counter synchronizes beam selection to real range–cell time. The counter outputs the azimuth/range window EEPROM address bits CPIADR00 through CPIADR03 each time the range cell count in a prt passes a 1–nmi increment (16 range cells). The prt start trigger RGPRET0- from the RAG generator loads the counter to count zero at the start of a prt. The counter then increments with each active low EQUALS signal from the range comparator. The EQUALS signal is active low when programmed DRNG04 through DRNG09 from the azimuth/range window EEPROM is equal to real time range cell count RGRNG04 through RGRNG09. DRNG04 through DRNG09 is the selected range start or stop time programmed into the EEPROM. RGRNG04 through RGRNG09 is part of the buffered range cell clock count output of the prt range counter on the RAG generator board. The four LSBs of the range cell clock count (binary count of range cell clocks 0 through 15) are not used since range data is selectable in 1–nautical mile (16 range cell clock) increments. The prt range counter provides a real time count of the 1.3-MHz range cell clocks. (The prt range counter is described in paragraph 2.3.1.1.3.3.2.4.2.) When the real time range count equals the programmed EEPROM range count, the nautical mile range counter generates the range address.

2.3.1.1.3.6.4 Beam Selection. See figure 11-8, sheets 2 and 4. The beam select signal ANTBS identifies the high/low beam mode programmed into the azimuth/range EEPROM for the 1–nmi range segment identified by CPIADR00 through CPIADR03. A low ANTBS signal selects

low beam mode and a high ANTBS signal selects high beam mode. The ANTBS signal is one of four inputs to the antenna high/low beam 4–to–1 multiplexer/register. The other three inputs are CHAANTBM, CHBANTBM, and HI/LO-CAL. Like the ANTBS signal, these three signals are low to select low beam mode and high to select high beam mode. The SICHA-/B, SELL/CP-, and CALTRIG- select signals choose the multiplexer input as described in the following three paragraphs. The antenna high/low beam 4–to–1 multiplexer/register outputs beam select signals BEAMSEL, BEAMONLOI, and SGBEAMSEL. The BEAMSEL signal goes to the maintenance monitor panel (if selected) via the maintenance monitor panel interface (described in paragraph 2.3.1.1.3.13). The BEAMONLOI signal goes to the beam select switch via cabinet cable entry chassis connector A5J9 * (sheet 4). The SGBEAMSEL signal goes to the filter and magnitude processor. (WSP Features) **Alternate Scan Processing:** When the ASR9 is in the WSP Circular Polarization mode switch 10A1S1 is used to switch the input to the high dynamic range WSP receiver between high and low beams on an alternating scan basis. The order to avoid continual data degradation at a single azimuth from "switching transients." The switch azimuth is incremented every scan by 75 sectors or 105.47 degrees. This strategy helps avoid a weather map with a dim azimuth located at a fixed crossover azimuth because weather data is average over a number of scans. *

2.3.1.1.3.6.4.1 ANTBS Selection. See figure 11-8, sheets 2 and 9. When the antenna is in circular polarization mode, the active low SELL/CP- signal from delay/logic buffer no. 1 (sheet 2) selects the ANTBS signal from the azimuth/range window EEPROM as the antenna high/low beam 4–to–1 multiplexer/register input. The SELL/CP- signal is the buffered SPLP/CP- signal from the system signal input buffer on system timing unit B A4A121 (sheet 9). The SPLP/CP- signal is the buffered SYSLP/CP- signal from the system control.

2.3.1.1.3.6.4.2 CHAANTBM or CHBANTBM Selection. See figure 11-8, sheet 2. When the antenna is in linear polarization mode, the weather channel uses the antenna high/beam selection signal from the online target channel. The SICHA-/B signal from delay/logic buffer no. 1 selects the buffered SBCHAABM or SBCHBABM signal (SBCHAABMNTBM or SBCHBABMNTBM) from the online target channel, receiver/processor A or B, as the antenna high/low beam 4–to–1 multiplexer/register input. The SICHA-/B signal is low when channel A is online or high when channel B is online. A low level SICHA-/B signal selects the beam select signal from channel A, SBCHAABM, as the antenna high/low beam 4–to–1 multiplexer/register input signal, and a high level SICHA-/B signal selects the beam select signal from channel B, SBCHBABM. (During linear polarization, the weather channel processes weather data from the online target channel instead of from the weather channel rf/i–f receiver, which accepts weather rf energy only in circular polarization mode.) The SICHA-/B signal is the buffered WXCHA-/B signal from system timing unit B A4A121 (described in paragraph 2.3.1.1.3.1.1.1).

2.3.1.1.3.6.4.3 SGHI/LO-CA Selection. See figure 11-8, sheet 2. During rf/i–f receiver calibration time, the active low calibration trigger CALTRIG- from delay/logic buffer no. 1 selects the calibration beam selection HI/LO-CAL as the antenna high/low beam 4–to–1 multiplexer/register input. The HI/LO-CAL signal is the buffered SGHI/LO-CA signal from STC/calibration generator A4A123. Refer to paragraph 2.3.1.1.3.11 for a discussion of rf/i–f receiver calibration time.

2.3.1.1.3.7 Data Path Select Interface. See figure 11-8, sheets 2 and 3. The data path select interface on system timing unit A A4A120 (sheet 3) transfers a three–bit data path select code DB02 through DB04 from the monitoring and control processor to the filter and magnitude processor. The code selects the appropriate input data path for the a/d interface board. The data path selection depends on whether the weather data input is live or test data (sheet 3). The data path select interface receives data DB02 through DB04 from the board data bus under control of the monitoring and control processor write command I0W- and the decoded monitoring and control processor address bit ADDRDEC05-. The multibus interface (sheet 2) transfers the data path select code from the multibus to the board data bus, buffers the write command, and decodes ADDRDEC05-. (Refer to paragraph 2.3.1.1.2 for a general discussion of the board multibus interfaces and the address decode process.) The data path select interface transfers (sheet3) the DB02

2.3.1.1.3.9.2 Filter/Blanking Control Signals. See figure 11-8, sheet 12. The FILTONA and FILTONB control signals are applied to the filter switch in the weather channel's waveguide. The control signals enable the filter output signal from the online target channel, and disable the filter output signal from the standby target channel. The control signals disable both output paths during transmission to prevent from energy leakage from damaging the rf/i–f receivers. The rf/i–f control signals interface receives guard window signal GDWDWA or GDWDWB from receiver/processors A or B. GDWDWA and GDWDWB define the channel A and channel B transmission windows, respectively. A guard window signal is high when channel transmitter is on. The CHA-/B signal from system control, low when receiver/processor A is online, or high when receiver/processor B is online, selects the guard window signal from the online channel to produce the FILTONA and FILTONB signals when either guard window signal goes high. The high–level FILTONA and FILTONB signals close the waveguide switches for approximately two microseconds at transmission.

2.3.1.1.3.10 Sensitivity Time Control. See figure 11-8, sheet 11. The stc/calibration generator A4A123 provides attenuation data to the stc unit in the weather channel waveguide. The attenuation data regulates the amplitude of the received weather energy signals to protect the rf/i–f receiver from saturation. The monitoring and control processor programs stc attenuation data into the STC EEPROM on STC/calibration generator A4A123. The stc attenuation data is programmable over the 60–nmi radar range, in 1–dB increments up to 63–dB maximum. The structure of the programmable 6–bit stc attenuation data word is as follows:

Bit 00 = 1 dB	Bit 03 = 8 dB
Bit 01 = 2 dB	Bit 04 = 16 dB
Bit 02 = 4 dB	Bit 05 = 32 dB

* (WSP Features) The WSP provides the STC attenuation data when it is online. The WSP STC data is switched in to replace the normal ASR9 data at the WSP/STC/CAL GEN board. The STC curve selection is based on the WSP_ENA signal and STCCALCTL signals (see Figure 11-7 sheet 5). *

2.3.1.1.3.10.1 Stc Curve. Weather energy returns are programmed for maximum attenuation at close range, and gradually decreasing attenuation as the range extends further out. This decreases the sensitivity of the radar to strong weather and clutter energy that originates from sources at close range, and increases the sensitivity to weaker returns at greater distances. From a range of 3/8 to 6 nautical miles, the value of the stc attenuation data decreases at a programmable exponential rate (0– to 12–dB per octave). Between nautical mile segments of 6 to 8, 8 to 12, 12 to 16, 16 to 24, 24 to 32, 32 to 48, and 48 to 60, the monitoring and control processor can control the value of the stc attenuation data independently, from 0– to 12–dB per octave in 1–dB steps. Figure 2-24 shows a typical stc curve.

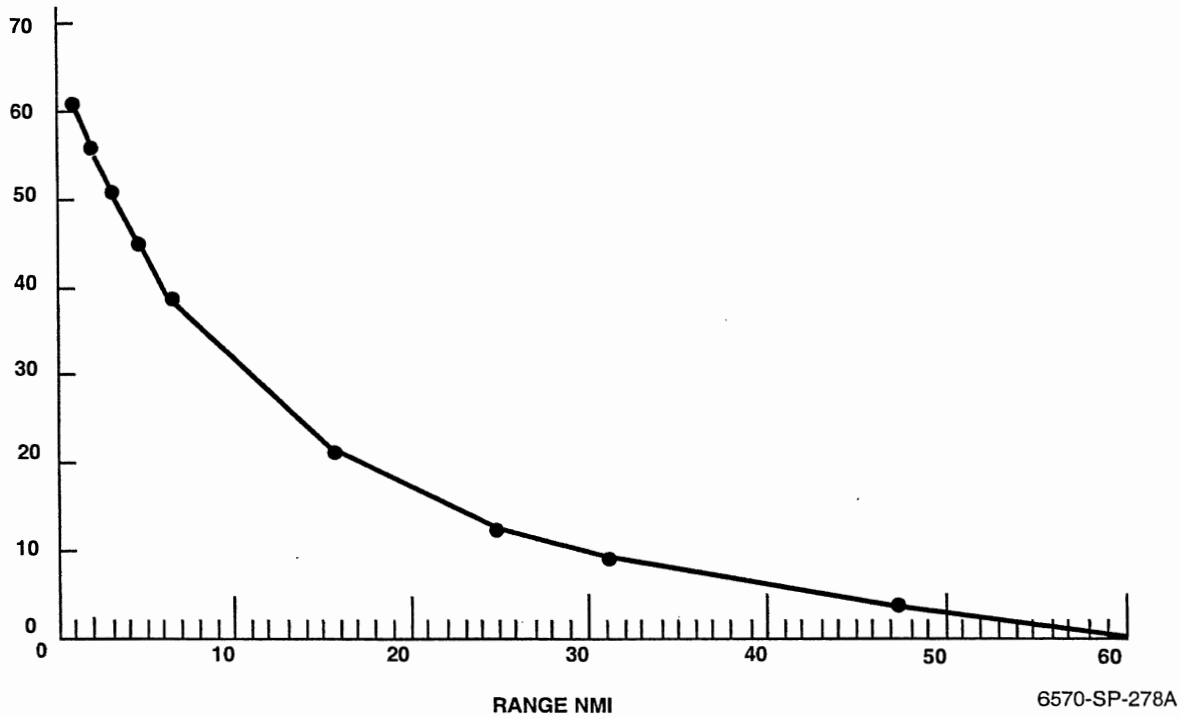


FIGURE 2-24. TYPICAL SENSITIVITY TIME CONTROL CURVE

2.3.1.1.3.10.2 Stc EEPROM Programming. See figure 11-8, sheet 11. The monitoring and control processor programs the stc EEPROM with stc attenuation data. The multibus interface receives the data from multibus lines DAT00- through DAT05-. The multibus interface places the data on the board data bus, and the board data bus transfers it to the data flow control circuit. The data goes to the stc EEPROM on data lines LDATA00 through LDATA05. The read enable IOR- enables the data flow control circuit input, allowing data to flow from the board data bus to the data flow control circuit. The SELMUXSTC- signal enables the data flow control circuit output, allowing the data to flow to the EEPROM. SELMUXSTC- is active low when the monitoring and control processor is writing to the EEPROM (AIOW- and IOW- active low) and the LOSTC- signal is low. The multibus interface decodes LOSTC- from three bits of monitoring and control processor address data (ADR13- through ADR15-). (Refer to paragraph 2.3.1.1.2 for a general discussion of the board multibus interfaces and the address decode process.) The EEPROM stores the stc data LDATA00 through LDATA05 in memory locations addressed by the monitoring and control processor.

2.3.1.1.3.10.3 Stc EEPROM Write Enables and Addressing. See figure 11-8, sheet 11. The monitoring and control processor supplies the stc EEPROM address via multibus address lines ADR01- through ADR12-. The multibus interface buffers the address lines and sends them to the stc PROM address counter/multiplexer as BADDR01 through BADDR12. The SELMUX signal (the inverted SELMUXSTC- signal) selects BADDR01 through BADDR12 to form EEPROM address lines STCADDR00 through STCADDR11. Port enable AWRITE- enables the EEPROM I/O ports to input the LDATA00 through LDATA05 data, and write enable WRITEABS- enables the data

transfer (write) to the addressed location. AWRITE- is active low to configure the EEPROM data ports for input when the monitoring and control processor IOWC- signal is active low and LOSTC- is active low. The multibus interface (described in paragraph 2.3.1.1.2) decodes LOSTC- from three bits of monitoring and control processor address data (ADR13- through ADR15-).

2.3.1.1.3.10.4 Stc EEPROM Data Output. See figure 11-8, sheet 11. The stc EEPROM is enabled to read (output) data when WRITEABS- and AWRITE- go high. AWRITE- is high when IORC- and LOSTC- are active low, configuring the stc EEPROM data ports for output. WRITEABS- is high after the write operation ends when the monitoring and control processor raises the level of the IOWC- write enable. When IOWC- goes high, SELMUXSTC- also goes high, disabling the data flow control function and selecting the read address in the stc PROM address counter/multiplexer.

2.3.1.1.3.10.4.1 Stc EEPROM Addressing (Read). See figure 11-8, sheet 11. The inverted high level SELMUXSTC- signal (low SELMUX) selects the output of a counter in the stc PROM address counter/multiplexer as the stc EEPROM address STCADDR00 through STCADDR11. The prt start trigger RGPRET0- from RAG generator A4A122 starts the counter at count zero. (Refer to paragraph 2.3.1.1.3.3.2.2 for a discussion of the prt start trigger.) The counter increments with each 2.6TSTRB1 clock until the next RGPRET0- signal restarts the count.

2.3.1.1.3.10.5 Stc Register/Multiplexer. See figure 11-8, sheet 11. The 2.6TSTRB1 clock shifts the stc attenuation data LDATA00 through LDATA05 through the stc register/multiplexer. During normal operation, a high SGCALCTRL- signal selects LDATA00 through LDATA05 as the stc register/multiplexer output (LDATA00B through LDATA05B). During receiver calibration tests, a low SGCALCTRL- signal selects the stc test attenuation data CALSTC00 through CALSTC05 as the stc register/multiplexer output. When CALSTC00 through CALSTC05 is selected, LDATA00B through LDATA05B carry stc test attenuation data. (Receiver calibration testing is described in paragraph 2.3.1.1.3.11.) The stc reset signal RESETSTC- clears the stc register outputs at system reset (MR3- low), when the channel is unavailable (SBCHUNAV high), and during odd–numbered antenna scans (SBWXSYNC- high). During odd–numbered antenna scans, the weather channel processes low level (level 1) weather energy and uses no stc attenuation. Therefore, stc attenuation is set to zero. The monitoring and control processor data bit DB00 controls the reset. DB00 is high to reset the stc attenuation to zero. The buffered monitoring and control processor write command IOW-, and the decoded register address signal ADDRDEC04- enable the DB00 data bit. The IOW- and ADDRDECO4- signals are from the multibus interface (described in paragraph 2.3.1.1.2).

2.3.1.1.3.10.6 Stc Attenuation Data Output. See figure 11-8, sheets 11 and 12. Line driver no. 1 couples the stc attenuation data word LDATA00B through LDATA05B to the differential output data lines LOSTCOO through LOSTCO5. The stc data clock function generates 2.6-MHz clock LOSTCCLK from the 5.1NSTRB clock. Line driver no. 1 drives the board LOSTCCLK output line.
* The LOSTCCLK clock latches the stc attenuation data word into the stc attenuator (sheet 12). (WSP Feature) In the case of the WSP, the LOSTC00 through LOSTC05 are intercepted before they leave the board and are muxed in with the WSP STC control signal WSPSTC00 through WSPSTC05. When the WSP is online, the WSPSTC00 through WSPSTC05 is selected. *

*

WSP / STC / Calibration Generator Board

Hardware sections:

1) Timing
2) STC (Sensitivity Time Control) EEPROM input, readback, and output.
3) Calibration PROP sequencer readback and output.
4) FIFO input and output.
5) RAM input and output.
6) Multibus I/O

1) Timing

Timing for the STC card originates on sheet 15 of the STC prints. The signals which are received and then buffered onto the card are:

1) 10.35MHZ
2) 5.1NSTRB
3) 2.6TSTRB1
4) 1.3TSTRB

The following diagram depicts these signals.

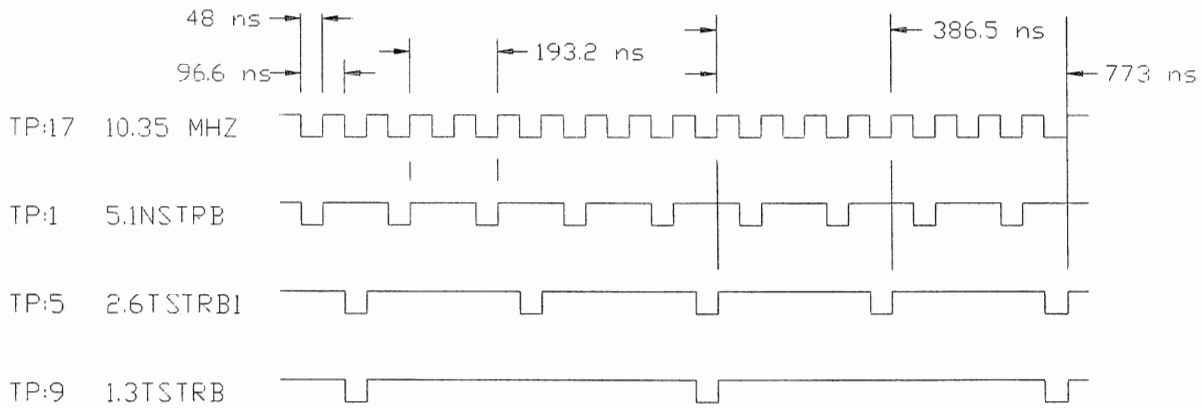


FIGURE 2-24a.

These signals were captured with a sample period of 10 ns but the periods listed are calculated values based on 10.35 MHz. *

* These timing signals are used for counter incrementing, data latching, and waveform creation. In other words, these signals keep the STC data and calibration data (generated on the STC card) in sync with the rest of the system.

2) STC EEPROM input, readback, and output. (Reference WSP/STC/CAL/GEN schematic for the following discussion).

STC EEPROM input and readback.

The WSP modification removed the circuitry associated with the target channel high beam from the original ASR9 STC/CAL Generator board, to make room for the WSP interface circuits. The circuits for the high beam are only used when the board is in the Target channel. The STC EEPROM is loaded with data from the monitoring and control processor multibus. The processor may also read back data from the multibus. WSP/STC/CAL Generator schematic sheets 3 and 4. The multibus can write data (6 bits) thru U13 and U15 I/O drivers to U50 EEPROM. Also, this data may be read back from U50 thru U112 drivers to the multibus. Notice on sheet 3 that the multibus signals –IOR, -IOW and –AIOW are qualified with –LOSTC control the EEPROM writes and reads. On sheet 3, notice that the signal –E2PROMWR must be low to enable the EEPROM writes. This signal is a safety lockout mechanism.

STC EEPROM output.

The following discussion describes how the STC data curve is output from the EEPROMS. This STC (Sensitivity Time Control) data curve controls the receiver attenuation. It is output to waveguide attenuators during active radar time. The near returns are max attenuated and the far returns are min attenuated. Therefore, as time increases (from Azimuth Pretrigger), the attenuation value decreases. The weight is: Bit 0 = 1dB, Bit 1 = 2dB, Bit 2 = 4 dB, Bit 3 = 8dB, Bit 4 = 16dB, and Bit 5 = 32dB.

The signal –APRETO (azimuth pretrigger) occurs once per radar transmitted pulse.

The following diagram shows the –APRETO signal referenced to 1.3TSTRB. –APRETO is received and then buffered onto the card of the STC prints. It starts the STC EEPROM counter sequence.

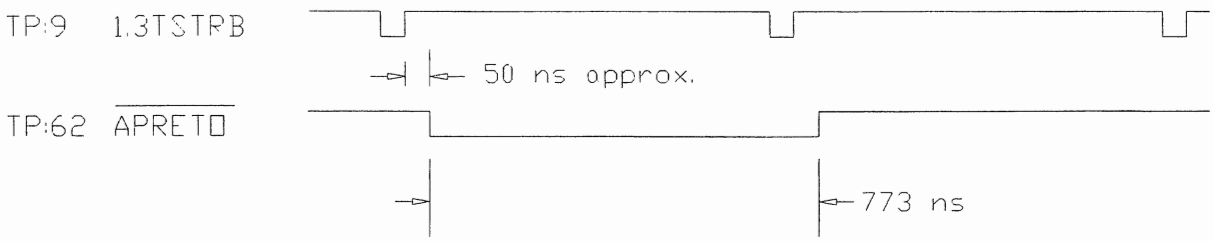


FIGURE 2-24b.

Reference sheet 2 of the prints. The STC EEPROM address counters U10, U11, and U12 are initiated to address 06E hex by the –APRETO signal. The STC address counters are then incremented by the 2.6TSTRB1 pulse starting with the rising edge of the first 2.6TSTRB1 pulse after –APRETO goes high. Therefore, the STC EEPROM outputs the STC data curve beginning at the radar transmitted pulse. *

* The following diagram shows the rest of the signals which control the STC EEPROM data output.

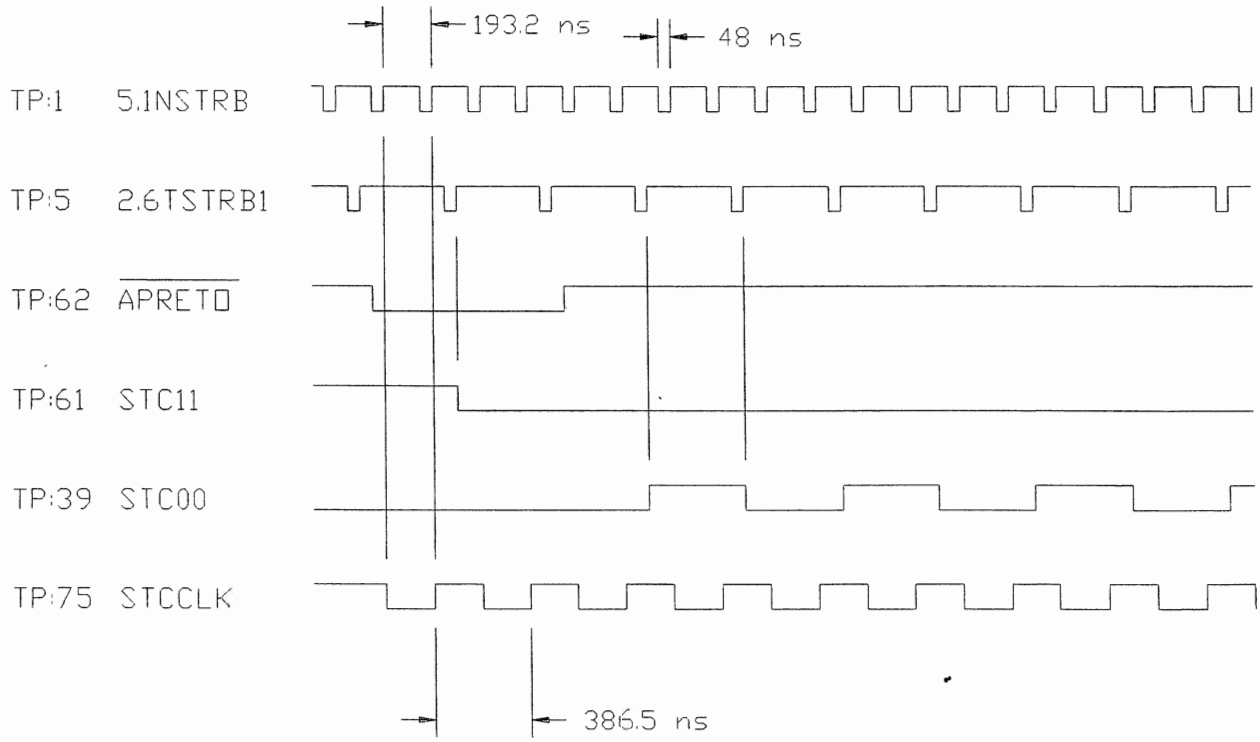


FIGURE 2-24c.

The counters will keep counting until STC11 goes active high. At this time, the signal "stacy" goes active low which freezes the count at 800 hex until the next –APRETO occurs. Therefore, the STC address counters count from 06E hex to 800 hex.

The total time for this count (the time to output the STC curve) can be calculated. The number of increments is 800 hex – 06E hex or 1939 (decimal) increments. The 2.6TSTRB1 clock is 386.5 ns period. Therefore, the total time to output the curve is: 386.5 ns X 1937 = 748650 ns or 748.65 us. Notice the latches U16 and U17 on sheet 5. The STC data is latched here by the same clock (2.6TSTRB1) which increments the STC address counters. Therefore, the data will appear at the line drivers on sheet 6 exactly one clock period after its associated EEPROM address was formed.

Furthermore, the last address applied to the STC EEPROMS is 800 hex and therefore the last EEPROM data to be driven off the card on sheet 6 comes from EEPROM address 800.

Notice on sheets 3 and 4 that address A12 of U50 and is no longer grounded. Since address A11 is only driven once (address 800 hex), then it follows that an entire ¾ of the EEPROM is wasted.

1FFF hex - 800 hex = 17FF hex locations wasted. Actually, this EEPROM space was recaptured to satisfy the EEPROM checksum BIT test because the HI beam EEPROM U51 was removed. *

* Refer to page 7 of the prints. STCCLK is generated from U106 to sheet 6 where it is driven off the card. STCCLK is a function of 5.1NSTRB. It is resynced with –APRETO.

Refer to figure 4 and sheet 2 of the prints. The waveforms were captured with an 8 us clock and therefore have an accuracy of +-8 us.

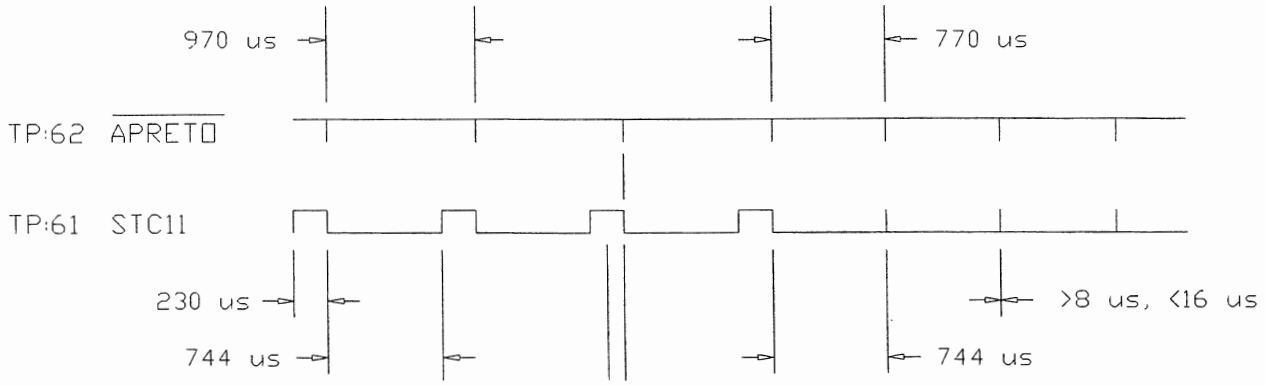


FIGURE 2-24d.

Notice that the time between –APRETO pulses varies between 970 us and 770 us approx. Specifically, the sequence alternates between 10 of the 970 us –APRETO pulses and 10 of the 770 us –APRETO pulses.

Since the time to output the STC curve data is approx. 744 us, then 970 us - 744 us = 230 us approx. for the dead time. It is during this time that the calibration sequences are output. Notice that for the 770 us –APRETO's, the dead time is only 8 us to 16 us approx. Therefore, no calibration occurs for these short dead times.

3) Calibration PROM sequencer readback and output.

Calibration PROM sequencer readback.

The monitoring and control processor has the capability (via the multibus) of reading the calibration EPROM data. Notice from sheets 9 and 14 that calibration EPROMs U53, U55 and U56 output their data to sheet 18. On sheet 18, the signals –CALPROM53, -CALPROM55, and –CALPROM56 choose which EPROM is read back. These signals originate on sheet 8 at U2 from a decode of a previous multibus write. On sheet 18, the multibus address decode –ADDRDEC06 is qualified with –IOR to create the signal –CHECK. This signal is further qualified with –CALPROM53, -CALPROM55, and –CALPROM56 to transfer the respective EPROM data to the multibus. This is how the data is read back to the processor.

Calibration PROM sequencer output.

Refer to the next diagram. These waveforms were captured with an 8 us clock and therefore have an accuracy of +-8 us. *

*

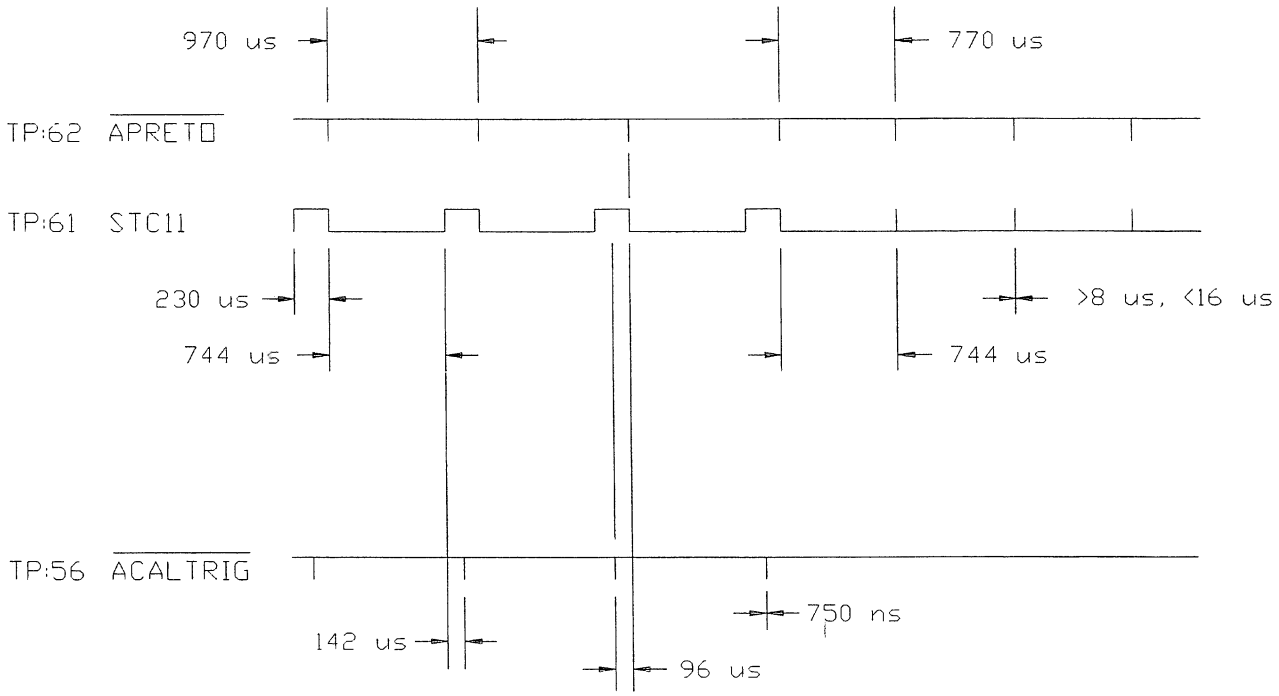


FIGURE 2-24e.

-ACALTRIG is the calibration "start" signal which is received onto the STC card on sheet 15. It is driven to sheet 8 to start the calibration EPROM address counters.

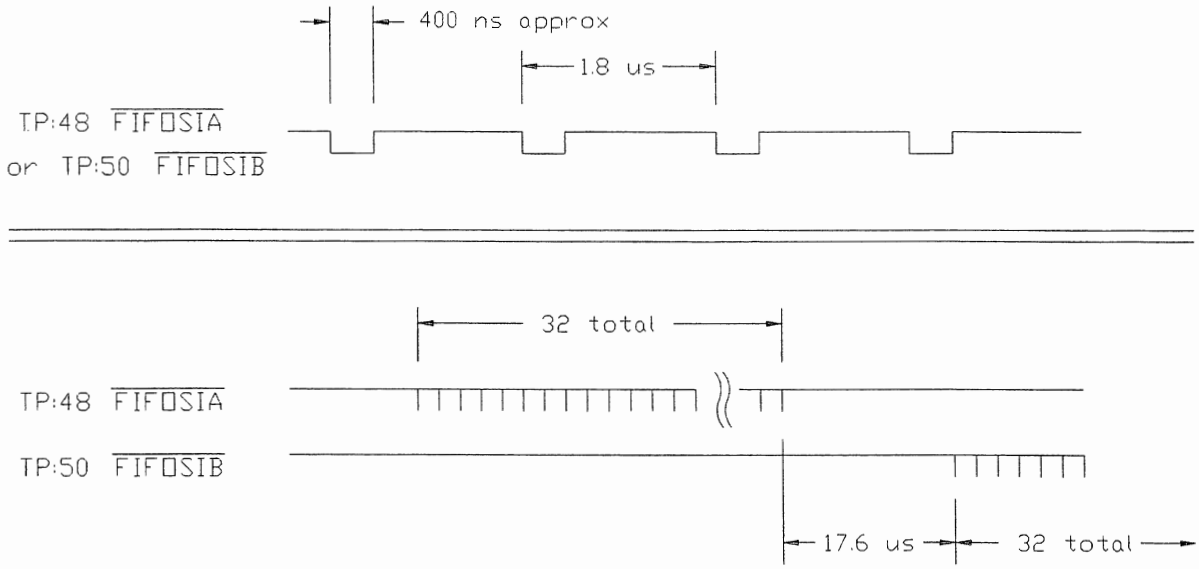
Notice that the signal -ACALTRIG only occurs for the 970 us period -APRETO signals. There are no –ACALTRIG signals. As previously stated, the calibration sequence only occurs for long period -APRETO signals.

On sheet 8, notice that the -ACALTRIG signal loads the calibration EPROM address counters U60, U61 and U62 with the value previously loaded into U4 and U116 latches. This value was previously loaded into the latches via the monitoring and control processor multibus interface on sheet 16 and 17 of the prints. Specifically, the multibus address decode is qualified with -IOW at U34B to create the signal CALIOW01. CALIOW01 loads the latches.

This calibration EPROM address value represents the starting address of the calibration test which the control processor is executing.

4) FIFO input and output.

Refer to figure 2-24f (below) and sheet 11 of the STC card prints. U79 and U88 are 64 X 4 bit FIFOS. These are loaded by the monitoring and control processor via a port write to the multibus. Notice that U36:A and U36:B qualify the multibus address decode with -IOW. The signals -FIFOSIA and -FIFOSIB are thus generated. There are 32 total -FIFOSIA pulses followed by 32 total -FIFOSIB pulses. The FIFOs are loaded by the monitoring and control processor during the active radar time (as opposed to the dead time during which the FIFOs data are shifted out). Notice that the FIFOs input is connected directly to the buffered multibus databus. *



*

FIGURE 2-24f.

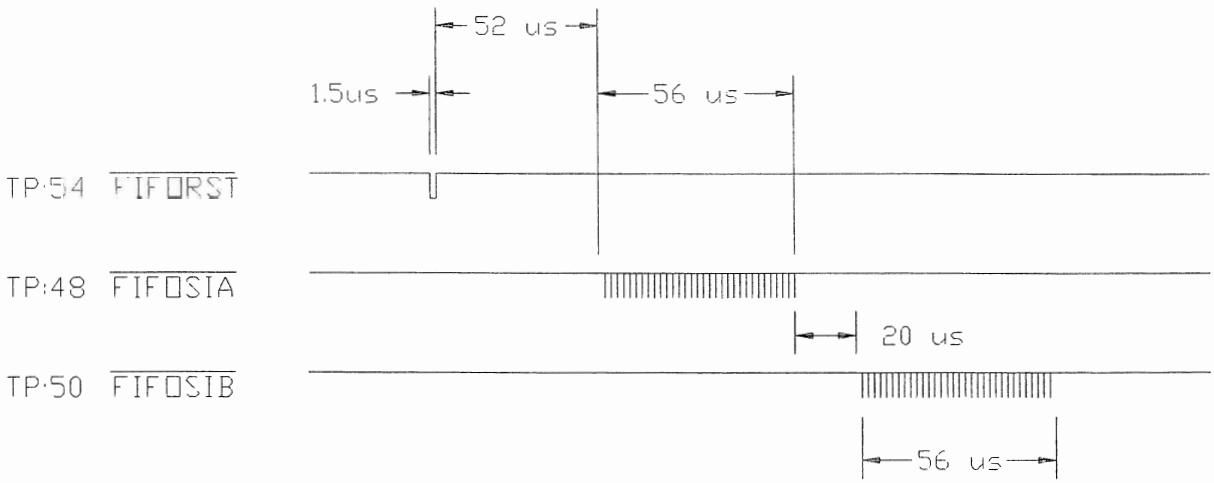


FIGURE 2-24g.

The -FIFORST pulse is generated from a multibus decode qualified with -IOW. This happens on sheet 14 of the prints. -FIFORST is also a function of -MR3 and 1.3TSTRB (see sheet 14).

Figures 2-24f and 2-24g clearly show that the FIFOs are first reset and then loaded 32 times each. They are therefore ½ full for the calibration test which uses them. *

* Next, refer to figure 2-24h.

FIFOSO and FOFOCLK both originate from the calibration EPROMs on sheet 9 of the prints. The calibration EPROMs act as PROM sequencers. Part of this calibration sequence is output control of the FIFOs.

Notice that this shifting out occurs during "dead time". First the -ACALTRIG loads the calibration EPROM address counter with the address of the calibration test to be performed. Next, the calibration EPROMs output the signals FIFOCLK and FIFOSO as part of a calibration sequence. Four FIFOCLK pulses and four FIFOSO pulses output data from the FIFO to U114 and U58 latches (see sheet 11). The rising edge of FIFOCLK will occur first so that the latches are loaded prior to the FIFO being shifted out.

STC11 then goes low (see sheet 2) signifying the start of another radar trigger (the end of dead time). The FIFOs output 4 times and they input 32 times.

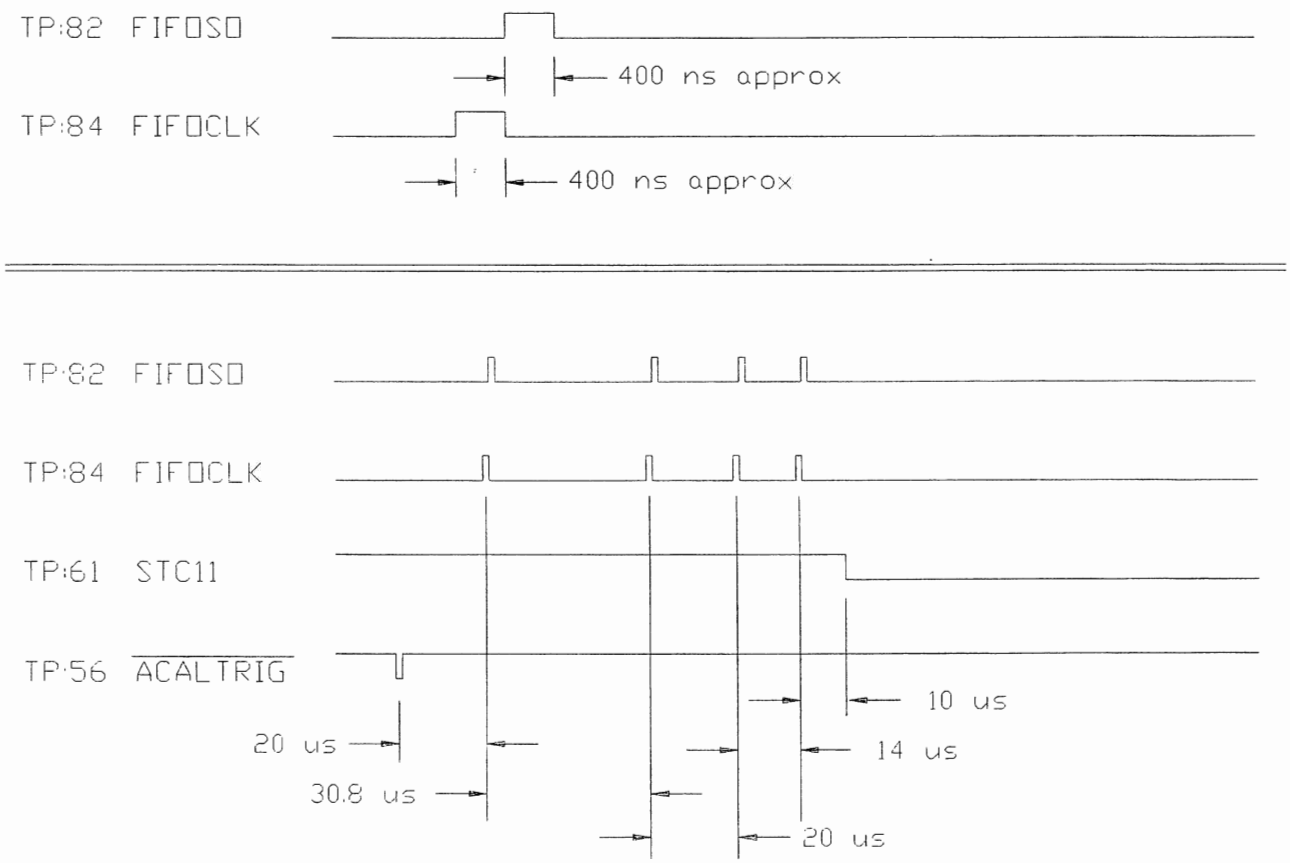


FIGURE 2-24h. *

* Refer to figure 2-24i and sheets 5 and 7 of the prints.

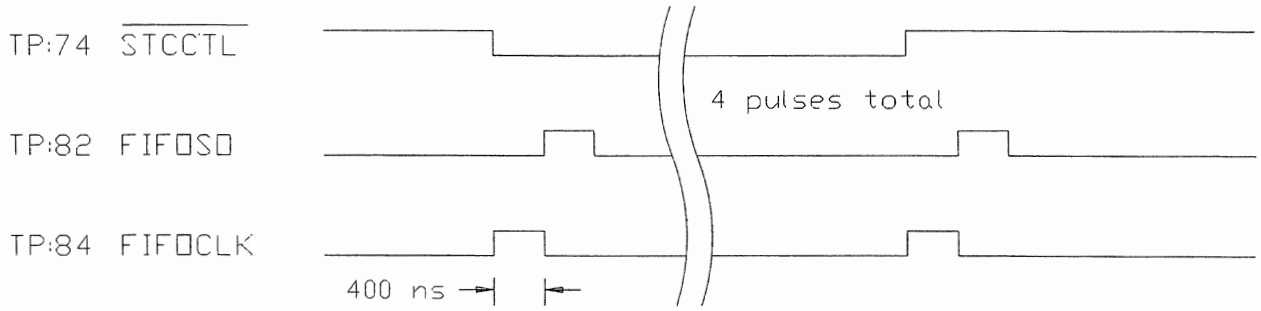


FIGURE 2-24i.

The FIFOs output 4 times. This data is STC calibration data. Notice that the signal -STCCTL becomes -STCCALCTL on sheet 7 of the prints and then is driven to sheet 5 to steer the muxers U18, U19, U111 and U20. Under the control of -STCCALCTL, the muxers choose calibration data from the FIFOs. As can be seen in figure 2-24i, this signal is active for the four FIFOCLK pulses. Therefore, the 4 FIFO outputs are STC calibration data.

5) RAM input and output.

RAM input and output:

RAM Input.

Refer to figure 2-24j and sheet 12 of the prints.

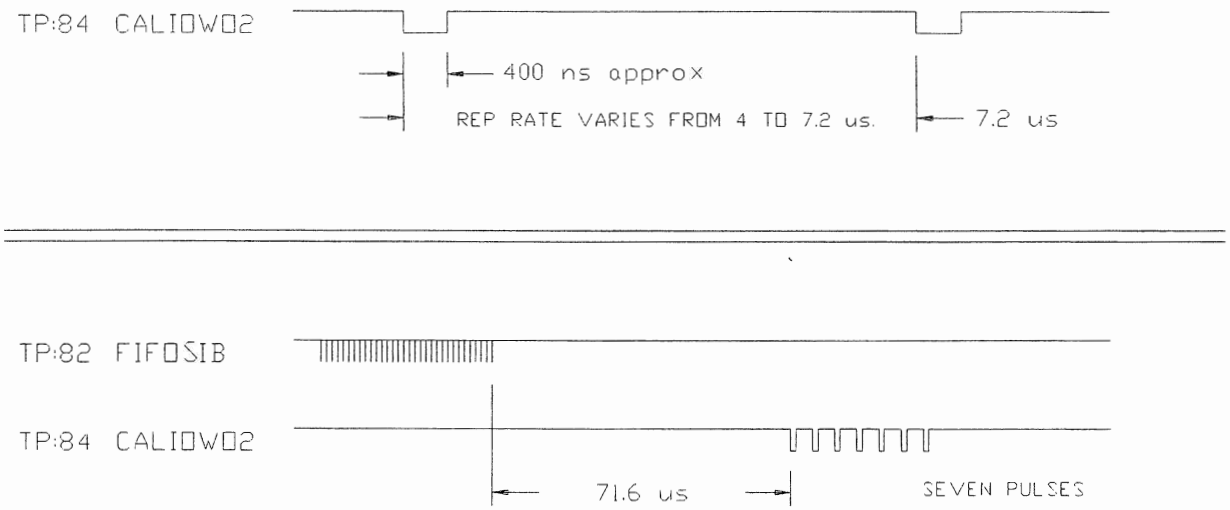


FIGURE 2-24j. *

* The 16 X 4 RAMs are U87, U98 and U99 on sheet 12. The RAM output address counter is U89. The RAM input address comes from the multibus.

CALIOW02 is a signal which loads the RAMs at the address originating from the monitoring and control processor multibus. The input data also originates from the multibus. CALIOW02 is derived from a multibus address decode qualified with -IOW at U36:C. Notice from figure 2-24j that there are seven (7) CALIOW02 pulses which load the RAM 7 times. This sequence occurs right after the FIFOs are loaded. It is unclear why there are 7 RAM load pulses when only 6 locations are used. The 6 are: 1001, AGC; 1010, I channel dc bias; 1011, Q channel dc bias; 1100, I/Q channel phase balance; 1101, I/Q channel gain balance; and 1110, A/D converter test. The RAM is loaded during active sweep time (as opposed to the dead time when it is output).

RAM Output:

Refer to figure 2-24k and sheet 12 of the prints.

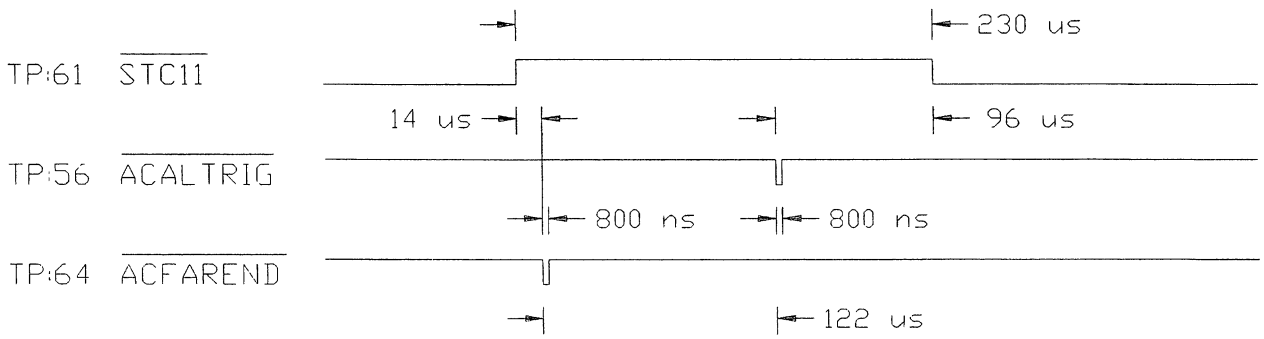


FIGURE 2-24k.

The signal -STC11 is active high during "dead" time. -ACFAREND is a pulse which signifies the absolute range limit of the radar. It is driven onto the card on sheet 15.

Approximately 14 us after -STC11 goes high (end of STC curve), the signal -ACFAREND (end of radar active time) goes active. Approximately 122 us after -ACFAREND goes high, -ACALTRIG occurs. As previously seen, this pulse starts the calibration sequence by initializing the EPROM address counter.

Reference figure 2-24l and sheet 12 of the prints. *

*

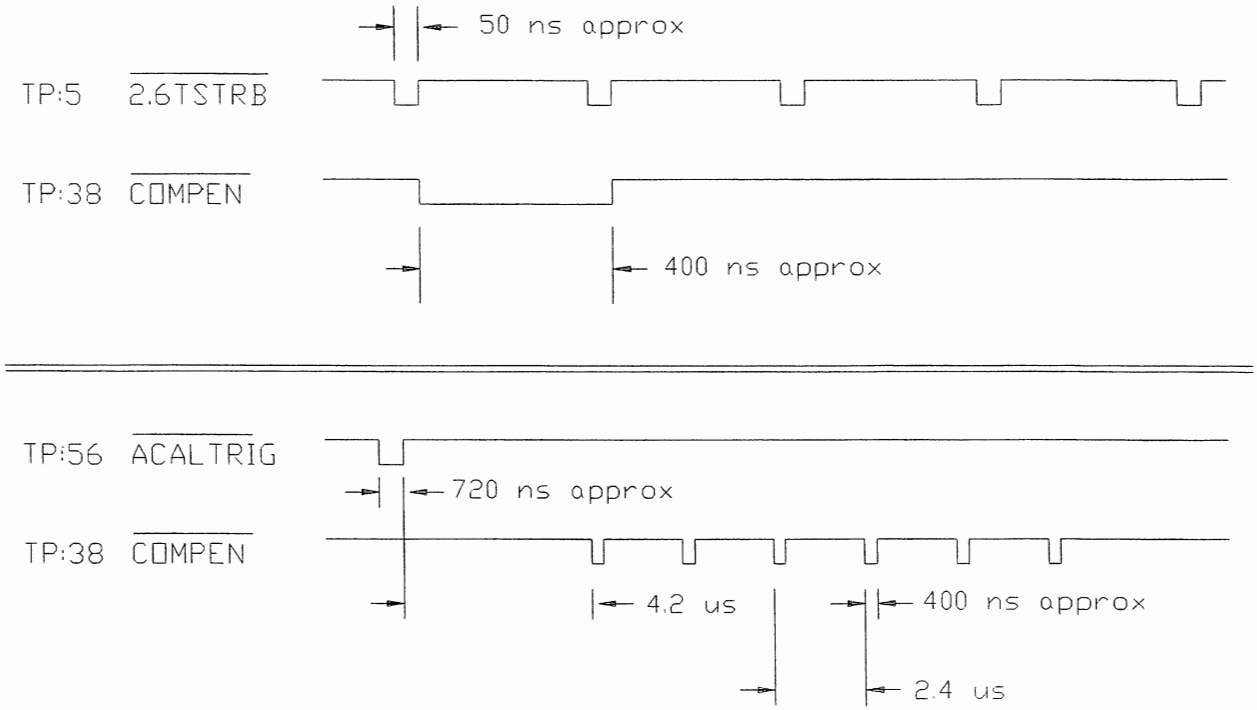


FIGURE 2-24I.

The RAM output address counter is U89. It is initialized by the signal –ACFAREND originating on sheet 15 of the prints. The loaded value is hardwired to 1001 or 9 hex. The counter is updated with two signals:

-COMPEN which originates from the calibration PROM sequencer on sheet 9, and the signal –2.6TSTRB which counts U89 when –COMPEN is active. Notice that a –2.6TSTRB will always occur for each –COMPEN signal. This is because the –2.6TSTRB signal is used to increment the calibration EPROM sequencer address (which in turn creates –COMPEN). This may be clearly seen from the top diagram in figure 2-24I. The bottom diagram clearly shows –ACALTRIG (which starts the calibration EPROM sequence) followed by six (6) –COMPEN signals originating from the calibration EPROM sequencer. Notice on sheet 12 that the signal CALUPCLK (also originating from the EPROM sequencer) will latch the RAM data into U108 and U120. From there, the data is driven off the board. 6 CALUPCLK pulses (not shown) are required to latch these data.

Notice that U89 will count 6 times from address 9 hex to address F hex. Then the –RCO output will stop the count until another –ACFAREND occurs.

Although the address counts from 9 hex to F hex, the data values used come from address 9 hex to E hex. *

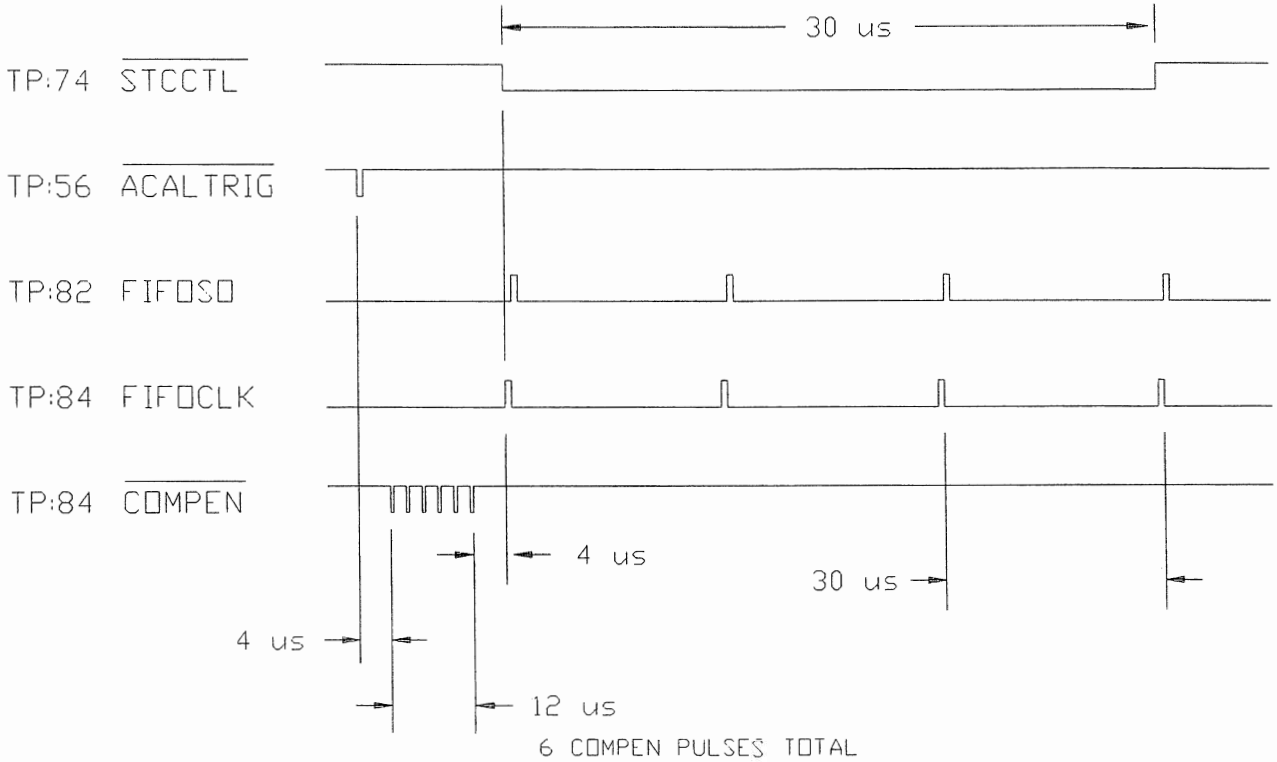


FIGURE 2-24m.

This diagram shows the relationship between the PROM sequencer, the FIFOs, and the RAM. First, the signal –ACALTRIG loads the EPROM sequencer address counter with the start address of the test to be executed. Next, the EPROM address counter will increment with 2.6TSTRBs and create 6 -COMPEN pulses to output 6 RAM locations. Next, the monitoring and control processor will set the signal –STCCTL to signify and STC calibration. The EPROM sequencer then outputs 4 FIFOCLK and 4 FIFOSO pulses. This FIFO data eventually becomes CALSTC0X to the STC output multiplexers on sheet 5.

6) Multibus I/O

The monitoring and control processor transfers data to and from resources (such as the STC card) via the multibus. The multibus controller used (on the processor card) is the Intel 8288. The clock which is applied to the 8288 is the 10.35 MHz clock / 2 (or 5.175 MHz) and therefore the clock period is 193.2 ns. The multibus control, address, and data signals used on the STC card are:

1) -AIOWC
2) -IOWC
3) -IORC
4) -ADR01 thru -ADR15
5) -DAT00 thru -DAT15 *

* Refer to figures 2-24n and 2-24o and sheets 16 and 17 of the prints.

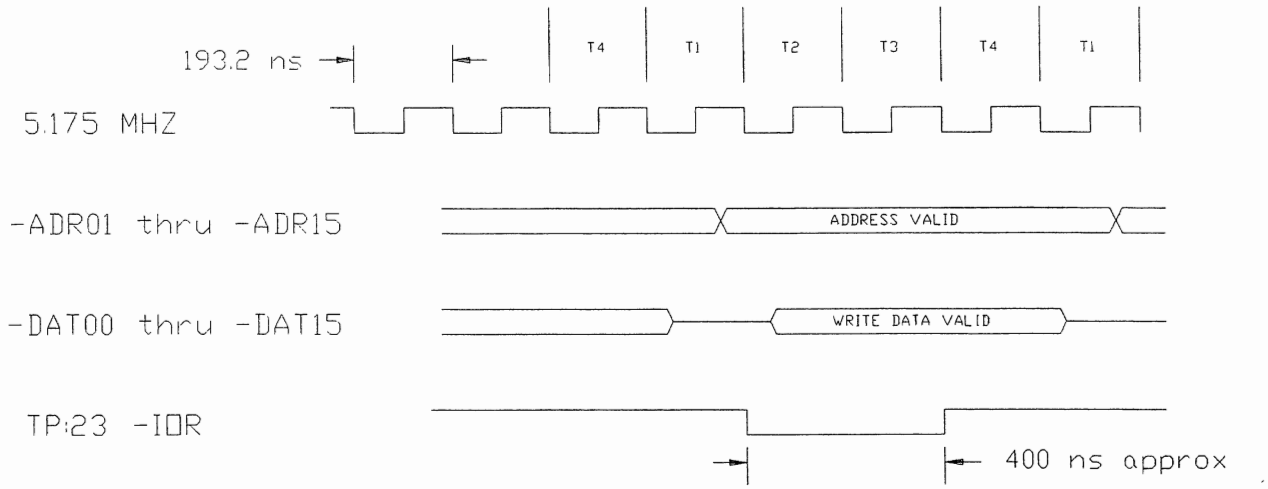


FIGURE 2-24n.

Sheet 16 has all the receivers for the multibus signals. Sheet 17 decodes the multibus addresses. These decodes are later qualified with -IORC, -AIOWC, and -IOWC to write and read the EEPROM, to read the EPROM, and write to the EEPROM, FIFOs and RAM.

Figures 2-24n and 2-24o were derived from the Intel Data Book "Microprocessor and Peripheral Handbook, Volume 1 – Microprocessor" assuming a 5.175 MHz clock. The signals –IOR, -IOW, and –AIOW were also measured with a logic analyzer.

Figure 2-24n shows a typical multibus. I/O output read cycle. The I/O read cycle would be used for multibus reads of the EPROM and EEPROM data. These reads would occur as part of a data verification sequence by the monitoring and control processor.

Figure 2-24o shows a typical multibus I/O write cycle. The I/O write cycle would be used for multibus writes to the EEPROM, FIFOs, and RAMs. The signal –AIOWC (advanced I/O write), is used only for EEPROM writes. Figure 2-24o needed two T3 states (1 wait state) to match the logic analyzer measurements. *

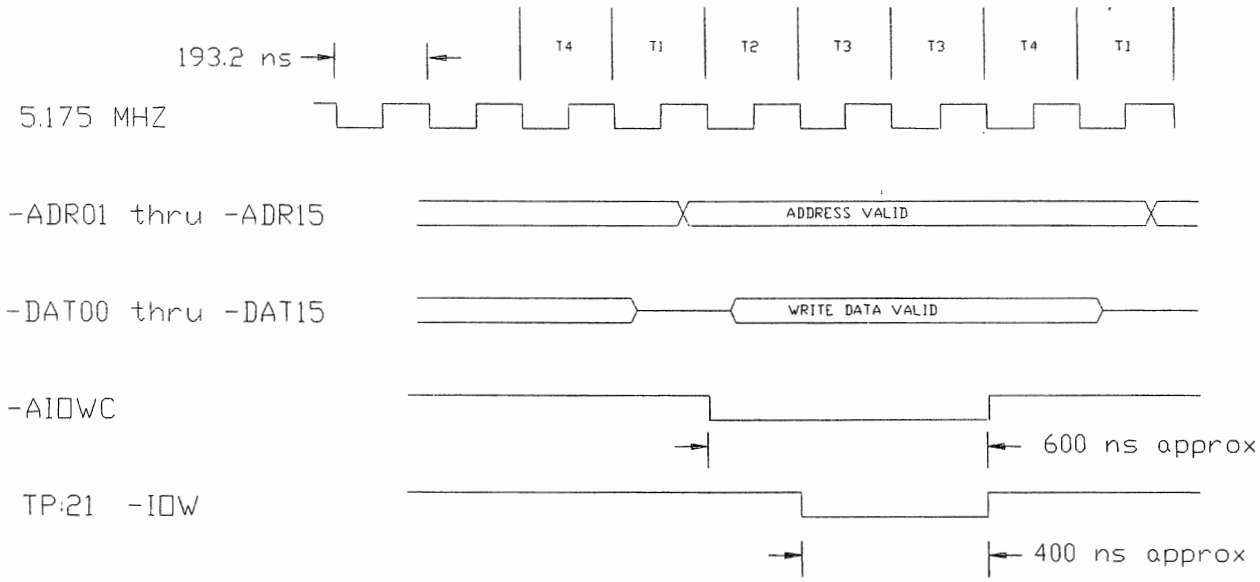


FIGURE 2-24o.

2.3.1.1.3.11 Receiver Calibration and Testing. See figure 11-8, sheet 11. The RAG calibration trigger RGCALTRIG- initiates receiver calibration and testing. Receiver calibration and testing functions on STC/calibration generator A4A123 are centered around three memory circuits, each programmed by the monitoring and control processor. The memory circuits are summarized below:

1. The receiver calibration data RAM — programmed with rf/i–f receiver servo algorithms for five servo loops: I channel dc bias, Q channel dc bias, agc, I/Q channel phase balance, and I/Q channel gain balance. The data is used to calibrate receiver servo loops once during each cpip. The RAM is also programmed with data for an a/d converter test that is run after the servo loop calibrations. *

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2. The FIFO memory — programmed with stc test attenuation data that is used during dead time rf/i–f receiver performance tests, when rf test target signals are provided to the weather channel from the online target channel frequency generator.

3. The calibration EPROM — programmed with the timing sequence for the receiver servo calibration updates, a/d converter test, and stc attenuation data flow.

2.3.1.1.3.11.1 Receiver Calibration Data RAM. See figure 11-8, sheet 11. The monitoring and control processor programs the receiver calibration data RAM with rf/i–f receiver calibration update data. The calibration update data consists of the following rf/i–f receiver servo values: I channel dc bias, Q channel dc bias, agc, I/Q channel phase balance, and I/Q channel gain balance. The desired state for each servo is updated and sent to the rf/i–f receiver as RCVRCA00 through RCVRCA11. The receiver decodes the digital update code (from CALTEST00 through CALTEST04) and sets the analog circuitry to the requested parameter value in RCVRCA00 through RCVRCA11. The monitoring and control processor collects, processes, and sends the calibration update data to the receiver calibration data RAM during batch time, in the 48 batch units that precede weather data processing at the beginning of the cpip absolute batch interval. (The absolute batch interval is described in paragraph 2.3.1.1.3.4.2.) The calibration update data is collected and processed by the monitoring and control processor from calibration tests run during rf/i–f receiver dead time. The rf/i–f receiver calibration occurs during the dead time that precedes range cell weather returns (live time) in prts 9 through 17, and is initiated by the RAG generator calibration trigger CALTRIG-. Figure 2-25 depicts a real time cpip. The figure shows the distribution of receiver live and dead times, and the occurrences of the calibration trigger CALTRIG- for prf pair set no. 0. (Refer to paragraph 2.3.1.1.3.3 for a discussion of prf pair set timing.)

2.3.1.1.3.11.1.1 Receiver Calibration Data RAM Programming. See figure 11-8, sheet 11. The monitoring and control processor programs rf/i–f receiver calibration data into the RAM from the multibus data lines DAT00- through DAT15-. The multibus interface places the data on the board data bus and the board data bus transfers it to the RAM as DB00 through DB15. The active high read/write enable CALIOW02 allows the RAM to accept data. Read/write enable CALIOW02 is high when the monitoring and control processor is writing to the RAM (AIOW- and IOW- active low) and the STCCAL3EN- signal is low. STCCAL3EN- is derived from monitoring and control processor address data, decoded in the multibus interface. Refer to paragraph 2.3.1.1.2 for a general discussion of the board multibus interfaces and the address decode process.

2.3.1.1.3.11.2.2 Calibration Test FIFO Output. See figure 11-8, sheet 11. During a calibration test, test control signal FIFOS0 shifts the test data from the FIFO, and FIFOCLK and CALUPCLK clock the data into the data latch line drivers. The calibration EPROM (described in paragraph 2.3.1.1.3.11.3) outputs the FIFOS0, FIFOCLK, and CALUPCLK signals when required for a specific calibration test. The data latch line drivers output stc attenuation data word CALSTC00 through CALSTC05. The stc attenuation test data (CALST00) is programmable from 000000 (minimum attenuation or 0dB) to 111111 (maximum attenuation or 63 dB). The data word is structured as follows:

Bit 00 = 1 dB	Bit 03 = 8 dB
Bit 01 = 2 dB	Bit 04 = 16 dB
Bit 02 = 4 dB	Bit 05 = 32 dB

The active low SGCALCTRL- signal selects data word CALST00 through CALST05 as the stc register/multiplexer output during the stc tests. (The calibration EPROM, described in the following paragraph, generates the SGCALCTRL- signal.) Data word CALSTC00 through CALSTC05 passes
* from the stc register/multiplexer to data word lines LDATA00B through LDATA05. (WSP Feature) Next the LDATA0XX data is muxed with WSP-LDATAXX from the WSP RIM, so the WSP can control the STC curve when it is online. Furthermore, the mux only selects the WSP-LDATAXX data during live time and reverts back to the ASR9 LDATAXX during CALIBRATION time so the Bit testing will not be affected. LOSTCCLK clocks the data word through line driver no. 1 to the stc * attenuator in the rf/i–f receiver.

2.3.1.1.3.11.3 Calibration EPROM. The calibration EPROM is preprogrammed with control signals for the servo calibration updates, mds or stc tests, the a/d converter test, and a "non–test" that sets the receiver controller to a known state at the end of the sequence.

2.3.1.1.3.11.3.1 Calibration EPROM Addressing. See figure 11-8, sheet 11. The monitoring and control processor selects the required EPROM sequence by addressing the EPROM. The monitoring and control processor supplies an address word to the test select data registers, via board data bus bits DB00 through DB07. Address ADDRDEC06- (low) and enable signal IOW- (high) from the multibus interface, allow the test select data registers to output address word DB00 through DB07 to the PROM address counter, as address data word CALDAT00 through CALDAT07. The RAG generator RGCALTRIG- trigger loads the PROM address counter to a start count provided by CALDAT00 through CALDAT07. The counter increments with each 2.6TSTRB2 clock. The counter output, CALADDR00 through CALADDR12, is enabled by a high level STOPSEQ signal from the calibration EPROM. The STOPSEQ signal goes low when the sequence ends, disabling the counter and ending the address generation.

2.3.1.1.3.11.3.2 Calibration EPROM Outputs. See figure 11-8, sheet 11. The control signal sequence from the calibration EPROM initiates receiver calibration time events, including the servo calibration updates, mds test, stc test, a/d converter test, and non–test. The calibration updates and a/d converter events scheduled by the monitoring and control processor results in the calibration EPROM outputs listed in table 2-13. The CALTEST00 through CALTEST04 signals identify the event to the rf/i–f receiver. After all events in the sequence have occurred, the calibration EPROM ends the sequence with a low level STOPSEQ signal that halts the EPROM address counter. The EPROM signals not required during a calibration–time event are normally high.

TABLE 2-13. ACTIVE SIGNALS IN CALIBRATION–TIME EVENTS

Event	Action
A/d Converter Test	High CALUPCLK clocks CALSTC00-05 (60 dB) through data latch. A/DTESTEN- low to rf/i–f receiver. SGHI/LO-CA high, sets BEAMONLOI high through system timing unit A. SGCALCTRL- low, places CALSTC00 through CALSTC05 on LOSTC00 lines. SGSMPLWDW- goes low and remains low for 27 1.3-MHz clock periods to allow filter and magnitude processor to sample test data.
Servo Updates	COMPEN- low, enables receiver calibration RAM address counter. CALUPCLK high clocks calibration RAM data RCDATA00 through RCDATA11 into data latch/line drivers. CALCLK low, latches calibration data into rf/i–f receiver. Action repeats 6 times until data is sent for each of the servo updates (agc, I channel dc bias, Q channel dc bias, I/Q channel phase balance, and I/Q channel gain balance).

2.3.1.1.3.15.5.4 BIT/FIT Logic Analyzer Control Words. See figure 11-8, sheets 2 and 3. The monitoring and control processor sends 24 bits of control data in two control words multiplexed on the multibus data lines DAT00- through DAT15-. The multibus interface (sheet 2) transfers the control words to the board data bus as DB00 through DB15. The write enable IOW- (buffered monitoring and control processor write command IOWC-) and the decoded address bits ADDRDEC01– and ADDRDEC02- transfer the control words from the board data bus to the BIT control word registers (sheet 3). The BIT control word registers output the control data as CONTROL00 through CONTROL23. (Refer to paragraph 2.3.1.1.2 for a general discussion of board multibus interfaces and the address decode process.) The bit allocation of the two control words is shown in figure 2-27. Each pair of control data words contains the information for one test.

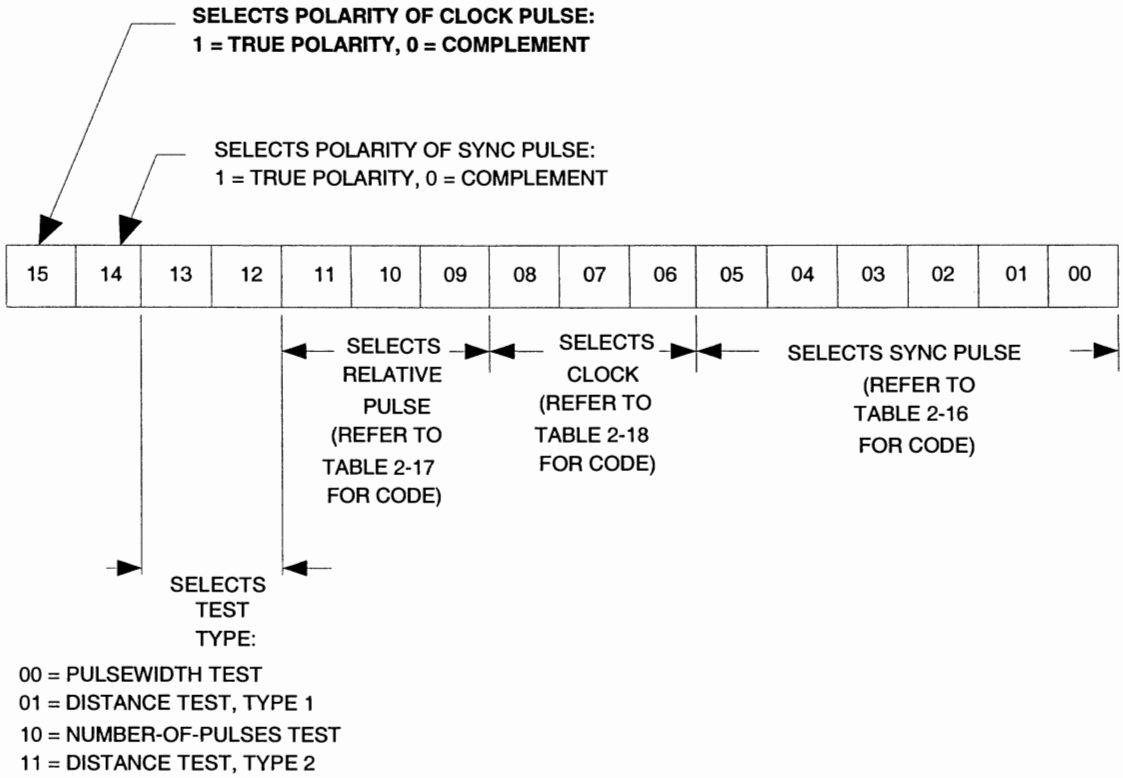
2.3.1.1.3.15.5.5 Test Execution, Stage 0ne. The selection and processing of the required sync and relative pulses (as defined by the test type described in paragraph 2.3.1.1.3.15.5.2) occurs during stage one of the test execution.

2.3.1.1.3.15.5.5.1 Sync Pulse and Polarity Selection. See figures 2-27 and 11-8, sheet 3. Sits 00 through 05 and bit 14 of monitoring and control processor control word 1 are placed on the CONTROL00 through CONTROL05 and CONTROL14 lines and applied to the sync pulse select/parity control circuit. The CONTROL00 through CONTROL05 signals select one of the sync pulse inputs as PULSERESYN. If the selected sync pulse is a logic low, the CONTROL14 line is low to reverse the polarity of the selected pulse. This is necessary because the BIT/FIT logic analyzer operates only with positive logic. The high level PULSERESYN signal is applied to the test select and control logic (paragraph 2.3.1.1.3.15.5.4.3) and to the clock select/polarity control (paragraph 2.3.1.1.3.15.5.6.1).

* **2.3.1.1.3.15.5.5.2 Relative Pulse and Polarity Selection.** See figure 11-8, sheet 3. Bits 09 through 11 and bit 16 of monitoring and control processor control word 1 are placed on the CONTROL09 through CONTROL11 and CONTROL16 lines and applied to the relative pulse select/polarity control circuit. The CONTROL09 through CONTROL11 signals select one of the relative pulse inputs as RELPUL. If the selected relative pulse is a logic low, the CONTROL16 line is low to reverse the polarity of the selected pulse. This is necessary because the BIT/FIT logic analyzer operates only with positive logic. The high level RELPUL signal is applied to the test select and control logic. *

2.3.1.1.3.15.5.5.3 Test Select and Control Logic. See figure 11-8, sheet 3. Test select bits 12 and 13 of monitoring and control processor control word 1 are placed on the CONTROL12 and CONTROL13 lines and applied to the test select and control logic. The test select and control logic decodes the test select bits, to determine which PULSERESYN or RELPUL pulse conditions to check. The pulse types that are checked are described in paragraph 2.3.1.1.3.15.5.3. The test select and control logic then performs one of four logic functions, which results in one of four interim test result signals, PULSEWDTH-, DISTBPLSE-, DISTB2IP-, or NOOFPULSE-, as shown in figure 2-28. A low level on any one of the four interim test result signals causes a high level CLKCNT signal to output the test select and control logic. This signal controls the second stage of the test execution, when the interim test result signal that resulted from the logic function performed on PULSERESYN and/or RELPUL is measured relative to a selected clock signal. (The second stage is described in paragraph 2.3.1.1.3.15.5.6.) Timing and control of the test select and control logic is provided by the STARTRST- and RUNTST- signals from the start test and timeout circuits, and the DONET0 signal from the test control logic. STARTRST- and RUNTST- are described in paragraph 2.3.1.1.3.15.5.7, and DONET0 is described in paragraph 2.3.1.1.3.15.5.8.

CONTROL WORD 1



CONTROL WORD 2

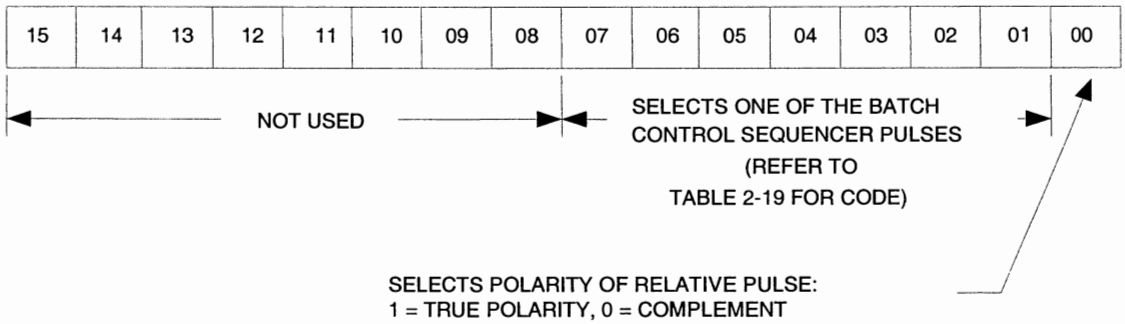


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FIGURE 2-27. CONTROL WORD FORMAT

monitoring and control processor address bit ADDRDEC03- are logic ORed to generate a timeout clock. This timeout clock is gated by the 0.65TST clock to form the active low STARTRST- signal. At the start of every test, the STARTRST- signal resets the start test and timeout circuits, the test select and control logic, and the clock counter/test result output port to prepare the circuits to receive new test data.

2.3.1.1.3.15.5.7.3 Run Test Signal (RUNTST-). See figure 11-8, sheet 3. The active low RUNTST- signal enables the test select and control logic to execute the first stage of the selected test. The RUNTST- signal is placed in the active low state by the STARTRST- signal at the start of a new test. It remains low until the DONE signal from the test control logic goes high. The DONE signal goes high when one of the interim test result signals PULSEWDTH-, DISTSPLSE-, DIST2IP-, or NOOFPULSE- is low.

2.3.1.1.3.15.5.8 Interrupt RUINT04- Generation. See figure 11-8, sheets 2 and 3. The interrupt request RUINT04- is sent to the monitoring and control processor when the DONETO signal is active high. The test control logic (sheet 3) sets DONETO high when DONE is high (one of the interim test result signals PULSEWDTH-, DISTSPLSE-, DIST2IP-, or NOOFPULSE- is low), or when the timeout signal TO goes high to indicate that the time interval allowed for a test has elapsed. After the monitoring and control processor receives the interrupt request, it resets the interrupt request/reset circuit by sending the read command IOR- and the address bit ADDRDEC03-. The multibus interface (sheet 2) transfers the buffered IORC- write command (IOR-) and decodes the ADDRDEC03- signal. (Refer to paragraph 2.3.1.1.2 for a general discussion of board multibus interfaces and the address decode process.) The monitoring and control processor responds to interrupt RUINT04- by reading the status register (sheet 3).

2.3.1.1.3.15.5.9 Status Register. See figure 11-8, sheet 3. When the monitoring and control processor receives the active low interrupt RUINT04-, it reads the status of the status register to determine if:

1. The test was completed (TESTCOMPLT high)
2. A timeout has occurred (TIMEOUT high), or
3. The test was never initiated (TIMEOUTEN high).

The TESTCOMPLT signal is generated by the test control logic when the test select and control logic tests are completed (DONE is high). The TIMEOUT signal is high (same as TO) when the time interval for a test has elapsed. The TIMEOUTEN signal is high when the RUNTST- signal does not go high to initiate a test. The three status bits are placed on the board data bus and transferred through the multibus interface to the multibus lines DAT00- through DAT02-. After the monitoring and control processor reads the status register, it takes action depending on which status bits are set. If the test was completed, the monitoring and control processor reads the clock counter/test result output port. (Refer to paragraph 2.3.1.1.3.15.5.6.3.) The contents of the clock counter/test result output port will be meaningless if the status register indicated that the test was never initiated or that timeout occurred. In these cases, the monitoring and control processor analyzes the reasons for a test initiation failure or a timeout.

2.3.1.2 Rf/I–f Receiver. A hardware block diagram of the weather rf/i–f receiver function is shown in figure 2-29 and a signal flow diagram is shown in figure 11-13. The hardware block diagram provides a quick reference overview of the assemblies and major components that make up the rf/i–f receiver function. The signal flow diagram shows the details of signal development and flow and provides
* assembly interconnection details. Low altitude windshear and microburst detection require the use of the low beam. When the low beam is employed over the airport, the ground clutter exceeds the dynamic range of the ASR9 if receiver. The WSP if receiver dynamic range exceeds 80 db so that the WSP if-receiver is able to pass the if signal without distortion to the WSP VME processor. The WSP function taps the ASR9 signal for the input to the WSP if receiver 4A12, located in the back of the cabinet. *

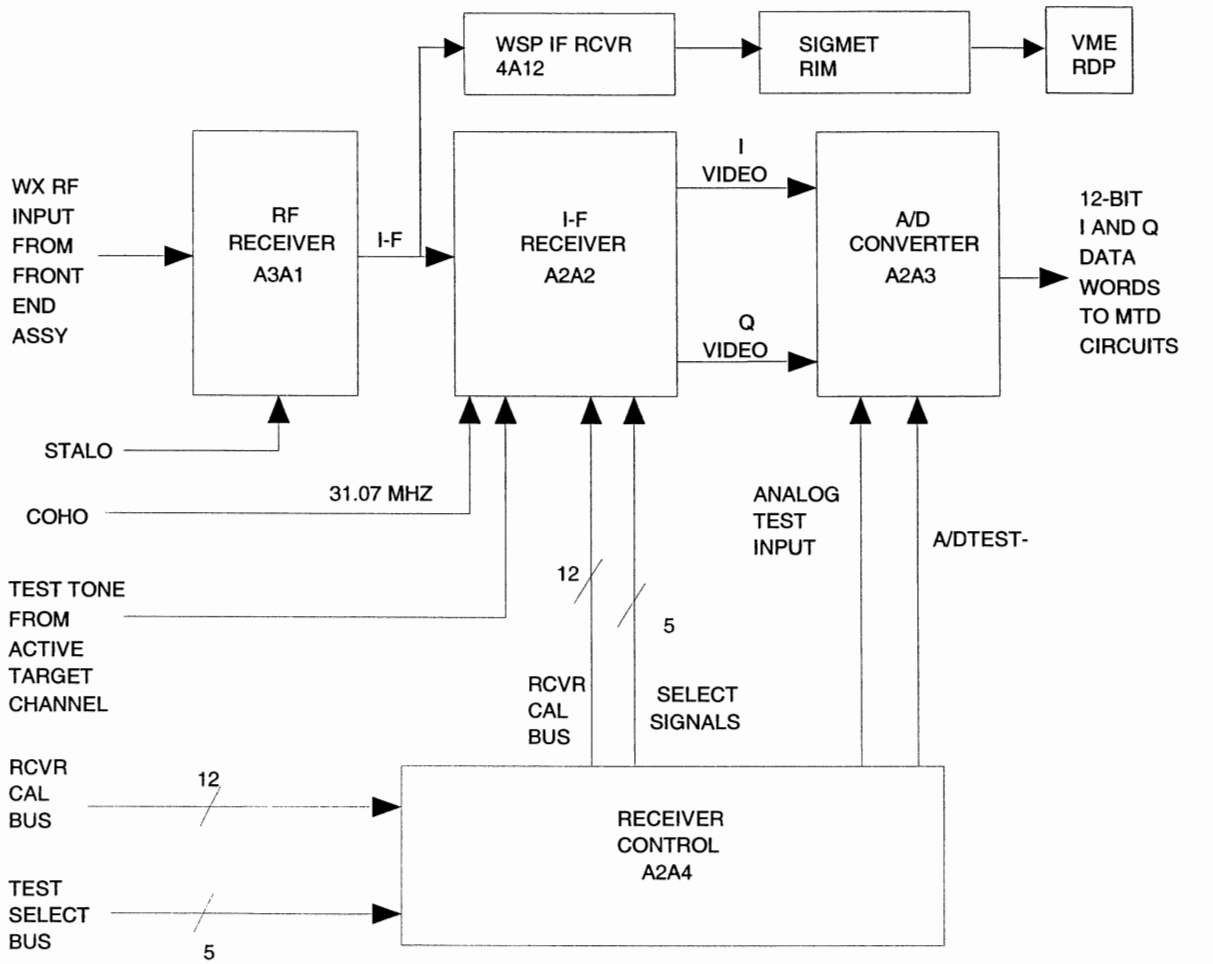

FIGURE 2-29. RF/I–F RECEIVER FUNCTION HARDWARE BLOCK DIAGRAM

2.3.1.2.1 Introduction. Refer to the hardware block diagram, figure 2-29. The rf/i–f receiver function, which is composed of weather receiver assembly A2 and weather i–f panel assembly A1, receives the weather channel rf signal and converts it to an i–f signal. I–f receiver A2A2 converts the i–f signal into two video signals: one representing the in–phase (I) component, and one representing the quadrature phase (Q) component of the incoming signal. The video signals are then converted into 12–bit digital words in a/d converter A2A3. The digital I and Q outputs are time–division multiplexed onto a data bus and supplied to the filtering and magnitude detection circuits for digital processing. The rf/i–f receiver function receives calibration data from the synchronizer via receiver control A1A4 that provide for gain and calibration adjustments of the receiver. (WSP Features) The WSP taps unused output J5 on the
* Receiver Mixer module 4A3A1 for the I-f radar return signal.

2.3.1.2.1.1 Rf to Digital Conversion. See figure 11-13, sheet 2. The weather channel rf/i–f receiver * function receives a 2.7- to 2.9-GHz weather rf signal from the radar antenna through the tuneable bandpass filter of the front–end assembly. The weather rf signal is applied to rf receiver A3AI where it is combined with the 2.668- to 2.868-GHz stalo local oscillator (STALO) signal from the frequency generator to produce a 31.07-MHz i–f signal. The 31.07-MHz output is amplified, filtered and synchronously detected to provide the I and Q video. The I and Q video is then converted into 12–bit digital words that are time–division multiplexed onto an I and Q data bus and applied to the filtering and magnitude detection circuits for processing.

2.3.1.2.1.2 Receiver Control and Test Tone Generation. Receiver calibration data is sent to the rf/i–f receiver function from the synchronizer circuits. The data is provided to receiver control A2A4 via two buses: the receiver calibration bus (RCVR CAL SUS) and test select bus (TEST SELECT SUS). The 12–bit–wide receiver calibration data words are time–division multiplexed onto the receiver calibration bus, and timing signals are provided on the 5–bit–wide test select bus for decoding the data from the receiver calibration bus. The specific calibration signals are automatic gain control (agc), I and Q amplitude and phase balance, I and Q dc offset (used in i–f receiver A2A2), and a test tone signal
* control. Because the WSP if receiver employs an A/D converter that samples at 35.9751 MHz, then a digital filter synthesizes the I and Q data, the requirement for the ASR9 style calibration servo loops (discussed next) is not required in the WSP architecture. The Sigmet RVP-7 manual delivered as part of the COTs equipment, discusses this technique for extracting the I and Q data. *

2.3.1.2.2 Detailed Discussion. See figure 11-13, sheet 1. The primary signal flow within the rf/i–f receiver function includes rf to i–f, i–f to I and Q video, and video to digital conversions. Following the primary signal flow, a detailed description of the receiver calibration and fault monitoring functions is provided in the following paragraphs.

2.3.1.2.2.1 Rf to I–f Conversion. See figure 11-13, sheet 1. Rf receiver A3A1 performs rf to i–f conversion. A 2.7- to 2.9-GHz weather rf signal (WXRF) from the front–end assembly low noise amplifier is coupled through an isolator to the rf amplifier. The isolator provides an rf signal input matching for the rf amplifier that has a noise figure of less than 6 db. The rf amplifier boosts the WXRF signal which is applied to the 90 degrees rf hybrid. The rf hybrid sends a 0 degree phase shift rf signal to mixer 1 and sends a 90–degree phase shift rf signal to mixer 2 (mixer 1 and mixer 2 form a 2–element balanced mixer).

2.3.1.2.2.1.1 Image Generation. See figure 11-13, sheet 1. The 2.66893- to 2.86893-GHz stable local oscillator weather signal (STALOWX), received from the frequency generator via connector J3, is sent to the stalo amplifier where it is amplified and sent to a 1:2 splitter and applied to mixer 1 and mixer 2. Mixer 1 sends a (RF-LO) and a (RF+LO) 0–degree phase shift signal to the 90–degree i–f hybrid. Mixer 2 sends a (RF-LO) and a (RF+LO) 90–degree phase shift signal to the 90–degree i–f hybrid.

2.3.1.2.2.1.2 Image Rejection. See figure 11-18, sheet 1. The 90 degree i–f hybrid sums the (RF-LO) 2.7-GHz– minus 2.66893-GHz = 31.07-MHz signal from mixer 1 and mixer 2, and

the (RF+LO) 2.7-GHz + 2.66893-GHz = 53668.93-MHz signal from mixer 1 and mixer 2. The 90–degree i–f hybrid selects (RF-LO) and sends it to the i–f amplifier. The (RF+LO) signal is cancelled by the 90–degree i–f hybrid. The i–f signal is amplified by the i–f amplifier and applied to a 1:3 splitter. The * J2 output of the 1:3 splitter (WXIF) is routed to i–f receiver A2A2. The J5 output of the 1:3 splitter (WXIF) is routed to the WSP if receiver 4A12A2. The J6 outputs of the 1:3 splitter are terminated by * 50–ohm line terminations. The overall gain of rf receiver A3Al is 14 +1.5 dB.

2.3.1.2.2.2 I–f to I and Q Video Conversion. See figure 11-13, sheet 2. I–f signal to video signal conversion is performed by i–f receiver A2A2. The 31.07-MHz WXIF signal from rf receiver A3A1 is applied to a series of i–f amplifiers via connector J1-A. At the output of the first amplifier, an agc attenuator controlled by the digital processor via AGC DAC is provided to maintain the receiver at a constant gain and thus, the receiver output noise at a constant level. For high clutter environments, a limiter may be connected in series between the third and fourth i–f amplifier. The limiter restricts the peak amplitude of the received signal thereby preventing a/d saturation. The limiter output is adjustable ”2 dB with respect to the signal level that saturates the a/d converter.

2.3.1.2.2.2.1 I and Q Amplification. The three stage agc amplifier output is summed and sent to a fourth i–f amplifier. The three stage agc amplifier has a minimum gain of +13 dB. The DTONE (0DBM) is a test signal supplied from the active target channel via J1-D and used for testing only. The output of the fourth i–f amplifier is applied to the phase detector input through a bandpass filter and sine wave i–f amplifiers. The pass band of the filter is 923–kHz wide at -6 dB and is designated to match the transmitted pulse characteristics.

2.3.1.2.2.2.2 I and Q Development. See figure 11-13, sheet 2. The phase detector develops the phase shift between the input i–f signal and COHO signal to produce the I and Q outputs. The 31.07-MHz COHO signal, supplied from the frequency generator via P1-J, provides the zero degree phase reference for the phase detector. The output of the AMPL DAC controls the amplitude adjustment of the phase detector Q output. Internally, the phase detector shifts the Q signal phase 90 degrees in relation to the I signal. The output of the PHASE DAC provides a phase adjustment to the Q output of the phase detector so that the Q VIDEO output is precisely 90 degrees out of phase with the I VIDEO output. The I output of the phase detector is the result of mixing the phase detector input with the COHO signal. When both signals are in–phase, the phase detector I output is at maximum amplitude. The Q output is the result of mixing the COHO signal with the phase detector input shifted by 90 degrees. The Q output is at maximum amplitude when it is out of phase with the COHO signal by 90 degrees. The I and Q signals from the phase detector are filtered through low band pass filters to remove the COHO signal. IDC DAC and QDC DAC adjust the dc offset for less than .25 of the LSB of the a/d converter.

2.3.1.2.2.2.3 Maintenance Display Video. The output of the sixth i–f amplifier is also applied to a video amplifier via a series of logarithm amplifiers. These amplifiers perform the logarithm function on the received signal and are summed before being passed onto the video amplifier. The video amplifier boosts the DISP VIDEO signal which is sent to the Maintenance Display (Unit 7) via dual card rack A4.

2.3.1.2.2.3 Video to Digital Conversion. See figure 11-13, sheet 3 and figure 11-14. The video to digital conversion process is accomplished by a/d converter A2A3. The IVIDEO and QVIDEO signals are applied to an analog switch from the i–f receiver. Receiver control A2A4 provides the analog switch control signal (A/DTEST-) that is input at connector P2-B8 and the ANALOG signal that is input at connector P2-D. The analog switch connects the ANALOG signal to the sample

board A2A4. This test generator provides three voltages (+7/8 full scale, -7/8 full scale, and 0) which are used to test the weather a/d converter. The test signal range is -4 to +4 volts corresponding to the dynamic range of the a/d converter. The +7/8 full scale and -7/8 full scale voltages are sampled for 100 cpi pairs each while the 0 setting is sampled for 56 cpi pairs. The data collected is a single range cell. To determine whether the a/d converter is performing properly, a "5% windowing technique is utilized. The "5% windowing technique verifies that the output of the a/d converter is "5% of the full scale test voltage provided by the test generator. The time required for this test to occur is 6.95 microseconds.

2.3.1.2.2.4.3 Monotonicity Test. The second test is the monotonicity test exercising every state of the a/d converter. To perform this test the input to the a/d converter is switched from the i–f receiver to a test generator which is integral to each receiver unit on the receiver control board. The test generator provides a slowly rising ramp voltage which is used to test the a/d converter for monotonicity. Checking for monotonicity means checking that the output digital signal increases regularly as the input analog voltage signal increases. Sixteen range cells (16 I words and 16 Q words) of data are captured and the mean value is computed during one prt. For the next prt, a new voltage is applied by the test generator to the a/d converter and 16 range cells of data are again sampled. The average is taken of these 16 cells and it is compared to the previous mean value. This determines whether the mean value is increasing monotonicity relative to the mean value of the previous test level. Data is collected at a rate of 16 samples per prt (1 level/prt) and 8192 levels must be tested. Therefore, it will take approximately four (4) scans (-20 seconds) for this test to reach completion.

2.3.1.2.2.4.4 DAC Circuit Inputs. During the time interval between BCLK pulses, the line decoder is enabled. The 12–bit calibration data word output from the buffer of receiver control A2A4 is loaded by one of five i–f receiver A2A2 latch and DAC circuits during the receiver calibration cycle. The 8–bit latch and DAC circuits have an output range of 0 to 9.961 volts dc with a resolution of 0.039 volt dc/bit. The 12–bit latch and DAC circuits have an output range of -0.715 to +0.715 volt dc with a resolution of 174 microvolts dc/bit.

2.3.1.3 Six–Level Weather Filtering and Magnitude. Figure 11-15 is the six–level weather filtering and magnitude hardware block diagram, and figure 11-16 is the signal flow diagram. The hardware block diagram shows an overview of the assemblies that make up the function. The signal flow diagram provides assembly interconnection details and shows signal development and flow.

2.3.1.3.1 Introduction. See figure 11-15. The six–level weather filtering and magnitude function consists of receiving digitized in–phase (I) and quadrature (Q) data, storing the data in bulk and scratch memories, applying the data to four doppler filters to determine weather magnitude, and combining the I and Q components from each filter to develop four relative–weather magnitude words. Each of the four words represent the amplitude of the weather returns from four associated doppler filters that have notches of different widths centered at zero velocity. One of the four weather–magnitude words is selected by, and applied to the six–level weather detector function one at a time, with the possibility of each of the four words being used within the range cell being tested. The major inputs to the six–level weather filtering and magnitude function are 12–bit I and Q weather return magnitude data from one of the two online target receivers in the target receiver processor function or the rf/i–f receiver in the weather receiver function, and timing and control signals from the. The I and Q weather return magnitude data words represent in–phase and quadrature components of phase–detected weather returns, and the timing and control signals

synchronize the six–level weather filtering and magnitude function operation with the operation of the radar timing. The major output is a selected 10–bit log (base 2) power combined (vectorially summed I and Q weather return magnitude) word. All boards within the six–level weather filtering and magnitude function interface with the configuration, monitor, and test (cmt) bus. The cmt bus allows the cmt function to send and receive variable site parameters (VSPs) for configuration, and to receive and send test data during BIT.

2.3.1.3.1.1 Weather Processing Timing. An inter–pulse period (IPP) is the time between two rf pulses. The frequency at which the transmit rf pulses occur is the prf (pulse repetition frequency). The 60–nmi radius airspace covered by the ASR-9 System is divided into 256 azimuth sectors (1.4 degrees in each sector) and 1/16–nmi range cells. Between 18 and 21 IPPs can occur during each 1.4 degrees of antenna rotation. Wind loading, which prevents the antenna from rotating at a constant speed, or the use of a high prf which requires additional IPPs to fill the time allotted for a 1.4–degree antenna rotation, accounts for this variation in the number of IPPs. The IPPs that occur during 1.4 degrees of antenna rotation are divided into two sets. The first set occurs at a high prf, and the second set occurs at a low prf. Typically, 10 IPPs occur at a high prf and eight IPPs occur at a low prf. A coherent processing interval (cpi) is the time it takes either the high prfs or the low prfs to occur during a 1.4–degree antenna rotation. A coherent processing interval pair (cpip) is the time it takes for both a high and low prf set to occur. For each 1.4 degrees of antenna rotation (cpip), weather data received during all IPPs are stored in a random access memory (RAM) in range gate order. The range gate order is the order in which the IPPs are received. One range cell is loaded into the RAM for each range cell of a prt for all 18 prts of a cpip. The stored data is read during the following cpip, one cell at a time but in an order which sequentially reads all the 18 cells from one range, then all those cells from the next higher ranges; this is called batch order. The doppler filters receive the data from each cpi in batch order and filter all the range cells from a specific range in batch segments. The six–level weather filtering and magnitude function processes the stored data while new data is input during the following 1.4–degree antenna scan. The six–level weather filtering and magnitude function repeats this process 256 times during each antenna rotation.

2.3.1.3.1.2 Digital Doppler Filtering. Digital doppler filtering uses a clear day map in the six–level weather detector function that selects the appropriate filtering independently for each of six levels. The clear day map derives its name from the requirement that the map is a function of where antenna modulated ground clutter generates weather–like returns on clear days. Six weather levels are generated by six weather thresholds, corresponding to standard National Weather Service (NWS) values. These values are measured in units of weather reflectivity levels in decibels, or dBz. NWS level one is less than +30 dBz, level two is between +30 and +41 dBz, level three is between +41 and +46 dBz, level four is between +46 and +50 dBz, level five is between +50 and +57 dBz, and level six is above +57 dBz. The clear day map cell size measures one cpip by one nautical mile. The FAA uses a different Level One Threshold than the NWS (National Weather Service), the FAA sets the threshold from 18 dbz (VSP adjustable) to 30 dbz., all other levels agree with the NWS. Each cell specifies, for that area, which filter output is best in terms of passing weather information and rejecting ground clutter while trying to detect each level of weather. Minimizing the effects of ground clutter is done through the selection of which of the four filter outputs produced for each range cell and cpip is used in threshold comparisons. The four filters differ in the width of the doppler frequency band, centered about zero doppler, that is rejected. The first filter is an all–pass filter, passing all doppler frequencies to allow use of the full spectrum in areas where ground clutter is not a concern. The remaining three filters all have a notch, or band reject, centered at zero doppler. In areas where antenna modulation of ground clutter produces larger returns, the output of the filter with more attenuation is used. The possibility that a cell may specify the

use of each of the filters (for example: all pass for levels one and two, first notch for level three, second notch for level four, third notch for level five, and all pass for level six) is the basis for having all four filter magnitudes available for each cpip and range cell. The clear day map also contains an indication of the level at which detection at or below this level is subjected to a censoring process in the post processing smoothing and contouring function. While the filter select enables the proper filter output from the six–level weather filtering and magnitude function to be passed to the six–level weather detector function, the censor level is also passed to the six–level weather detector function.

2.3.1.3.1.3 Input Data Sources. The six–level weather filtering and magnitude function can receive I and Q data from three different sources. The source of the input depends on the weather and the operating status of the two target receiver processors. The level of the weather determines the selected radar polarization, linear or spherical. The target channels use the nearly spherical shape of raindrops to reflect circularly polarized radio waves back to the antenna that transmitted them and with a rotation * opposite to the one in which they were transmitted, causing the antenna to reject their returns. Co-Polarized is the term used to describe this opposite rotation, the WSP may use this information in the future to increase it's sensitivity to weather. Without any weather present, the target channels use * linear polarization. When operating with a linear–polarized signal, the six–level weather magnitude and filtering function receives the same data that is applied to the target channels. This data is from the output of the a/d converter of the online target receiver via the a/d interface board of the online target receiver/processor filtering and magnitude function. The ASR-9 System has redundant target receiver processors. Therefore, the first two possible sources of data to the six–level weather filtering and magnitude function are the two target receivers. As low level weather enters the 60–nmi radar range, the target receiver processors continue operating in linear polarization, constant false alarm rate (CFAR) circuits in the target receiver processors eliminate the weather from the target processing, and the six–level weather filtering and magnitude function continues to receive data from the online target receiver. During periods of heavy precipitation, as identified by the weather channel's smoothing and contouring process, polarizers in the antenna feed assembly may be automatically or manually switched (operator selectable) to circular polarization. When the antenna switches to circular polarization, the weather channel uses its own rf/i–f receiver. While the target channel receivers use same–sense circular polarization to reject weather returns, the weather channel receiver uses opposite–sense polarization to enhance the weather returns. The separate receiver also provides for separate weather channel sensitivity time constant (STC) to be used.

2.3.1.3.2 I and Q Data Input. See figure 11-16, sheet 1. The 12–bit I and Q weather return magnitudes are applied to the input buffer of a/d interface board A4A103. The input buffer is controlled by the input control circuit. The input control circuit allows the 12–bit I/Q weather return magnitudes IQDATA00 through IQDATA11 to be buffered and passed on to the adders and limiter for additional * processing during the 973 range cell processing interval or live time. See figure 2-30. The WSP employs unused backplane ribbon cable connector J106 to tap the 12-bit I and Q weather return magnitudes. The WSP changes the input control circuit for the I and Q Data when it is online. The following scenario describes the changes that the WSP processor required for the interface to the ASR9.

Linear Polarization. See Figure 11-1a. In the Linear Polarization State, the low beam microwave returns are not available to the WSP receiver if the surveillance channel is using the low beam. In this case, the WSP must obtain radar return information I/Q (In-phase and Quadrature) digital data is available on back-plane connector 4A4J106 (manufacturing test set connector.) I/Q data source selection for the 4A4J106 connector port follows the ASR9 Six Level Weather Processor I/Q data source selection. Therefore, the Weather Receiver Monitor software in the ASR9 baseline *

* configuration determines the I/Q data source selection for the 4A4J106-output port. The WSP is connected to the ASR9 by a 50-pin ribbon cable plugged into 4A4J106. It extracts the appropriate I/Q data for weather product development from this cable.

The WSP employs a different I/Q data selection process than the baseline ASR9 Weather Processor. To accomplish this goal, the ASR9 Weather Receiver Monitor software must be modified to allow the correct I/Q data selection in the WSP modes. The following table illustrates the differences.

I/Q DATA SELECTION TO FILTERS	
Radar Mode (Past)	**WSP Co-polarized (Present)**
Linear Polarization use Online Channel A I/Q data	Linear Polarization use Channel A I/Q data
Linear Polarization use Online Channel B I/Q data	Linear Polarization use Channel B I/Q data
Circular Polarization use Weather Channel I/Q data	Circular Polarization use Online Channel I/Q data (Co-Polarized)
Calibration Time use Weather Channel I/Q data	Calibration Time use Weather Channel I/Q data

Circular Polarization. The WSP-CP high/low beam switching is directed on a periodic (little more than a scan) basis, not on a range (VSP 30 nmi) basis as in the ASR9 mode. In this state, the ASR9 must supply the WSP with Co-Polarized I/Q data from the target channel A/D converter. The Weather Receiver Monitor software determines data source selection. The ASR9 Weather Processor ADI board shall direct the target channel (Co-Polarized) I/Q data to the WSP through the cable connected to th ASR9 4A4J106 connector. A byproduct of this mechanism is the ASR9 Weather Processor. It will also receive the Co-Polarized returns while the WSP is online and in the Circular Polarization mode.

2.3 I/Q Data Selection Controls: Three signals control the I/Q data selection for the Six Level Weather Processor and the 4A4J106 ASR9 connector. The control signals are Local-, ALTCH1-, and ALTCH2- on the ADI board slot 4A4A103. These signals are derived from three STU A board signals SELAD100-02, which are in turn controlled by the WSP Receiver Monitor Software. Backplane wires for SELAD100-02 are difficult to modify because they are intertwined with other backplane wires as they traverse the distance between these two boards.

We determined that a modification to the ASR9 Weather Receiver Monitor Software is required to select only the onklne surveillance channel when the WSP mode is selected. If the WSP is offline, the signals will behave as if the ASR9 is in baseline configuration. The Weather Receiver Monitor in slot 4A4A119 will know the WSP is online by reading the PIO port UP1021 at backplane pin B81. It is connected to the STC/CAL/GEN board signal WSP_EN 4A4A123 pin A73. *

The interval after the live time until the next 973 range cell processing interval is called dead time. Dead time is the interval where the radar receiver/processor can perform self–testing or calibration tests. Synchronizer timing signals control the operation of the input control circuit. Refer to paragraph 2.3.1.3.7 for more details on self–testing and calibration.

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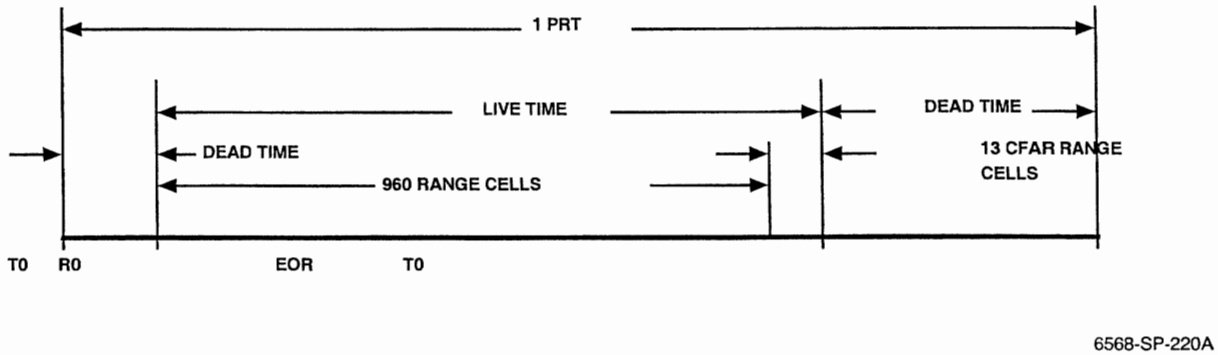


FIGURE 2-30. I AND Q DATA PROCESSING INTERVAL DIAGRAM

2.3.1.3.2.1 Live Data Processing Interval. The total radar range coverage (60 nmi) is provided by 960 range cells. Each range cell represents 1/16 nmi of range coverage.

2.3.1.3.2.2 I and Q Weather Magnitude Return Input Control. See figures 2-31 and 2-32. Each of the 960 range ordered I and Q interleaved weather return magnitudes received during the live time interval constitute one part of weather return magnitudes. The I and Q components of each range cell are input successively and clocked through the output register at twice the range cell rate of 2.6 MHz. The I and Q components of each range cell applied to the output register requires two 2.6-MHz clocks (0.38 microsecond), one for the I and one for the Q.

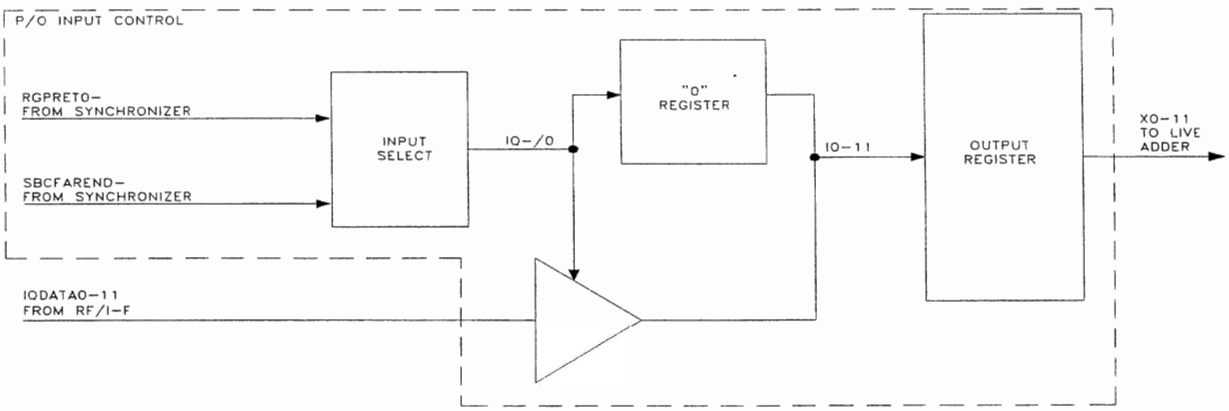


FIGURE 2-31. IQ INPUT SELECTION

stations. The detection process begins when the weather batch data (in magnitude format) is classified into six successive levels of intensity. A clear–day standard is level one and increases to a maximum storm intensity of level six. The span of weather is encompassed by the two–level weather detector of the receiver/processor, but with one–third the resolution of the weather detector. The two–level weather detector serves as a backup to the six–level weather detector.

2.3.1.4.3.1 Six–Level Weather Detection. The weather detector has a self–contained memory which enables it to store clear day and threshold maps. This, in turn, allows the detector to determine the level of weather in each range cell. The weather detector compares the output level from a selected filter with a value stored in the threshold map to determine the level of weather in a particular range cell. An M out of N criteria for 16 range cells is used for each of the six levels. The threshold versus range memory is 23K words by 11 bits. This provides for six levels of weather, two polarization modes, and two beam modes. Second–time–around ambiguity is determined by requiring a detection in a given cell of a 10–pulse cpi to match a detection in an adjacent 8–pulse cpi. These weather detections are accumulated in memory and output to the smoothing and contouring functions contained in the single board computer (SBC).

2.3.1.4.3.2 Six–Level Weather Filtering. The weather detection function uses thresholds developed by clear day and threshold maps stored in its memory to determine the level of weather in each range cell. Thresholds developed in the CDM determine which of the four filter outputs from the filter and magnitude processor the weather detector will select for processing from a particular range cell. The filter containing all velocities is used in regions that do not contain clutter. The threshold map stores thresholds for high and low beam signals in order to eliminate remote ground clutter returns when the amplitude of the clutter exceeds the capability of the filters and the dynamic range of the system, which could occur in some mountainous areas. Censoring does not affect the coverage to an appreciable extent and prevents clutter breakthrough from appearing on the displays.

2.3.1.4.3.3 Filter Outputs. The output of the selected filtering and magnitude function filter (LC6WXDAT) is sent to six–level weather detector (10 parallel input lines) to be compared with six–level weather threshold values (threshold data) from the six–level CDM/threshold to determine which weather level is crossed. There are four signal input lines associated with the six–level weather detector which are derived from six–level CDM/threshold. In addition to threshold data, there are CDM generation, censor, and SMFILSEL.

2.3.1.4.3.4 Error Data. Error data, which is derived from the six–level CDM/threshold, is sent to the six–level weather detector for comparison with the weather–level crossings. If the weather–level crossing is higher than or equal to the censor data, the weather–level crossing will be censored. The six–level weather detector accumulates the weather–level crossing data (WXXINGS) for 60 nautical miles by one cpi pair and outputs this data to the SBC processor upon request.

2.3.1.4.3.5 Input/Output Signal. The six–level weather detector receives the same input signals as the six–level CDM/threshold circuit from the channel synchronizer and monitor and control with the exception of the batch control signals. Batch control signals BCCTL80 through BCCTL84 go to the six–level weather detector while BCCTL74 through BCCTL79 go to the six–level CDM/threshold. The remaining signals of the synchronizer and monitor/control groups are common to both boards. Other input signals are the LC6WXDAT from the filtering and magnitude processor and the HEADER SELECT from the SBC processor. Two output signals, CPI INTERRUPT and CLOCK, are sent to the SBC processor. Details on these and other signals pertaining to the six–level weather detector are described in paragraph 2.3.1.4.7.2.

2.3.1.4.4 SBC Processor. The function of the SBC processor is to use its smoothing and contouring processor circuitry to generate a weather map. It has an RS-422 serial link to system control. The main bus between the six–level weather detector and the SBC processor is called the weather crossings data bus. Its main function is to transmit the header data followed by the weather–level crossing data to the SBC processor. Header data consists of corresponding cpi pair number, filter number, polarization mode, beam mode, and CDM generation mode. This weather level crossing data is used to generate a weather map. The weather map is stored in the data memory until it is requested by the local system control. Upon such a request, the weather map is supplied in serial format via the programmable interface.

2.3.1.4.4.1 Smoothing Weather Contours. The smoothing establishes weather contours. The purpose of the smoothing filters, contained within the SBC processor, is to eliminate isolated threshold crossings and zeros. The purpose of the contouring function is to provide a final weather level for each of 30,720 weather cells. At the end of range (60 nautical miles), the cpi interrupt signal informs the SBC processor that the weather–level crossing data is ready to be transmitted. The SBC processor sends the header select signal to the six–level weather detector to initiate the data transfer. The weather crossing data bus transmits the header data followed by the weather–level crossing data to the SBC processor which uses the weather–level crossing data to generate a weather map. The weather–level crossing data is smoothed to eliminate isolated threshold crossings and zeros. The smoothing function calculates a median weather level for each of the 30,720 cells (120 0.5–nautical–mile range units by 256 cpi pairs) over a six–scan period. The weather smoothing and contouring functions use five thresholds to generate six weather levels corresponding to the standard NWS values. Because there are 30,720 weather cells, the raw weather input may contain a very large number of threshold crossings for a single antenna scan.

2.3.1.4.4.2 Smoothing Weather Declarations. The smoothing function counts the weather declarations for each level over a six–scan period and creates polarization change request messages based on weather declarations of level two or greater. The weather amplitudes do not change appreciably between scans so weather can be stored and smoothed on a scan–to–scan basis over a period of six scans. Smoothing is performed over three scans for threshold 1 and over the next three scans for the other four thresholds. The smoothed weather data is then read out to the remote site in 2.4 antenna scans. If a weather cell is censored, the weather–level threshold crossing of a neighboring cell is assigned to the censored cell. In the CDM generation mode, the smoothing function also outputs a raw CDM. The contouring function declares a final weather level for each of the 30,720 cells by determining the largest weather level in a nine–cell cluster. If all nine cells are censored, the weather level from a neighboring cluster is used for the censored cluster.

2.3.1.4.4.3 Smoothing and Contouring Function. The built–in test (BIT), in the SBC processor, outputs the status messages on the differential serial link signal to the weather monitoring and control function. VSPs are supplied from the weather monitoring and control function. In addition, the smoothing and contouring function has a serial link to the local system control to communicate status messages. After the weather data has been properly configured in the SBC processor, it is stored in the SBC data memory. Serial signal lines for the control, address, and data functions between the SBC processor and the SBC data memory are used for this process.

2.3.1.4.5 SBC Data Memory. The purpose of the SBC data memory is to store the weather map. * Data is output via the programmable interface to the local system control processor. The WSP weather map is muxed or replaces this weather map when it is online. The mux function resides on the local system control board. The SBC data memory is tested by reading test data out of the memory onto the * response bus (CICMTR). Signal lines associated with the SBC data memory carry control, address, and data information.

2.3.1.4.5.1 Weather Map. The final weather map is generated over a nine–scan period and stored in the SBC data memory until the local system control reads it out via the programmable interface. The SBC processor sends the address and control signals to write the weather map data into the SBC data memory.

2.3.1.4.5.2 Weather Map Output. The programmable interface addresses the SBC data memory to read the weather map data through the data bus. The programmable interface converts the parallel weather map data from the SBC data memory to a serial format and sends it to the local system control processor as the differential SDATOUT0A signal.

2.3.1.4.6 Programmable Interface. The programmable interface reads the weather map out of the SBC data memory. The programmable circuitry converts the parallel data from the SBC data memory to a serial format and outputs this data to the local system control. There are three modes of operation associated with the programmable interface: input, output, and text.

2.3.1.4.6.1 Output Mode. When the interface is in the process of reading out a weather map, it is in the output mode, converting parallel data to serial data, with the serial output continuously enabled. Data flow to the programmable interface is controlled by the SBC processor.

2.3.1.4.6.2 Local System Control Interface. The programmable interface utilizes three internal signal lines: address out, data I/O, and input control. There are three signal lines to/from the local system control processor, namely SDATOUTOA(+/-) out, CLKOUTOA(+/-) out, and WXCTSO(+/-) in. A description of these signals, including a detailed theory of operation of the programmable interface, is covered in the following paragraphs.

2.3.1.4.7 Detailed Functional Flow. The following paragraphs discuss the detailed functioning of the signal flow on each of the boards described in the previous paragraphs and shown in figure 11-17. The corresponding signal flow diagram is shown in figure 11-18. Since the operation of the BIT can span several boards, details of the BIT are described in a separate paragraph at the end of this section.

2.3.1.4.7.1 Six–Level CDM/Threshold Detailed Functional Flow. See figure 11-18, sheet 1. The following paragraphs describe the detailed signal flow of the six–level CDM/threshold.

2.3.1.4.7.1.1 Batch Control Buffer. See figure 11-18, sheet 1. The batch control buffer functions to hold/condition certain input signals in order that they can be used, in an orderly fashion, in succeeding stages.

2.3.1.4.7.1.1.1 Nautical Mile Counter. See figure 11-18, sheet 1. Batch control signal BCCTL75 is input to the batch control buffer and output as signal NMICNT, which increments the NMI counter every nautical mile. The output of the NMI counter (NMI0 through NMI5) is sent to the CDM address multiplexer. Batch control signal BCCTL76 is input to the batch control buffer and output as signal PRECPIPR. The PRECIPR signal resets the NMI counter and the range cell counter to zero at the beginning of each azimuth cpi pair. The PRECIPR signal also increments the CPIPR counter at the beginning of every cpi pair (1.4 degrees azimuth). The output of the CPIPR counter (CPIPR0 through CPIPR7) is sent to the CDM address multiplexer.

2.3.1.4.7.1.1.2 Weather Filter Selection. See figure 11-18, sheet 1. Batch control signal BCCTL74 is input to the batch control buffer and output as signal WXLVLCNT, which increments the weather–level counter from one to six every cpi pair. The output of the WLVL counter (WLVL0

through WLVL2) is used as part of the threshold EEPROM address multiplexer to select the appropriate filter select data from the CDM data multiplexer. The output of the CDM data multiplexer (FILSEL0 and FILSEL1) and the censor data (CENSOR0 through CENSOR2) are sent to the CDM output buffer. The censor data (SMCENSOR0 through SMCENSOR2) is sent to the six–level weather detector. The filter select data (SMFILSEL0 through SMFILSEL1) is sent to the six–level weather detector and to the filter and magnitude function. The SWPORT0WR- signal disables the censor–level outputs when the six–level weather detector is performing stimulus/response testing. The LCPORT0WR- signal disables the filter select outputs when the filtering and magnitude function is performing stimulus/response testing.

2.3.1.4.7.1.1.3 Range Cell Counters. See figure 11-18, sheet 1. Batch control signal BCCTL79 is input to the batch control buffer and output as signal RCCNTEN, which increments the range cell counter every range cell. The PRECPIPR signal resets the range cell counter to zero at the beginning of every cpi pair. The output of the range cell counter (RC00 through RC09) is sent to the threshold address multiplexer. The polarization mode signal (SBLP/CP-) is input to the batch control buffer and output as CP/LP, indicating linear or circular polarization. The CP/LP signal is sent to the threshold address multiplexer to be used as part of the threshold memory address. The LC6BEAMSEL signal, from the filtering and magnitude function, is input to the batch control buffer and output as signal BTCHBEAM. This signal indicates the active beam (high or low).

2.3.1.4.7.1.1.4 Beam Selection. See figure 11-18, sheet 1. Batch control signal BCCTL78 is input to the batch control buffer and output as signal NEGRNG-, indicating that the beam is in negative range. Because the weather monitoring and control function cannot be allowed to override the beam signal while in negative range during testing, the negative range signal (NEGRNG-) selects the actual beam signal (BTCHBEAM) instead of the possibly overridden beam signal (LIVEBEAM). The LIVEBEAM signal is selected at all times when not in negative range. The output of the second beam multiplexer (BEAM) is sent to the threshold address multiplexer.

2.3.1.4.7.1.1.5 Threshold Selection. See figure 11-18, sheet 1. Batch control signal BCCTL74 is input to the batch control buffer and output as signal WXLVLCNT, incrementing the weather–level counter from one to six every cpi. The output of the weather–level counter (WLVL0 through WLVL2) multiplexes the appropriate filter select data out of the CDM data multiplexer. Signals WLVL0 through WLVL2 are delayed by the weather level count delay (WLVLDL0 through WLVLDL2), and then input to the threshold address multiplexer. Since the threshold EEPROM is addressed after the CDM data multiplexer, the CDM data is output one weather–level count ahead of the threshold output. The output of the threshold address multiplexer (THRADR00 through THRADR14) addresses the threshold EEPROM. When in the local mode, the operation mode signal (LOCMODE-) enables the threshold EEPROM continuously. The output of the threshold EEPROM (THRDAT00 through THRDAT10) is sent to the threshold data output buffer, and then output to the six–level weather detector as SMTHRDAT0 through SMTHRDAT9. The SWPORT1WR- signal disables the threshold data outputs when the six–level weather detector is performing stimulus/response testing.

2.3.1.4.7.1.2 Weather Threshold. See figure 11-18, sheet 1. For every range cell, the six–level CDM/threshold sends a set of six consecutive weather–level threshold values to the six–level weather detector. The threshold comparator compares the threshold data (SMTHRDAT0 through SMTHRDAT9) with the filter magnitude data (LC6WXDAT0 through LC6WXDAT9) to determine which weather–level threshold has been crossed. The 24K by 11–bit threshold EEPROM stores the weather–level threshold values. This is a non–volatile memory and the weather–level threshold values are, of course,
* programmable. The transmitter must be radiating when these thresholds are loaded (generated); that is, the transmitter power measured at the RMS power meter is used in the calculation of the weather-level thresholds. The value of the weather–level thresholds depends on the current polarization mode, *
beam

through HDR10 consists of the cpi pair count (CPIPR0 through CPIPR7), the CDM generation mode (SMCDMGFEN0-) from the CDM output buffer on the same board, the filter select (SMFILSEL0 and SMFILSEL1), the polarization mode (SBLP/CP-), and the beam mode (SBWXSYNCB-). Signals SBLP/CP- and SBWXSYNCB- are sent from the synchronizer. The 120 weather data cells and the two test words read out of the RAM follow the header data. Because the RAMs and their address counters are not tested during stimulus/response testing, the weather data is duplicated in the RAM. When the weather data is read out, it is compared to duplicate weather data. If they are the same, an error is sent for the weather monitoring and control processor to read.

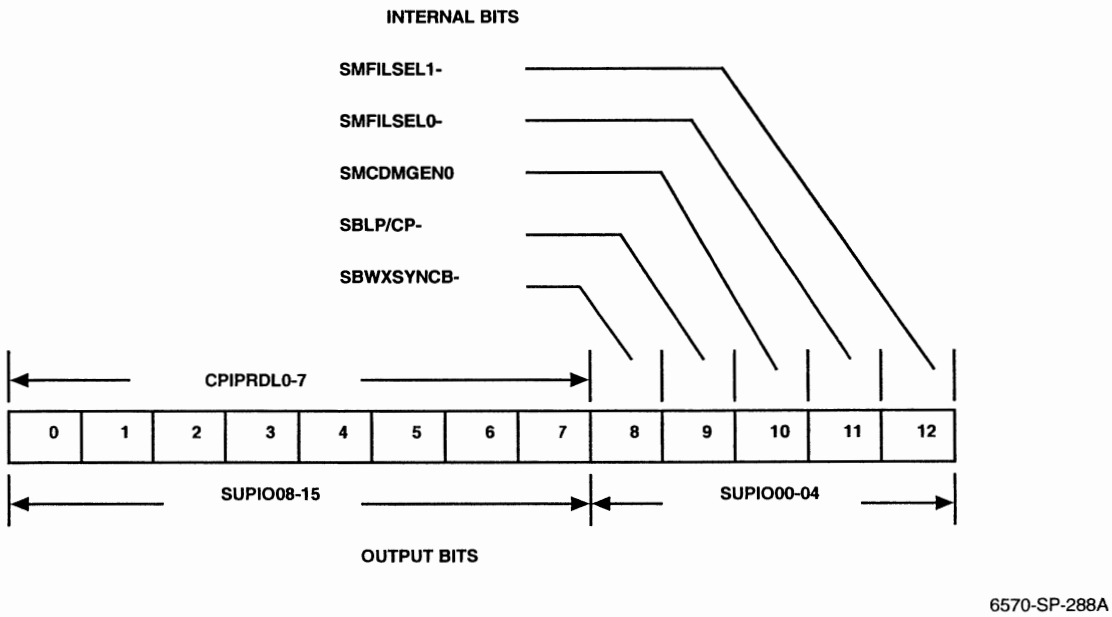


FIGURE 2-47. SIX–LEVEL WEATHER DETECTOR HEADER OUTPUT WORD

2.3.1.4.7.3 SBC Processor Detailed Functional Flow. See figure 11-18, sheet 3. The SBC processor receives inputs SUPIO00 through SUPIO04, and SUPIO08 through SUPIO15 from the six–level weather detector and develops a weather map with 0.5–nautical mile range and 1.4–degree azimuth increments. The SBC processor performs the following: temporal and spatial smoothing processing, contouring processing, polarization change request, raw CDM generation [transferring this map to the remote monitoring subsystem (RMS)], status messages, and performance data outputting upon request of the RMS.

2.3.1.4.7.3.1 Smoothing Processing. See figure 11-18, sheet 3. The temporal smoothing processing approximates the median weather level detected during three pairs of scans (scans 1 and 2, 3 and 4, and 5 and 6) and develops an intermediate working map for 30,720 cells (1.0 to 60.5 nautical miles in 0.5–nautical mile range increments) for storing weather data over a six–scan interval. The temporal smoothing processing is performed as follows. Weather–level data for a scan pair is generated by replacing odd scan data (0, level 1, or censored) with even scan data other than zero (levels 2 through 6, or censored). If the weather levels on the first two scan pairs match, this level is stored in the smoothed map; the weather level from the third scan pair

is ignored. If the weather levels on the first two scan pairs do not match, the smaller weather level of the first two scan pairs is stored, unless the weather level for the third scan pair is higher. In that case, the weather level stored is one level higher than the smaller weather level of the first two scan pairs. If the weather level for one of the three scan pairs is censored, the smaller of the other two weather levels is stored. If more than one of the weather levels are censored, the censor value is stored. The spatial smoothing processing declares a weather level for each of the 30,720 cells. This level is the maximum level that is equaled or exceeded in a programmable fraction of uncensored cells within a nine–cell cluster. The cluster is the cell of interest and its eight surrounding neighbors. The fraction is a smoothing parameter set by the remote monitoring subsystem. The number of censored cells are subtracted from nine when calculating the fraction. If there are too many censored cells (designated by the smoothing parameter) in the nine–cell cluster, the cell is designated as censored until the contouring processing.

2.3.1.4.7.3.2 Contouring Processing. The contouring processing declares the final weather level for each of the 30,720 cells. The final level is the maximum value of declared weather in a nine–cell cluster. A censored cell is filled in with the value from an adjacent range and azimuth cell. The contouring processing starts at a nine–cell cluster with a center at 60 nautical miles. The contouring processing declares the weather level for the cell of interest by finding the largest in the nine–cell cluster. Censored cells are ignored in determining the largest. If all nine cells are censored, the weather level for the cell of interest is the weather level of the previous nine–cell cluster. The range is decremented by 0.5–nautical mile increments, and repeats the process down to 0.5 nautical mile.

2.3.1.4.7.3.3 Antenna Polarization. The SBC processor requests an automatic antenna polarization change if the current polarization is linear and the number of weather cells of level 2 or greater exceeds the circular polarization threshold, or if the current polarization is circular and the number of weather cells of level 2 or greater is less than the linear polarization threshold. The VSPs determine the circular and linear polarization thresholds (selectable from 0 to 40 percent). The circular polarization threshold specifies the percentage of weather cells from several antenna scans that must be at a weather level of 2 or greater in order to switch from linear to circular polarization. The linear polarization threshold specifies the percentage of weather cells that must be below weather level 2 to automatically switch
* from circular to linear polarization. The WSP controls the Antenna Polarization when it is online. When the WSP is online, it performs the automatic switch function by reading the ASR9's circular and linear polarization threshold VSPs, then it uses these values in the WSP software to control the ASR9 polarization. *

2.3.1.4.7.3.4 CDM Generation Mode. See figure 11-18, sheet 3. In the CDM generation mode, the SBC processor outputs a raw CDM after the six–scan temporal smoothing (no spatial smoothing or contouring). The serial link (RXD3+ and RXD3-) RMS and local system control sends the raw CDM signals RXD3+ and RXD3- status messages to the local system control. The local system control serially transmits the input of the status messages and VSPs from the RMS using signals TXD3+ and TXD3-. The handshaking signals used in the serial data transfers are the clear–to–send signals (RTS3+ and RTS3-) and the request–to–send signals (CTS3+ and CTS3-). Details on BIT are contained in paragraph 2.3.1.4.7.6.

2.3.1.4.7.4 Weather Map Storage. See figure 11-18, sheets 3 and 4. The SBC processor uses the SBC data memory to store the weather map. The SBC processor writes the weather map data in the SBC data memory via the SUDAT00- through SUDAT15- data bus. The SBC processor addresses the memory locations in the SBC data memory through the SUADR00- through SUADR19- address bus. The SBC processor uses the following control signals to transfer data to the SBC data memory: the write (SUAMWC-), read (SUMRDC-), data bus lock (SULOCK-), constant clock (SUCCLK-), and clock (15 MHz). The SBC data memory sends the SBC transfer

acknowledge signal (SUXACK-) to the SBC processor to indicate a successful data transfer. Details on BIT are contained in paragraph 2.3.1.4.7.6.

2.3.1.4.7.5 Programmable Interface Functional Flow. See figure 11-18, sheet 5. The programmable interface reads the weather map out of the SBC data memory. The programmable interface converts the parallel data from the SBC data memory to a serial format and outputs this data to the local system control. The programmable interface is a general purpose serial interface. Its operation is divided into three modes: input, output, and test. In this case, the programmable interface is an output device, converting parallel data to serial data, with the serial output continuously enabled. The SBC processor controls the data flow to the programmable interface. This programmable interface board is used in several applications. The latches circuit routes the internal low order data bus bits to the address lines of the multibus, and provides bidirectional control of the low order address bits. The board has three identical transceiver channels. The channels are individually enabled by a direct memory access (DMA) controller, which ensures that only one channel sends or receives data at a time. The source of the data and associated clock that is applied to the enabled channel is selected by a channel selection switch. The channel converts the serial input data to a parallel format. The parallel data is placed on an internal bus and applied to a microcontroller. The microcontroller verifies the data and checks the associated message status flags. The data is then applied to a RAM with an I/O ports circuit. The RAM with I/O ports circuit enables reading the valid data via bus transceivers. The programmable interface board can also convert parallel data to serial data using the serial–to–parallel conversion in reverse order. The functions on the programmable interface board are individually enabled by the board function decode logic.

2.3.1.4.7.5.1 Weather Map Control. See figure 11-18, sheet 5. Control line SUBHEN- and address lines SUADR00- through SUADR19- from the SBC processor address the programmable interface by entering the board function decode logic circuit. Control lines SUIORC- (for reading data) and SUIOWC- (for writing data), and address lines SUADR01- through SUADR05- from the SBC processor also activate the enable and reset lines to each transceiver channel function via the board function decode logic circuit. The board function decode logic determines the board address and develops a board select signal when the programmable interface board is addressed. This board also develops one of two read and one of eight write signals. Two signals determine if the programmable interface has priority on the multibus. The first is the bus request interrupt signal (SUBREQ1-), which is sent from the programmable interface to the SBC processor. The second is the bus busy signal (SUBUSY-), which is sent from the SBC processor to the programmable interface board. The DMA controller then interrupts the SBC processor through the SUINT02- interrupt signal, which tells the SBC processor that the programmable interface is ready to receive new weather map data. The SBC processor sends control signals to initiate the data transfer from the SBC data memory to the programmable interface. The DMA controller sends the following control signals to read weather map data out of the SBC data memory: the memory read control (SUMRDC-) and memory write control (SUAMWC-) signals. The DMA controller addresses the SBC data memory using address lines SUADR00- through SUADR19-. The weather map data is input to the transceiver and output to the data bus by the transceiver enable signal. The weather map data is input to the next transceiver from the data bus by the transceiver enable signal. The weather map data is output from the transceiver to the RAM and input/output ports by the RAM enable.

2.3.1.4.7.5.2 DMA Controller. See figure 11-18, sheet 5. The DMA controller is controlled by the SBC processor through decoded address lines SUADR01- through SUADR05- and interrupt signal SUPRN1-. The board function decode logic receives the control signals and address lines

from the SBC processor. The SBC processor controls the microcontroller through the control and status latches, which relay commands from the data bus to bus 0. The microcontroller accesses the PROM which contains the control program for the microcontroller. The timer provides the timing functions for the microcontroller. The microcontroller sends the weather data from the RAM and I/O ports through bus 0 to the parallel–to–serial data conversion. Once the SUPU00 signal from the SBC processor selects the channel, the online weather data is converted from a parallel to a serial format. * The differential serial data (SDATOUTOA) is output to the local system control, it connects to line 3 communications channel. Differential serial lines SDATOUT1A is output to local system control when SSM-011 modification is installed, it connects to link 5 communications channel. SDATOUT2A is connected to the local system control but is not used. *

2.3.1.4.7.6 BIT Testing. The following paragraphs discuss the manner in which system functions are tested using BIT capabilities.

2.3.1.4.7.6.1 Overview. The weather monitoring and control function is the key element for conducting BIT in the weather signal processor. Tests are requested and scheduled for the weather synchronizer and weather DSP functions utilizing a multibus. Results from the tests and the smoothing and contouring function self–test are reported to this function which includes the results of its own self–test to determine the health of the weather signal processor. The weather monitoring and control function collects results from the other functions, includes the results of self–test, and determines the status of the weather channel. It schedules tests for the weather synchronizer and weather DSP functions. The weather monitoring and control function also provides the link to the RMS processor for conducting fault isolation testing.

2.3.1.4.7.6.1.1 Non–Interruptive Testing. The weather synchronizer BIT performs a real non–interruptive test process, causing no system degradation. The weather monitoring and control function requests tests to be run; then the weather synchronizer allocates the test in a time slot that permits it to be executed without system interruption. A multibus serves as the link between the functions. Tests are requested by the weather monitoring and control function through a multibus link. The tests are then executed at a time that will not corrupt weather data. The concept used is a stimulus/response test. Results are reported back to the weather monitoring and control function.

2.3.1.4.7.6.1.2 Error Checking. The weather monitoring and control function periodically checks the errors on the six–level CDM/threshold, the six–level weather detector, the SBC processor, and the SBC data memory. The weather monitoring and control function reads the errors through response bus CICMTR00 through CICMTR11. The SBC processor (figure 11-18, sheet 3) is BIT–tested and outputs the status messages on the differential serial link signal (RUSTXD) to the weather monitoring and control function. The smoothing and contouring function has a serial link to the local system control to communicate status messages. The six–level CDM/threshold (figure 11-18, sheet 1) is tested by the weather monitoring and control function by injecting test data through stimulus bus CICMTS and reading the test data through response bus CICMTR. The response bus also includes memory address counter errors.

2.3.1.4.7.6.2 Error Buffer. The error output buffer holds the errors from the six–level CDM/threshold; all errors are cleared after being read. The CPIPR, NMI, and range cell counters, and CDM and threshold data are checked for errors. The cpi pair count CPIPR0 through CPIPR7 is checked at the north mark signal BNRTH (developed from the SBARP- signal) to make sure it reached the terminal count of 255. If the terminal count is not 255 at the north mark, the error signal (CPIPRERR) is sent to the error output buffer. The NMI counter count, NMI1 through NMI5, is checked at end of range by the CNTERR signal. If the nautical–mile count is not at a terminal

select board through the CMT data bus (DAT). Simultaneously, the 6WX/RM applies an address value to the CMT address bus (ADR) which specifies the location for storage of the data in the EEPROM. The six MSBs of the address value are decoded to generate the EEPROM chip enable signal which activates the EEPROM. The four MSBs are compared to a prewired jumper identifier. The next two MSBs specify the EEPROM. Address bits 0 and 13 (ADA00 and ADA13) set to 0 generate an active low external write enable signal (E2PROMWR-) to specify the write mode for the EEPROM. An RMS operation activates E2PROMWR- which allows operator control of the write operation to prevent inadvertent changes of the remaining address bits and to address the EEPROM directly. The data on the DAT bus is passed through the byte swap transceiver to the EEPROM for storage.

2.3.1.5.2.6.2 VSP Transfer to Weather Channel. See figure 11-20, sheet 3. The 6WX/RM reads from the EEPROM, via the CMT data bus (DAT00- through DAT15-), at locations designated by address signals provided by the CMT address bus (ADR00- through ADR19-). VSPs for the FEE are sent to the FEE via the synchronizer. Data is read from the EEPROM to the transceiver where it is applied to the data bus. The 6WX/RM then addresses the target data synchronizer (described in paragraph 2.3.1.5.2.3.2). VSPs used in the DSP are read from the EEPROM by the 6WX/RM just as FEE VSPs. The data word is applied to the memory data bus transceiver (sheet 2). The CMT memory transceiver receives the enable signals from the 6WX/RM (paragraph 2.3.1.5.2.3.4.4). This allows the VSP data to be input to the CMT memory bank RAM via the memory bus. The RAM address decoder supplies RAM address signals (CIRAMADR03 through CIRAMADR12) to designate the CMT memory bank and RAM address location for the VSP data as described for response data storage. Once they are stored, the VSPs are output from the CMT memory to the WX DSP boards when the radar is not processing real–time data. The VSP values are read out and transmitted to the desired WX DSP board on the stimulus bus as described for stimulus words.

2.3.2 Local Display Processor

A hardware block diagram of the local display processor function is shown in figure 11-27, and a signal flow diagram of the local display processor function is shown in figure 11-28. The hardware block diagram provides a quick reference overview of the assemblies and major components that make up the function. The signal flow diagram shows details of signal development and flow, and provides assembly interconnection details.

2.3.2.1 Introduction. See figure 11-27. The local display processor receives CD messages from the radar receiver/processor (channel A or B). The local display processor provides analog target and weather video, developed from the CD messages, to the maintenance display plan position indicator (PPI). Selection of the active receiver/processor channel is from switch action on the maintenance display. Selection of the type of video from the local display processor that can be displayed on the maintenance PPI is from switch action on the maintenance display video control box. The local display processor also generates timing signals. Some of these signals are used by the local display processor, while others are amplified and distributed to the maintenance display. The local display processor contains its own built–in test (BIT) routines, which are initiated by two SBC processors. The results of the BIT are sent to the RMS for maintenance and fault reporting purposes.

2.3.2.1.1 Input Data Selection. See figure 11-27. The input target data channel selection for local display processor A4 is controlled by switch action from the channel selection switch

on the maintenance display. This switch allows for either radar receiver/processor channel A or B to be
* online as needed. The input weather data is the online weather processor (including the WSP), which *
has been selected at the local system control through switches on the maintenance display prior to being sent to local display processor A4. The channel/level selection for the weather data occurs at the local system control.

2.3.2.1.2 Message Input Formatting. See figure 11-27. Programmable interface A4A204 and A4A205 take the input serial surveillance and weather data, convert it to parallel format, and determine the type of data that was processed. SBC processor no. 1 A4A202 controls this process along with validating and formatting incoming surveillance and weather data. The surveillance and weather data is then stored in SBC data memory A4A208. SBC processor no. 1 further formats the surveillance and weather data and places the reformatted surveillance and weather data in storage on the SBC data memory board. SBC processor no. 1 maintains the target data base in azimuth order. The new surveillance and weather data stored on the SBC data memory board is used later by SBC processor no. 3 A4A211 for output purposes.

2.3.2.1.3 Surveillance and Weather Video Output. See figure 11-27. The local display processor produces the video for the maintenance display. The video output is selected for the maintenance display by pushbutton switches on the maintenance display video control box. The video control box enables the distribution control board to pass the desired surveillance and weather video to the maintenance display for viewing. The surveillance and weather output generation for local display processor A4 is controlled by SBC processor no. 3 A4A211. The SBC processor no. 3 reads and processes the surveillance and weather data that was formatted and stored in SBC data memory board A4A208 by SBC processor no. 1.

2.3.2.1.3.1 Surveillance Video. See figure 11-27. The surveillance data is sent to video output board A4A212, by SBC processor no. 3, every time a video pretrigger signal is encountered from general interface A4A201. The video output board arranges the surveillance data into beacon, correlated, uncorrelated, and mapped video types. The video output board then sends all four of the reconstituted surveillance video data outputs to the distribution control board.

* **2.3.2.1.3.2 Weather Video.** See figure 11-27. The weather data (including the WSP data, when
online) is sent to weather output A4A213, by SBC processor no. 3, every time the azimuth change *
pulse (ACP) trigger timing function determines that 16 ACPs have occurred. The weather output board reconstitutes the weather data, and determines the level of weather that is currently available as input. The reconstituted weather data is then sent to the distribution control board along with the weather status lines. The output data processing is done via multibus 2.

2.3.2.1.4 Video Distribution and Control. See figure 11-27. The amplification and distribution of the reconstituted surveillance and weather data is controlled by the distribution control board. The surveillance and weather video, selected by the maintenance display video control box, is amplified and sent out to the maintenance display. The azimuth reference pulse (ARP), ACP, and video pretrigger timing signals from the general interface board are also amplified and distributed to the maintenance display for timing purposes. The distribution control board also lights video status lamps on the maintenance display video control box.

2.3.2.1.5 BIT/FIT. See figure 11-27. The built–in test (BIT) circuitry is designed to provide SBC processor no. 1 A4A202 and SBC processor no. 3 A4A211 the ability to verify the operation of the boards they control to the maximum possible degree. This is possible through special BIT circuitry on each board. To verify the operation of the two SBC processors, each processor must periodically reset a watchdog timer located on general interface A4A201. If the processor fails

in paragraph 2.3.2.6.3.3, except SBC processor no. 1 controls the testing and lights the fault lamp through the FLTLED/ signal from the fault LED output logic on the general interface board. Refer to figure 11-28, sheet 5. SBC processor no. 1 performs additional tests on the timer, EEPROM, and PROM logic located on the general interface board. The control signals 1IORC/, for reading data, and 1IOWC/, for writing data, along with address signals 1ADR02/ through 1ADR05/ on multibus 1 enable SBC processor no. 1 to read from and write to the general interface board, via the bus decoder logic, to perform verification. SBC processor no. 1 also stores and maintains the fault status list for all testing procedures. The results of the test data are stored on SBC data memory. If SBC processor no. 1 detects a fault in any of the local display processor functions, a summary fault SUMFLT/ signal is sent to system control via the general interface board. If a fault has occurred in the communication links, a communications fault COMMFLT/ signal is sent to system control via the general interface board. The fault signals are used by system control to report display processor status to remote monitoring subsystem.

2.3.2.6.3.5 Video Output and Weather Output Board BIT. Refer to figure 11-28, sheets 8 and 9. BIT procedures for video output A4A212 and weather output A4A213 are the same. The testing procedure is controlled by SBC processor no. 3. The BIT is performed in two ways. The first way involves on–line testing that will not disturb any actual surveillance and weather video output. The selected surveillance video SURTSTVID- signal from the video output board, weather video WXVDST0 through WXVDST2 signals internal to the weather output board, or beacon video BCNTSTVID- signal from the video output board, is sent to the BIT logic on the weather output board.

2.3.2.6.3.5.1 Watchdog Timer. The watchdog timer in the BIT logic begins counting when a PRT timing signal is encountered from the general interface board. The counter stops when the first pulse is encountered on the selected test video. The time is measured between the pretrigger and the occurrence of a known video, which verifies the existence of the video and the timing of the video signal. The control lines 2IORC/, for reading data, and 2IOWC/, for writing data, and address lines 2ADR01/ through 2ADR05/, 2ADR12/, and 2ADR13/ from multi–bus no. 2 to the bus decoder logic on the weather output board enables the on–line BIT test for the weather output and video output boards. The BIT test is software–controlled by SBC processor no. 3.

2.3.2.6.3.5.2 Read After Write Verification. The second way BIT is performed involves read–after–write verification performed by SBC processor no. 3 at power turn–on. SBC processor no. 3 writes to each board, then reads the data back to verify the input/output operation of the board under test. Control lines 2IORC/, for reading data, and 2IOWC/, for writing data, and address lines 2ADR01/ through 2ADR05/ from multi–bus no. 2 to the bus decoder logic on the board under test enables the read–after–write BIT test for the weather output and video output boards. The BIT test is software–controlled by SBC processor no. 3. If the video output board or the weather output board fail either test, the general interface board lights a fault indication lamp located on the defective board using the FLTLED08/ signal to the video output board and the FLTLED09/ signal to the weather output board. These signals go low to light the associated fault lamps. Most failures on the video output and weather output boards cause no video, video all the time, or video in the wrong place.

2.3.3 Local System Control

The local system control provides for the transfer of target, beacon, and weather data from the local ASR-9 radar site to the remote site via modems. Figure 11-30 provides a block diagram overview of the local system control and shows the functional relationship of all assemblies and major components. Figure 11-31 is a signal flow diagram which shows assembly interconnections.

2.3.3.1 Introduction. See figure 11-30. The local system control, located in Weather Receiver/Surveillance and Communications Interface Processor (SCIP) Unit 4, processes input/output data for the surveillance and weather data transmission and distribution circuits. The local system control consists of microcomputer–based processing, interface circuits, and a local system control panel. The local system control provides a communication link to supply system operational configuration data entered at the RMS terminal and system control panels (remote, local) to the ASR-9 system functions. The local system control also receives periodic status messages from the target receiver/processor and six–level weather processor and uses the information to control the flow of surveillance and weather messages to the local data communication facility. The local system control supports the following data and control selections:

1. Target receiver/processor channel A or B as the source of surveillance data and two–level weather data.
2. * Weather receiver/processor or the WSP as the source of six–level weather data. *
3. Control of the ASR-9 Radar System by the local system control panel, remote system control panel, or remote monitoring subsystem.

2.3.3.1.1 System Control Panels. The channel or data source selected is controlled by the operator at the local system control panel or the remote system control panel. Three independent serial streams of surveillance data from the selected target receiver/processor channel are organized into word fields and messages. See figure 2-54. A word field is composed of up to 12 data bits plus one odd parity bit, for a total of 13 bits. The parity bit is the last bit transmitted in each word field. A message is a combination of serially transmitted word fields. Depending on the type of message, there can be 4, 7, 10, or 32 word fields in a message. Word fields in a message are received in order, that is, word field one is first followed by word field two, word field three, etc.

2.3.3.1.2 Idle Character Words. Idle characters are received at least once between each message and, in the absence of messages, are received continuously. Idle character words consist of 3 binary 0s followed by 10 binary 1s, and employ even parity to distinguish them from word fields. The local system control looks for idle character words to establish word and message synchronization. Surveillance messages contain position information associated with aircraft or test targets. The local system control routes the surveillance messages to the local data communications facility.

2.3.3.1.3 Weather Data Streams. Three two–level weather serial data streams are received from * the selected target receiver/processor, WSP system and one six–level weather serial data stream is * received from the weather receiver/processor. The data rates are 9600 bits per second. A weather message consists of 32 13–bit word fields. The receiver/processors transmit at least one idle pattern between each message. The local system control routes the weather messages to the local data communications facility.

2.3.3.1.4 Status Messages. Status messages, consisting of four 13–bit fields, are received from * the WSP, target receiver/processor and the weather receiver/processor. The status messages, * received periodically and whenever a change in status occurs, provide system configuration and summary fault alarms of the ASR-9 Radar System to the local system control. The local system control converts the status messages into signals which control the flow of surveillance and weather messages to the local data communications facility.

2.3.3.1.7 Interface Generator Board. The RS-449 interface generator board A4A209 is used to terminate any unused modem signals to comply with the RS-449 protocol. The RS-449 interface generator also provides a common ground point for the unit 12 and 13 modems. Termination is provided using 47 ohm resistors tied to +5 volts dc.

2.3.3.1.8 Waveguide Switch Positions. The local system control interface No. 1 board develops the TXAON-/OFF(+/-) and TXBON-/OFF(+/-) signals that are routed through the receiver/processor backplanes. These signals determine waveguide switch positions.

2.3.3.2 Hardware Description. To accomplish the above operations, the local system control contains system control panel A1, local panel interface A4A219, Single Board Computer (SBC) processor A4A218, system control interface no. 1 A4A216, system control interface no. 2 A4A215, system control interface no. 2 A4A217, and System Timing Unit (STU) trigger amplifier. The relationships between these hardware components are shown in the hardware block diagram figure 11-30. The system control multibus interconnects data, address, and control lines to the local SBC processor, local panel interface, and system control interface no. 1. A signal flow diagram of the local system control is shown in figure 11-31. The hardware block diagram provides a quick reference overview of the assemblies and major components that make up the local system control. The signal flow diagram shows signal development, flow details and provides assembly interconnection details.

2.3.3.2.1 SBC Processor. The desired ASR-9 Radar System configuration is established by the operator at the system control panel and instructions executed by the local SBC processor. In general, switch settings established at the system control panel are routed to the local panel interface. The local single board computer (SBC) processor addresses the local panel interface and loads the switch settings into its internal storage area, validates the switch settings, and executes the desired operations by addressing system control interface no. 1. System control interface no. 1, in turn, controls the operation of system control interface no. 2 and the STU trigger amplifier.

2.3.3.2.2 SBC Processor Instructions. The instructions executed by the local SBC processor perform the following operations:

1. Transfers program data from system control interface no. 1 to the local SBC processor.
2. Transfers ASR-9 Radar System configuration switch settings, established by the operator at the system control panel, from the local panel interface to the local SBC processor.
3. Displays system configuration switch settings on the system control panel.
4. * Transfers the status of channels A and B target receiver/processors, WSP and the antenna control function to the local SBC processor.
5. Displays system and WSP status on the system control panel. *
6. Defines the operational characteristics and checks the status of a timer (baud rate generator) located in system control interface no. 1.
7. Defines the operational characteristics and checks the status of Correlation and Interpolation (C and I) processor serial ports located in system control interface no. 1.
8. Defines the operational characteristics and checks the status of weather processor serial ports located in system control interface no. 1.

9. Defines the operational characteristics and checks the status of Automatic Network Supervisor (ANS) wrap test serial ports located in system control interface no. 1.

10. Transfers surveillance, two–level weather, and control data from channels A and B target receiver/processors to the local SBC processor.

2.3.3.2.3 I/O Instructions. Each of the above operations is accomplished by execution of read or write (I/O) instructions by the local SBC processor. Each I/O instruction identifies the I/O device (local panel interface or system control interface no. 1) which shall participate in the I/O operation and whether I/O operation is a read (I/O device to local SBC processor) operation or a write (local SBC processor to I/O device) operation. The following paragraphs describe how the local system control accomplishes the above operations.

2.3.3.3 System Control Interface No. 1 Data Transfer. See figure 11-31, sheet 5. The instructions which specify the operations performed by the local SBC processor reside in a program PROM logic located in system control interface no. 1. In order to perform an I/O operation which involves system control interface no. 1, the local SBC processor must load the instructions stored in the program PROM logic into its internal random access memory (RAM). To accomplish this operation, the local SBC processor first resets a PROM address counter and presets a PROM clock generator by executing a write to address $0D0C_{16}$ instruction. The PROM address counter and PROM clock generator are both located in the program PROM logic. This instruction is specified by a low bus high enable (3BHEN/) signal, low input output write command (3IOWC/) signal, a high input output read command (IORC/) signal, and the following address bit 00 through 11 (3ADR00/ through 3ADR11/) binary bit configuration:

ADR11/	ADR10/	ADR09/	ADR08/	ADR07/	ADR06/	ADR05/	ADR04/	ADR03/	ADR02/	ADR01/	ADR00/
0	0	1	0	1	1	1	1	0	0	1	1

2.3.3.3.1 Logic Levels. The logic level of signal 3BHEN/ and the binary value of address bit 3ADR00/ control local SBC processor data transfers in accordance with the following rules:

3ADR00/	BHEN/	Function
1	0	Word transfer of data bits 3DAT00/ through 3DAT15/ on the system control multibus.
0	0	Byte transfer of data bits 3DAT00/ through 3DAT08/ on upper half of the system control multibus.
1	1	Byte transfer of data bits 3DAT00/ through 3DAT07/ on lower half of the system control multibus.
0	1	Reserved

7. Total CPC messages received by the SCIP. This is intended to help with situations where alarm 861 is being declared by Local System Control.

8. Total unidentifiable messages received by the SCIP.

IMPORTANT: Since the purpose of these performance counts is to support investigation of intermittent communication channel problems, all information displayed is **accumulative in nature**. The information is not updated every northmark, like those of the post processor. Instead, these counters will increment indefinitely, until the SCIP resets, or the counters are cleared to zero by manual command. Therefore, checks spanning minutes, hours, or even days will be possible.

CAUTION

Certain normal system events can be expected to create a very brief burst of error declarations at the SCIP. This behavior is strictly transitory in nature, disappearing after the system event is over. Examples of these transitory bursts of error declarations follow. Be are that the numbers listed below are based on early test results. Due to the variety of communications equipment currently in use, variations may be experienced from site to site.

1. When a post processor switch is performed, the "no sync" counter for each surveillance channel can be expected to increase by approximately 10. If two level weather is online, the "no sync" counter for the weather channel can be expected to increase by approximately 15.

2. When a weather source switch is performed at the maintenance display, the "no sync" counter for the weather channel can be expected to increase by approximately 15.

NOTE

On occasion, no errors might be observed. The reason is the weather channel's data load is not evenly distributed (6 scan interval between map updates).

3. When the SCIP runs FIT, the "other" counters can be expected to increase by approximately 10 for all channels but the spare, which does not exist for the local SCIP. This will also happen as a result of power up initialization.

When interpreting the performance counts, other sources of information must be taken into account, especially the alarm buffer in RMS. These performance counts are intended to complement, not replace the other sources of information.

3.2.3.7.4 Command Key. To reset all of the above performance counts to zero, enter the command key C (hit the C key). This command separates the results of upcoming events with those corresponding to previous events. This command is necessary because the performance counts displayed by the P command are not updated every north mark. If an intermittent communication problem is suspected, this command should be used first.

3.2.3.8 Terminating the Session. To terminate the session at any point, simultaneously hit the control key and the E key. This will end the current session and produce the terminating message:

SCIP PARAMETER UPDATE PROGRAM ABORT. . .

. . . ENTER CONTROL-D TO RESTART

All parameter values are then set to the most recent values stored in NVRAM. A new session may be started by simultaneously hitting the control key and the D key.

3.2.3.9 Terminal Turn–Off Procedure. To turn off the display unit press the bottom half of the ON/OFF switch. The display unit should then power down and the screen should go dark.

* **3.2.3.10. Clear Day Map and Weather Threshold Generation.** Clear Day Maps (CDMs) reduces non-weather clutter in weather detection. Maps are generated and loaded during site installation. However, conditions, such as a change in seasons or new building or road construction, may arise that necessitate the modification of the existing map. Use the procedure in paragraph 3.2.3.10.1 to build the 6 weather threshold tables when the WSP is installed. A subsequent ASR9 software change (9PAC phase II) should eliminate this step, but for now it is necessary to insure the thresholds for the different levels are correct. Use the procedure in paragraph 3.2.3.10.2 to generate a CDM when the WSP is installed.

3.2.3.10.1 Creating New Weather Thresholds

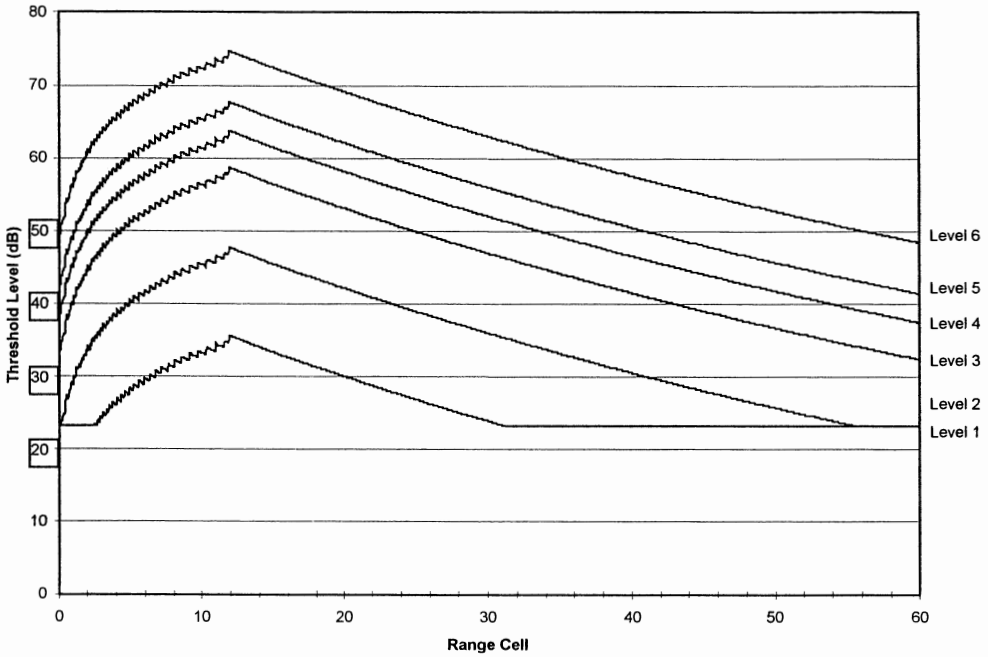
NOTE

Load New Weather Threshold Values

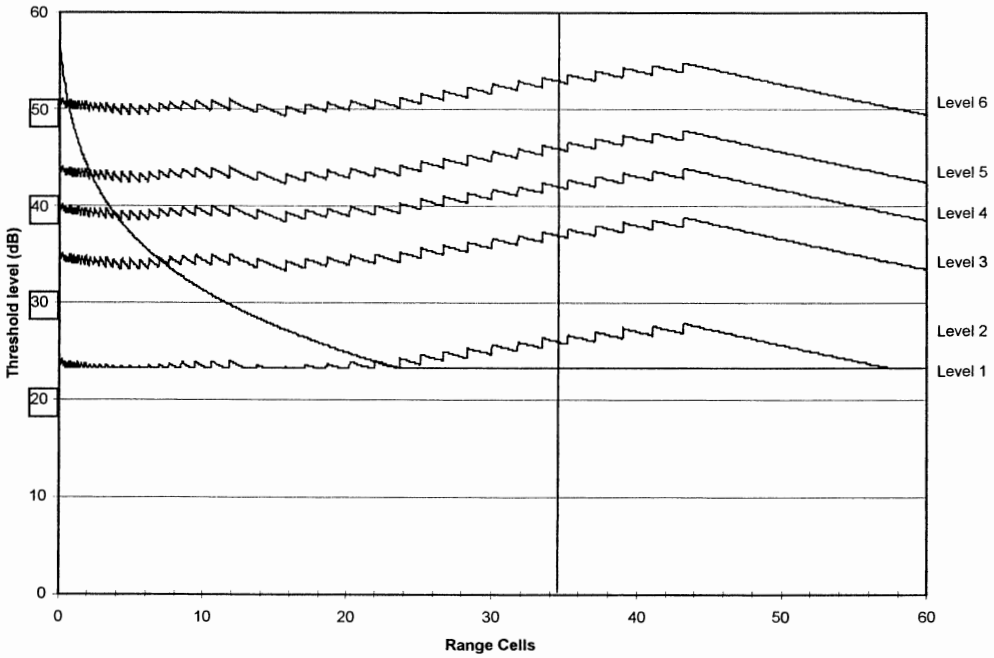
Weather Thresholds values are both calculated and stored on the Data Collect Select board when the RMS loads them. Threshold calculations come from the ASR9 range, STC values, High Low Beam crossing, storms vertical structure, and system characteristics. ASR9 baseline vertical reflectivity profiles are flat for 0-4 km altitude and fall off at 3 db/km above this altitude. For storms not following this model we may need to make additional threshold adjustments, depending on the radars location. The following graphs illustrate the values of the thresholds for a baseline ASR9 with WSP modifications. *

*

b - Linear High Beam (U35-U25)



c - Circular Low Beam (U36-U26)



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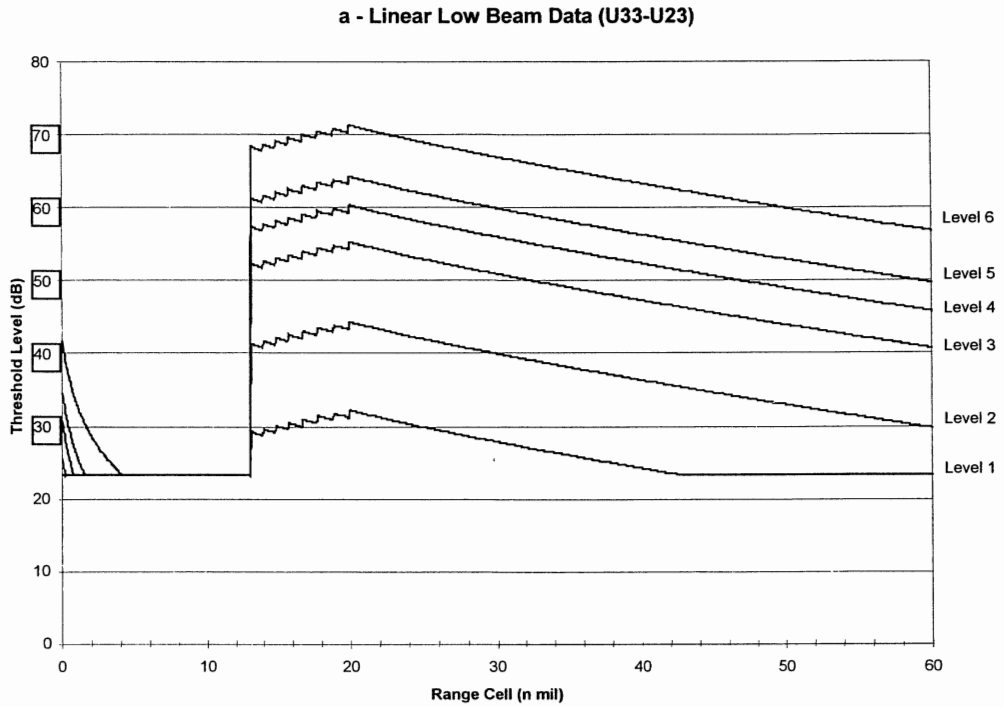
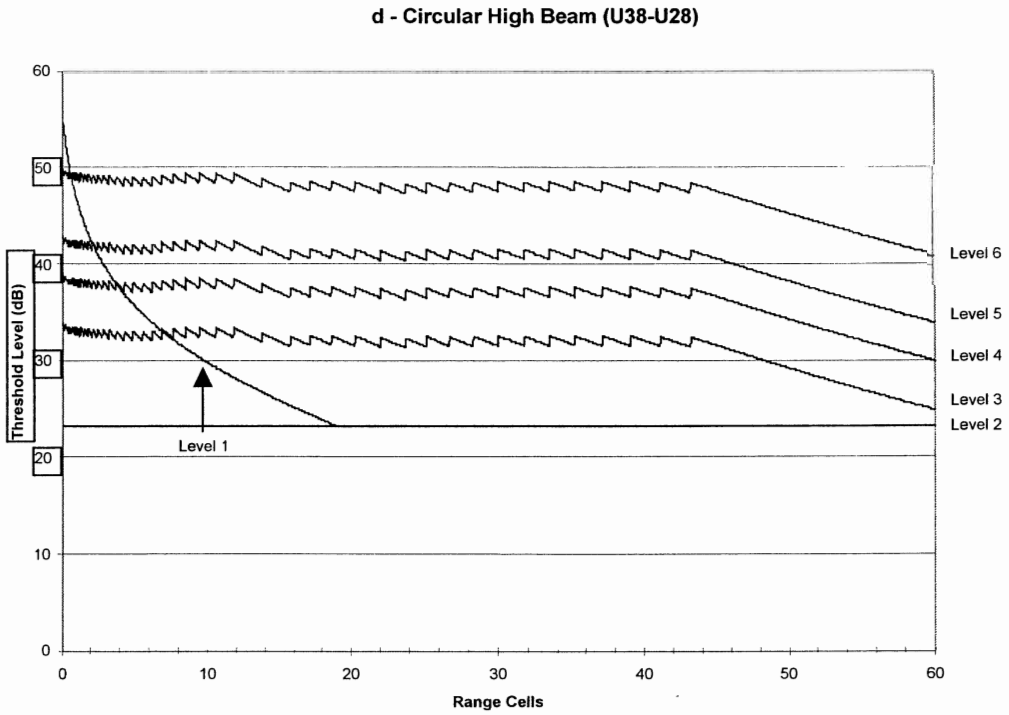




The WSP SSM-012 modifications changed the waveguide path of the radar return signals and added to the differences between the ASR9 receive path signals. The idea is to adjust for the *

* radar return signal strength differences by changing the weather thresholds in order to compensate for the receive paths differences, and in turn normalize the output weather display. It is not possible to directly adjust the weather threshold values when they are individually calculated then stored on the Data Collect Select EEPROM U20 and U30 during the load weather threshold procedure. That is, the RMS computer calculates (960 range cells * 6 levels * 6 modes (CHA_HI, CHA_LO, CHB_HI, CHB_LO, CIRCULAR) or 34560 values during the weather threshold load procedure. Therefore new Weather thresholds can only be obtained by changing the VSP values employed in their calculations.

PROCEDURE FOR CREATING NEW WEATHER THRESHOLD:

1. Place each Target Channel in turn to unavailable and perform the following:

   a. Access the SYNCHRONIZER-GENERAL menu (0.5.3.1.5). The baseline WSP value for VSP 1501 (Lo Beam STC Reference Attenuation) is **82**. Set this VSP to a value of **85.**

   b. Access the SYNCHRONIZER-GENERAL menu (0.5.3.1.6). Record the current value of VSP 1601 (Hi Beam STC Reference Attenuation); and set it to a value of **77.**

   c. Access the 6WX GENERAL PARAMETERS (0.5.3.6.5). Record the current value of VSP 6401 (Hi Beam STC Reference Attenuation); and set it to a value of **58** minus (old weather 645A791 cable length multiplied by 0.026 db/foot.).

   d. Remove all isolated windows by setting them to low beam

      VSP1205 (window1)
      VSP1210 (window2)
      VSP 1305 (window3)
      VSP 1310 (window4)

   e. Set the HI/LO Beam crossing at 14 nmi for both target channels and the 6weather channel. That is, it is not clear why the circular polarization weather channel high/low beam crossing was originally set at 32 nmi. The high beam underside -3db coverage chart is at 7000 ft. when the VSP is set at 32 nmi. The experience of the WSP team showed storms over hilly terrain (eg. Knoxville, Portland) sites exhibited a lack of detections for the lower level weather products between ranges 20 to 32 nmi. The 14nmi. Setting will be the baseline setting for all the WSP sites.

   f. Record the changes to the VSPs on Table 3.18.1 .

2. Place the 6WX channel in unavailable mode and perform the following:

   a. Access the VSP CATEGORIES menu (0.5.3); enter <9> <RET> to load the six-level weather threshold tables.

   b. Take the 6WX channel out of unavailable mode.

   c. Put 6WX online.

3. Place target channel A in unavailable mode and perform the following:

   a. Access the VSP CATEGORIES menu (0.5.3), enter <8> <RET> to load the two-level weather threshold tables. *

* b. Take target channel A out of unavailable mode.

4. Place target channel B in unavailable mode and perform the following:

   a. Access the VSP CATEGORIES menu (0.5.3), enter <8> <RET> to load the two-level weather threshold tables.

   b. Take target channel B out of unavailable mode.

5. Return all VSPs to baseline values after all the Weather Thresholds are loaded. In the future these VSPs must be modified any time the Weather Thresholds are loaded. Never use these VSPs other than when loading the Weather Thresholds. The baseline WSP VSPs must be used any time the system is placed in operation.

6. Please double check and make sure all VSPs are returned to baseline WSP values except the Weather Beam Select Rag Windows new baseline is 14nmi. For VSPs6109-6116. The ASR9 manuals do not have a procedure for loading the weather thresholds, and this needs to be done anytime a Data Collect Select board is replaced in the WSP configuration. In the future we will work with the RMS software to try to automat this procedure, but for now this manual procedure is all we can do to get the correct weather thresholds.

Table 3.18.1

Setup for Loading the Weather Threshold						
VSP	Channel A		Channel B		6WX	
STC	baseline	Record Adjusted	baseline	Record Adjusted	Baseline Old/New	Record Adjusted
1501	82	85	82	85		
1601	74	77	74	77		
Target Channels Beam Select Isolated Window						
1205	Opt	0	Opt	0		
1210	Opt	0	Opt	0		
1305	Opt	0	Opt	0		
1310	Opt	0	Opt	0		
Weather Channel STC						
6401					61	58
Weather Channel Beam Select Rag Window						
6109					32/14	14
6110					32/14	14
6111					32/14	14
6112					32/14	14
6113					32/14	14
6114					32/14	14
6116					32/14	14

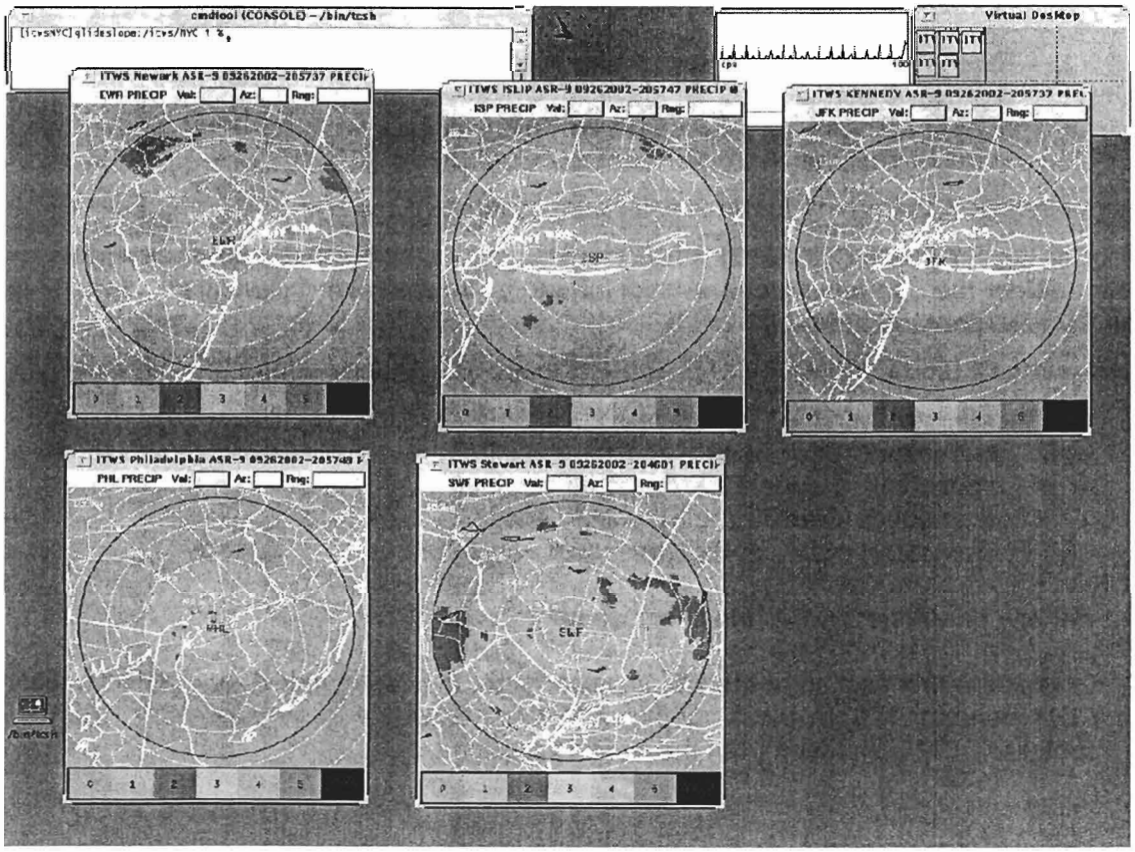
*

* **3.2.3.10.2. Creating a New Clear Day Map @ WSP Sites.**

7. Verify all VSPs are at the WSP baseline settings.

NOTE

The WSP uses a unique clutter map for every mode of the ASR9. But only one Clear Day Map exists for all ASR9 beams, channels, and polarization modes because memory was expensive when the old Six Level Weather Processor was developed. Unfortunately the map algorithm does not average the input data; it can only add to the previous map input sums, therefore it is not possible to reduce a map bias. Specifically, if one return signal such as the Weather Channel Circular Polarization mode yields stronger clutter returns, the map will be bias up for this mode, and this results in excessive filtering of the linear polarization returns. Therefore all signals going to the CDM processes must be nearly equivalent or a bias will be set in the CDM. The end effect will be a selection of an overly aggressive filter for all modes but the strongest one, and a weather presentation that underreports the storms in most cases. The WSP waveguide modifications make this problem worse but it still exists in the baseline ASR9. The following images demonstrate the ability of the ASR9 system to display the same storm with different results for five different ASR9 systems. The calibration differences account for much of the product differences.



*

* A new map should only be generated when no significant storm activity is present or forecasted for the entire radar surveillance area. However, should some storm activity occur during the clear day map generation process, all is not lost. It may be possible to edit out the offending data using the CDM update procedure in paragraph 3.3.2.6.3.2. Schedule downtime for CDM data collection for a minimum of two 2-hour sessions. Collect data four times in each session (once for each combination of linear polarization, circular polarization, channel A online, and channel B online). Spread the data collection sessions throughout the day for a more representative map. The system may be returned to normal operation between data collection session

Both two-level and six-level maps are generated simultaneously, but they are loaded into the system separately. The preconditions for generating CDMs are: (1) only the local RMS terminal is used, (2) it must have system control, and (3) manual antenna polarization must be selected. To collect two-level (2WX) and six-level (6WX) weather data proceed as follows:

8. Repeat steps 7 through 14 for each 2-hour session.

NOTE

At least two sessions are recommended; one session should be in the morning when the typical morning inversion period is present. A second session should be in the afternoon during a typical sunny day. A third session should be scheduled at any other time at which unusual, yet typical, clutter environments are present.

9. Each session consists of collecting data for 2 hours. The data collection for each session is broken down into 4 half-hour sections as follows:

½ hour - Channel A online, Linear Polarization
½ hour - Channel B online, Linear Polarization
½ hour - Channel B online, Circular Polarization
½ hour - Channel A online, Circular Polarization

10. Repeat steps 7 through 11 for each half-hour section.

11. Access the SYSTEM CONTROL PANEL menu (0.1.1). Verify that manual polarization is selected. Select the appropriate online channel and polarization for this section. Switch high voltage on in the online channel.

12 Access the CLEAR DAY MAP GENERATION menu (0.5.4) and perform the following:

a. The "modification window" parameters should be set to include all of space. That is:
parameter 3 (Start Range) should equal 0
parameter 4 (Range Extent) should equal 60
parameter 5 (Start Azimuth)) should equal 0
parameter 6 (Azimuth Extent) should equal 256

Set any parameters not at these values appropriately.

b. If this is the first section of the first session, enter the command <14> <RET> to initiate CDM generation from blank maps; otherwise, enter the command <13> <RET> to continue CDM generation from the existing scratch maps.

*

* c. Wait 30 minutes for the current half-hour section period to elapse. While you are waiting, observe the CDM generation activity on the maintenance display's group 2 six-level weather output. The CDM generation process follows a repeated pattern:

(1) About 7 seven scans with 6WX filter 0 selected. Observe large amounts of ground clutter.

(2) About 7 seven scans with 6WX filter 1 selected. Observe somewhat less amounts of ground clutter than during filter 0.

(3) About 7 seven scans with 6WX filter 2 selected. Observe somewhat less amounts of ground clutter than during filter 1.

(4) About 7 seven scans with 6WX filter 3 selected. Observe even less amounts of ground clutter than during filter 2.

(5) About 7 seven scans with 6WX in normal operating mode. At this time, 2WX CDM is being generated. Observe no six-level weather detections during this period. If any weather detections are seen, verify that the indications are ground clutter and that real weather has not moved into the area.

(6) If you are having trouble seeing this pattern, the 6-LEVEL WEATHER DETECTION PERFORMANCE menu (0.3.2.6) may help.

13. After the 30 minute period has elapsed, from the CDM GENERATION menu (0.5.4), enter the command <15> <RET> to terminate CDM generation.

14. The RMS will now display the number of "30 scan sequences" completed. If there was no live weather activity within the 60-nautical mile radius of the radar, write the new CDM data to the scratch area of the VSP disk as follows:

a. Enter <1> <RET> to write the two-level CDM.

b. Enter <3> <RET> to write the six-level CDM.

15. If data is suspect, use the purge commands <2> and <4> to discard the collected data.

16. If more data collection is required for this session, then reconfigure the system for the next data collection section and then repeat steps 7 through 11.

17. When normal system operation is resumed, place the 6WX channel in unavailable mode and perform the following:

a. If the new 6WX CDM is to be loaded into the weather channel, access the CHANNEL, GEO-CENSOR AND CDM LOADS menu (0.5.5); enter <7> <RET> to download the new 6WX clear day map.

b. Take the 6WX channel out of unavailable mode.

c. Put 6WX online.

18. Place target channel A in unavailable mode and perform the following:

a. If the new 2WX CDM is to be loaded into the target channel A, access the CHANNEL, GEO-CENSOR AND CDM LOADS menu (0.5.5); enter <6> <RET> to download the new 2WX clear day map.

b. Take target channel A out of unavailable mode.

c. Put target channel A online.

19. Place target channel B in unavailable mode and perform the following: *

*

a. If the new 2WX CDM is to be loaded into the target channel B, access the CHANNEL, GEO-CENSOR AND CDM LOADS menu (0.5.5); enter <6> <RET> to download the new 2WX clear day map.

b. Take target channel B out of unavailable mode.

20. Access SYSTEM CONTROL PANEL menu (0.1.1) and restore normal operating conditions.

21. Now that the new maps have been loaded into the system, access the READBACK PARAMETERS FOR CLEAR DAY MAPS menu (0.6.8) and perform the following:

NOTE

A TRACS PROCOMM script file exist that automates the following steps.

WSP Sites should examine Level 1 and Level 2 Maps for excessive Thresholding.

a. Each clear day map is read back in 16 CPI-pair wide pieces. Enter the necessary commands to readback each piece of each map.

b. As each piece is displayed, use the <PRINT SCREEN> function key to make a hardcopy print out.

c. Inspect the maps for any signs of real weather, atypical anomalous propagation, or interference. Use the procedure in paragraph 3.3.2.6.3.2 to remove these unwanted cells.

*

3. Open weather i–f panel assembly door.

4. See figure 11-46. At faulty OR circuit assembly (A9A1 or A9A2), remove mounting hardware from OR circuit cover plate and remove cover plate.

5. Disconnect cables from OR circuit assembly case.

6. Remove mounting hardware securing OR circuit assembly to component panel A9 and remove assembly.

7. Place OR circuit assembly insulator between OR circuit assembly case and component panel A9 and secure with original mounting hardware.

8. Connect cables to OR circuit assembly connectors.

9. Secure circuit cover plate to component panel A9 with original mounting hardware.

10. At multivoltage power supply PS1, perform the following:

    a. See figure 11-38, sheet 2. Switch MAIN POWER circuit breaker CB1 to on (up) position.

    b. At voltage selector switch S1, select each switch setting and verify that indication on front panel meter M1 is within power supply adjustment card tolerance value for corresponding module(s). If module value(s) are not within power supply adjustment card tolerance values, perform alignment procedure for required module(s) as indicated in table 6-1.

    c. Switch BATTERY ON/OFF toggle switch S2 to ON position.

11. At RMS terminal, access SYSTEM CONTROL PANEL menu (0.1.1) and restore high voltage to both transmitters.

12. At RMS terminal, access ANS MONITOR AND CONTROL menu (0.1.4) and restore modem links.

7.5.8.3 Operation Verification. The following instructions describe how to check OR circuit assemblies A9A1 and A9A2 after installation. Proceed as follows:

1. See figure 11-36. At rear of weather receiver/SCIP cabinet, remove rear panel.

2. See figure 11-46. At assembly to be checked (A9A1 or A9A2), remove hardware securing OR circuit assembly cover.

3. At OR circuit assembly, connect positive lead of multimeter to OR circuit assembly case and negative lead to component panel A9 chassis.

4. Verify that multimeter reads between 5.3 and 5.0 volts.

5. Connect negative lead of multimeter to OR circuit assembly case, and connect positive lead to anodes of each of three diodes (CR1, CR2, and CR3) of OR circuit assembly. The voltage drop between reading attained in step 3 and reading at anode of each diode must be between 0.3 volt and 0.5 volt, and all anode voltages must be within 20 millivolts of each other.

6. Secure OR circuit assembly cover with original mounting hardware.
7. At weather receiver/SCIP cabinet, replace rear panel.

* **7.5.9 Sigmet I.F. Digitizer A12A1.** The following instructions describe how to remove I.F. Digitizer A12A1 from the Weather Receiver/SCIP cabinet and how to install a replacement unit. I.F. Digitizer A12A1 is located on the right inside wall of the Weather Receiver/SCIP cabinet. The I.F. Digitizer is accessible through the back panel of Unit 4. See figure 11-36.

7.5.9.1 Equipment Required. The following equipment is required:

Name	Quantity
Torque Wrench	1
Screwdriver Set	1

7.5.9.2 Removal and Installation Procedure. Proceed as follows:

1. At Weather Receiver/SCIP (Unit 4) cabinet system control panel A1, verify that Weather 2-LEVEL indicator is lit.
2. See Figure 11-9 of TI 6310.27. Disconnect AC Cord from A19 J4 in the RMS cabinet Unit 3, accessible through rear panel of Unit 3. (Note that turning off the cabinet breaker does not insure that power is off at A19 J4.
3. Disconnect all external wires and cables to I.F. Digitizer A12A1.
4. Remove hold-down screws at left and right sides of I.F. Digitizer A12A1 and remove from Weather Receiver/SCIP cabinet wall.
5. Hold replacement I.F. Digitizer A12A1 in position against Weather Receiver/SCIP cabinet inner wall and secure with hold-down screws at left and right sides of I.F. Digitizer A12A1.
6. Connect all external wiring and cables to I.F. Digitizer A12A1.
7. Connect AC power cord to A19 J4 in the RMS Unit 3. *

7.6 REPAIR PROCEDURES

The following paragraphs provide step–by–step procedures for equipment repair tasks that must be performed in the field.

7.6.1 System Control Panel A1 Bulb Replacement

The following instructions describe how to remove a bulb from system control panel A1, and how to install a replacement bulb.

7.6.1.1 Equipment Required. No equipment is required.

7.6.1.2 Removal and Installation Procedure. Proceed as follows:

1. See figure 11-47. At either control panel, grasp bulb cover firmly and pull from panel.
2. Pull bulb extractor corresponding to defective bulb forward to extract bulb from socket.
3. Push extractor back into place and insert replacement bulb into socket.
4. Push bulb cover back into place.

7.6.2 Multivoltage Power Supply PS1

In general, the repair of multivoltage power supply PS1 involves removal and replacement of defective plug–in modules, or removal and replacement of a defective battery, or the investigation of faults not attributable to those items. Figure 11-53 is an overall schematic diagram of the supply, figure 11-54 is a schematic diagram of the mother board, and figure 11-55 is a schematic diagram of the battery charger. Figures 11-53 and 11-54 are to be used to investigate non–module or non–battery problems. Since the replaceable modules are designated for repair at the CRF/depot level, schematic diagrams for each of them are located in the field/CRF/depot maintenance schematic diagrams book, TI 6310.38. Each module output is monitored via Remote Monitor Subsystem; hence, defective modules are usually detected automatically. Paragraph 7.6.2.2 describes how to remove a defective module and install a replacement. The scheduled battery capacity check described in paragraph 6.3.1 will detect an exhausted battery. Paragraph 7.6.3 describes how to remove a defective battery and install a replacement.

7.6.2.1 Equipment Required. The following equipment is required:

Name	Quantity
Adjustment Tool	1
Screwdriver Set	1

7.6.2.2 Removal and Installation Procedure. Proceed as follows:

WARNING

System disruption will occur when high voltage is removed from both transmitters.

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PARTS LIST

REF DES	I N	NAME OF PART/DESCRIPTION	MFR CODE NO.	JAN/MIL MFR. PART. NO	NOTES
N1	C	REDISTRIBUTION PANEL ASSEMBLY (NOTE - SOME PANELS HAVE 2 JUMPER WIRES AS FOLLOWS: FROM J1-05 TO J6-19; FROM J1-09 TO J6-20)	97942	1D21692G01	
4					
A9	B	COMPONENT PANEL ASSEMBLY	97942	1D25977G01	
4A9					
A1	C	RECTIFIER ASSEMBLY	97942	1A20642H01	
A2	C	SAME AS 4A9A1			
4A9					
CR1	C	SEMICONDUCTOR DEVICE, POWER SCHOTTKY RECTIFIER, PRV 45, VF 0.68MA, IO 22.5A AT TC-125C, IR 40MA, PEAK SURGE CURRENT 600A, MIL-S-19500-553	81349	JANTX1N6391	
J1	C	ADAPTER, CONNECTOR, ELECTRICAL, MALE/FEMALE, RFI FILTER CONTACTS, SHELL SIZE 1, MFR PN 859730-7, MFR CODE 00779	97942	645A826H01	
TB1	C	TERMINAL BOARD, MOLDED, BARRIER SCREW TYPE, 4 TERMINALS, CLASS 38TB, 2.516IN. LONG, MIL-T-55164/2E.	81349	38TB4	
4					
A11	B	TERMINAL BOARD ASSEMBLY	97942	156C948G01	
4A11					
TB1	C	TERMINAL BOARD, MOLDED, BARRIER SCREW TYPE, 4 TERMINALS, CLASS 38TB, 2.516IN. LONG, MIL-T-55164/2E.	81349	38TB4	
4					
DS1	B	INDICATOR LIGHT	96312	249-7B41-0331-544	
DS2	B	LAMP ASSEMBLY	97942	1D23338G01	
* 4A12					
2051	E	SIGMENT IF DIGITIZER, WSP SITE SPARES	97942	7A11800H03	
2003	E	ASR-9 RF MOD KIT, WX PREINSTALLATION KIT	97942	7D11432G01	
2004	E	ASR-9 IF MOD KIT PREINSTALLATION KIT	97942	7D11433G01	
3002	E	SIGMENT IF DIGITIZER, ASR-9 IF MOD KIT	97942	7A11800H03	
3003	E	PREINSTALLATION CABLES, ASR-9 IF MOD KIT	97942	7A11790G08	
3004	E	PREINSTALLATION CABLES, ASR-9 IF MOD KIT	97942	7A11790G09	
3005	E	PREINSTALLATION, ASR-9 IF MOD KIT	97942	7A11725	
3006	E	SIGMET IF RCVR PANEL, ASR-9 IF MOD KIT	97942	ASR9-003.9.1	
3007	E	SIGMET IF RCVR, 115VAC C, ASR-9 IF MOD KIT	97942	ASR9-003.9.2	
3008	E	4A3A3 POWER SPLITTER BRACKET, ASR-9 IF MOD KIT	97942	ASR9-003.9.3	
3009	E	AMPLIFIER BRACKET, ASR-9 IF MOD KIT	97942	ASR9-003.9.5	
3010	E	RG141 BENDING TOOL, ASR-9 IF MOD KIT	26805	2098-5286-54	
3200	E	SCREW, PAN HEAD (.190-32)	96906	MS51958	
3204	E	POWER SPLITTER, ASR-9 IF MOD KIT	11869	HJ-22010	
3205	E	CASCADABLE RF AMPLIFIER, ASR-9 IF MOD KIT	97942	7A11820H01	

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PARTS LIST

REF DES	I N	NAME OF PART/DESCRIPTION	MFR CODE NO.	JAN/MIL MFR. PART. NO	NOTES
3206	E	SCREW, PAN HEAD (2-56UNC-2), ASR-9 IF MOD KIT	96906	MS51957-3	
3207	E	WASHER, FLAT NO.2, .089, ASR-9 IF MOD KIT	80205	NAS620C2	
3208	E	WASHER, LOCK SPRING, CR, ASR-9 IF MOD KIT	96906	MS35338-134	
3209	E	TERMINAL STRIP, 2 POSITION, ASR-9 IF MOD KIT	13150	77002-49	
3210	E	SCREW, PAN HEAD, .138-32X, ASR-9 IF MOD KIT	96906	MS51957-30	
3211	E	WASHER, LOCK SPRING, CR, ASR-9 IF MOD KIT	96906	MS35338-136	
3212	E	WASHER, FLAT, NO.6 (.1, ASR-9 IF MOD KIT	96906	MS15795-805	
3213	E	HOOK-UP WIRE, PVC INSULATED, ASR-9 IF MOD KIT	16428	9912-5	
3215	E	CABLE, POWER, ASR-9 IF MOD KIT	16428	17650	
3217	E	CLAMP, CABLE, NYLON, ASR-9 IF MOD KIT	6383	CCS31-S8-C	
3218	E	SCREW, PAN HEAD (.164-32), ASR-9 IF MOD KIT	96906	MS51957-43	
3219	E	WASHER, FLAT, ASR-9 IF MOD KIT	96906	MS15795-841	
3220	E	WASHER, LOCK-SPRING, CR , ASR-9 IF MOD KIT	96906	MS35338-137	
3224	E	FUSEHOLDER, INDICATING, ASR-9 IF MOD KIT	75915	344125A	
3225	E	FUSE, 1A, 3AG (LITTLE FUSE), ASR-9 IF MOD KIT	75915	312001	
3226	E	SCREW, ASR-9 IF MOD KIT	96906	MS51957-36	
3227	E	NUT, PLAIN, HEX (.138-32), ASR-9 IF MOD KIT	96906	MS35649-264	
3228	E	WASHER, FLAT. NO.6, ASR-9 IF MOD KIT	96906	MS15795-806	
3229	E	WASHER, PLASTIC (.149 DI), ASR-9 IF MOD KIT	96906	MS51859-15	
3230	E	HOOK-UP WIRE, PVC INSULATED, ASR-9 IF MOD KIT	16428	9921-2	
3231	E	HOOK-UP WIRE, PVC INSULATED, ASR-9 IF MOD KIT	16428	9921-10	
3232	E	HOOK-UP WIRE, PVC INSULATED, ASR-9 IF MOD KIT	16428	9918-10	
3236	E	SCREW. PAN HEAD (.112-40), ASR-9 IF MOD KIT	96906	MS51957-15	
3237	E	WASHER, LOCK-SPRING, CR, ASR-9 IF MOD KIT	96906	MS35338-135	
3238	E	WASHER, FLAT, .115ID x ??. ASR-9 IF MOD KIT	80205	NAS620C4	
3241	E	NUT, PLAIN, HEX (#8-32), ASR-9 IF MOD KIT	96906	MS35649-284	
3242	E	SCREW, PAN HEAD (.164-32), ASR-9 IF MOD KIT	96906	MS51957-45	
3243	E	TERMINAL LUG, ASR-9 IF MOD KIT	96906	MS25036-153	
3244	E	SCREW. PAN HEAD (.190), ASR-9 IF MOD KIT	96906	MS51958-63	
3245	E	TERMINAL LUG, ASR-9 IF MOD KIT	96906	MS25036-101	
3246	E	TERMINAL LUG, ASR-9 IF MOD KIT	96906	MS25036-108	
3247	E	WASHER, FL, (.219 DIA), ASR-9 IF MOD KIT	96906	MS15795-842	
3248	E	WASHER. LOCK SPRING, CR, ASR-9 IF MOD KIT	96906	MS35338-138	
3249	E	SPACER, NYLON, #10X, ASR-9 IF MOD KIT	55566	1225-10-N	
3300	E	ATTENUATOR, FIXED, 6DB, SM, ASR-9 IF MOD KIT	64671	18AH-06	
3301	E	ATTENUATOR, FIXED, 7DB, SM, ASR-9 IF MOD KIT	64671	18AH-07	
3302	E	ATTENUATOR, FIXED, 8DB, SM, ASR-9 IF MOD KIT	64671	18AH-08	
3303	E	ATTENUATOR, FIXED, 9DB, SM, ASR-9 IF MOD KIT	64671	18AH-09	
3304	E	ATTENUATOR, FIXED, 10DB, SM, ASR-9 IF MOD KIT	64671	18AH-10	
3305	E	ATTENUATOR, FIXED, 11DB, SM, ASR-9 IF MOD KIT	64671	18AH-11	
4DS2					
TB3	C	TERMINAL BOARD, MOLDED, BARRIER SCREW TYPE, 4 TERMINALS, CLASS 38TB, 2.5161N. LONG, MIL-T-55164/2E.	81349	38TB4	
ZZ1	C	LAMP, INCANDESCENT, CLEAR, 60 WATTS, 4.44 IN. H,	97942	330C766H11	

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PARTS LIST					
REF DES	I N	NAME OF PART/DESCRIPTION	MFR CODE NO.	JAN/MIL MFR. PART. NO	NOTES
		2.38 IN. W			
ZZ2	C	LAMPHOLDER, WATERTIGHT, USE WITH STD 115-120 VOLT LAMP, SOCKET RATING 600 VOLTS AND 600 WATTS MAX, 4.50 IN LEAD LENGTH	97942	138C575H01	
4					
J3	B	ADAPTER, CONNECTOR, 50 OHM COAXIAL, RADIO TERMINALS, CLASS 39TB, 6.625IN. LONG MIL-T-55164/3F	81349	M55339-28-30001	
J4	B	SAME AS 4J3			
N1	B	SYSTEM CONTROL PANEL	97942	1D17990G01	
N2	B	TERMINAL BOARD ASSEMBLY	97942	1D23362G01	
4N2					
TB1	C	TERMINAL BOARD, MOLDED, BARRIER SCREW TYPE, 10 TERMINALS, CLASS 39TB, 6.625IN. LONG, MIL-T-55164/3F.	81349	39TB10	
TB2	C	SAME AS 4N2TB1			
4					
N3	B	PANEL ASSEMBLY, CABINET BLOWER, FUSE	97942	1D23364G01	
4N3					
F1	C	FUSE, INSTRUMENT, POWER AND TELEPHONE (NONINDICATING), 125 VOLTS, 5 AMP, STYLE F03, MIL-F-15160-3	81349	F03B125V5A	
F2	C	SAME AS 4N3F1			
F3	C	SAME AS 4N3F1			
F4	C	FUSE, INSTRUMENT, POWER AND TELEPHONE (NONINDICATING), 250 VOLTS, 2 AMP, STYLE F03, MIL-F-15160-3	81349	F03A250V2A	
TB4	C	TERMINAL BOARD, MOLDED, BARRIER SCREW TYPE, 8 TERMINALS, CLASS 38TB, 4.266IN. LONG, MIL-T-55164/2E.	81349	38TB8	
XF1	C	FUSEHOLDER, EXTRACTOR POST TYPE, BLOWN FUSE INDICATING, TYPES FHL17G1, MIL-F-19207-8	81349	FHL17G1	
XF2	C	SAME AS 4N3XF1			
XF3	C	SAME AS 4N3XF1			

*

10.0 WSP COMPUTER SOFTWARE

10. 1 Scope

There is one National baseline for all ASR-9 software subsystems for all FAA operated systems. The WSP system is not being deployed at all FAA ASR-9 sites. However, a new single baseline is required that will support both WSP and non-WSP installations. All ASR-9 software subsystems being modified to support WSP has been modified in such way that both configurations are supported. This has been accomplished by using a "*WSP Exists*" Variable Site Parameter (VSP).

This document provides a complete functional description for all ASR-9 new or modified software pertaining to the ASR-9/WSP interface.

10.1.1 Overview

ASR-9 software has been modified to include the functionality of which includes changes in the following areas:

Remote Monitoring Subsystem (RMS)
Local System Control (LSC)
Remote System Control (RSC)
Six level Weather Smoothing and Contouring (6WX/SC)
Digital Signal Processing Receiver Monitor (DSP/RM)

10.2 RMS

10.2.1 ASR-9 VSP and Performance Data Needed by WSP

The WSP requires certain ASR-9 VSP values to properly generate weather estimates. Each channel's operating frequency, the Sensitivity Time Control (STC) curve, and any other desired VSP has been sent to the WSP as needed.

The WSP also requires certain ASR-9 performance data. Transmit power, Minimum Discernible Signal (MDS), and any other desired performance monitoring data values are sent to the WSP on a regular basis.

10.2.2 ASR-9 Performance Monitoring of the WSP

The current operational status of the WSP (online, summary alarm, unavailable) is displayed by the RMS and recorded in its logs (alarm buffer).

Current performance statistics for the WSP is displayed by the RMS. The number of cells declared for each weather level, the number of micro-bursts present, and other WSP numerical data has been retrieved from the WSP upon user request.

10.2.3 Physical Interface

There is no direct physical interface between the ASR-9 RMS and WSP. All RMS communication with the WSP is via the existing RS-422 communications port with Local System Control.

The RMS software physically resides in fourteen EPROMs (U5P, U3P, U5N, U3N, U5M, U3M, U5K, U3K, U5J, U3J, U5H, U3H, U5E, and U3E) on the RMS SBC 428 EPROM Expansion board (slot 2 in the Intel 310 box). *

* **10.2.4 Logical Interface**

There is no direct logical interface between the ASR-9 RMS and the WSP. All RMS communication with the WSP is handled via Local System Control. A direct logical interface between the RMS and the WSP could have been made using a repeater channel in LSC. But, since the WSP also needs to talk directly to LSC, its easier to limit the WSP to talking only to LSC and not both LSC and RMS.

All RMS/LSC communications use the existing RMS/LSC logical channels (601 through 606). Refer to the non-ASP ICD SE009.

10.2.5 Numbered Alarms

LSC has a new Built-In-Test (BIT) alarm for the LSC/WSP communications interface. The RMS receives pass/fail status for this alarm (809) via the standard path currently used for all LSC alarms. Standard N of M threshold factoring is used for this alarm.

RMS displays the current results of the new BIT test on the SYSTEM CONTROL ALARMS screen (0.2.8). RMS automatically sends changes in the state of this alarm (pass to fail alarms, fail to pass return-to-normals) to the Maintenance Processing Subsystem (MPS). RMS will automatically log pass to fail alarms in the Alarm Buffer (screen 0.3.9).

RMS displays the current N of M values and allows operator changes to these values on the SYSTEM CONTROL PAFs screen 0.7.4.8.

This BIT test is also used for FIT. Test 809 has been inserted into the System Control FIT tree. RMS displays appropriate text for the new Logically Replaceable Unit (LRU) reference designators added for the new WSP components (screen 0.4.1).

10.2.6 Operational Status

LSC receives operational status information from the WSP via a periodic status message. This data includes WSP summary alarm/normal and WSP unavailable/available information. Based on this information, LSC determines if WSP is online or not.

LSC reports to the RMS and other subsystems the current status of these data points via the Control Panel Configuration (CPC) message.

RMS displays the current values of these items on the SYSTEM CONTROL PANEL screen (0.1.1) and the SYSTEM STATUS SUMMARY screen (0.3.1.1). Whenever the current value of any of these data points changes, the RMS logs the event as a state change in the Alarm Buffer and report the change to the MPS.

The possible values for each data point are:

Online Weather Source	WSP, 6WX, or 2WX
WSP Alarm	Alarm or Normal
WSP Unavailable	Unavailable or Available

The data point currently used to indicate the online weather channel (6WX or 2WX) has had the WSP option added to it.

10.2.7 WSP Exists VSP

The RMS provides the capability to download and read-back a *WSP Exists* VSP to LSC. The new parameter has been added to the existing LSC VSP download screen (0.5.3.12.1) and the existing LSC VSP read-back screen (0.6.11). *

* **10.2.8 VSP Data Requests from WSP**

The WSP requires certain ASR-9 VSP values to properly generate weather estimates. These VSPs include but are not limited to:

D106 Channel A Center Frequency
D109 Channel B Center Frequency
1501 Low Beam STC Reference Attenuation
1502 Low Beam STC Slope - Zone 1
1503 Low Beam STC Slope - Zone 2
1504 Low Beam STC Slope - Zone 3
1505 Low Beam STC Slope - Zone 4
1506 Low Beam STC Slope - Zone 5
1507 Low Beam STC Slope - Zone 6
1508 Low Beam STC Slope - Zone 7
1509 Low Beam STC Slope - Zone 8
6502 CP Select Threshold
6503 LP Select Threshold

Whenever the WSP desires VSP data, the WSP sends a VSP data request message to LSC. This message includes the logical unit (LU) number for the desired VSP set. LSC forwards this VSP data request message to RMS. RMS translates the LU number into VSP ID and channel information for each VSP desired. The RMS reads back the current values for these VSPs from the appropriate subsystem(s). The RMS then sends this information back to LSC for relaying back to the WSP.

Basically, RMS pretends the WSP is a fifth terminal accessing a VSP Readback screen.

The RMS and LSC software has been designed in a generic manner. Thus, if the WSP should in the future desire additional VSP data, the WSP would need only to ask for the new logical unit without any software modifications to the ASR-9. A complete list of logical units and their contents can be found in the RMS/MPS ICD (SE005).

10.2.9 ASR-9 PM data requests from WSP

The WSP requires certain ASR-9 performance data. These data include but are not limited to:

Average Transmitter power (both channels)
Low Beam MDS (both channels)
High Beam MDS (both channels)

All of the desired data exists in the certification data logical unit. Whenever the WSP desires this data, typically on a regular basis, the WSP will send a performance data request message to LSC. LSC forwards this request message to the RMS. RMS generates a response message containing the current performance monitoring data (all the certification data) and sends it to LSC for relaying back to the WSP.

The RMS does not re-compute any of the PM data upon this request (except for receiver recovery). RMS will simply provide the current values. This is identical to an operator accessing the CERTIFICATION DATA screen 0.3.8.

*

* **10.2.10 WSP PM data requests from ASR-9**
Under the PERFORMANCE DATA SOURCES screen 0.3.2, the RMS provides access to a new screen for WSP PERFORMANCE (0.3.2.11). This screen provides the ASR-9 operator with some basic numerical statistics on the WSP's performance to be determined by MIT/LL.

Upon operator access of screen 0.3.2.11, the RMS sends a WSP PM data request message to LSC. LSC will forward this message to the WSP. LSC receives the WSP's PM data response message and relays it back to the RMS for display to the user.

10.3 Local System Control

LSC monitors the health of the WSP. If the WSP is healthy, then LSC declares the WSP to be online. When online, the WSP provides an improved Six-Level Weather (6WX) output. This weather data output is free of the Anomalous Propagation (AP) that manifests itself as false weather detections in the existing ASR-9 6WX.

Neither the ASR-9's existing 6WX nor its backup, 2WX, are being replaced by the WSP. The WSP's AP free 6WX exists as a third weather source. The ASR-9's LSC software is being modified to control and display the WSP as one of the potential online weather sources.

10.3.1 WSP Health Monitoring
LSC and WSP exchange status messages on a regular basis. The WSP informs LSC of its health using its status message. LSC can also determine the health of the WSP by detecting the presence or lack of status messages.

10.3.2 WSP Control
If communications with the WSP are working (successful receipt of status messages), and the WSP's status message indicates the WSP is available and not summary faulted, then LSC will declare the WSP to be online. LSC uses a discrete line to control the hardware's operating mode.

10.3.3 Local System Control Panel
At the time of this modification, there were no spare indicators on the local system control panel. The "6WX Unavailable / Local SCIP Alarm" has been removed as the least necessary. This button has been replaced by a new one to indicate WSP status.

Changes to the local system control panel are identical to those on the remote system control panel. Most system control indications are Boolean (dual-state). There are a small number of tri-state indications. The weather source indicator is a Boolean (6WX or 2WX) indicator. This has been changed to a tri-state indicator (WSP, 6WX, or 2WX).

Adjacent to the "2-LEVEL" / "6-LEVEL" weather source indicator on the system control panel exists a "6-LEVEL ALARM" indicator. This indicator has been replaced by one that indicates "WSP". Although this position on the panel is not a push button, a push button is not needed for WSP. The WSP online/offline function will always operate in an "AUTO" type of mode.

The existing "6WX UA" / "LSCIP AL" indicator has been replaced by a "6WX AL" / "WSP AL" indicator.

The WSP modified System Control Panel includes two new lexan covers. One lexan cover replaces the existing "6-LEVEL ALARM" (red) with a "WSP" (white) lexan cover. The other lexan *

* cover replaces the existing "6WX UA" (amber) / "LSCIP AL" (red) cover with a "6WX AL" (red) / "WSP AL" (red) lexan cover.

10.3.4 ASR-9 Parameter Readbacks

The WSP requires certain ASR-9 VSP and performance values to properly generate weather estimates. The ASR-9's RMS processor has access to the required data. LSC acts as a middleman to relay data readback requests from the WSP to the RMS and to relay RMS's responses back to the WSP.

10.3.5 Physical Interface

The physical link between the LSC software and the WSP software is an RS-232 serial connection. The protocols and message formats used on this interface are identical to the ASR-9's existing inter-processor communications package (ZSI). Refer to Westinghouse Data Item SE009 for details.

LSC also writes and reads various hardware registers on the SCI#1 and SCI#2 boards. These registers control WSP online.

The LSC software physically resides in two EPROMs (U20 and U30) on the System Control Interface #1 (SCI#1) board (slot 216 in the weather channel).

10.3.6 Communications Link

To facilitate the LSC to WSP communications path, one of LSC's five existing USARTs has been redirected. The SCI#1 board has five 8251A Universal Synchronous Asynchronous Receiver/Transmitter (USART) chips. Here are LSC's five communication links:

	Chip U#	Hardware Read/Write Function	Data Address	Command Address	Destination
Channel 1	U60	FUNx0-	0D00	0D02	MIP A
Channel 2	U61	FUNx1-	0D04	0D06	MIP B
Channel 3	U63	FUNx2-	0D08	0D0A	6WX S/C
Channel 4	U51	FUNx10-	0D28	0D2A	ANS 1
Channel 5	U53	FUNx11-	0D2C	0D2E	ANS 2

Channel 5, the ANS 2 port, has been reassigned for communication with the WSP. This port is the least utilized of the five ports. The ANS 2 port is only used to perform Patch Loopback fault isolation testing at facilities that have a Dual Remote SCIP. This is a very rare activity. The Patch Loopback procedure has been modified so that the channel 4 USART is used for both ANS 1 and ANS 2 testing. This allows the channel 5 USART to be dedicated for WSP use.

During initialization, the LSC software configures the channel 5 USART for WSP use.

ANS 2 Control Port (FUNW11-):

	7	6	5	4	3	2	1	0
0D2C WRITE	COMMAND							

*

* MODE COMMAND: 0Ch = Synchronous, 8-bit data, no parity (ANS)
4Eh = Asynchronous, 8-bit data, no parity,
1 stop bit, 16x baud factor (WSP)

Note, the channel 5 USART on the SCI#1 board is wired to have an external (from ANS 2) input clock. This is necessary for synchronous mode of operation. For asynchronous mode (WSP), this USART needs an internal input clock. This is accomplished by jumpering the output clock to the input clock on the backplane (B10 to B08 and B11 to B09).

10.3.7 WSP Online Control

Local System Control will maintain a VSP (downloaded by RMS) for WSP existence. The LSC software has been designed to operate at all ASR-9 facilities, both WSP and non-WSP. If WSP exists, and there is no WSP COMM Alarm (*WSP status messages* being received), and the contents of the WSP *Status Message* indicate that the WSP is not summary faulted and not unavailable, then the LSC software shall declare the WSP online. LSC will use a discrete line (bit B of SCI#1 output port ODIO) to control the STC/CAL board and the 6WX/WSP output of the SCI#2 boards.

Discrete Output Latch (FUNW4- TP21):

	15	14	13	12	11	10	9	8
0D10 WRITE	X	X	**WSP ONLIN 1=ON**	DUAL REMTE 1=DR	WX SORCE 1=2WX	PP AT/MN 1=ATO	X	DSP LP/CP 1=LP

7	6	5	4	3	2	1	0
HV B ON 1=ON	HV A ON 1=ON	ANTNA ROT 1 1=ON	ANTNA CP/LP 1=CP	CHNNL A/B 1= B	PP A/B 1= B	ANTNA ROT 2 1=ON	LOCAL REMTE 1=LCL

Spare	not used			
Spare	not used			
WSP Online (ex Dual Redundant)	**216 TP74**	**216 C91**	**215/217 B41**	**123 A73**
Dual Remote	216 TP73	216 C90	215/217 B40	
Weather Source	216 TP72	216 C89	215/217 C10	
PP Auto/Manual	216 TP71	216 C88	215/217 C06	
Spare	not used			
DSP LP/CP	216 TP69	northmark	216 C20/C21/C22/C23 J12 031/032, 121 B87/B88, J14 031/032	
High Voltage B On/Off	216 TP45	216 B79	J14 014	
High Voltage A On/Off	216 TP44	216 B77	J12 014	
Antenna Drive Motor 1	216 TP43	216 B75	J25 030	
Antenna CP/LP	216 TP42	northmark	216 B73	J25 018
Online Channel A/B 017/018	216 TP41	216 A77/A78	221 A72/A71 and J12	
Online PP A/B	216 TP40	216 C92	215/217 C07	
Antenna Drive Motor 2	216 TP39	216 A73	J25 032	
Local/Remote 019/020	216 TP38	216 A71/A72	121 B83/B84 and J14	

*

* **10.3.8 WSP Online Readback**

By definition, the online weather source is the weather source currently being output by the system for display to the air traffic controllers. Multiplexors and a sequencer on the SCI#2 board (slots 215 and 217) control which weather source outputs data to the modems. The 2WX A or 2WX B multiplexor on the SCI#2 boards is controlled by the Online Post Processor A/B discrete from the SCI#1 board. The 2WX/6WX multiplexor on the SCI#2 boards is controlled by Weather Source discrete from the SCI#1 board. The WSP/ASR-9 sequencer on the SCI#2 board is controlled by the WSP online discrete from the SCI#1 board.

Normally, SSM-ASR9-007 is the current baseline, the SCI#2 board in slot 215 (SCI#2A) drives target and weather data to modem links 1, 2, 3 and 4 on both ANS 1 and ANS 2. Note, links 1, 2 and 4 carry target data only; link 3 is for the weather data. Normally, the SCI#2 board in slot 217 (SCI#2B) drives target and weather data only to modem links 5, 7, 8 and 9 on both ANS 1 and ANS 2. Normally, both boards are enabled for output (quadruple remote).

With the WSP modification, both SCI#2s are now able to drive modem links 3 and 5 (weather link 5). The boards themselves are not being modified. The 6WX/2WX inputs and outputs of SCI#2A (215) are also unmodified. The modification is done to the SCI#2B (217) inputs and outputs. For this board, the 6WX data stream is replaced with the WSP data stream. The master sequencer PROM (SCI#2A) controls which SCI#2 board is enabled. Only the enabled SCI#2 can drive weather data to the weather modems (links 3 and 5).

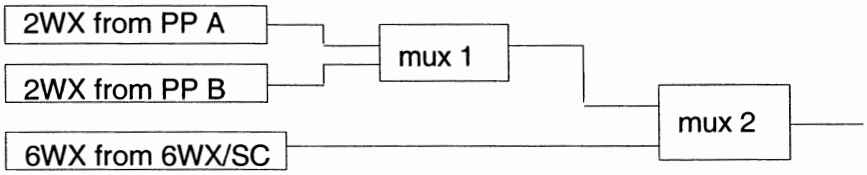
Although LSC's control discrete should result in the proper mux and enable settings on the SCI#2 boards, there is no guarantee. LSC will display on the system control panel the actual online weather source based on readbacks of the muxes and enable signals on the SCI#2 boards (input port ODIC).

Each SCI#2 board has two muxes for controlling the online weather source. The online Post Processor signal controls a 2WX A/ 2WX B mux. The output of this mux goes into the second 2WX/6WX mux, which is controlled by the online weather channel signal. On the SCI#2A board the 6WX data is from the ASR-9. On the SCI#2B board the 6WX data is from the WSP.

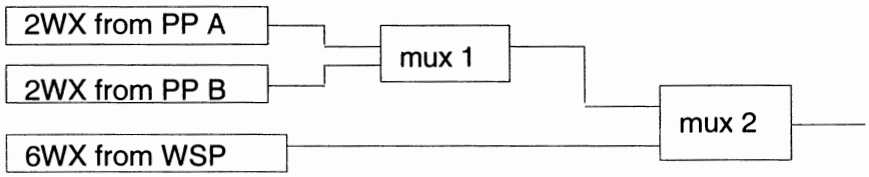
*

*

SCI#2A (215) mux layout



SCI#2B (217) mux layout



For WSP data to be output to the modems, the sequencer PROM must enable SCI#2B for output and the weather source discrete must indicate 6WX.

Weather output and target (surveillance) output are enabled separately. A normal WSP modified system will have both SCI#2 boards enabled for surveillance data (links 1, 2, 4, 7, 8 and 9); but only one has been enabled for weather data (links 3 and 5).

*

* LSCI#2 Readback (FUNR7- TP14):

	15	14	13	12	11	10	9	8
0D1C READ								

7	6	5	4	3	2	1	0
	PP DATA 1=A	WX DATA 1=2WX				WX OUTPT ENABL	SURVL OUTPT ENABL

not used	216 C93	215/217 C93
not used	216 B97	215/217 B97
not used	216 B96	215/217 B96
not used	216 B95	215/217 B95
not used	216 B94	215/217 B94
not used	216 B93	215/217 B93
not used	216 B92	215/217 B92
not used	216 B91	215/217 B91
not used (spare 6WX channel mux)	216 B90	215/217 B90
PP mux position	216 A97	215/217 A97
WX mux position	216 A96	215/217 A96
not used (2WX A/B mux position)	216 A95	215/217 A95
not used (2WX/6WX maint. display mux)	216 A94	215/217 A94
not used	216 A93	215/217 A93
Wx Output Enable	216 A92	215/217 A92
Surveillance Output Enable	216 A91	215/217 A91

10.3.9 Local System Control Panel

Changes to the local system control panel are identical to those on the remote system control panel. Refer to the *ASR-9/WSP Software System Design Document for ASR-9 Remote System Control* document. However, the control ports for lighting the various panel lamps occur at different addresses.

Panel Lamps 1 (1 = lamp on) (FUNW0- TP13):

	15	14	13	12	11	10	9	8
0D40 WRITE	CHN B ONLNE	HV A OFF	HV A ON	CHN A ALARM	CHN A UNAVL	CHN A STNBY	CHN A ONLNE	ANTNA AUTO

7	6	5	4	3	2	1	0
ANTNA MANUL	CIRCL POL	LINER POL	ANTNA ALARM	ANTNA OFF	ANTNA ON	RELSE CNTRL	TAKE CNTRL

Channel B Online lite	219 B67	J08 030
High Voltage A Off lite	219 B66	J07 013
High Voltage A On lite	219 B65	J07 016
Channel A Summary Alarm lite	219 B64	J07 009
Channel A Unavailable lite	219 B63	J07 046

*

* Channel A Standby lite	219 B62	J07 023
Channel A Online lite	219 B61	J07 024
Antenna Polarization Auto lite	219 B60	J08 038
Antenna Polarization Manual lite	219 B59	J08 039
Circular Polarization lite	219 B58	J08 033
Linear Polarization lite	219 B57	J08 032
Antenna Summary Alarm lite	219 B56	J07 005
Antenna Rotation Off lite	219 B55	J07 042
Antenna Rotation On lite	219 A57	J07 043
Release Control lite	219 A56	J08 023
Take Control lite	219 A55	J07 045

Panel Lamps 2 (1 = lamp on) (FUNW1- TP14):

	15	14	13	12	11	10	9	8
0D44 WRITE	MODES	ASR-9	**WSP ONLNE**	6WX	2WX	PP AUTO	PP MANUL	PP B ALARM

7	6	5	4	3	2	1	0
PP A ALARM	PP B	PP A	HV B OFF	HV B ON	CHN B ALARM	CHN B UNAVL	CHN B STNBY

Data Source Mode-S lite	219 B83	J08 026
Data Source ASR-9 lite	219 B82	J08 025
WSP Online lite (ex 6WX Alarm)	219 B81	J08 008
Weather Source 6WX lite	219 B80	J08 017
Weather Source 2WX lite	219 B79	J08 015
PP Auto lite	219 B78	J07 026
PP Manual lite	219 B77	J07 027
PP B summary Alarm lite	219 B76	J07 007
PP A Summary Alarm lite	219 B75	J07 008
PP B Online lite	219 B74	J07 017
PP A Online lite	219 B73	J07 018
High Voltage B Off lite	219 B72	J08 021
High Voltage B On lite	219 B71	J08 020
Channel B Summary Alarm lite	219 B70	J08 014
Channel B Unavailable lite	219 B69	J08 016
Channel B Standby lite	219 B68	J08 029

*

* Panel Lamps 3 (1 = lamp on) (FUNW2- TP15):

	15	14	13	12	11	10	9	8
0D48 WRITE		FILTR ENABL	PP A UNAVL	**6WX ALARM**	RMS ALARM		AUDBL ALARM	MAINT ALERT

7	6	5	4	3	2	1	0
SCIPB ALARM	SCIPA ALARM	SCIP B	SCIP A	MODES ALARM	ASR-9 ALARM	BECON AUTO	BECON MANUL

not used (SCIPBON)	219 A62	214 C74
SCIP SRAP Filter Enable lite	219 A95 A88	J08 044
PP A Unavailable lite	219 A94 A79	J07 012
6WX Alarm lite (ex 6WX Unavail)	219 A93 A86	J07 019
RMS Alarm lite	219 A92 A81	J07 029
not used (OVERTEMP-)	219 B94	not used
Audible Alarm sound	219 B93	J08 010
Maintenance Alert lite	219 B92	J07 010
SCIP B Alarm lite	219 B91	J08 011
SCIP A Alarm lite	219 B90	J08 012
SCIP B Online lite	219 B89	J08 043
SCIP A Online lite	219 B88	J08 042
Mode-S Alarm lite	219 B87	J08 007
ASR-9 Alarm lite	219 B86	J08 006
Data Source Auto lite	219 B85	J08 035
Data Source Manual lite	219 B84	J08 036

Panel Lamps 5 (1 = lamp on) (FUNW5- TP18):

	15	14	13	12	11	10	9	8
0D54 WRITE		FILTR DISBL	PP B UNAVL	**WSP ALARM**	SCC ALARM			

7	6	5	4	3	2	1	0

not used		
SCIP SRAP Filter Disable lite	219 A85 A97	J08 046
PP B Unavailable lite	219 A84 A96	J07 011
WSP Alarm lite (ex Local SCIP Alarm)	219 A83 A91	J07 021
SCC Alarm lite	219 A82 A89	J07 030
not used (LS2)	219 C94	not used

Bits 9-0 are used by RSCC for panel 2

Note: The SCC Alarm lite can also be lit by the hardware watchdog timer (SUMMFLT-).

*

* **10.3.10 Logical Interface**

Various messages are passed between the LSC processor and the WSP's RPG processor. Refer to the *non-ASP Interface Control Document* for details on the formats of these messages. No communication will take place if the WSP exists VSP is set to NO.

Most message traffic is in the form of message pairs. Basically, this means one processor sends a request message to another processor. As a reaction to receipt of the request message, the other processor then sends a response message back to the original processor.

10.3.10.1 Status Message

LSC generates a *Request for Status Message* on a periodic basis (once per second). Upon receipt of this message, the WSP responds with a *Status Message*. The message contains WSP summary alarm (YES/NO) and WSP unavailable (YES/NO) information.

The WSP determines the health of LSC by using a timer on receipt of the *Request for Status Message*. The WSP will report loss of LSC communication on the WSP RMS terminal.

LSC uses the contents of the *Status Message* or the lack thereof to determine the health of the WSP.

M of N filtering of WSP *Status Messages* occurs before declaring a WSP communication alarm (809).

10.3.10.2 Performance Message

LSC generates a *Request for Performance Readback Message* when requested by the RMS. Upon receipt of this message, the WSP will generate a *Response to Performance Readback Message*. This message contains the number of weather cells currently declared for each of the six weather levels. LSC forwards this information to RMS for display to the operator.

10.3.10.3 Polarization Change Message

The WSP generates a *Polarization Change Request Message* whenever the WSP determines that a change in polarization is desired or on a periodic basis. Upon receipt of this message, LSC makes the polarization change if the request is valid (WSP online and polarization in AUTO mode). LSC then generates a *Polarization Change Response Message* to inform WSP of the result.

10.3.10.4 CPC Message

Once every 4.8 seconds, or whenever a change in state occurs, LSC sends a *Control Panel Configuration (CPC) Message* pair to WSP. The WSP includes this CPC message pair into its AP free 6WX output data stream on a priority basis. No response is sent back to LSC on receipt of these messages. The WSP examines the contents of the CPC message to determine the current state of the ASR-9 system.

Note, LSC sends its CPC message pair to all potentially online weather data sources (PP A, PP B, 6WX/SC, and WSP). Each weather source includes the CPC messages along with its weather data for transmission to Remote System Control over the weather modem (link 3 or 10). These modem links are bi-directional. These links are used by RSC to send *CPC Messages, BIT/FIT Results Messages,* and *Firmware Version ID Messages* to LSC. These messages are intercepted by LSC before they reach the weather source. As such, there is no need to have WSP relay them. The WSP should not see them; but if it does, the WSP should ignore them.

*

* **10.3.11 ASR-9 Parameter Readbacks**
Whenever the WSP requires ASR-9 VSP or performance values, the WSP sends properly formatted *WSP Request to Readback VSPs* and *Request for ASR-9 Performance Monitoring Data* messages to LSC. LSC relays these requests from the WSP to the RMS and to relay RMS's responses back to the WSP.

In order for the WSP to receive updated VSP data after a VSP change has been made in the ASR-9, the WSP must re-request the data. The WSP is prompted to do this. Whenever a VSP change is made, the RMS informs LSC that a change has occurred by setting a bit in the periodic maintenance message that RMS sends to LSC. LSC then relays this information to the WSP in the next *Request for Status Message* sent to WSP.

10.4 Remote System Control
The WSP provides an improved Six-Level Weather (6WX) output. This weather data output is free of the Anomalous Propagation (AP) that manifests itself as false weather detections in the existing ASR-9 6WX.

Neither the ASR-9's existing 6WX nor its backup, 2WX, are being replaced by the WSP. The WSP's AP free 6WX exists as a third weather source. The ASR-9's RSC software has been modified to display the WSP as one of the potential online weather sources.

10.4.1 Remote System Control Panel
There are no spare indicators on the remote system control panel. The "6WX Unavailable / Local SCIP Alarm" has been removed as the least necessary. It has been replaced by a new one to indicate WSP status.

10.4.2 Update Monitor Port
The Update Monitor Port screen has been updated to include information about the WSP. This information includes: WSP Exists VSP, WSP Online, WSP Alarm, and WSP Unavailable.

10.4.3 Physical Interface
There is no direct physical interface between the ASR-9 RSC and WSP. The RSC and the WSP do not communicate with each other. RSC receives all its information regarding WSP from Local System Control (LSC) via the existing Control Panel Configuration (CPC) message. This message is received over the online weather channel (modem link 3 or 10).

The RSC software physically resides in two EPROMs (U21 and U23) on the Panel Interface board (slot A44 in the remote SCIP).

10.4.4 Logical Interface
There is no logical interface between the ASR-9 RSC and the WSP. The RSC and the WSP do not communicate with each other. RSC receives all its information regarding WSP from LSC via the existing CPC message. Previously unused bits in the CPC message have been used to indicate WSP status.

10.4.5 System Control Panel
Most system control indications are Boolean (dual-state). There are a small number of tri-state indications. The weather source indicator is a Boolean (6WX or 2WX) indicator. This has been changed to a tri-state indicator (WSP, 6WX, or 2WX).

Adjacent to the "2-LEVEL" / "6-LEVEL" weather source indicator on the system control panel exists a "6-LEVEL ALARM" indicator. This indicator has been replaced by one that indicates "WSP". *

* Although this position on the panel is not a push button, a push button is not needed for WSP. The WSP online/offline function will always operate in an "AUTO" type of mode.

The existing "6WX UA" / "LSCIP AL" indicator has been replaced by a "6WX AL" / "WSP AL" indicator.

Remote Panel 1 Lamps 1 (1 = lamp on):

	15	14	13	12	11	10	9	8
0D00 WRITE	CHN B ONLNE	HV A OFF	HV A ON	CHN A ALARM	CHN A UNAVL	CHN A STNBY	CHN A ONLNE	ANTNA AUTO

7	6	5	4	3	2	1	0
ANTNA MANUL	CIRCL POL	LINER POL	ANTNA ALARM	ANTNA OFF	ANTNA ON	RELSE CNTRL	TAKE CNTRL

Remote Panel 1 Lamps 2 (1 = lamp on):

	15	14	13	12	11	10	9	8
0D04 WRITE	MODES	ASR-9	**WSP ONLNE**	6WX	2WX	PP AUTO	PP MANUL	PP B ALARM

7	6	5	4	3	2	1	0
PP A ALARM	PP B	PP A	HV B OFF	HV B ON	CHN B ALARM	CHN B UNAVL	CHN B STNBY

Remote Panel 1 Lamps 3 (1 = lamp on):

	15	14	13	12	11	10	9	8
0D08 WRITE		FILT* ENABL	PP A* UNAVL	**6WX* ALARM**	RMS* ALARM		AUDBL ALARM	MAINT ALERT

7	6	5	4	3	2	1	0
SCIPB ALARM	SCIPA ALARM	SCIP B	SCIP A	MODES ALARM	ASR-9 ALARM	BECON AUTO	BECON MANUL

THESE BITS LIGHT BOTH PANELS

Remote Panel 2 Lamps 1 (1 = lamp on):

	15	14	13	12	11	10	9	8
0D0C WRITE	CHN B ONLNE	HV A OFF	HV A ON	CHN A ALARM	CHN A UNAVL	CHN A STNBY	CHN A ONLNE	ANTNA AUTO

7	6	5	4	3	2	1	0
ANTNA MANUL	CIRCL POL	LINER POL	ANTNA ALARM	ANTNA OFF	ANTNA ON	RELSE CNTRL	TAKE CNTRL

*

* Remote Panel 2 Lamps 2 (1 = lamp on):

	15	14	13	12	11	10	9	8
0D04 WRITE	MODES	ASR-9	**WSP ONLNE**	6WX	2WX	PP AUTO	PP MANUL	PP B ALARM

7	6	5	4	3	2	1	0
PP A ALARM	PP B	PP A	HV B OFF	HV B ON	CHN B ALARM	CHN B UNAVL	CHN B STNBY

Remote Panel 2 Lamps 3 (1 = lamp on):

	15	14	13	12	11	10	9	8
0D08 WRITE		FILT* DISBL	PP B* UNAVL	**WSP* ALARM**	SCC* ALARM		AUDBL ALARM	MAINT ALERT

7	6	5	4	3	2	1	0
SCIPB ALARM	SCIPA ALARM	SCIP B	SCIP A	MODES ALARM	ASR-9 ALARM	BECON AUTO	BECON MANUL

* THESE BITS LIGHT BOTH PANELS

10.4.6 Update Monitor Port

pre-WSP Update Monitor Port Screen

CONTROLS AND READBACKS

ON-LINE CHANNEL ____
CHANNEL A ALARM ____
CHANNEL A UNAVAILABLE ____
CHANNEL B ALARM ____
CHANNEL B UNAVAILABLE ____
HV A ON ____
HV B ON ____
HV A READY ____
HV B READY ____
ANTENNA ALARM ____
ANTENNA ROTATION ____
ANTENNA POLARIZATION ____
POLARIZATION AUTO/MANUAL ____
BEACON CHANNEL A ALARM ____
BEACON CHANNEL B ALARM ____
ON-LINE WEATHER PROCESSING ____
6WX ALARM ____
6WX UNAVAILABLE ____
SCC/COMM ALARM ____
LOCAL SCIP ALARM ____
MODE-S EXISTS ____
DUAL REMOTE ____

ON-LINE POST PROCESSOR ____
POST PROCESSOR A ALARM ____
POST PROCESSOR A UNAVAILABLE ____
POST PROCESSOR B ALARM ____
POST PROCESSOR B UNAVAILABLE ____
POST PROCESSOR AUTO/MANUAL ____
BEACON SOURCE AUTO/MANUAL ____
ON-LINE BEACON SOURCE ____
ON-LINE BEACON CHANNEL ____
ATCBI ALARM ____
MODE-S ALARM ____
ASR-9 SOURCE ALARM ____
MAINTENANCE ALARM ____
RMS ALARM ____
ON-LINE SCIP ____
SCIP SRAP FILTER MODE ____
SCIP A ALARM ____
SCIP B ALARM ____
SCIP A COMM ALARM ____
SCIP B COMM ALARM ____
SOURCE OF CTS ____
AUTO SWITCH FRONT-END ____
WHITE SANDS MODE ____

*

* WSP Modified Update Monitor Port Screen

CONTROLS AND READBACKS

ON-LINE CHANNEL	____	ON-LINE POST PROCESSOR	____
CHANNEL A ALARM	____	POST PROCESSOR A ALARM	____
CHANNEL A UNAVAILABLE	____	POST PROCESSOR A UNAVAILABLE	____
CHANNEL B ALARM	____	POST PROCESSOR B ALARM	____
CHANNEL B UNAVAILABLE	____	POST PROCESSOR B UNAVAILABLE	____
HV A ON	____	POST PROCESSOR AUTO/MANUAL	____
HV B ON	____	BEACON SOURCE AUTO/MANUAL	____
HV A READY	____	ON-LINE BEACON SOURCE	____
HV B READY	____	ON-LINE BEACON CHANNEL	____
ANTENNA ALARM	____	ATCBI ALARM	____
ANTENNA ROTATION	____	MODE-S ALARM	____
ANTENNA POLARIZATION	____	ASR-9 SOURCE ALARM	____
POLARIZATION AUTO/MANUAL	____	MAINTENANCE ALARM	____
BEACON CHANNEL A ALARM	____	RMS ALARM	____
BEACON CHANNEL B ALARM	____	ON-LINE SCIP	____
ON-LINE WEATHER PROCESSING	____	SCIP SRAP FILTER MODE	____
6WX ALARM	____	SCIP A ALARM	____
6WX UNAVAILABLE	____	SCIP B ALARM	____
WSP ALARM	____	SCIP A COMM ALARM	____
WSP UNAVAILABLE	____	SCIP B COMM ALARM	____
WSP EXISTS	____	SCC/COMM ALARM	____
MODE-S EXISTS	____	LOCAL SCIP ALARM	____
DUAL REMOTE	____	AUTO SWITCH FRONT-END SOURCE OF CTS	____

Note: "ON-LINE WEATHER PROCESSING" which currently displays "2WX" or "6WX" has been changed to indicate "WSP" or "6WX" or "2WX".

10.5 Six Level Weather Smoothing and Contouring

The ASR-9 Weather channel processes 6-level weather data regardless of the status of the WSP. All sources of weather data (PP A, PP B, 6WX/SC, and WSP) process and output weather data as if they were online. A set of multiplexors on the SCI#2 board controlled by LSC actually selects the online weather data for transmission to the modems. This allows efficient switching between online weather data sources.

For the WSP to operate properly in circular polarization, the weather channel must not process local data, the weather channel must process the online target channel's data as in linear mode. This control is provided by the weather channel's Digital Signal Processor Receiver Monitor (DSP/RM). For the DSP/RM to control its data input multiplexor properly in WSP mode, 6WX/SC needs to inform it of WSP's existence.

Although this mode is correct when WSP is online, 6WX/SC receives incorrect data. Thus, when the WSP is online and in circular polarization, the ASR-9's weather channel processes bogus weather primitives. This causes 6WX/SC to generate and output erroneous weather maps. Normally, the air traffic controllers would never see this data because the SCI#2 board's mux selects WSP data when WSP is online. However, when a switch from WSP online to 6WX online occurs; the SCI#2 board's mux switches immediately. 6WX/SC requires 6 to 12 scans to generate *

a good weather map. Thus, during this transition phase, bogus weather data would be displayed to the controllers.

To prevent this, 6WX/SC determines whether WSP is online and in circular and does not output any weather maps during this period. This allows the SCIP to coast the existing good weather map received from the WSP until 6WX/SC can generate it's own good weather map.

10.5.1 Physical Interface

There is no direct physical interface between the ASR-9 6WX/SC and WSP. The 6WX/SC and the WSP do not communicate with each other. The use of the Sigmet receiver and altered STC values while WSP is online can cause the 6WX front-end to receive bogus weather primitives.

The 6WX/SC software physically resides in two EPROMs (U96 and U98) on the Data Collect Select board (slot 115 in the weather channel).

10.5.2 Logical Interface

There is no logical interface between the ASR-9 6WX/SC and the WSP. There is no communication between the WSP and 6WX/SC at all. 6WX/SC knows of WSP's existence and whether it is online or not by examining bits in the CPC message received from Local System Control.

10.5.3 Transmit WSP Exists VSP to DSP/RM

6WX/SC determines the value of the WSP Exists VSP from the CPC message. This value is then sent to the weather channel DSP/RM as part of the existing once-per-second alive message. This is message number 36 as described in the Non-ASP ICD SE009.

6WX Alive Message (#36):

word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	WSP VSP	0	0	0	0	0	0	0	SA OFF							

bit 15: WSP Exists VSP (1 = Yes)
bits 8-14: not used
bits 0-7: Summary Alarm Off (FF = No 6WX alarms present)

10.5.4 Disable 6WX Output when WSP is Online

When 6WX/SC detects that the WSP is online and in circular polarization (determined from the CPC message), 6WX/SC will not output any weather map data (CPC messages has been output as normal). When 6WX/SC detects a transition from this state (WSP online AND circular polarization) to another state (WSP offline OR linear polarization), 6WX/SC will resume outputting weather map data after first completing its normal 6 scan temporal smoothing, spatial smoothing, and contouring sequence.

To hasten the recovery of valid weather data, upon detection of this transition, 6WX/SC will terminate processing of the current 6 scan sequence and resynchronize to scan 1 as quickly as possible. Thus, a maximum 7 scan delay before output of the new weather map begins.

10.6 Digital Signal Processor Receiver Monitor (DSP/RM)

As part of the WSP installation, a beam splitter is placed in the high beam waveguide in each target channel. The 3 dB loss caused by this additional component can cause certain Built-In-Test (BIT) alarms to fail in the ASR-9. Those BIT tests with programmable alarm thresholds can have those

thresholds adjusted; and therefore, are not a problem. However, some of those BIT tests have fixed (hardcoded) thresholds. The ASR-9's DSP/RM software has been modified to adjust the hardcoded thresholds of those BIT tests.

These thresholds have been modified so that a single software baseline is maintained. Only one side of the thresholds has been modified. This allows the same DSP/RM software to operate at both WSP and non-WSP facilities.

The WSP accesses the target channel's low beam data via the ASR-9 I/Q Data Port A4AJ106 (manufacturing test set connector) in the weather channel. In linear polarization, the online target channel's data is available at this port. In circular polarization, the weather channel's DSP/RM normally processes local weather channel data. The DSP/RM software has been modified to process the online target channel's data in circular polarization in the weather channel.

10.6.1 Physical Interface
There is no direct physical interface between the ASR-9 DSP/RM and WSP. The DSP/RM and the WSP do not communicate with each other. The DSP/RM is responsible for running BIT tests on the ASR-9 receiver. Many of these BIT tests employ test targets injected during dead-time. The 3 dB loss caused by installing the WSP beam splitter reduces the amplitude of these test targets.

The DSP/RM software physically resides in six EPROMs (U21, U23, U25, U31, U33, and U35) on the Data Collect Select board (slot 119 in the target channel, and slot 115 in the weather channel).

10.6.2 Logical Interface
There is no logical interface between the ASR-9 DSP/RM and the WSP. There is no communication between the WSP and DSP/RM at all. The target channel DSP/RM is completely unaware of the WSP existence. All affected BIT tests are modified to operate at either WSP or non-WSP facilities.

The weather channel DSP/RM is made aware of the WSP's existence by Six Level Weather Smoothing and Contouring (6WX/SC). The weather channel DSP/RM is made aware of the WSP being online or offline by Local System Control (LSC) via a discrete wire on the backplane.

10.6.3 Alarms

10.6.3.1 High Beam MDS Degrade (Alarm 212)
The pre-WSP test looked for the calculated MDS value, based on 1024 good samples, to be within a given range of a given reference value. The upper threshold has been increased by 1 dB. The lower threshold remains the same.

Pre-WSP Values

	Low Threshold	High Threshold
Online Channel	-3 dB	+3 dB
Standby Channel (HV Off)	-3 dB	+3 dB
Standby Channel (HV On)	-6 dB	+6 dB

WSP Values

	Low Threshold	High Threshold
Online Channel	-3 dB	+4 dB
Standby Channel (HV Off)	-3 dB	+4 dB
Standby Channel (HV On)	-6 dB	+7 dB

10.6.3.2 High Beam MDS Fail (Alarm 213)
The pre-WSP test checked to see how many detections occurred every 32 good samples. If the number of detections is less than 2, then the test fails. This threshold (2 detections) was not modified.

10.6.3.3 High Beam STC Reference Degrade (Alarm 225)
The pre-WSP test checked the STC unit at 0 dB attenuation. The test checks to see if the measured amplitude of a test target is +/- 3 dB from a given reference value. The lower threshold has been reduced by 3 dB. The upper threshold will remain the same.

Current Values		WSP Values	
Low Threshold	High Threshold	Low Threshold	High Threshold
-3 dB	+3 dB	-6 dB	+3 dB

10.6.3.4 High Beam STC Reference Fail (Alarm 226)
This test is similar to the reference degrade test (225) except that a larger threshold of +/- 6 dB is used to detect gross failures. The lower threshold has been reduced by 3 dB. The upper threshold will remain the same.

Current Values		WSP Values	
Low Threshold	High Threshold	Low Threshold	High Threshold
-6 dB	+6 dB	-9 dB	+6 dB

10.6.3.5 High Beam STC Degrade (Alarm 216)
The pre-WSP test checked the STC unit at the 11, 22, 33, and 40 dB attenuation points. The test checks to see if the measured amplitude of a test target is within a given range of an adjusted given reference value. The lower threshold has been reduced by 3 dB. The upper threshold remains the same.

	pre-WSP Values (in quanta (3/32 dB))	
	Low Threshold	High Threshold
11 dB test point	98	136
22 dB test point	215	253
33 dB test point	330	372
40 dB test point	399	452

	WSP Values (in quanta (3/32 dB))	
	Low Threshold	High Threshold
11 dB test point	66	136
22 dB test point	183	253
33 dB test point	298	372
40 dB test point	367	452

10.6.3.5 High Beam STC Fail (Alarm 217)
This test is similar to the STC degrade test (216) except that a larger threshold is used to detect gross failures. The lower threshold has been reduced by 3 dB. The upper threshold remains the same.

	pre-WSP Values (in quanta (3/32 dB))	
	Low Threshold	High Threshold
11 dB test point	77	155
22 dB test point	196	272
33 dB test point	308	393
40 dB test point	373	478

	WSP Values (in quanta (3/32 dB))	
	Low Threshold	High Threshold
11 dB test point	45	155
22 dB test point	164	272
33 dB test point	276	393
40 dB test point	341	478

10.6.4 I/Q Data Port (J106)
The weather channel DSP/RM controls the input data to the weather channel DSP via the data mux select port E018. Consequently, this data is available to the WSP at the I/Q data port 4A4J106).

Data Mux Select Port:

	7	6	5	4	3	2	1	0
E018 WRITE	COMMAND							

MUX COMMAND: 08h = Select Local Data
04h = Select Channel A Data
0Ch = Select Channel B Data

Normally, the weather channel DSP/RM selects the online target channel's data when linear polarization is selected and 6WX is online, standby, or unavailable for evaluation. Normally, the weather channel DSP/RM selects local data when circular polarization is selected or 6WX is unavailable for FIT, unavailable for Test, or unavailable for VSP change.

The DSP/RM software has been modified so that when the WSP is online, the online target channel's data is selected in both linear and circular modes. Thus, when WSP is online, local data is selected only in the various unavailable submodes. When WSP is offline, the mux selection reverts to the normal (original) method.

The weather channel DSP/RM determines if WSP is online or offline by reading SBC Port B (0022h) bit 7. This indication is tied to WSP online control discrete output by Local System Control (0D10 bit 13).

SBC Port B:

	7	6	5	4	3	2	1	0
0022 READ	**WSP ONLN**	X	X	X	X	X	X	X

WSP Online (1=Yes) 119 C94 123 A73 216 C91

This will work well for WSP sites. For non-WSP sites, SBC Port B bit 7 (backplane pin 119 C94) has nothing connected to it. As such, it will float to an unknown state. Thus, to guarantee proper operation of the data mux at non-WSP sites; the weather channel DSP/RM needs to know the state of the WSP exists VSP.

Local System Controls puts the current value of this VSP in the CPC message. LSC sends the CPC message to 6WX/SC as well as other locations. 6WX/SC has been modified to include this information in its periodic status message (the "6WX Alive Message"). The weather channel DSP/RM receives the alive message, and the WSP exists information, from 6WX/SC once per second.

Thus, all data mux selection logic involving WSP online was modified to check if WSP is online AND WSP Exists VSP equals yes.

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