

MX-6A Card

Universal Six-Channel Multiplexer for Microcomputers

User Guide (July 8, 1996 Revision C)



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About This Guide

This guide provides you with minimal information to be able to quickly and easily operate your MX-6A Card.

Related Guides

In addition to this User Guide, the MX-6A Card includes:
MX-6A User Manual And Tech Reference

Change Proposals

Change proposals, comments and requests for copies should be directed to:



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2. MX-6A Card

Universal Radar Interface Multiplexer - Six Channel

Introduction

The MX-6A Card, the six channel universal radar interface multiplexer, has the capability of interfacing six (6) synchronous serial data streams to a microcomputer through the standard personal computer advanced technology (PC/AT) expansion bus. The MX-6A Card, in conjunction with a COTS PC, provides the Federal Aviation Administration (FAA) an inexpensive, reliable and portable radar data interface for radar sensor performance analysis.

The MX-6A Card is a PC/AT compatible computer card which, in conjunction with the PC, can capture for display or storage radar data for analysis. It is designed to operate in 8 MHz or faster IBM compatible 80286, 80386, 80486, and Pentium microprocessor based PC's in an 8 or 16 bit PC/AT expansion bus slot. PC software displays or records data to a file in the FAA's universal Common Digitizer radar record file format (CD-record format).

The MX-6A's six channels can accept IEEE data communication standard transmission formats; RS-232, RS-422, and TTL inputs. Maximum data transmission throughput is 9600 baud of data.

Radar Interface

The MX-6A can connect to several radars in the FAA inventory including CD-1, CD-2, ARSR-3, ARSR-4, ASR-9, MODE-S, FPS-117 (MAR), and modems at the ARTCC or TRACON.

Interface Cables

Interface cables are required for each connection to a radar sensor. The various cable designs used for each type of radar sensor are included in the Interface Cable section (reference drawing numbers: 3159.1.2.3 thru 3159.1.2.15 and 3159.1.2.20).

Hardware Configure

The MX-6A is delivered in the RIT (Radar Intelligent Tool) system configured as shown in drawing # 3159.1.2-1. For more information on hardware setup, reference page 2, 3 and 4.

Make sure that your MX-6A is configured the same way as shown in drawing # 3159.1.2-1 or # 3159.1.2-2.

MX-6A Software

Be sure to use the software which matches the hardware configuration.

MX-6A Installation

Before installing the MX-6A card and to avoid PC hardware interrupt and memory address conflicts, ensure no other AT bus card is using the address range selected for the MX-6A. The MX-6A factory default settings occupy the address range 380-383 hex and IRQ 5.

To install the MX-6A in a PC:

- STEP 1.** Make sure power is turned off.
- STEP 2.** Remove the top cover or panel such that the expansion bus, (PC or AT bus), is exposed.
- STEP 3.** Choose an empty slot (8 or 16 bit)
- STEP 4.** Remove the metal bracket from the computer chassis at the back of the chosen slot.
- STEP 5.** Make sure the MX-6A is configured as shown in drawing 3159.1.2-1 or 3159.1.2-2.
- STEP 6.** Install the MX-6A in the slot and using the screw removed in step 4, secure the card in place.
- STEP 7.** Reinstall the cover or panels removed in step 2.
- STEP 8.** Install cabling from the MX-6A to the radar.
- STEP 9.** Power on the machine.

Hardware Configuration

Reference Drawing # 3159.1.2-1 and # 3159.1.2-2

MX-6A Versions

There are two basic versions of the MX-6A which are currently supported with available software. These are:

1. The RIT (Radar Intelligent Tool) version which uses IRQ 5 and I/O address 380-383 hex. The switch and jumper settings are shown in

drawing # 3159.1.2-1. MX-6As are shipped as RIT versions unless otherwise specified.

2. The standard version which uses IRQ 3 and address 300-303 hex.

The switch and jumper settings are shown in drawing #3159.1.2-2.

Interrupts (IRQ)

The MX-6A Card supports up to four hardware interrupts, i.e., IRQ 2, 3, 4, and 5. Potentially, up to four MX-6A Cards may be installed into a single PC representing 24 channels of radar data or 8 radar sensors.

A higher performance PC is recommended for applications utilizing more than one MX-6A Card in a single PC system. Since each two bytes of data transferred across each channel invokes a PC hardware interrupt service routine. This represents a high on-line software throughput. Also the PC chosen must have available all four IRQs, i.e. 2,3,4 and 5.

Note: As shipped, the software executables support IRQ 3 or 5. All other IRQ settings require the PC software (source code) to be altered and recompiled with the selected IRQs. See the MX-6A software section for more information.

Jumpers

The following discussion references the RIT version MX-6A configuration and drawing # 3159.1.2-1.

There are nine (9) jumpers on the MX-6A card. The purpose and default settings are as follows:

Jumper Number	MX-6A Option	RIT (Factory) Default Setting	Comments
1	CK1	Synchronous, normal clock	Ref. Draw # 3159.1.2-1, coordinates 7B - 7D, 8B - 8D These jumpers were originally provided as a clocking option. Three options: 1. Synchronous, normal clock 2. Synchronous, inverted clock 3. Asynchronous clock The clock cannot be hardware inverted and currently, the asynchronous clock is not supported. These jumpers are <u>always</u> set to the "synchronous, normal position" as shown in drawing # 3159.1.2-1.
2	CK2	Synchronous, normal clock	
3	CK3	Synchronous, normal clock	
4	CK4	Synchronous, normal clock	
5	CK5	Synchronous, normal clock	
6	CK6	Synchronous, normal clock	

Jumper Number	MX-6A Option	RIT (Factory) Default Setting	Comments
7	IRQ	IRQ 5	<p>Ref. Draw # 3159.1.2-1, coordinates 3B.</p> <p>Other available interrupts are 2, 3, and 4.</p> <p>IRQ 2, also referenced as IRQ 9 in AT systems, is usually available.</p> <p>IRQ 3 and IRQ 4 are usually reserved for serial ports but these may be available in some machines by disabling the serial port.</p> <p>Check your machine and AT bus cards to see which interrupts are in use.</p> <p>As delivered, the MX-6A PC software can be invoked by interrupt IRQ 5 or IRQ 3. See the software section for more details.</p>
8	DELAY	5	<p>Reference drawing # 3159.1.2-1, coordinates 3C.</p> <p>DELAY creates an IORDY (I/O ready) signal back to the AT bus circuitry in order to stretch the I/O read pulse.</p> <p>Modern components along with a standardized 8 MHz AT bus allows a setting of 0 (minimum delay time). AT bus read time has almost no effect on total data throughput, therefore, the DELAY setting is not significant.</p>
9	RESET	Enabled	<p>Reference drawing # 3159.1.2-1, coordinates 3D.</p> <p>RESET allows the 8085 to be automatically reset in the event of a hardware failure. RESET may also be activated via the software. To prevent reset from occurring, the 8085 must access the "Watchdog Reset" memory location at least once every 70 ms</p>

TABLE 2. -1: MX-6A JUMPERS

DIP Switches

There is an 8 position DIP switch on the MX-6A card, SW1, and is used to set the I/O address range of the MX-6A card.. Reference coordinates B4 of drawing #3159.1.2-1.

The MX-6A uses four (4) I/O addresses; the first of which must be set on DIP switch SW1. The factory default setting is set to address range 380-383 HEX. There are 64 memory address ranges available for the MX-6A.

1. 3X0-3X3 hex, X = any hex digit between 0 and F
2. 3X4-3X7 hex

3. 3X8-3XB hex
4. 3XC-3XF hex

The switch settings for the 64 ranges are shown in the following table.

A9	A8	A7	A6	A5	A4	A3	A2	Address lines
POS1	POS2	POS3	POS4	POS5	POS6	POS7	POS8	SW1 Dip switch
Off	Off	On	On	On	On	On	On	Address Range 300-303 hex
Off	Off	On	On	On	On	On	Off	Address Range 304-307 hex
Off	Off	On	On	On	On	Off	On	Address Range 308-30B hex
Off	Off	On	On	On	On	Off	Off	Address Range 30C-30F hex
Off	Off	Off	Off	Off	Off	On	On	Address Range 3F0-3F3 hex
Off	Off	Off	Off	Off	Off	On	Off	Address Range 3F4-3F7 hex
Off	On	Address Range 3F8-3FB hex						
Off	Address Range 3FC-3FF hex							

TABLE 2. -2: MX-6A DIP SWITCH SETTINGS

Any of the addresses, shown in the above table can be used. For addresses other than 380-383H or 300-303H, the PC software (source code) must be altered and recompiled with the selected address. See the MX-6A software section for more information.

Note: As shipped, the software executables support memory addresses 380-383H and 300-303H. All other address ranges require the PC software (source code) to be altered and recompiled with the selected address. See the MX-6A software section for more information.

3. MX-6A Card Operation

Overview

The MX-6A Card can receive synchronous serial data from up to six (6) channels. Up to four (4) MX-6A Cards may be installed and configured in one PC provided the required IRQs are available.

Note: IRQs required are 2,3,4,and 5. MX-6As were originally designed for the IBM compatible PC bus (8 bit ISA bus). They therefore may also be used in the 16 bit AT bus or the 32 bit EISA bus.

Received data and clocks may be RS232, RS422, or TTL type signals. The MX-6A transfers the received data to the PC in a two byte format as determined by the on board MX-6A firmware. The on board firmware and PC software are selected dependent upon application. Programs within the PC may record, alter, display, and/or send radar data to other users.

Data Formats

For receiving radar data, the MX-6A hardware and firmware will assemble each 13 bit radar data message into a 16 bit computer word, compatible with COTS PC hardware and software. The 13 bit radar data message length is standard for many radars, i.e., 12 bits for data followed by a parity bit.

Figure 1 below depicts a typical beacon message. Note the length of 7 fields. Radar, RTQC, and Status are only 4 fields long. 7 fields and 4 fields are the standard lengths. Exceptions do occur however in MAR, ASR9, and other radars. These special cases are not covered in this document. In general, this discussion applies to CD1, CD2, and ARSR3.

DATA FORMAT, RADAR TO MX6A
SYNCHRONOUS SERIAL TRANSMISSION

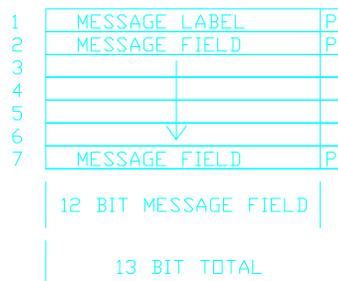


FIGURE 3. -1 DATA FORMAT, RADAR TO MX-6A

At least one idle character is transmitted between any and all radar messages regardless of their type. The MX-6A will sync on idle messages to frame the input data. Thereafter the MX-6A recognizes the message types from the label and therefore knows when the next message label will occur.

An idle message is one field long and its pattern is three zeros (0s) followed by 10 ones (1s). See figure 3-2 below.

IDLE MESSAGE, RADAR TO MX6A
SYNCHRONOUS SERIAL TRANSMISSION



FIGURE 3. -2 IDLE MESSAGE, RADAR TO MX-6A

The format for radar data as transferred from the MX-6A to the PC is 13 bits of data (including parity) followed by 3 bits allocated for other information.

For any field, the MX-6A passes the original 13 bits as they were received.

For all message labels, i.e., the first 13 bit field of a message, the MX-6A adds a sync error bit, an invalid message bit, and a 0 bit. For all other 13 bit fields being translated to 16 bit fields by the MX-6A, the first 13 bits are data followed by 3 bits inserted by the MX-6A which define the channel address.

For valid messages, the sync error and invalid bits are normally 0. They are set to a 1 in the first valid message label after an out of sync condition or other malfunction occurs. Figure 3 below shows what a beacon message would look like as transferred from the MX-6A to the PC. As in figure 1, Radar, RTQC, and Status would be only 4 fields long. At this point a field is 16 bits long or 2 bytes. The MX-6A will transfer this 16 bit field as 2 eight (8) bit bytes to the PC.

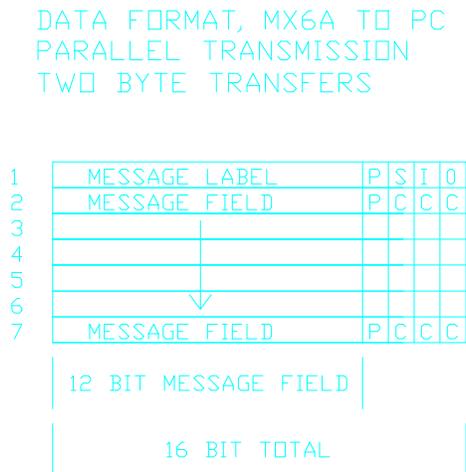


FIGURE 3. -3 DATA FORMAT, MX-6A TO PC

Regardless of the length of the radar message transmitted by the MX-6A to the PC, the PC always assembles a 10 word message. Therefore, all radar messages regardless of their length are translated to 10 sixteen (16) bit words.

The first 7 words are reserved for the message and the last 3 words are reserved for the channel number and the time stamp both of which the PC software inserts. Only a beacon message will use the entire 7 allocated words. All other radar message types such as Search, Status, RTQC, and any others use only 4 words of the 7 allocated. The remaining 3 words are padded with zeros by the PC software.

In addition to changing the length format, the PC software also changes the 16 bit fields as shown in figure 3-4 (next page).

Now the message field is located in the last 12 bits of the 16 bit field.

Also the parity bit is stripped and 4 new status bits are added; i.e., SOM, EOM, Field parity error, and Malfuction.

These occur for both message labels and fields. Notice that SOM is set for the first field and EOM is set for the last field. The channel address is stored in word 8 in EBCDIC (Extended Binary Coded Decimal Interchange Code). The time stamp occurs in words 9 and 10 in hexadecimal format. This time stamp is a hex number which represents the total number of 0.1 second intervals which had occurred from midnight on that date.

DATA FORMAT, PC TO DISK

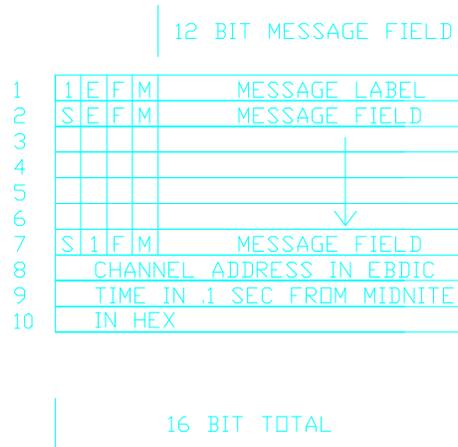


FIGURE 3. -4 DATA FORMAT, PC TO DISK

The PC assembles 100 messages, i.e., 1000 words (or 2000 bytes,) prior to recording this data to the disk drive. These 2000 byte records will continue to be written to the disk until the software is interrupted by the user; i.e. the file ends.

Prior to writing the first 2000 byte record, the PC software will insert a 2000 byte header record to the front of the file. This record includes information inserted by the PC software and information which the user inserted at startup. It is written in EBCDIC. This record starts with the word "C D R E C O R D" and then the date when the file was recorded. Next in the record are the channel number and site identification codes for channel groupings 1,2,3 and 4,5,6. The last entry are the user comments which can be up to eighty (80) characters. Any extra space from the end of the comments to the end of the 2000 byte record is padded with the EBCDIC space which is a 40.

Hardware/Software/Firmware Overview

The hardware and software/firmware may be divided into three sections;

1) the MX-6A 8742 slave processors with associated firmware, 2) the MX-6A 8085 master processor and associated firmware, and 3) the PC and associated software.

The primary purpose of the 8742 slave processors is to frame the incoming serial 13 bit messages into parallel data. It does this through recognition of idle messages and label fields. If sync is lost the 8742 will immediately attempt resync.

The primary purpose of the 8085 is as a convenient interface between the 8742 slave processors and the PC / AT bus.

The 8085 does this by collecting data from the 8742s via interrupts from them and then handshaking this data to the PC via the 8155 and 8255. Data is not altered but information such as invalid, malfunction, and channel number is added.

The primary purpose of the PC hardware and software is to provide a convenient user interface to the system by providing graphic screens, keyboard input, etc. The PC will provide some on-line filtering and processing of radar data for screen display. Also the PC will assemble messages received from the MX-6A into a 20 byte message, a 100 message record, and then write records to the disk in a file for later retrieval / and off-line analysis. Data added includes SOM, EOM, Field Parity Error, the channel number in EBCDIC, and the time stamp in hex. A 2000 byte header is also added to the front of the file in EBCDIC which includes the date, the site ID with associated channel numbers, and user comments.

There are two sets of MX-6A onboard firmware; the 8742 slave processor firmware, and the 8085 master processor firmware. In addition, there are several PC software choices which are user selected dependent upon application. The onboard firmware (both sets) are normally not changed, i.e., PROM switching is not normally required. The PC software, at startup, will vector the onboard firmware to their appropriate routines for that application. In other words, several common applications are already programmed into the PROMS.

Startup/Initialization

The selected PC software, when executed, will require various inputs such as data and clock types, (RS232, RS422, or TTL) and/or polarity to be entered by the operator. Normally, polarity is not altered from the startup default although this option is available for the FPS117/MAR radar.

Operator inputs and selected PC software determines 8 bytes which are sent by the PC to the MX-6A for initialization. The 8 bytes are a configuration byte, program selection bytes for each of the six 8742 slave processors, and a program selection byte for the 8085 master processor. The 8742s execute firmware from their own internal 2048 byte PROM. The 8085 executes its firmware from a 2764 8K byte PROM.

After the PC software is started it issues a reset to the MX-6A by writing 1 bit to Port C of the 8255 Programmable Peripheral Interface (U39) and then clearing that bit. (U39 is reset by the PC hardware.) This reset assures that the 8085 and 8742s start executing at the proper address.

The 8085 routine is expecting to receive 8 bytes, and each 8742 routine is expecting to receive a single byte. Each of these routines are in a very small loop following reset and waiting for the required byte or bytes. The 8085 receives, saves, and distributes the 8 bytes to their proper place.

The PC sends bytes of data to the MX-6A by writing to the 8255 Port A. This occurs at startup time. The 8255 will in turn create a status condition in the 8155, U38, an IO port chip (these two ICs are hardware connected). The 8085 constantly looks for a byte from the PC by reading the status of the 8155 (Take note that the 8155 also has RAM and Timer functions which are not used.) When the 8155 status indicates a byte is available, the 8085 reads Port A of the 8155 to get the byte.

The PC monitors the 8255 status (Port C) to determine that the 8085 has accepted the byte. When the PC determines that the 8085 has accepted the byte, the sequence is repeated until all 8 bytes are sent. This is the sequence for data being sent from the PC to the MX-6A at startup. The sequence for data being sent from the MX-6A to the PC will be described later.

The 8 bytes sent at start up are sent in the following order; the configuration byte, the six (6) 8742 program bytes starting with channel 1's 8742, and last the 8085 program byte. When the first of the 8 bytes is received, the 8085 writes this byte to the channel mode control register U25. This register selects the type and the polarity of input signals by steering the selector PALs U37 and U42. Reference figure 5 (next page) and drawing number 3159.1.2.17.

CHANNEL MODE CONTROL REGISTER (BITS 0-3 AT ADDRESS 4600H)

CHANNELS 1, 2, & 3			CHANNELS 4, 5, & 6		
BITS	SIGNAL TYPE		BITS	SIGNAL TYPE	
1	0		3	2	
0	0	RS-232	0	0	RS-232
0	1	TTL	0	1	TTL
1	0	RS-422	1	0	RS-422
1	1	NOT DEFINED	1	1	NOT DEFINED

CHANNEL MODE CONTROL REGISTER (BITS 4-7 AT ADDRESS 4600H)

CHANNELS 1, 2, & 3				CHANNELS 4, 5, & 6			
BIT	CLK LINES	BIT	DATA LINES	BIT	CLK LINES	BIT	DATA LINES
4		5		6		7	
0	NORMAL	0	NORMAL	0	NORMAL	0	NORMAL
1	INVERTED	1	INVERTED	1	INVERTED	1	INVERTED

FIGURE 3. -5 CHANNEL MODE CONTROL REGISTER

The second through seventh bytes received by the 8085 are written to input buffers of the respective 8742s starting with channel 1. This byte, when received by the six (6) 8742s, vectors the 8742s firmware to the appropriate selection for that application. The last byte received by the 8085 vectors the 8085 firmware to its appropriate selection for that application.

Synchronization

Each MX-6A channel interfaces to data and clock via selected line receivers, a shift register, and an 8742. Data and clock enter the MX-6A via a 37 pin D-sub connector to line receivers which convert these signals to TTL. These signals are then passed through U37 and U42 PALs. These PALs are selectors of input signals and polarity. The PAL outputs are inputs to serial to parallel shift registers. Data is shifted into the shift registers by its associated clock. The parallel outputs of the shift registers are applied to the associated 8742s.

An 8742 samples its input data from the shift register to synchronize on idles or messages. It then can read a message field at the correct time, i.e., framing has occurred.

An 8742 synchronizes by detecting two consecutive idle messages. For initial synchronization the input data of an 8742 is sampled following each data clock until an idle message is read. After an 8742 detects an initial idle message, a counter (initialized at 0) in the 8742 is incremented by each data clock. When its

count is 13, the 8742 again reads its input data. If its input data is another idle message, synchronization has been achieved. If its input data is not another idle message, the initial synchronization process restarts.

With synchronization achieved, an 8742 reads its input data once a field (13 clocks). The action an 8742 takes on a field of data depends on which field of a message the 8742 anticipates receiving. After synchronization an 8742 provides two bytes for the 8085 microprocessor for each non-idle message field of a valid message. If an invalid message label or an out of sync condition is detected by the 8742, it will set a corresponding flag bit in the next valid two byte message label field after it resynchronizes. An 8742 detects invalid message labels for a non-idle message field which follows an idle message when the non-idle message field is NOT a valid message label. An out-of-sync flag is set when an invalid message label is detected or when the field following the last field of a message is not an idle message.

For either condition, i.e., an invalid message label or an out-of-sync, an 8742 must resynchronize. In resynchronizing, an 8742 will sample its input data once a field (every 13th clock) for the next 15 fields or until it finds an idle message. If the 8742 finds an idle message in the 15 fields it is again synchronized but if it does not find an idle message in the 15 fields it begins (same as beginning) sampling the input data after every clock until synchronization (two consecutive idle messages) is achieved.

Data Transfers from MX-6A to PC

For each received field of a synchronized valid message, an 8742 provides two bytes for the 8085. When an 8742 writes a byte to its output buffer, the 8742 interrupts the 8085 because its output buffer full bit is set. By examining the 8742 status registers output buffer full bit, the 8085 interrupt service routine determines which 8742s are interrupting the 8085.

When the 8085 reads the output buffer of an interrupting 8742, the 8742 status registers output buffer full bit is cleared.

The 8085 saves this byte in RAM U31 in an allocated buffer area for the associated input channel. The interrupt service routine of the 8085 waits until the associated 8742 provides the second byte for the 8085. The 8085 monitors the output buffer full bit in the status register of the associated 8742 until it is set. When the 8742 writes the second byte to its output buffer, the output buffer full bit of its status register is set. The 8085 reads the second byte from the output buffer of the 8742 which clears the 8742 status register's output buffer full bit. The 8085 saves this byte in the next sequential address of the allocated buffer area. After each interrupting 8742 is serviced the 8085 will exit its interrupt service routine.

Because each input field to the 8742s is 13 bits, and the 8742 transfers these fields to the 8085 as 16 bit fields (two bytes), 3 bits are thus available for other purposes. For message label fields, the 8742 uses 2 bits of the 3 available bits for out-of-sync and invalid message label flags and the remaining bit is set to 0. For fields other than message label fields, the 8742 passes these 3 extra bits to the 8085 as zeros (0s). The 8085 firmware replaces these zeros (0s) with the channel number (0 thru 6 in binary) prior to sending this data to the PC. Reference Figure 3.

When the 8085 is not servicing an 8742 interrupt, available data in the allocated buffer area is passed to the PC. The 8085 will pass the two byte message label field to the PC unchanged as received from the 8742s. For any two byte field other than the message label field, the 8085 will add the channel number to the second byte of the field in the three bits which the 8742 left as zeros (0s). The 8085 passes two bytes to the PC by writing two bytes to the 8155. When the second byte is written to the 8155 an interrupt is generated to the PC via the 8255. (The 8155 and 8255 are hardware connected). The interrupt service routine of the PC will read these two bytes from ports A and B of the 8255.

The 8085 determines that the PC has read the two bytes by examining the status register of the 8155.

The PC and the MX-6A communicate via PC I/O instructions and PC interrupts. This is called interrupt driven I/O. Each and every message field is transferred as two bytes requiring an interrupt to the PC. Idle messages are not transferred.

After the PC program starts, the PC writes 8 bytes to the MX-6A for initialization purposes. The flow of data is thus initially from the PC to the MX-6A. During this 8 byte transfer, interrupts are not used. After initialization, radar data recording starts and thus the flow of data is from the MX-6A to the PC. This data flow continues until the operator hits the escape key to terminate the recording. Any data remaining in the PC's 2000 byte buffer is lost at exit time, i.e. only completed 2000 byte buffers are recorded to disk.

4. MX-6A Software Setup

There are four programs shipped (on 1.44 M floppy) with the MX-6A which are currently supported by the FAA / AOS-500. These are:

Executable Program	Memory Address and IRQ
WRTCDRIT.EXE	I/O address 380 and IRQ 5
WRTARRIT.EXE	I/O address 380 and IRQ 5
WRTCDSTD.EXE	I/O address 300 and IRQ 3
WRTARSTD.EXE	I/O address 300 and IRQ 3

These programs were written by Vick Pestana, FAA, Honolulu. Copy these programs to the hard drive. Be sure to choose the appropriate program.

Note: The hardware must be set up in one of these two configurations. See the hardware configuration instructions.

To run the WRTCDRIT program, use the following example.

STEP 1. At the DOS prompt type: `W R T C D R I T`

STEP 2. Press `<ENTER>` to execute the command

The operator is prompted to select the input data configuration for the MX-6A Card as follows if a previous selection to record data to disk was made.

CHNL #1,2,3	CHNL #1,2,3	SELECTION
RS-232	RS-232	(a)
TTL	TTL	(b)
RS-422	RS-422	(c)
RS-232	TTL	(d)
TTL	RS-232	(e)
RS-232	RS-422	(f)
RS-422	RS-232	(g)
TTL	RS-422	(h)
RS-422	TTL	(i)

SELECT MX-6A DATA INPUT CONFIGURATION (A,B,C,D,etc.) [A]:

Choose one selection and press enter;

The operator is prompted to select the type of radar for channel 1

CD-1, CD-2, ARSR-3 (a)

FPS-117 (MAR) (b)

ARSR-4 (FUTURE) (c)

MODE-S (FUTURE) (d)

ASR-10 (FUTURE) (e)

CD-3 (FUTURE) (f)

SELECT RADAR TYPE FOR CHANNEL 1 (A,B,C,D, etc.) [A]:

Select appropriate letter and hit enter.

The operator is then prompted to select channels 1 thru 6.

The operator is then prompted:

Disable Input Channels ? Y/N [N]:

Record Data to Disk ? Y/N [Y]:

Realtime Analysis Required ? Y/N [Y]:

Filter Out All 1200 Codes ? Y/N [N]:

Enter Analysis Scan Interval (1,2,4,8) [1]:

4.8 SEC. (A)

9.6 SEC. (B)

10.0 SEC (C)

12.0 SEC (D)

Enter Antenna Scan Time (A,B,C,D) [D]:

Enter Three Character Site Ident For 1st Site:

Here the operator enters three characters of his/her choice.

Enter Three Character Site Ident for 2nd Site:

Here the operator enters three characters of his/her choice.

ENTER FILENAME: - operator enters DOS filename

ENTER COMMENTS (max 80 characters)

The following screens appear

xxx	xxx yyy	xxx yyy
PAR	MSGs	SEARCH
MAL	SCANS	BEACON
INV	BEACON	DUP CODE
SYN	SEARCH	R/L AVG
	STATUS	BIT 25
PAR	MAP	0000 3/A
MAL	STROBE	R/R
INV	AIMS	MODE 3/A
SYN	HEIGHT	MODE C
FILESIZE		MODE 2

ESC to EXIT

5. MX-6A Interface Cable Designs

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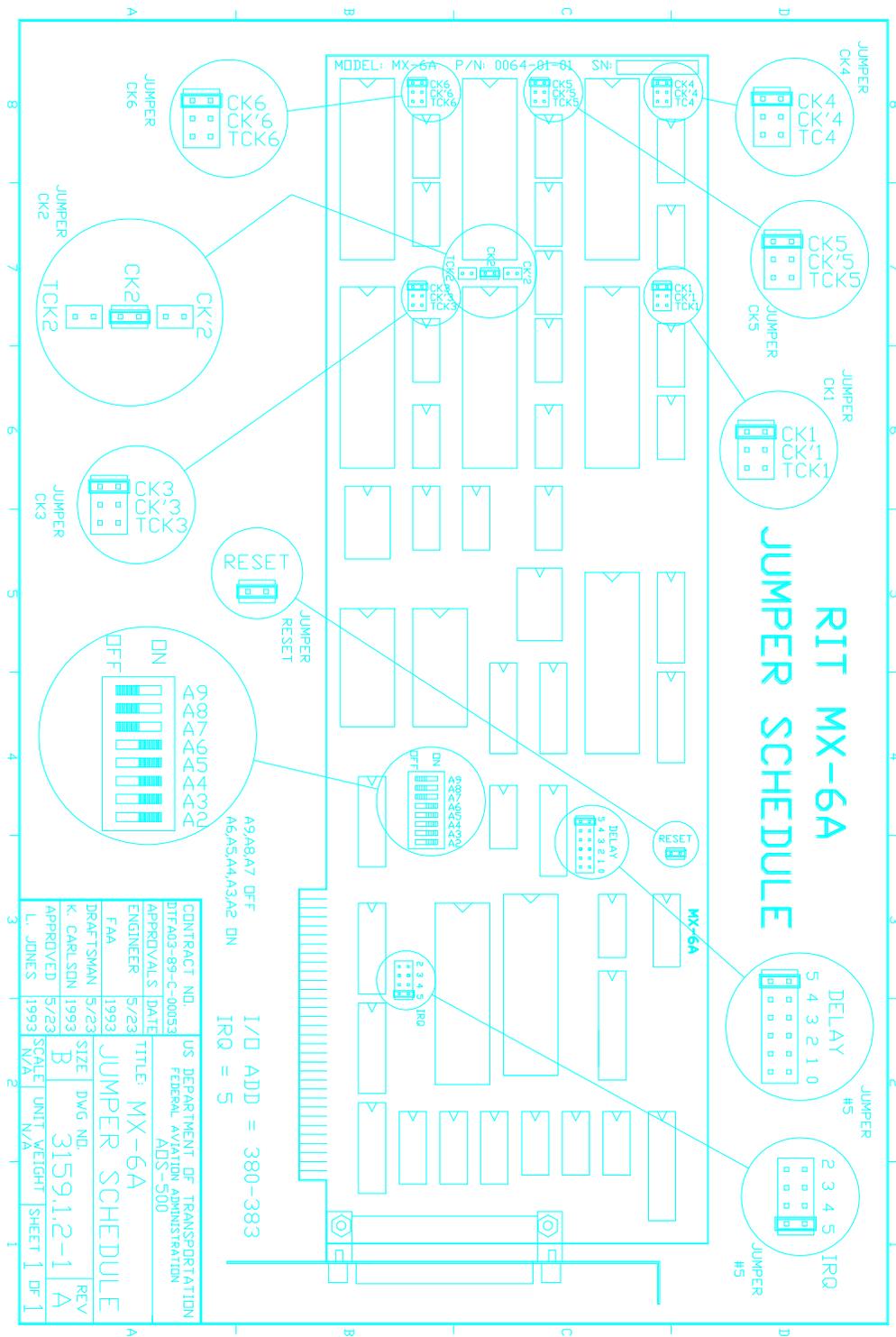


FIGURE 5. -6 RIT MX-6A JUMPER SCHEDULE (DWG: 3159.1.2-1)

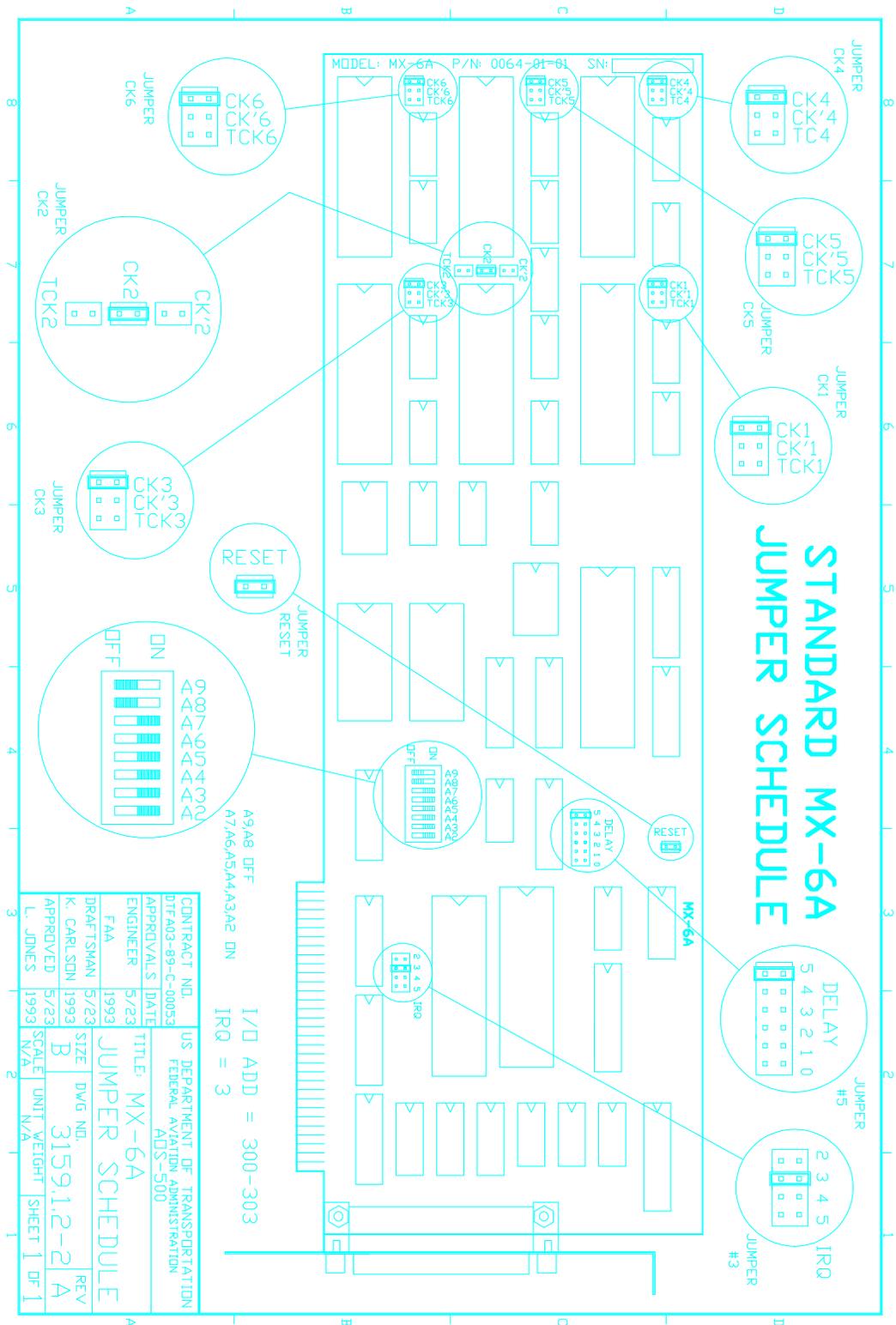


FIGURE 5. -7 STANDARD MX-6A JUMPER SCHEDULE (DWG: 3159.1.2-2)

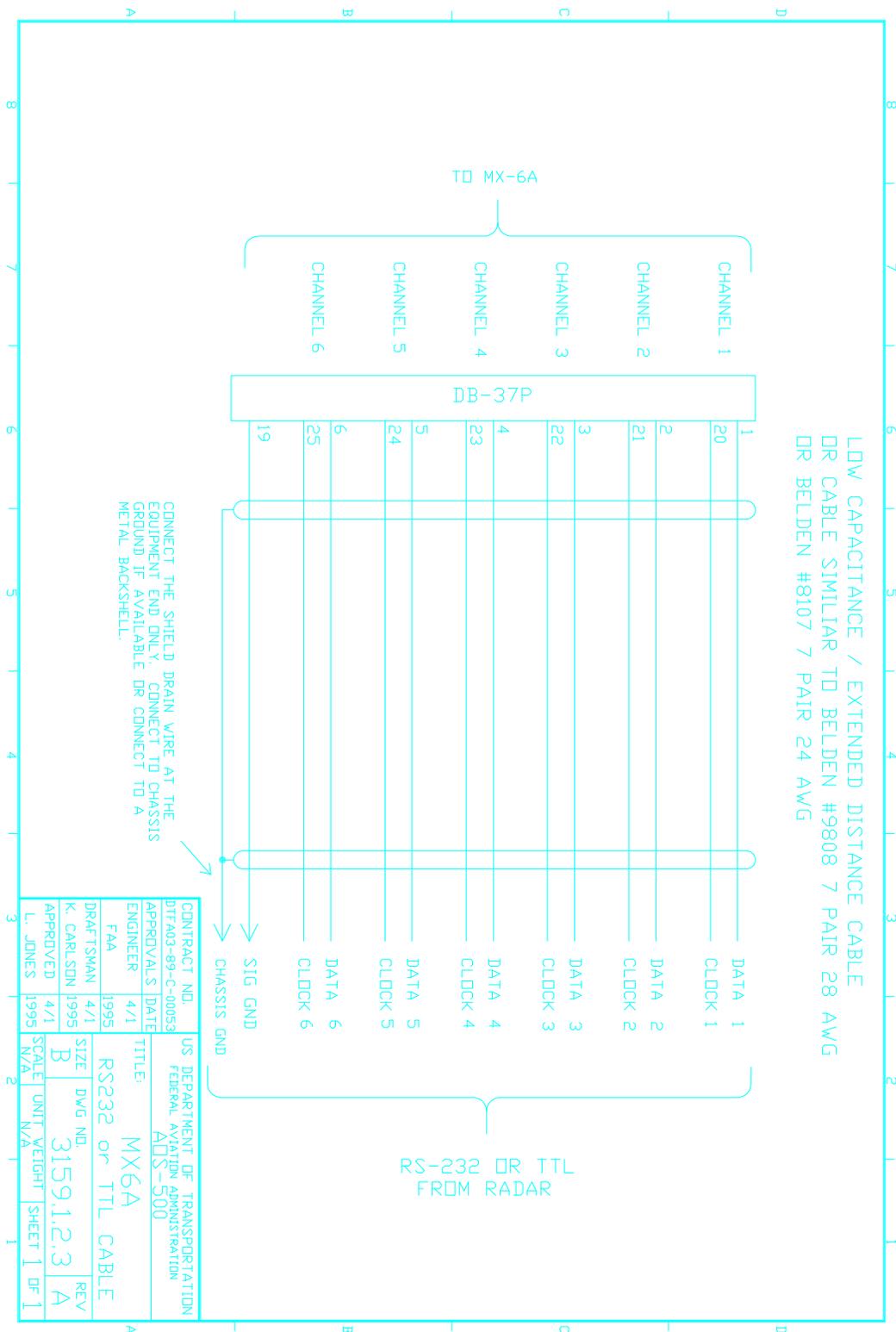


FIGURE 5. -8 RS232 OT TTL CABLE (DWG: 3159.1.2.3)

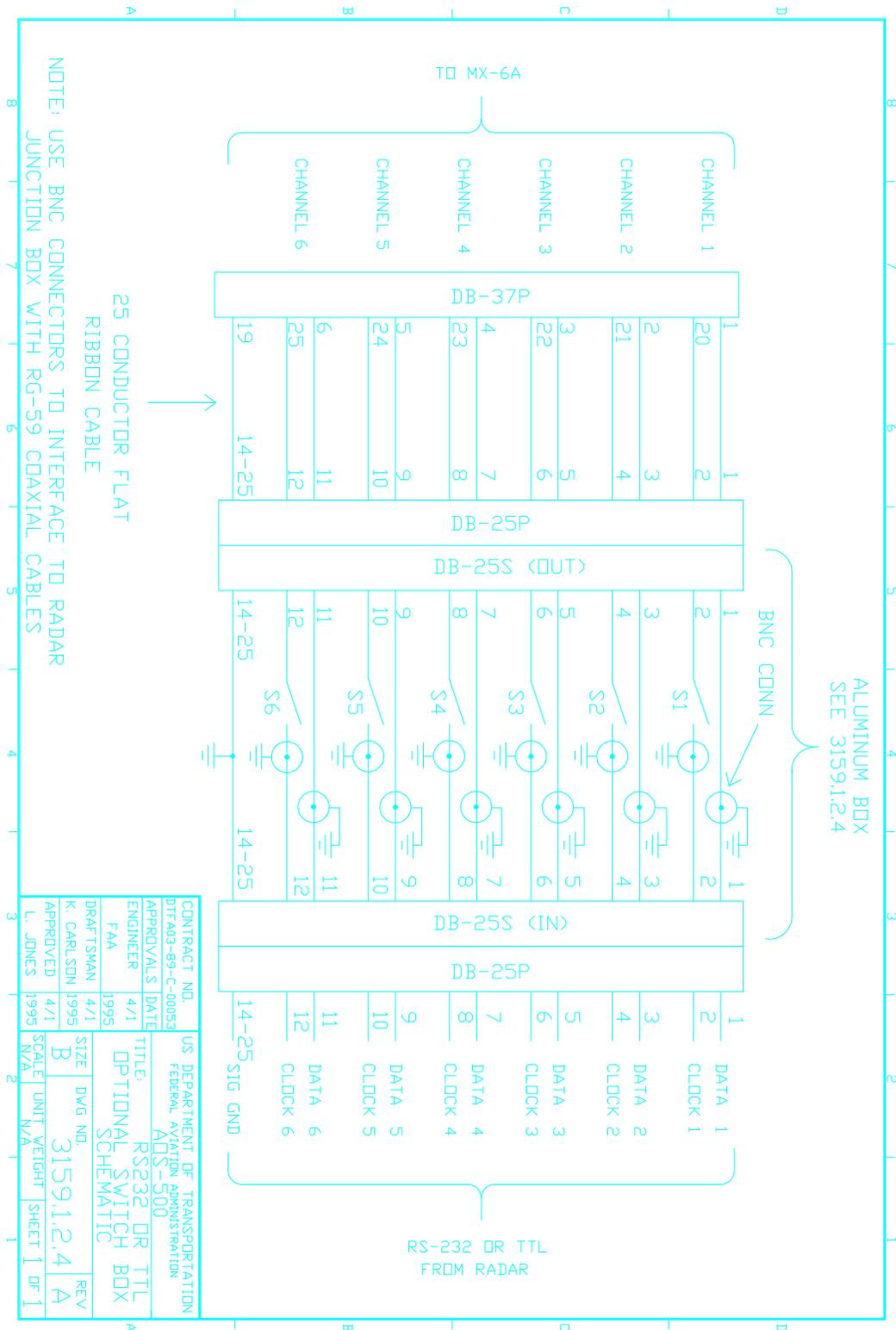


FIGURE 5. -9 OPTIONAL SWITCH BOX SCHEMATIC (DWG: 3159.1.2.4)

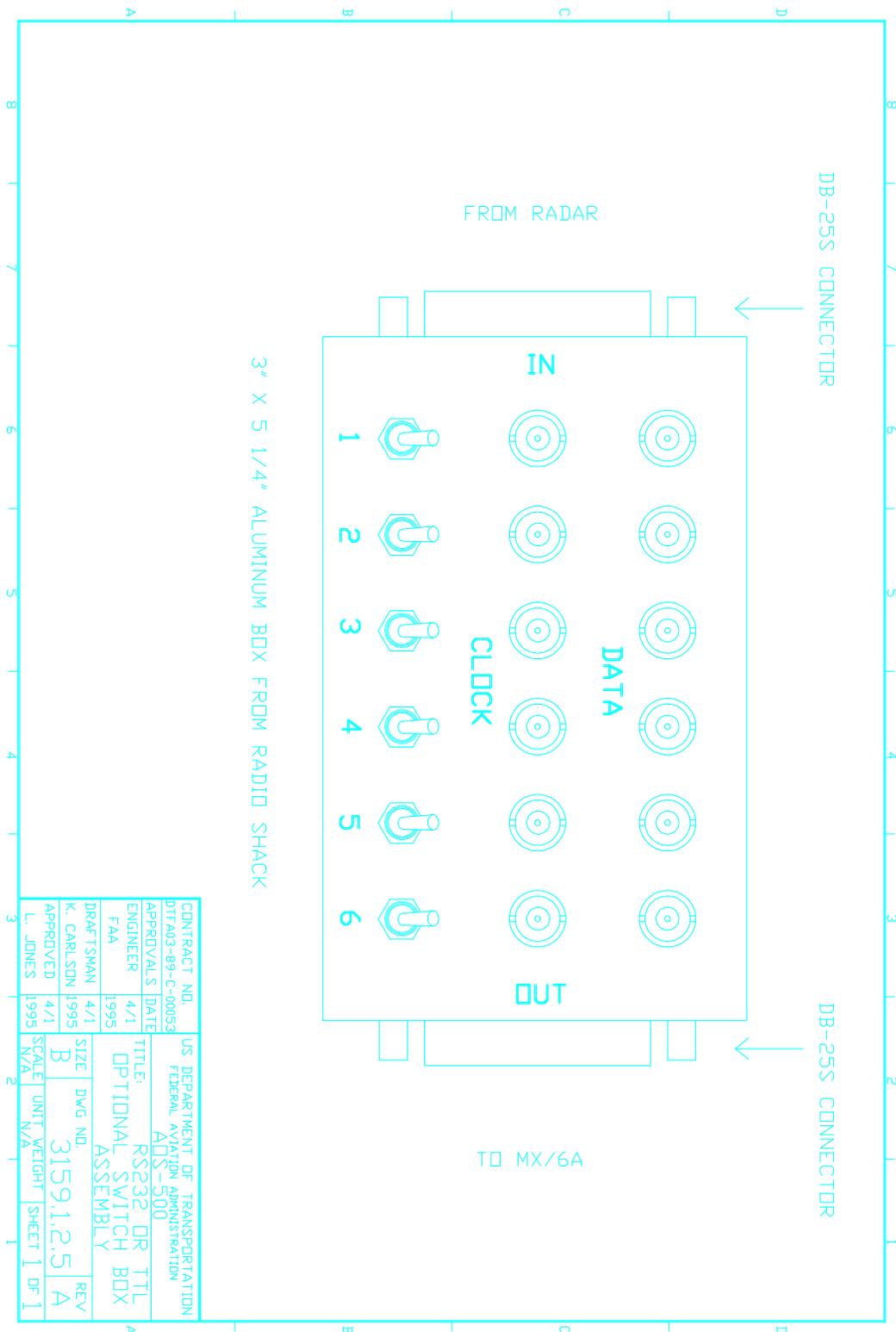


FIGURE 5. -10 RS232 OR TTL OPTIONAL SWITCH BOX ASSEMBLY (DWG: 3159.1.2.5)

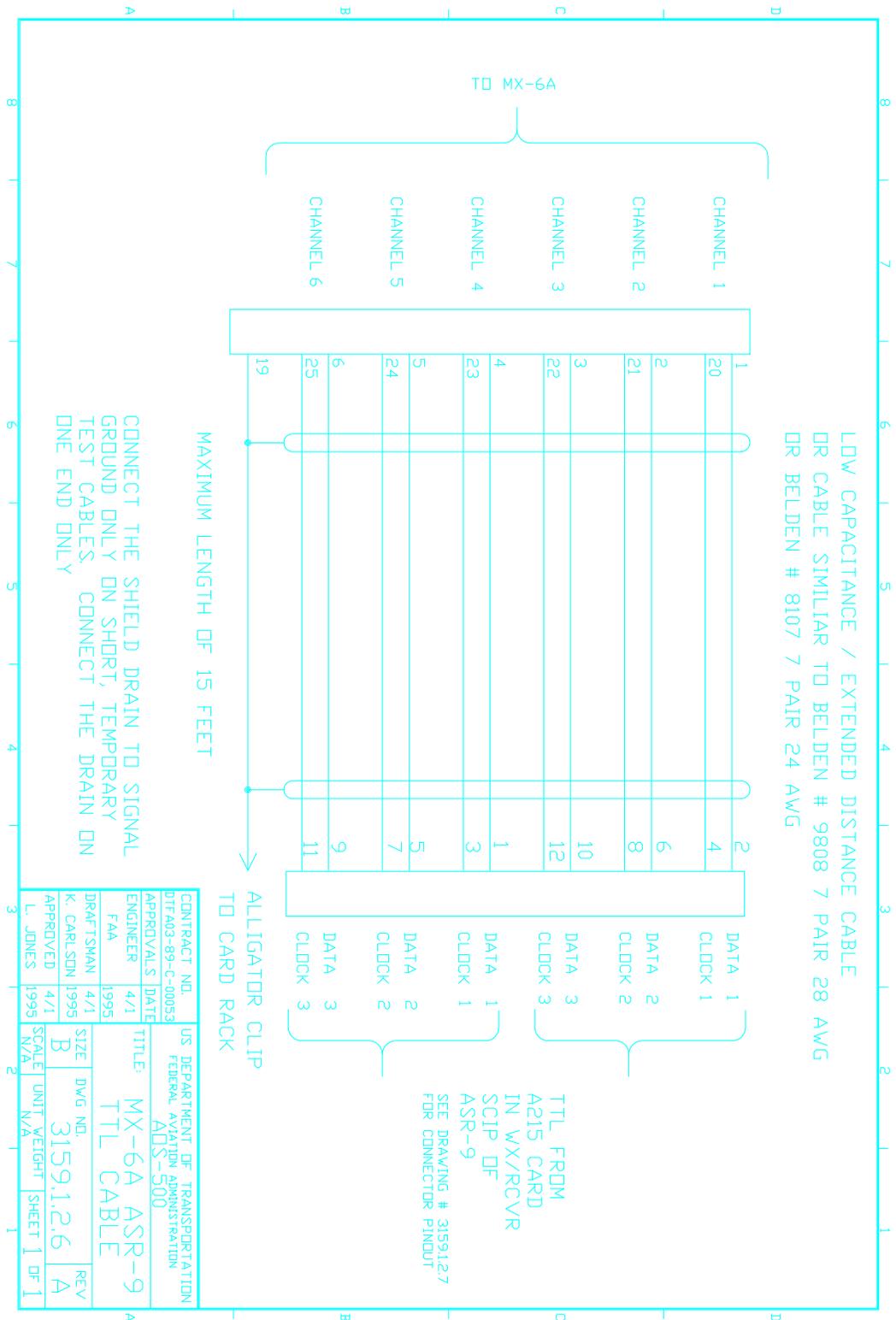


FIGURE 5. -11 ASR-9 TTL CABLE (DWG: 3159.1.2.6)

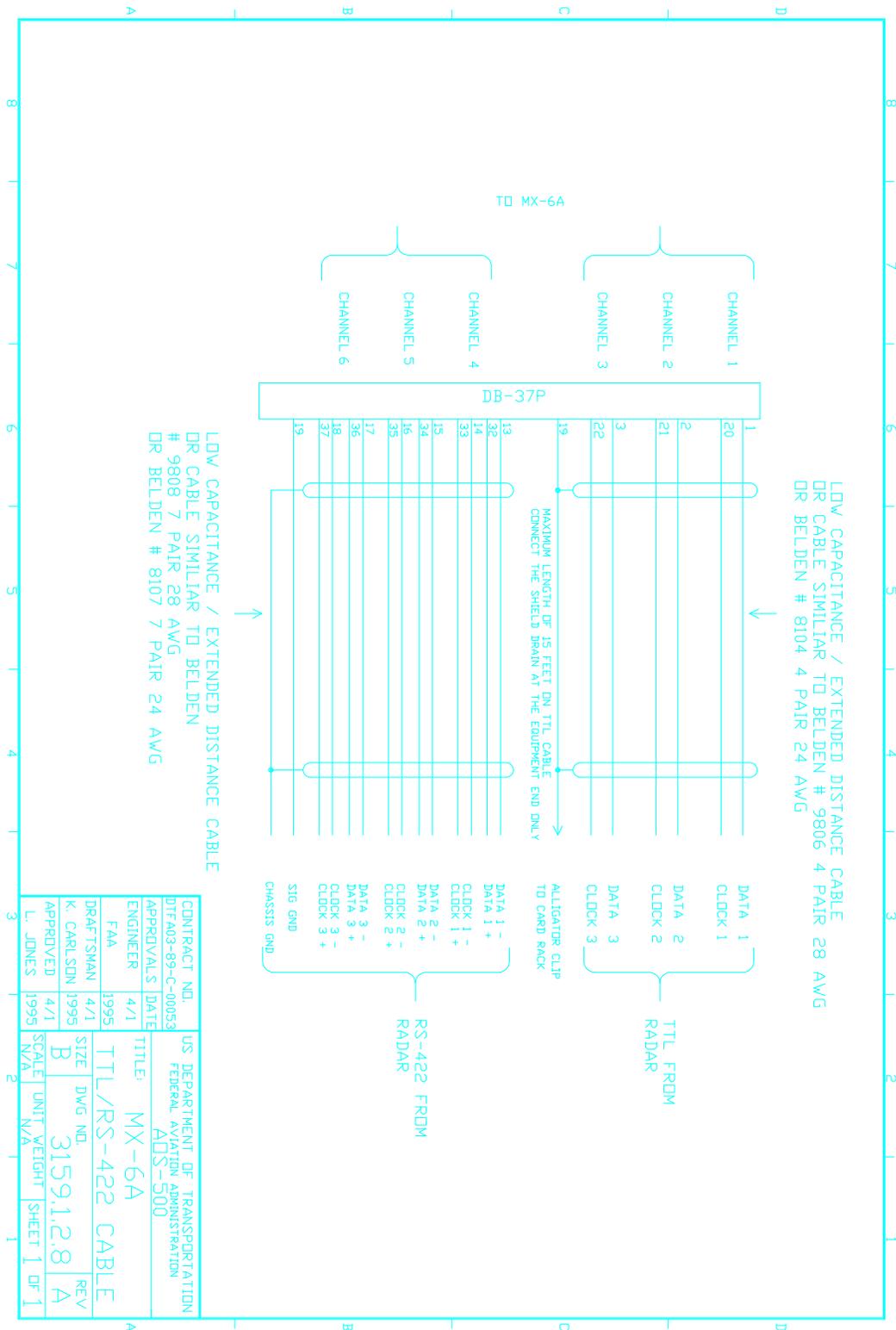


FIGURE 5. -12 TTL / RS-422 CABLE (DWG 3159.1.2.8)

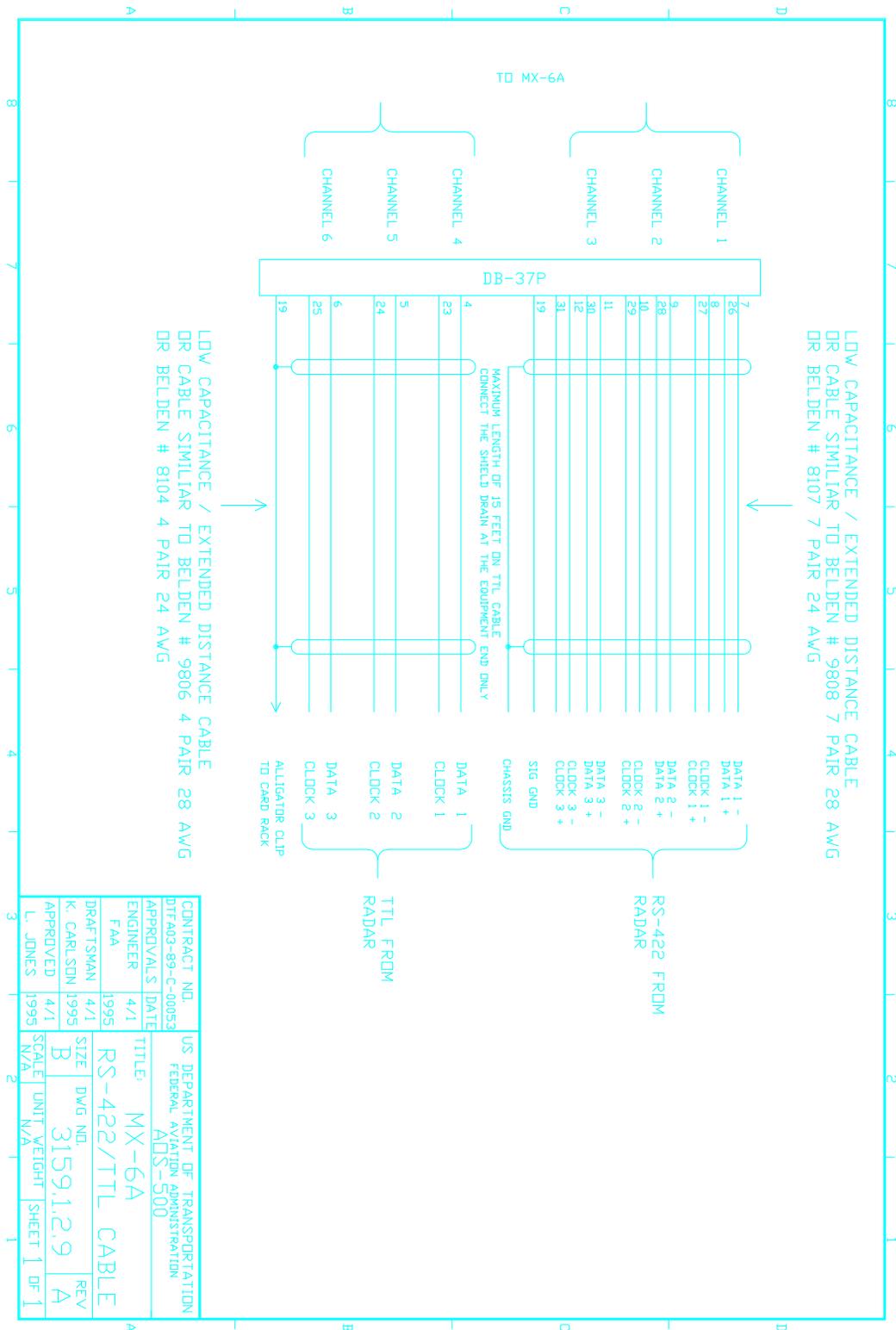


FIGURE 5. -13 TTL / RS-422 CABLE (DWG 3159.1.2.9)

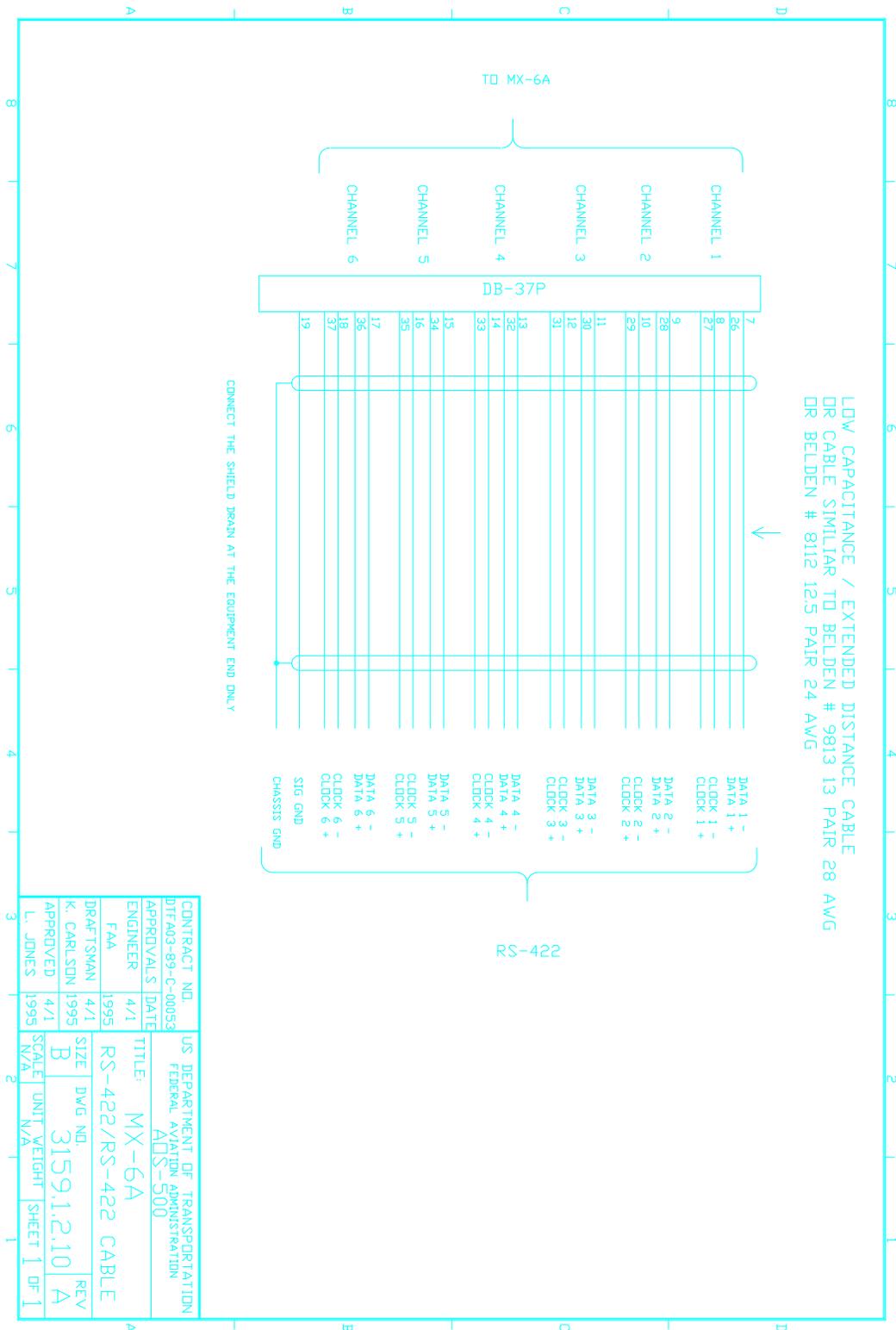


FIGURE 5. -14 RS-422 / RS-422 CABLE (DWG 3159.1.2.10)

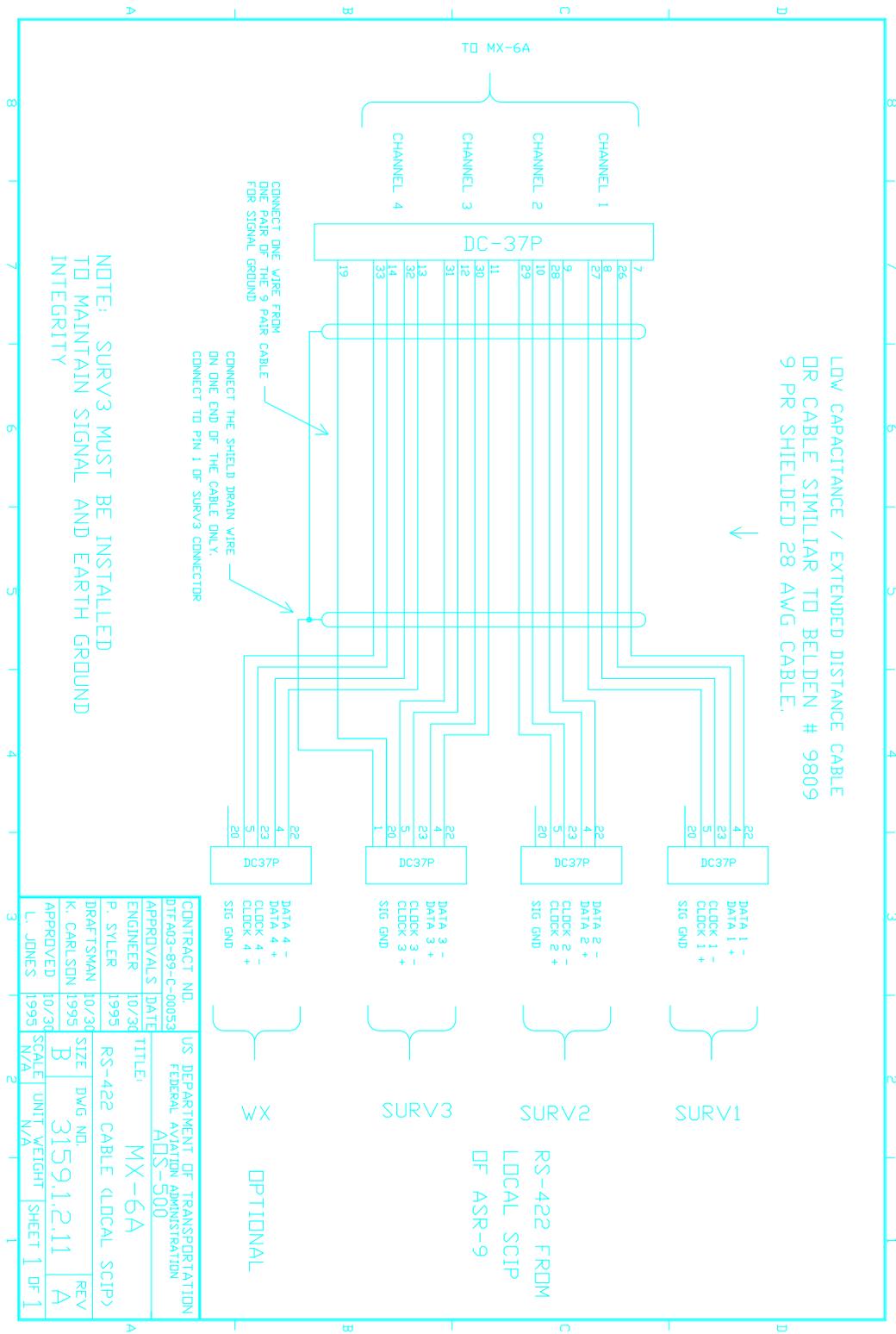


FIGURE 5. -15 RS-422 CABLE - LOCAL SCIP (DWG 3159.1.2.11)

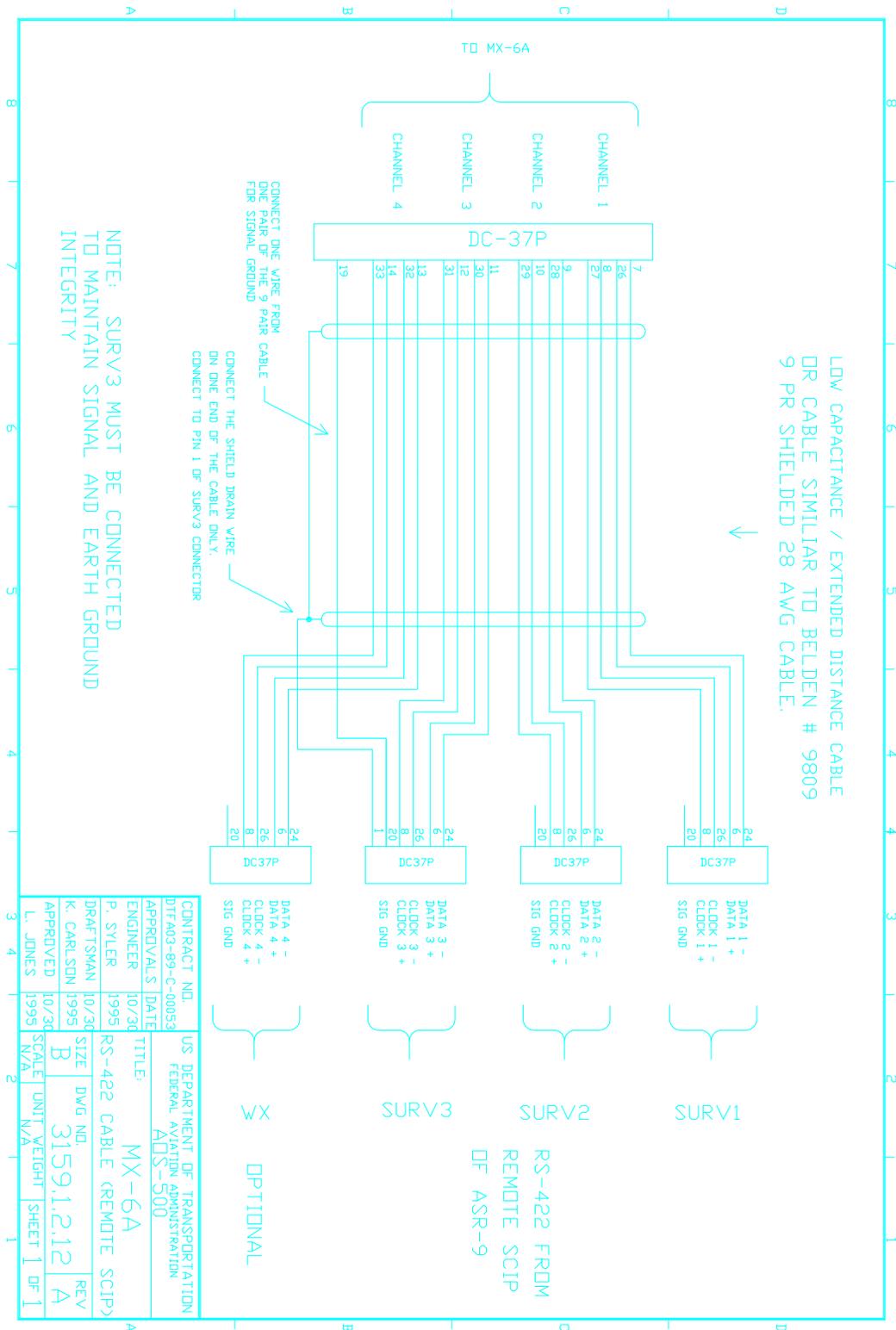


FIGURE 5. -16 RS-422 CABLE - REMOTE SCIP (DWG 3159.1.2.12)

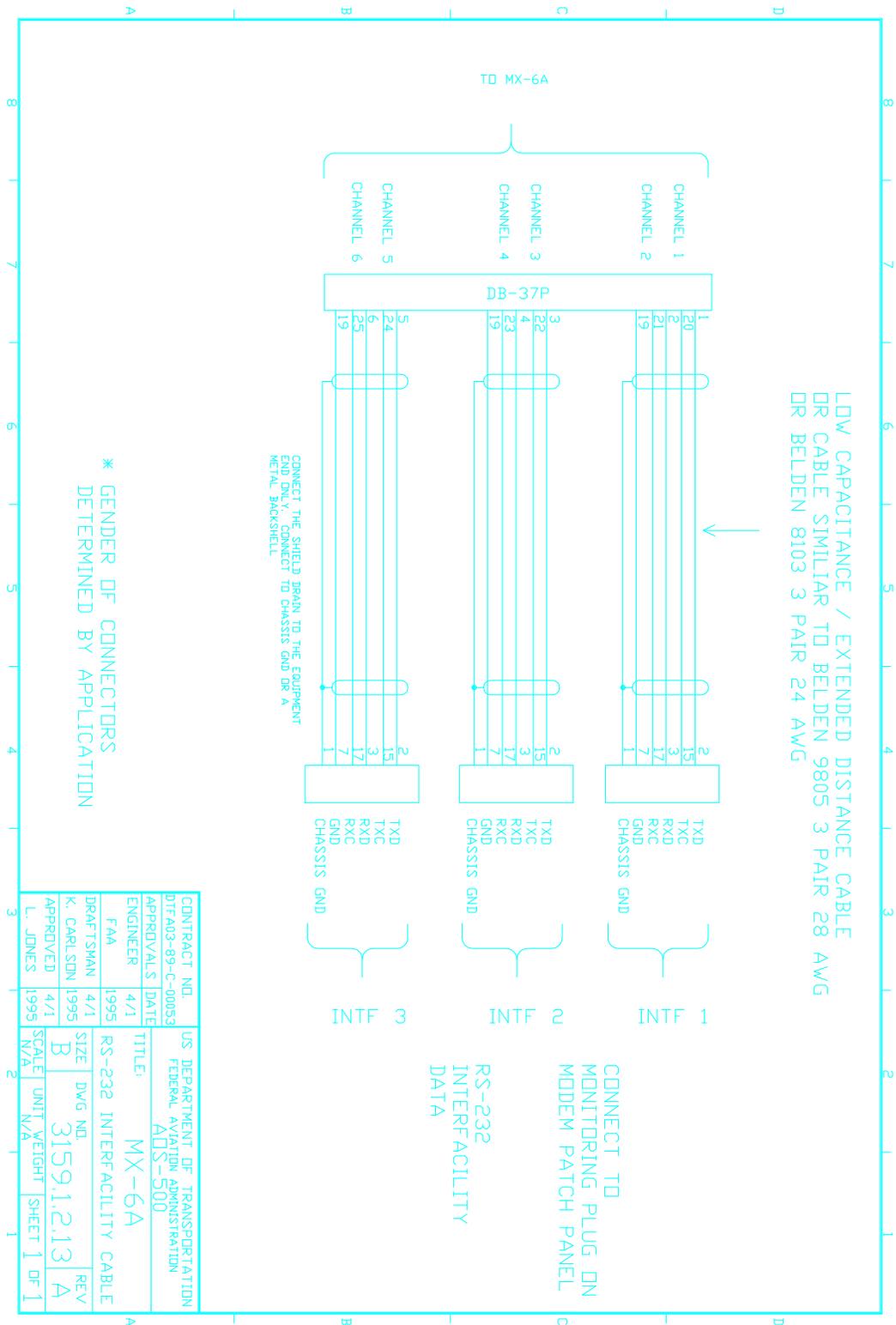


FIGURE 5. -17 RS-232 INTERFACILITY CABLE (DWG 3159.1.2.13)

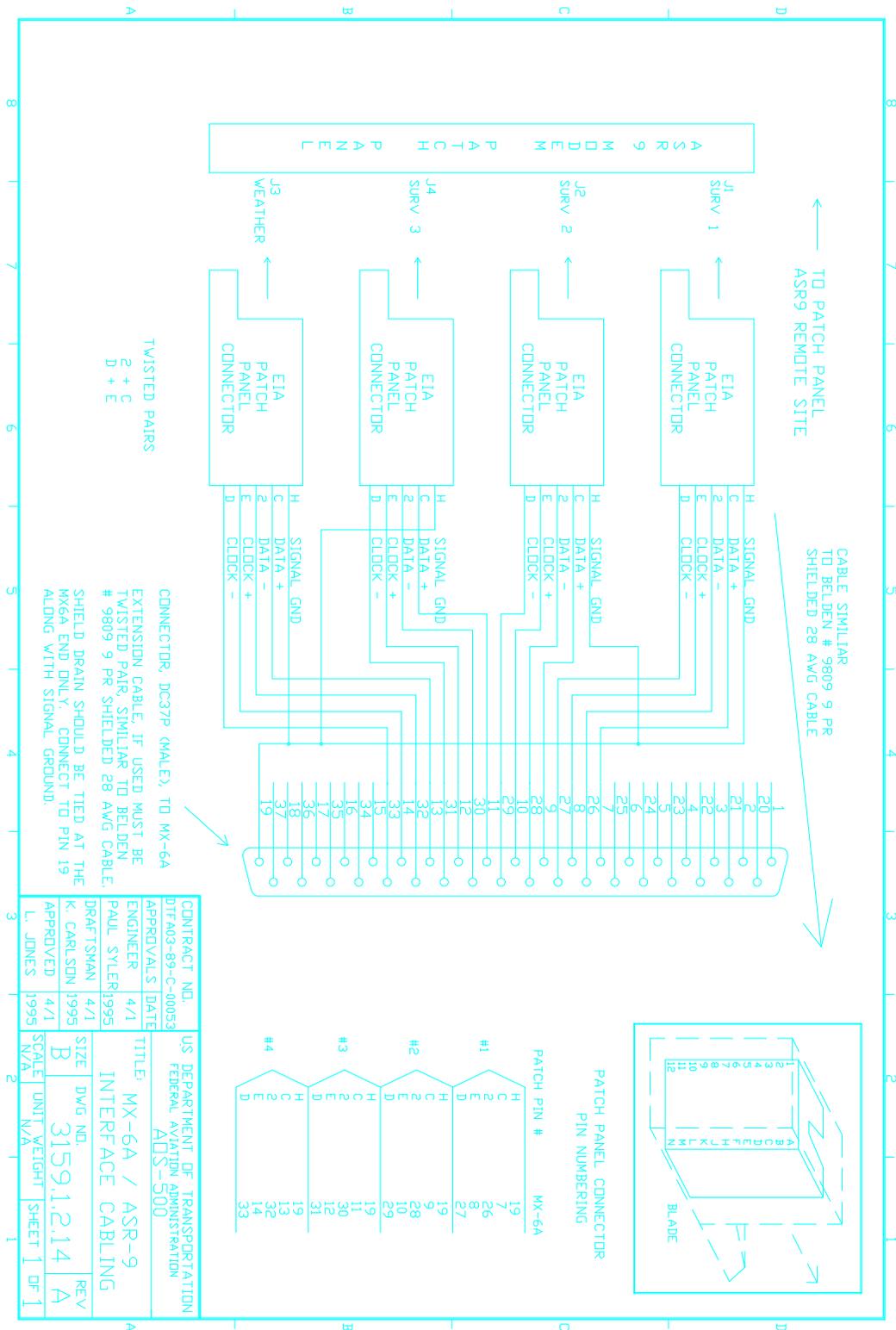


FIGURE 5. -18 ASR-9 INTERFACE CABLING (DWG 3159.1.2.14)

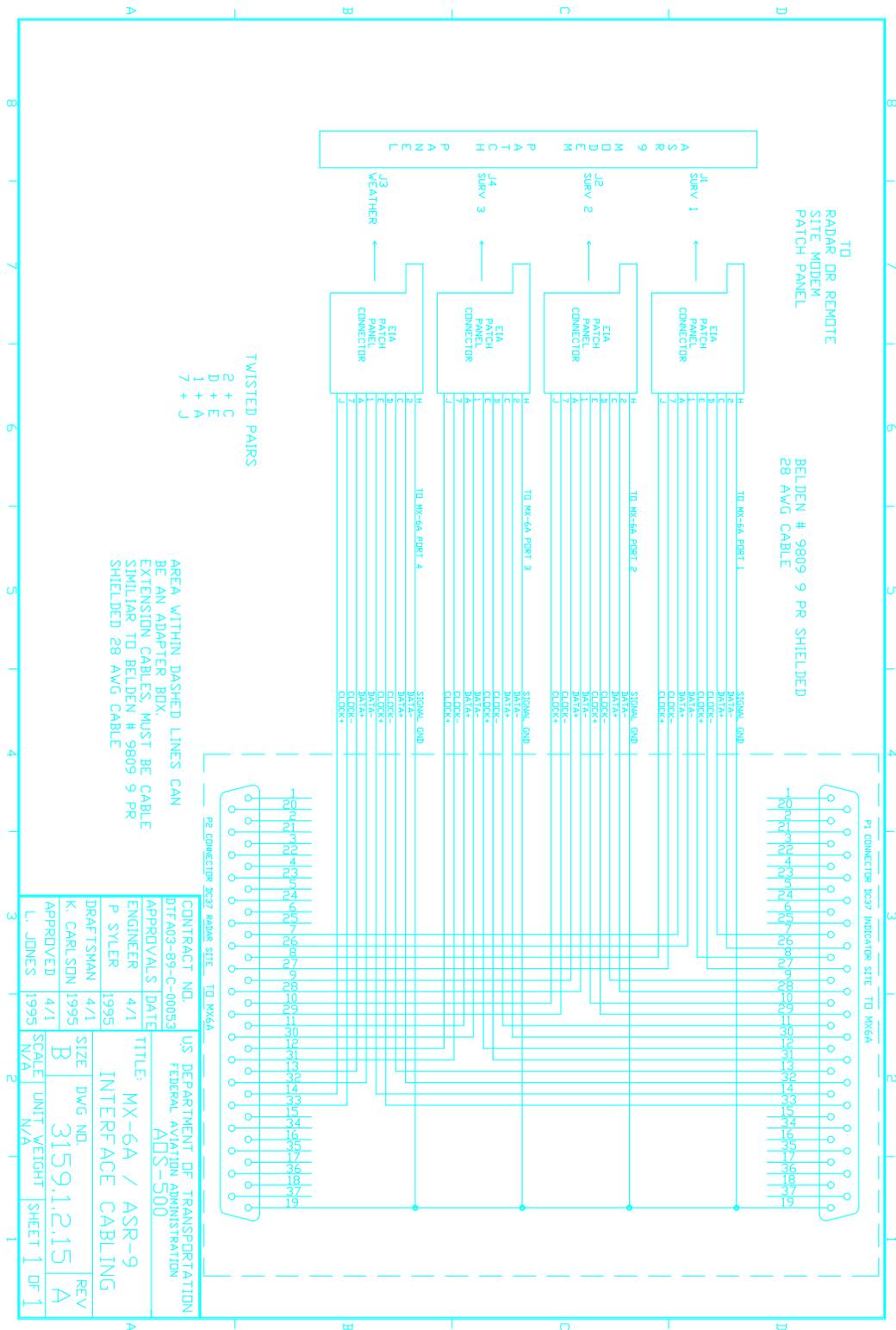


FIGURE 5. -19 ASR-9 INTERFACE CABLING (DWG 3159.1.2.15)

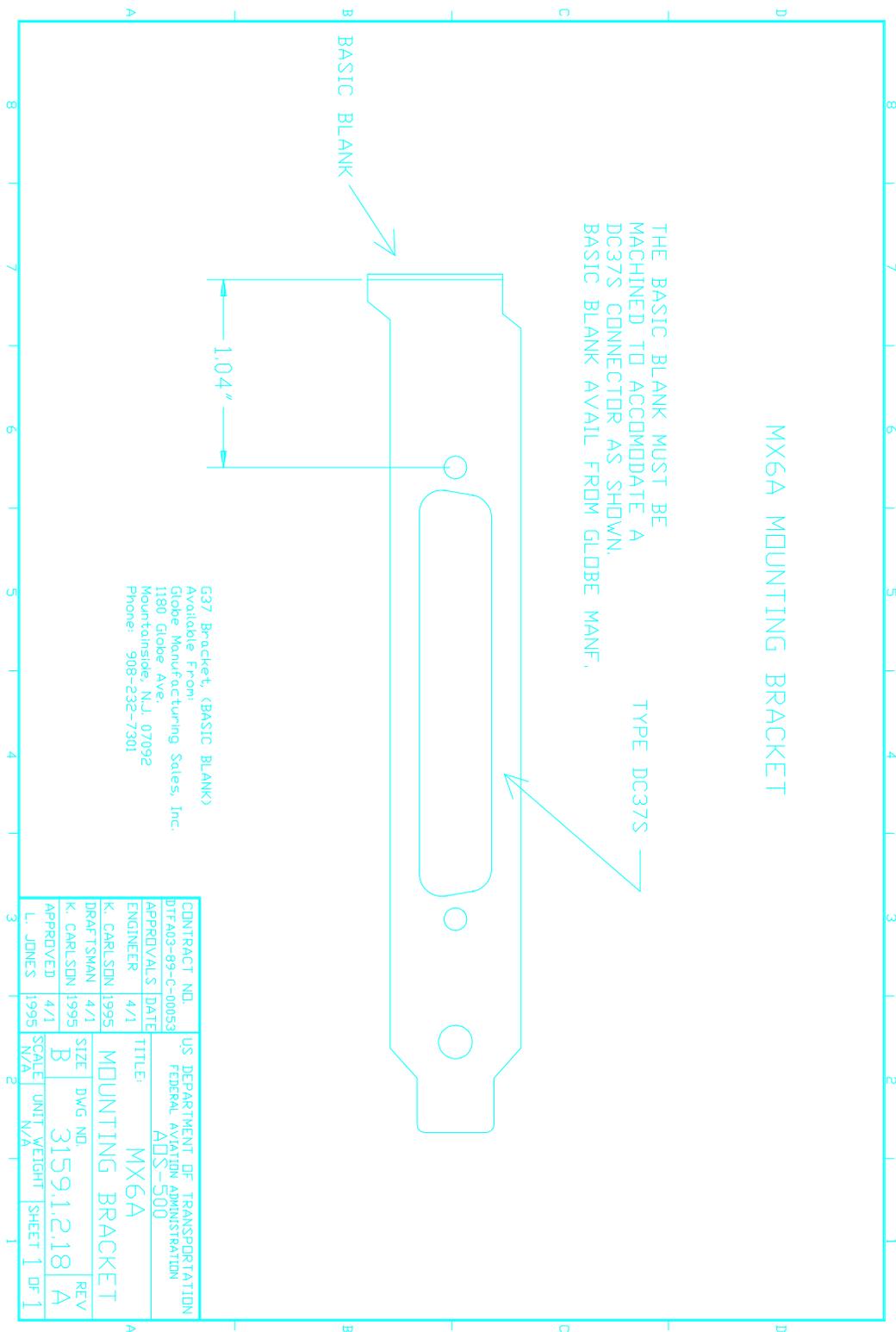


FIGURE 5. -20 MOUNTING BRACKET (DWG 3159.1.2.18)

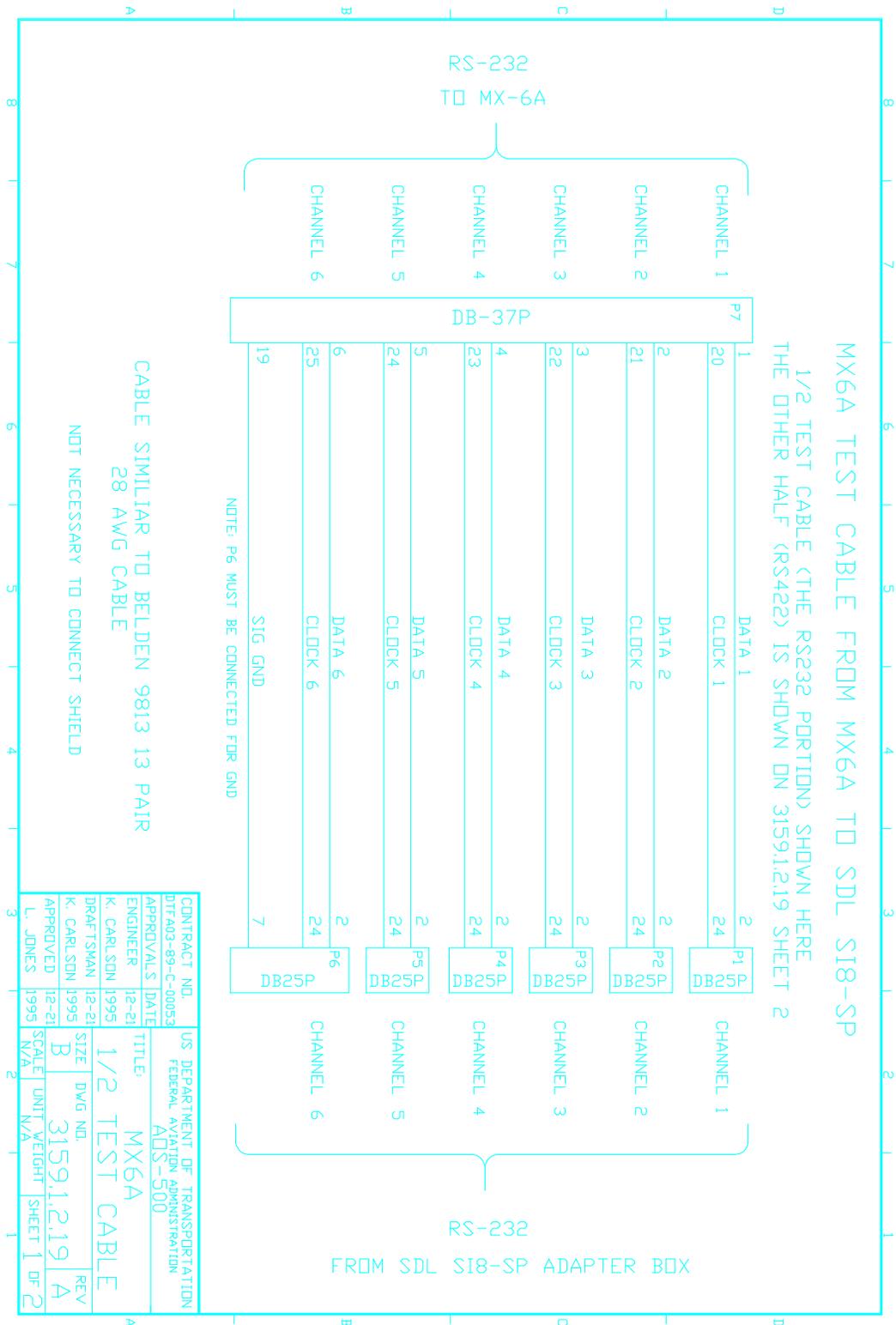


FIGURE 5. -21 RS-232 1/2 TEST CABLE (DWG 3159.1.2.19 SHEET 1 OF 2)

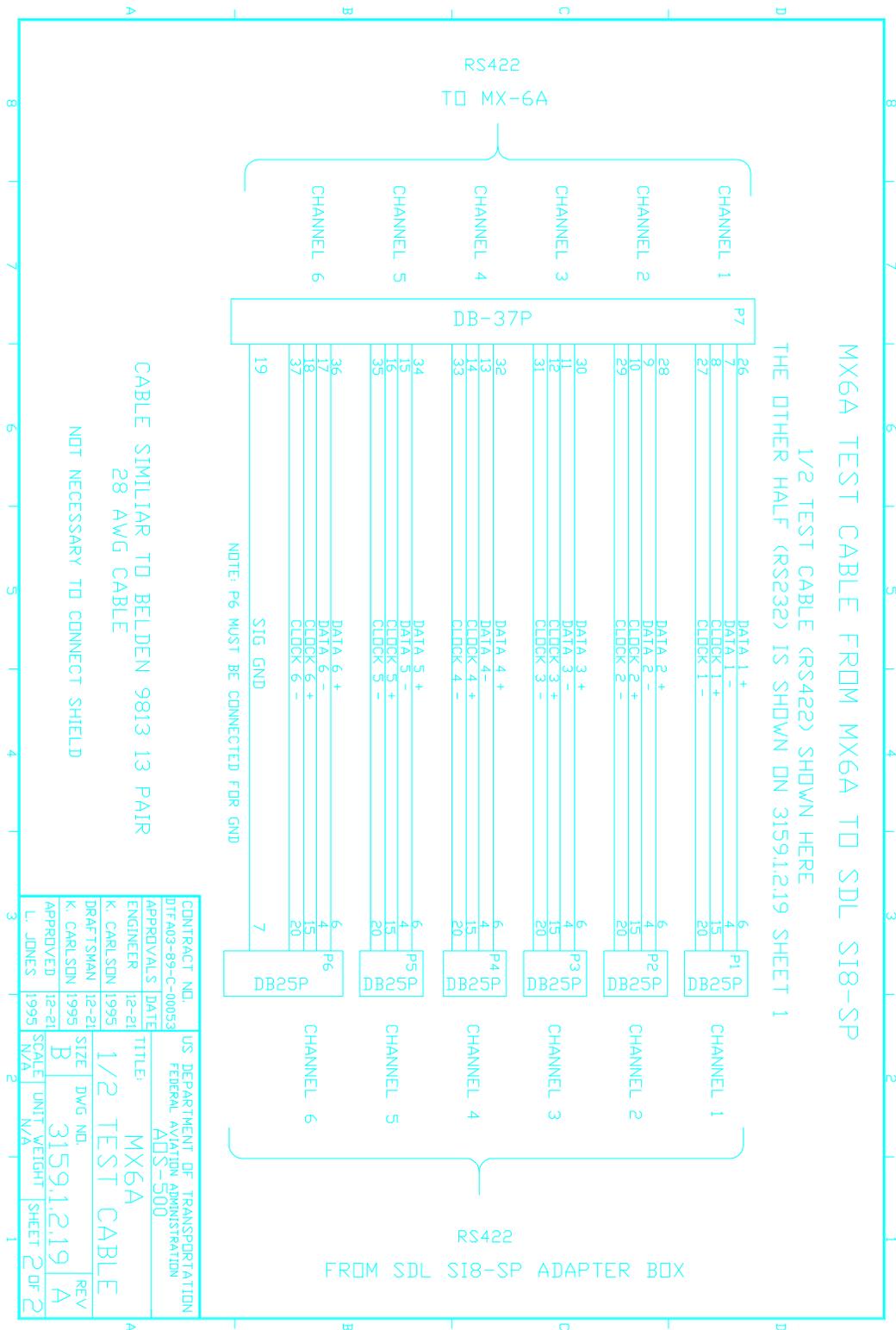


FIGURE 5. -22 RS-422 1/2 TEST CABLE (DWG 3159.1.2.19 SHEET 2 OF 2)

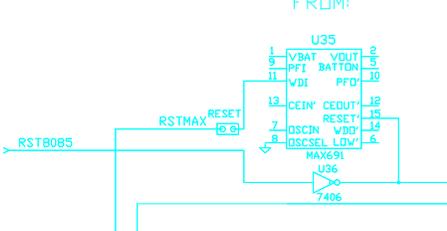
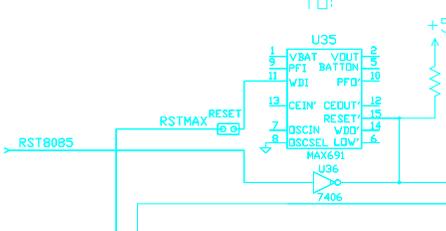
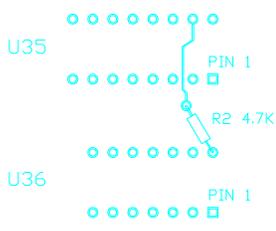
<h1 style="margin: 0;">ENGINEERING CHANGE ORDER</h1>		US DEPARTMENT OF TRANSPORTATION FEDERAL AVIATION ADMINISTRATION AOS-500																					
TITLE: MX-6A PCB ASSEMBLY DWG NO: 0064-01-02 REV B T C																							
1 ORIGINATOR K CARLSON DATE 12-21-95 REASON NO PULLUP RESISTOR AT THE RESET' OUTPUT OF U35, MAX691 WATCHDOG TIMER WHICH IS OPEN DRAIN OUTPUT.																							
2 DOCUMENTATION AFFECTED YES <input checked="" type="checkbox"/> NO <input type="checkbox"/> ON SHEET 2 OF THE PRINTS, COORDINATES C1, CHANGE FROM: 																							
TO: 																							
3 REWORK FINISHED GOODS Y <input checked="" type="checkbox"/> N <input type="checkbox"/> REWORK INSTRUCTIONS		4 PURCHASING AFFECTED Y <input checked="" type="checkbox"/> N <input type="checkbox"/> PARTS ADDED Y <input checked="" type="checkbox"/> N <input type="checkbox"/> PARTS DELETED Y <input type="checkbox"/> N <input type="checkbox"/> PARTS CHANGED Y <input type="checkbox"/> N <input type="checkbox"/> INSTRUCTIONS 1) 4.7K 1/8W Resistor R2																					
 <p style="text-align: center;">ON THE BACK OF THE BASEBOARD SOLDER A 4.7K 1/8W RESISTOR AS SHOWN BETWEEN PIN 14 OF U36 AND THE FEEDTHRU NEAR PIN 2 OF U35</p> <p style="text-align: center;">BACK OF BASEBOARD SHOWN</p>																							
COPIES <input checked="" type="checkbox"/> ORIGINATOR <input checked="" type="checkbox"/> Q ASSURANCE <input checked="" type="checkbox"/> ENGINEERING <input checked="" type="checkbox"/> PURCHASING <input checked="" type="checkbox"/> DOCUMENTATION <input checked="" type="checkbox"/> INVENTORY CONTROL <input checked="" type="checkbox"/> MANUFACTURING <input checked="" type="checkbox"/> CUST SERVICE		<table border="1" style="width: 100%; border-collapse: collapse; font-size: x-small;"> <tr> <td colspan="2">CONTRACT NO. DTFA03-89-C-00053</td> <td colspan="2">US DEPARTMENT OF TRANSPORTATION FEDERAL AVIATION ADMINISTRATION AOS-500</td> </tr> <tr> <td>APPROVALS</td> <td>DATE</td> <td colspan="2">TITLE:</td> </tr> <tr> <td>ENGINEERING K CARLSON</td> <td>12/22 1995</td> <td colspan="2">MX-6A ASSEMBLY</td> </tr> <tr> <td>MANUFACTURING</td> <td></td> <td colspan="2">DWG NO. 0064-01-02</td> </tr> <tr> <td>Q ASSURANCE</td> <td></td> <td>REV</td> <td>B T C SHEET 1 OF 1</td> </tr> </table>		CONTRACT NO. DTFA03-89-C-00053		US DEPARTMENT OF TRANSPORTATION FEDERAL AVIATION ADMINISTRATION AOS-500		APPROVALS	DATE	TITLE:		ENGINEERING K CARLSON	12/22 1995	MX-6A ASSEMBLY		MANUFACTURING		DWG NO. 0064-01-02		Q ASSURANCE		REV	B T C SHEET 1 OF 1
CONTRACT NO. DTFA03-89-C-00053		US DEPARTMENT OF TRANSPORTATION FEDERAL AVIATION ADMINISTRATION AOS-500																					
APPROVALS	DATE	TITLE:																					
ENGINEERING K CARLSON	12/22 1995	MX-6A ASSEMBLY																					
MANUFACTURING		DWG NO. 0064-01-02																					
Q ASSURANCE		REV	B T C SHEET 1 OF 1																				

FIGURE 5. -23 MX-6A ENGINEERING CHANGE ORDER (DWG 0064-01-02)

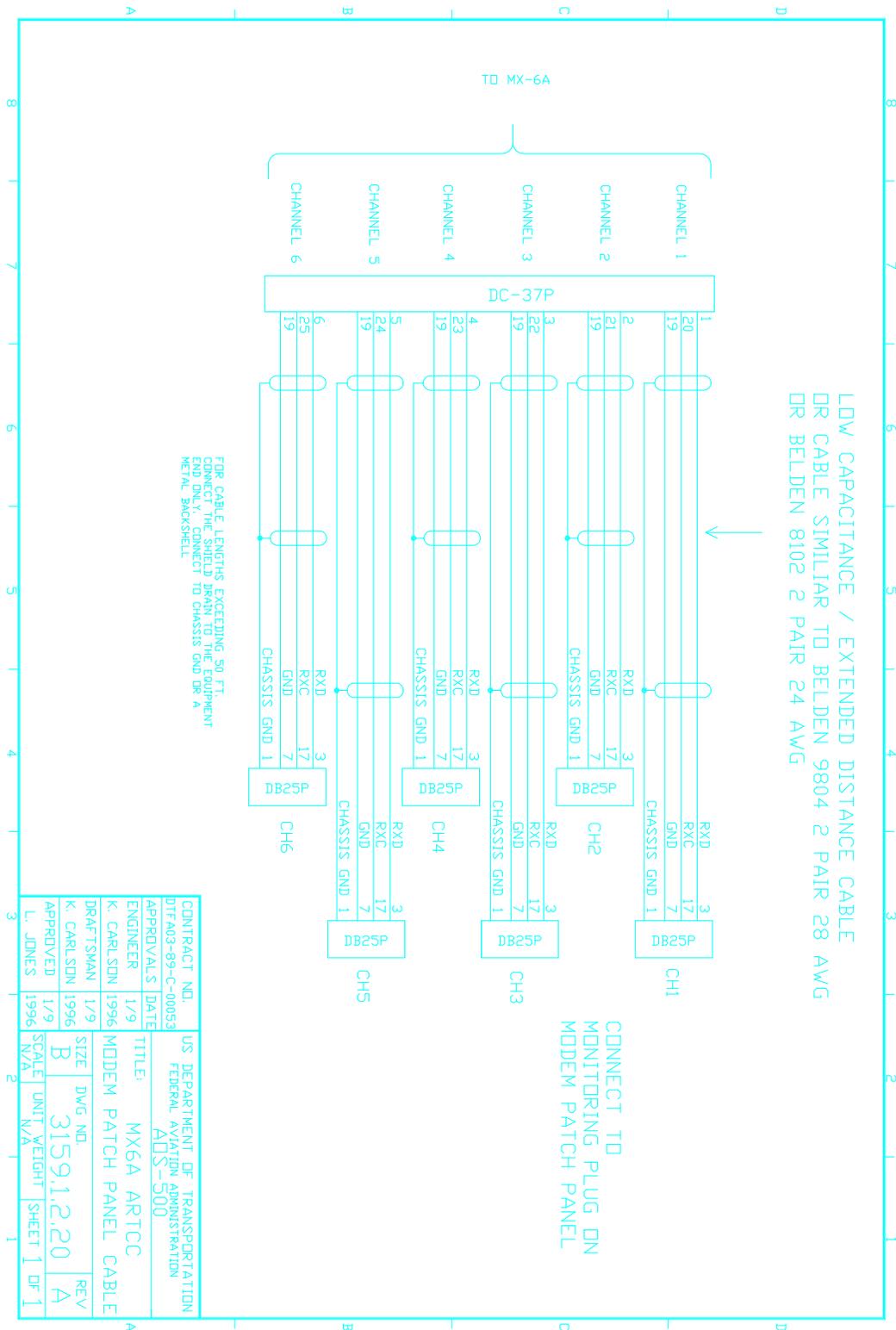
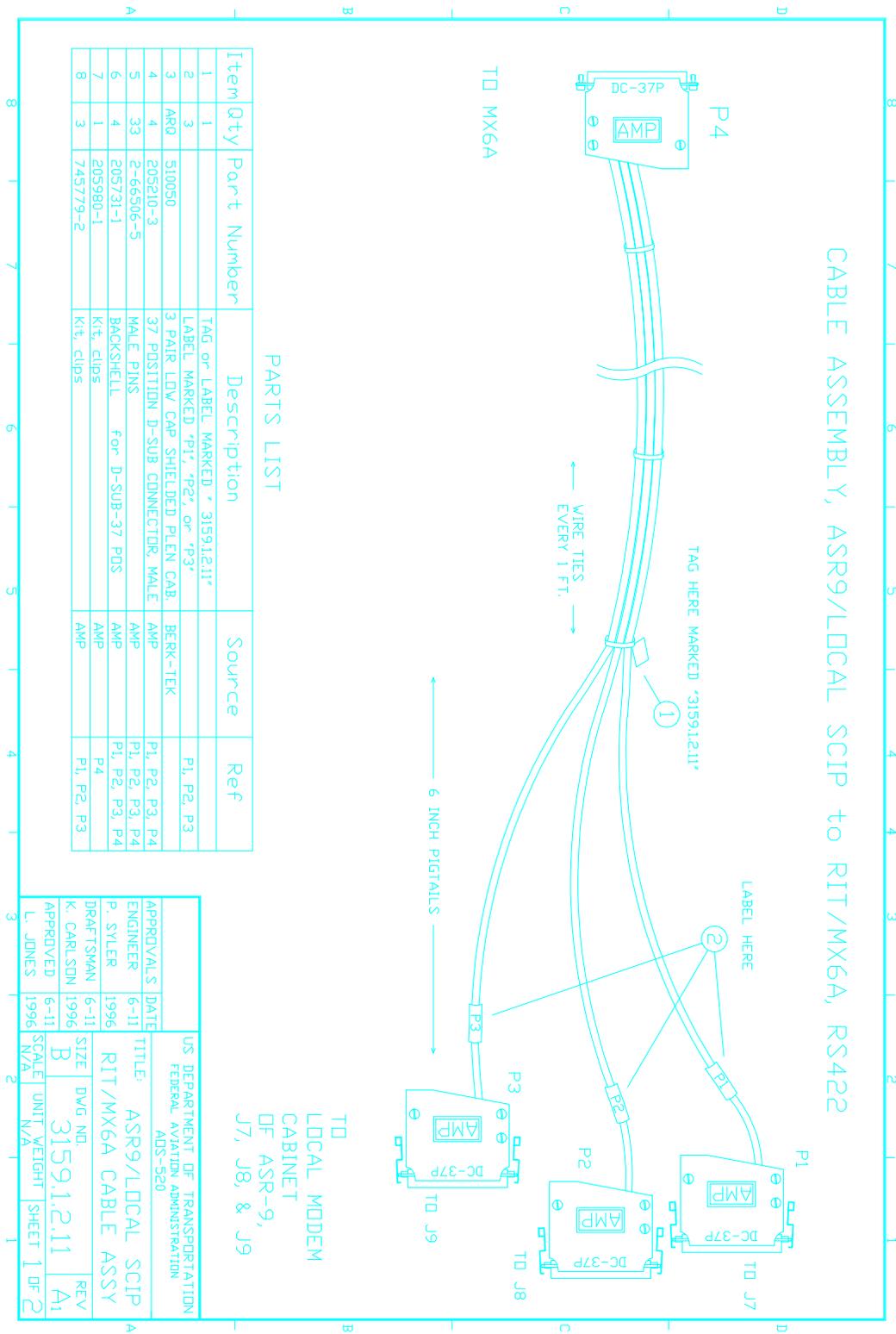


FIGURE 5. -24 ARTCC MODEM PATCH PANEL CABLE (DWG 3159.1.2.20)



PARTS LIST

Item	Qty	Part Number	Description	Source	Ref
1	1		TAG OR LABEL MARKED '3159.12.11'		P1, P2, P3
2	3	510050	LABEL MARKED 'P1', 'P2', OR 'P3'	BERK-TEK	
3	ARO		3 PAIR LEAD CAP. SHIELDED PLEN. CAB.	AMP	P1, P2, P3, P4
4	4	205210-3	37 POSITION D-SUB CONNECTOR, MALE	AMP	P1, P2, P3, P4
5	33	2-66506-5	MALE PINS	AMP	P1, P2, P3, P4
6	4	205731-1	BACKSHELL FOR D-SUB-37 PDS	AMP	P1, P2, P3, P4
7	1	205980-1	KIT, CLIPS	AMP	P4
8	3	745779-2	KIT, CLIPS	AMP	P1, P2, P3

US DEPARTMENT OF TRANSPORTATION FEDERAL AVIATION ADMINISTRATION ADS-520	
APPROVALS	DATE
ENGINEER	6-11
P. SYLER	1996
DRAFTSMAN	6-11
K. CARLSON	1996
L. JONES	1996
TITLE: ASR9/LOCAL SCIP RIT/MX6A CABLE ASSY	SIZE: DWG NO. 3159.12.11 SCALE: N/A
REV A1	SHEET 1 OF 2

TD LOCAL MODEM CABINET OF ASR-9, J7, J8, & J9

FIGURE 5. -25 ASR-9/LOCAL SCIP CABLE ASSEMBLY (DWG 3159.1.2.11 SHEET 1 FO 2)

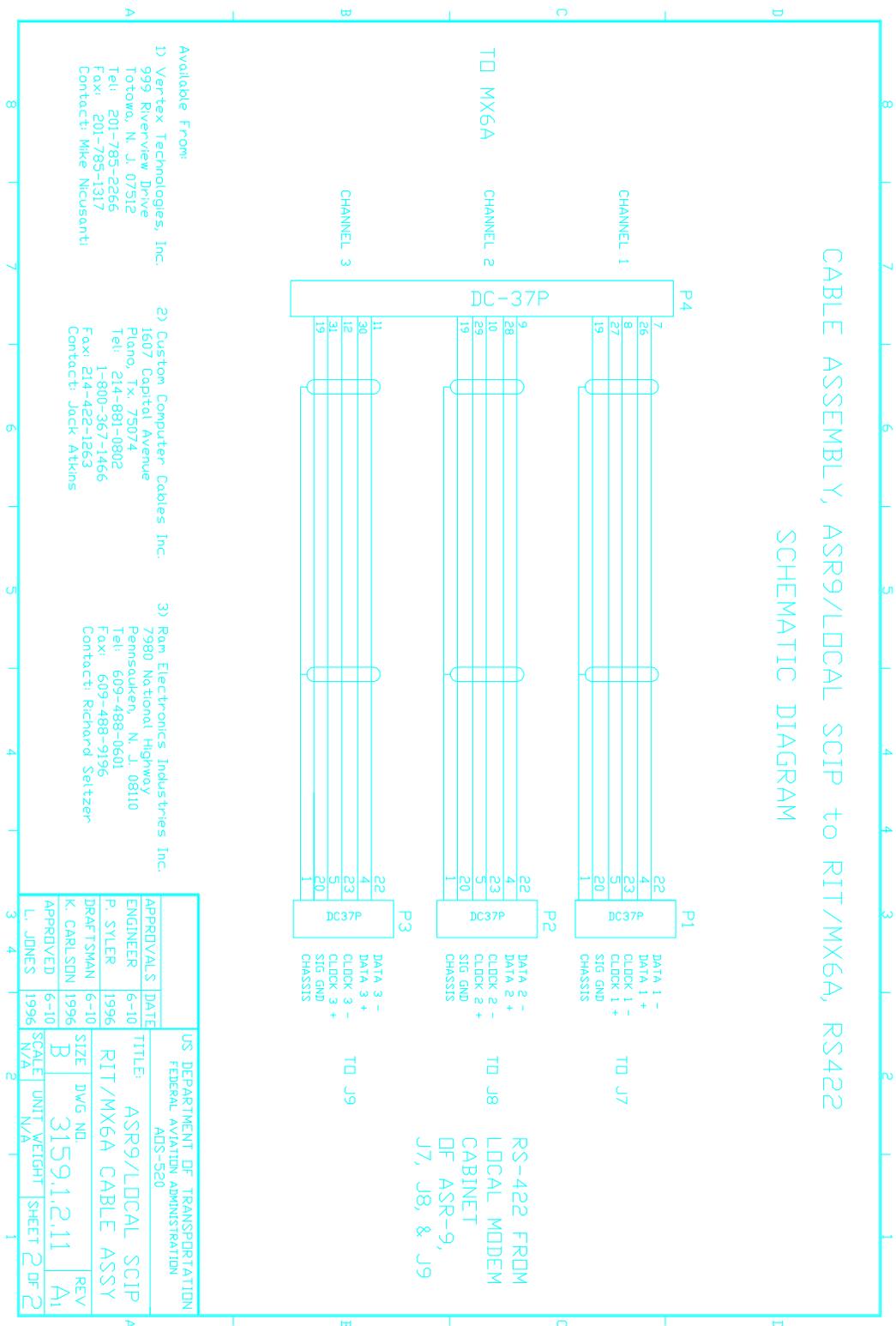


FIGURE 5. -26 ASR-9/LOCAL SCIP CABLE ASSEMBLY (DWG 3159.1.2.11 SHEET 2 FO 2)