SECTION D TROUBLESHOOTING ACCORDING TO FMT STATUS LINES

This section is intended to be used when a problem occurs during operation and a reject code is sent from the formatter (FMT) to the host/controller. The user can then refer to the reject code table, that reference the associated troubleshooting flow chart. Because the error could result from an operator mistake or a problem in the MTU, the user should evaluate the quickest method to correct the problem. All PCAs described in this section are located in the FMT unless otherwise noted.

If REJECT signal is asserted, the reject code is provided in error multiplex byte 2, bit 0 through 7.

* OP-INC (Operation Incomplete) is also set.

Table D.1 Reject codes

Octal	Description	Nick Name	Cause of Error	MAP No.
001	The addressed MTU is in On-line and Not Ready Status.	IRQ	OP-Miss	D0020
002*	A parity error is detected in the microprogram words.	CSPE	Hard Error	D1011
003*	A timeout of TRAK response to the first TREQ (more than 75 msec.) occurred on a WRT or LWR command.	WCZ	Hard Error	
004*	The FMT cannot analyze the cause of the microprogram trap.	UEX TRAP	Hard Error	
005	The addressed MTU is in File Protect Status when a WRT, WTM or ERS command is attempted.	FP	OP-Miss	
006*	The addressed MTU did not go to Erase Status only.	Set ERS	Hard Error	D1410
007	The addressed MTU is not in Write Status when DSE command is attempted.	DSE CRJ	OP-Miss	
010*	The addressed MTU did not go to Read Status.	Set RDS	Hard Error	D1410
011*	The tape subsystem does not have NRZI capability and no ID burst is detected.	NCAP NRZ	OP-Miss Hard Error	D0070
012*	The addressed MTU did not assert Gap Control Signal.	GAPC Error	MTU Hard Error	D1320
013	The addressed MTU is not in Online Status.	BUSY	OP-Miss	
014*	The addressed MTU did not go to Write Status after a WRT, WTM or ERS command is issued.	Set WRS Frror	MTU Hard Error	D1410

Table D.1 Reject codes (continued)

Octal	Description	Nick Name	Cause of Error	MAP No.
015*	Reserved.			
016*	The addressed MTU did not go to Backward Status.	Set BWD Error	MTU Hard Error	D1410
017*	Noise (possible data) was detected during an erase operation of a ERS or WTM command.	NOIS IN ERS	Tape Media Hard Error	D2100
020	Reversed.			
021*	Ready Status of the MTU was reset by the cause of TUC *2.	TUCK	OP-Miss MTU Hard Error	
022*	The PE or GCR ID burst was not written correctly.	IDB WRT Error	Tape Media Hard Error	D1230
023	A backward type command except a RWD or UNL command was issued, when a tape was positioned at BOT.	BWD BOT	OP-Miss	
024*	In the ARA burst just read the specified signal pattern was not detected and SAGC check was not reported by the MTU.	SAGC CIRCUIT Error	MTU Hard Error	D1260
025*	An IBG longer than 20 m was detected on a RD, FSP or FSF command.	20 m check	OP-Miss Hard Error	D0060
026*	LWRRW mode of the MTU could not be set.	Set LWR2 Error	Hard Error	D1420
027*	The instructed rewind operation was not initiated by the MTU.	Set REW Error	Hard Error	D1430
030*	The instructed density could not be reset.	Mode Set Error	Hard Error	D1410

Table D.1 Reject codes (continued)

Octal	Description	Nick Name	Cause of Error	MAP No.
031*	The Write Circuit Alarm of the MTU was detected during a positioning operation.	WCARM	Hard Error	
032*	After a tape motion was started, the tacho-pulse was not detected within the specified limit.	Tach Start Failure	Hard Error	D1320
033*	Reversed.			
034*	There was no IBG following the ID or ARA-ID burst within the specified distance.	IBG Non Detected	Tape Media Hard Error	D1255
035*	The addressed MTU attempted to backspace over a bad record just written or read but was unable to detect the record.	Missing Position	Tape Media Hard Error	D1460
036*	The ARA-ID was written correctly and could not be read back.	ARAID Write Error	Tape Media	D1230
037*	During the read back check of a WRT command, no data was detected.	No Block	Tape Media Hard Error	D1270
101	The addressed MTU is selected by another formatter.	USED	-	
102*	A parity error is detected in the microprogram reqister.	REGE	Hard Error	D1012
104*	Unexpected trap on MTU interface occurred.	UEX DV TRAP	Hard Error/ OP-Miss	
106*	The addressed MTU could not be set to Low Slice Level.	Set LOWSL	Hard Error	D1420

Table D.1 Reject codes (continued)

Octal	Description	Nick Name	Cause of Error	MAP No.
107	The requested command is invalid.	INVLD CODE	OP-Miss	
110*	The addressed MTU did not go to High Speed Mode.	Set HSP	Hard Error	D1420
111*	The MTU does not have CGR capability and attempted to read GCR tape.	NCAP GCR	OP-Miss	D0070
112*	After starting the command, the tape speed did not get up within acceptable limit till the specified length.	Velocity check	MTU Hard Error	D1330
113	The addressed MTU is not operational.	NOT INSTALL	OP-Miss	D0020
114*	LWR TUIF mode of the MTU could not be set.	Set LWR Error	MTU Hard Error	D1410
115*	During a backward motion after detecting the ARA-ID, BOT was not reached in the expected distance.	ARAID BRD Error	Tape Media	D1240
116*	The instructed disconnect FSF operation was not initiated by the MTU.	Set FSF Error	MTU Hard Error	D1420
121*	Ready Status of the MTU was reset by the Reset Key.	RST KY	OP-Miss	D1300
124*	During a SAGC operation, the gain adjustment of the Read Amplifier was not performed within the specified limit.	SAGC Check	Tape Media	D1260
125*	A high-up of a read or write operation was detected.	R/W OVRN	OP-Miss Hard Error	D1450

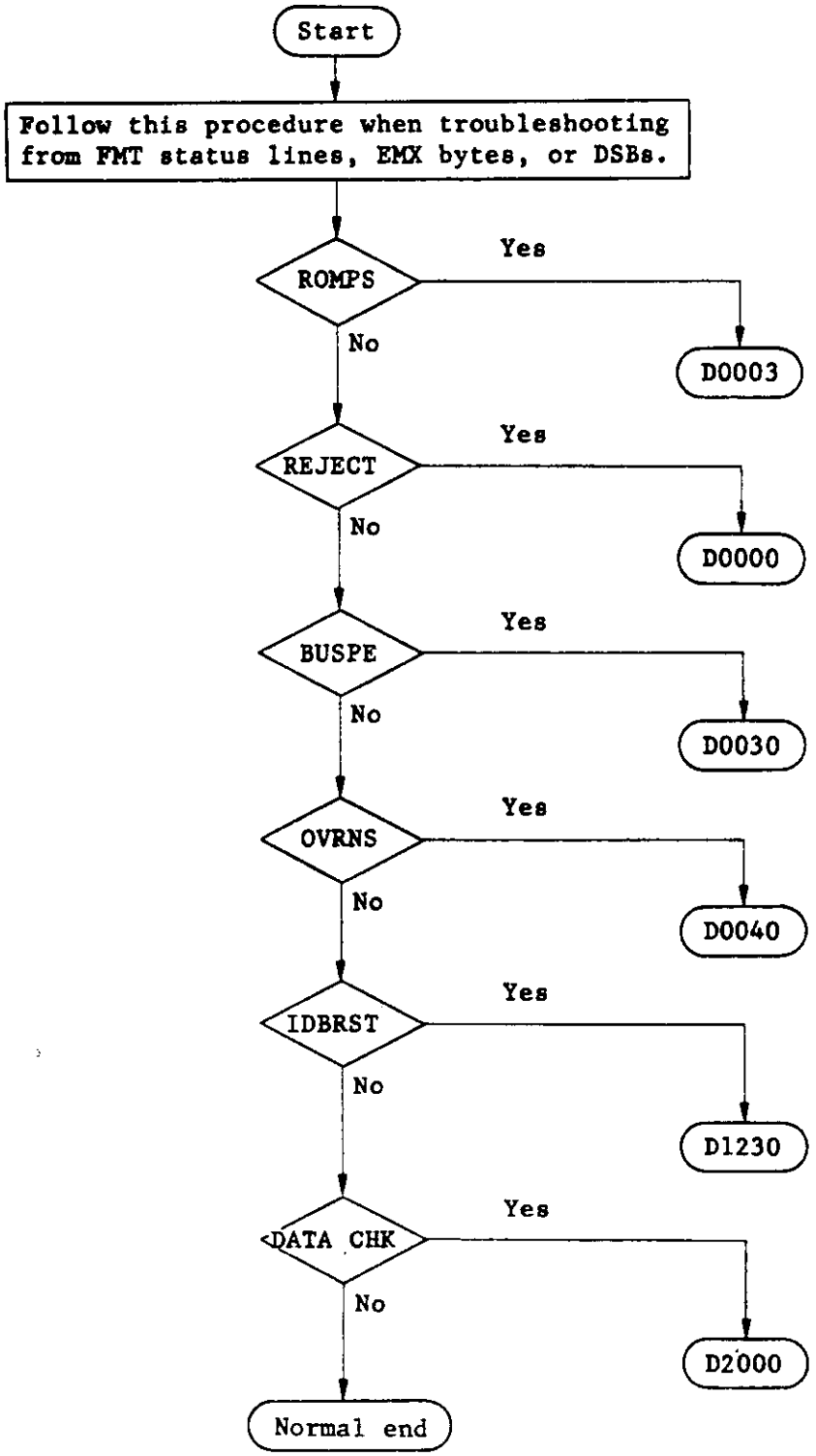
Table D.1 Reject codes (continued)

Octal	Description	Nick Name	Cause of Error	MAP No.
126*	LWRRW mode of the MTU could not be reset.	Reset LWR2 Error	Hard Error	D1420
127*	The instructed unload operation was not initiated by the MTU.	Set UNL Error	Hard Error	D1430
131*	The MTU was in High Speed Mode and in NRZI mode.	NRZI HSP	Hard Error	
132*	During a tape moving, the tacho-pulse was not detected within the specified limit.	Tach Stop	Hard Error OP-Miss	
133*	The Set ERM instruction was not performed.	Set ERM Error	Hard Error	D1430
137*	On a Write Tape Mark command, a tape mark was not written correctly with seven retry operations.	WTM Retry Out	Tape Media Hard Error	D1220
202	An abnormality of ALU circuit is detected.			
206*	The addressed MTU could not be reset from Low Slice Level.	Reset LOWSL	Hard Error	D1420
207	The condition of the MTU does not meet with the requested diagnostic operation.	DIAG NCAP	OP-Miss	
210*	The addressed MTU did not go to Normal Speed Mode.	Set NSP	Hard Error	D1420
211*	The command operation is attempted in the tape speed which does not meet the capability of VFO circuit.	VFO Not Capable	Install Miss	D0070

Table D.1 Reject codes (continued)

Octal	Description	Nick Name	Cause of Error	MAP No.
213	The corresponding ENABLE SWITCH to the MTU is set to Disable.	DISABLE	OP-Miss	D0020
214*	LWR TUIF mode of the MTU could not be reset.	Reset LWR Error	MTU Hard Error	D1410
215*	During a forward motion in a diagnostic mode EOT was detected.	DIAG EOT	OP-Miss	
216*	The instructed disconnect BSF operation was not initiated by the MTU.	Set BSF Error	MTU Hard Error	D1420
221	TAGIN response by the MTU was not detected within the specified limit.	TAG IN Check	Hard Error	D1440
226*	An error was detected in data of the MTU communication register.	Communication Reg Error	Hard Error	D1420
227*	The instructed DSE operation was not initiated by the MTU.	Set DSE Error	Hard Error	D1430
233*	Dynamic Reversal Error was detected.	DYRV	Hard Error	D1310
302	An abnormality is detected in a part of the formatter hardware during Power-On diagnostics, Test Formatter operation or Patrol diagnostics.	DIAGE	Hard Error	
316*	Some manual handling has done to the MTU in Skip File command before TMS is reported. And now the MTU is in Ready Status.	SKIPF Error	OP-Miss	D1465
327*	TUC or TUINT in the MTU could not be reset.	Reset TU Error	Hard Error	D1410

D0001	FMT Status Line Troubleshooting Flowchart



D0002	Error Multiplex and Drive Sense Bytes (DSB)

The formatter status lines are as follows:

(1) Reject (REJECT)
(2) Operation incomplete (OP-INC)
(3) ROM parity error (ROMPS)
(4) Data bus parity error (BUPER)
(5) Overrun status (OVRN)
(6) Data check (DCK)
(7) ID burst (ID BRST)
(8) Corrected error (CRERR)

Table D.2 Error multiplex bus decode

MUX byte	Error multiplex bit									Description
	P	7	6	5	4	3	2	1	0	
0	DTP	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	Dead tracks
1	CRC ERR	WTM CHK	UCE	PART REC	MLT ERR	MISC DATA ERR	END DATA CHK	VEL ERR	DIAG MODE	Read/write errors
2	TACH	RJC7	RJC6	RJC5	RJC4	RJC3	RJC2	RJC1	RJC0	Reject code
3	WRTS	EOTS	BOTS	NSPM	PROS	BWDS	HDNS	RDYS	ONLS	Drive sense byte 0
4	Reserved									
5	Reserved									
6	Reserved									
7	Reserved									

Table D.3 Drive sense bytes

Bit byte	P	7	6	5	4	3	2	1	0
DSBO	WRTS	EOTS	BOTS	NSPM	FPS	BWDS	HDNS	RDYS	ONLS
1	'0'	'1'	'1'	D1	D0	'0'	M2	M1	M0
2	'0'	'0'	'0'	S1	S0	'0'	'0'	'0'	'0'
3	'0'	TUC	Reset key	DSE	Test mode	SAGC count			
4	'0'	HERS	HACT	HBWD	HWCON	H65S	TOVR	H1600	TMD
5	'0'	MISC error	TLA left	TLA right	ROM parity error	Write circuit alarm	'0'	Air bearing alarm	Load failure
6	'0'	MTU error code							
7	LWR TUIF	Stream-ing function	Skip File function	High speed mode	Low slice mode	Slice level 0 1 2			LWR RW
8	'0'	TU unique ID high order							
9	'0'	TU unique ID low order							
10	'0'	FMT function ID							
11	'0'	IBG detect	Start read check	CRC III check	Early begin read back check	SAGC check/ noise error	Slow begin read back check	Slow end read back check	PCMP
12	'0'	X-call	800 BPI feature	LWR FMT	Velo-city retry	SKEW error	WEC over-flow	Enve-lope check	Write trigger VRC
13	'0'	2^7	Write error count						2^0
14	'0'	FRU1							
15	'0'	FRU2							

D0002	Error Multiplex and DSB

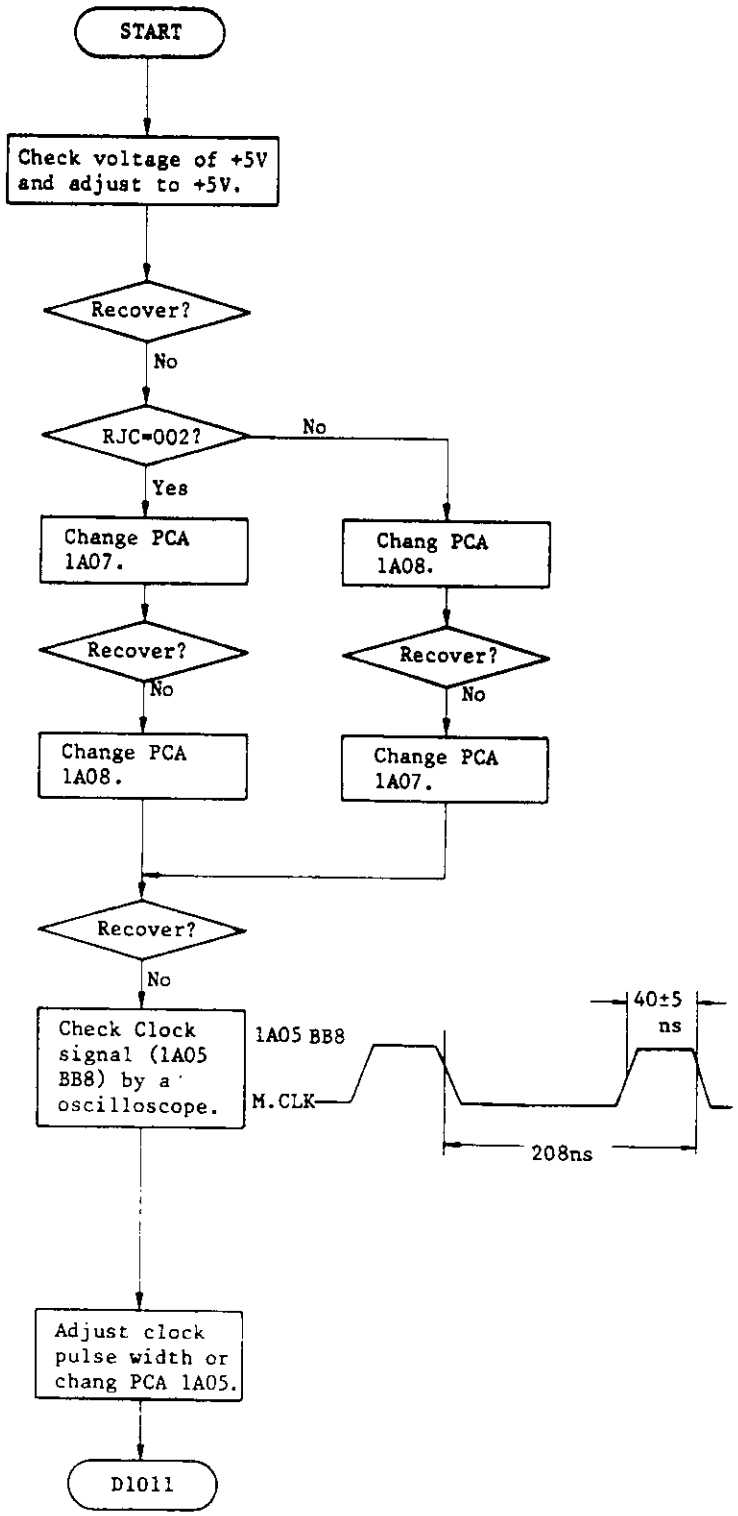
FRU refers to a field replaceble unit. When cyclic redundancy (CRC) error in error multiplex byte 1 is set or PCMP in drive sense byte 11, FRU1 and FRU2 have the following meaning:

	P	7	6	5	4	3	2	1	0
FRU1	'0'	'0'	'0'	'0'	'1'	'0'	AB reg parity C	DB check	Write BOC
FRU2	'0'	Unmatch CRC	Unmatch CRC zoro	EP ≠ CR	B ≠ D	B ≠ C	Unmatch CRCC	A ≠ B	XBIC

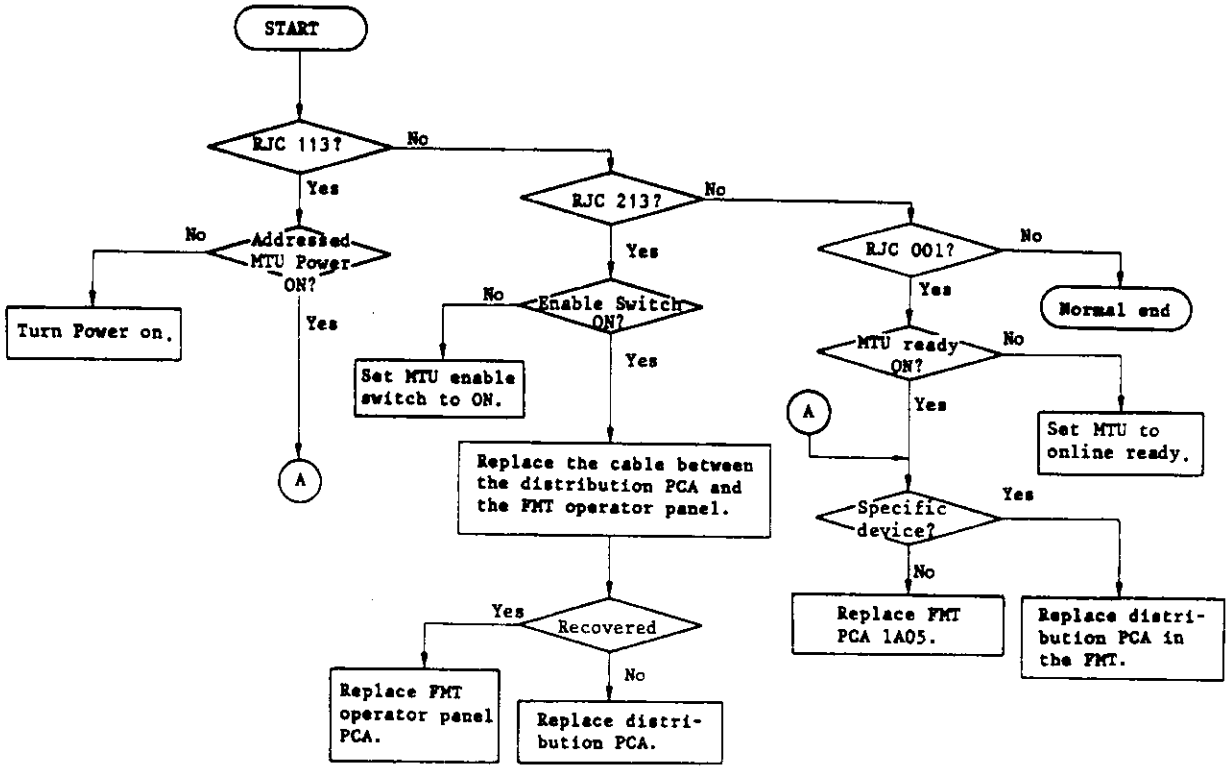
D0003	ROM Parity Error

This error signal is asserted when there is an incorrect parity word in microprogram control storage (EPROM), or an incorrect parity byte in local storage register (RAM). When the above error occurs, microprogram traps address "00E0" and loops to waiting START signal.

Reject Code (RJC) Octal (002) ..... EPROM Parity Error
Reject Code (RJC) Octal (102) ..... RAM Parity Error



D0020	Intervention Required (Reject Codes 001, 113, 213)



D0030	Data Bus Parity Error - 1

Parity error is detected in transferred data from or to the controller through bi-directional data bus.

(1) Write or loop-write-to-read command:

Data transferred from the controller is checked at the receivers of bi-directional data bus. The check timing is the same as data setting timing to bus out register. If this error occurs, data check will be set. MUX byte 1; bit P, CRC ERROR, and bit 3, MISC DATA ERROR will be set.

(2) Read or read backward command:

Read data transferred from the FMT is checked through receivers at the reading edge of TRAK signal. Generated parity bit is added to the input data to the drivers of bi-directional data bus.

(3) SDIA command:

Diagnostic flag bytes transferred from the controller is checked in the same manner as the write command. It is checked when TREQ and TRAK signals are asserted.

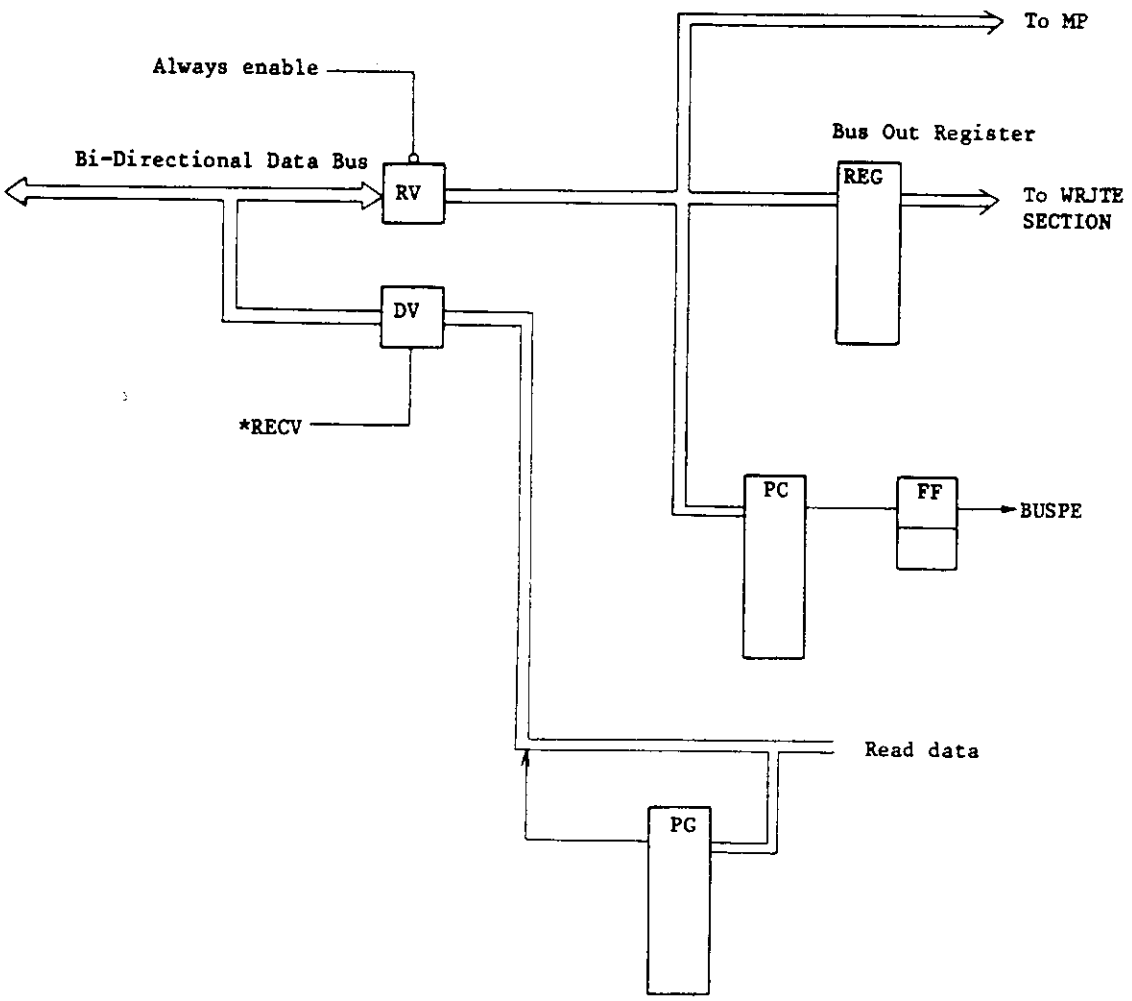
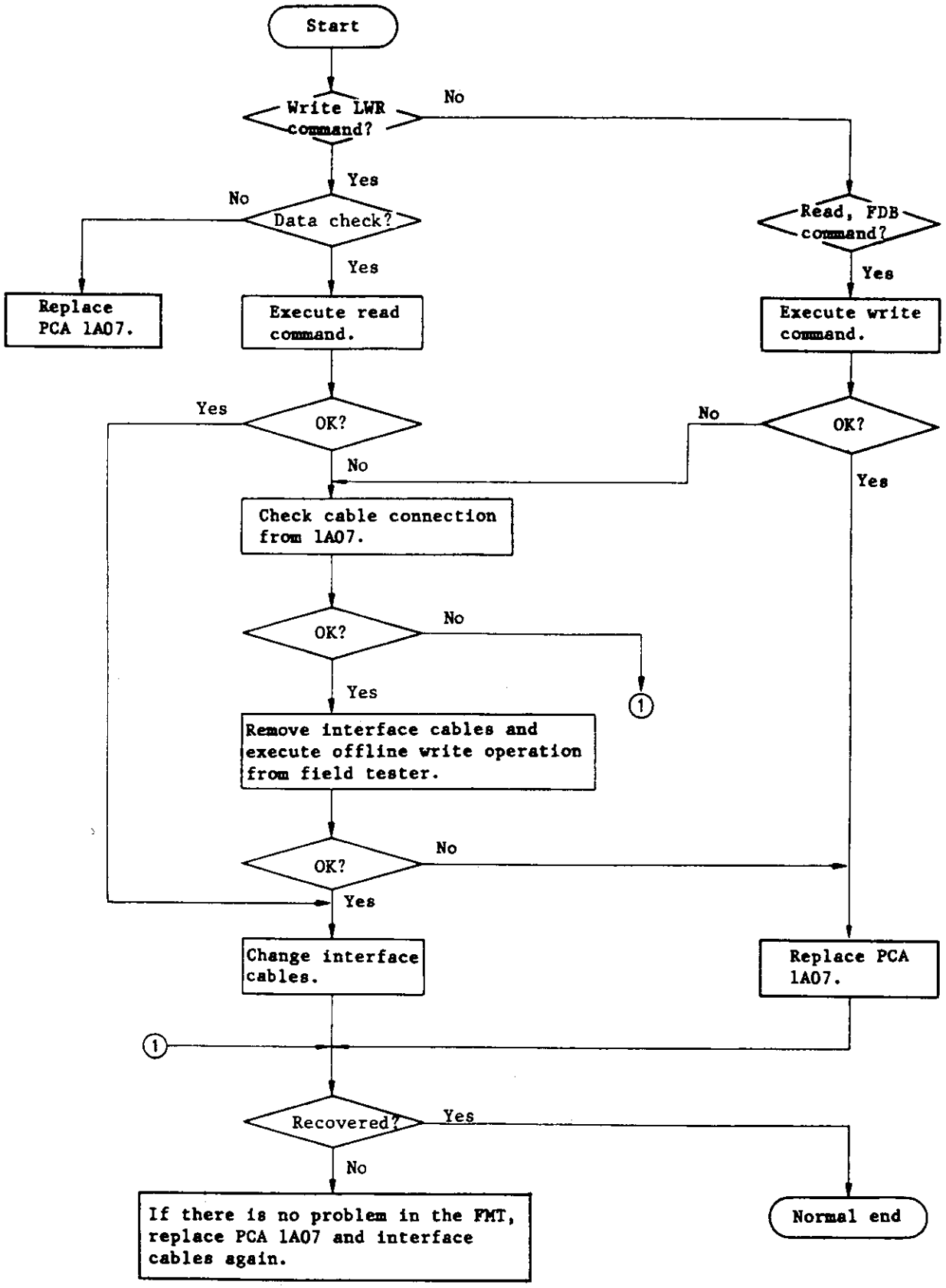


Figure D.1 Data bus parity error detection circuit

D0031	Data Bus Parity Error - 2



D0040	Overrun Status

This error is reported when controller has not responded to transfer request within the capability of data transfer buffer.

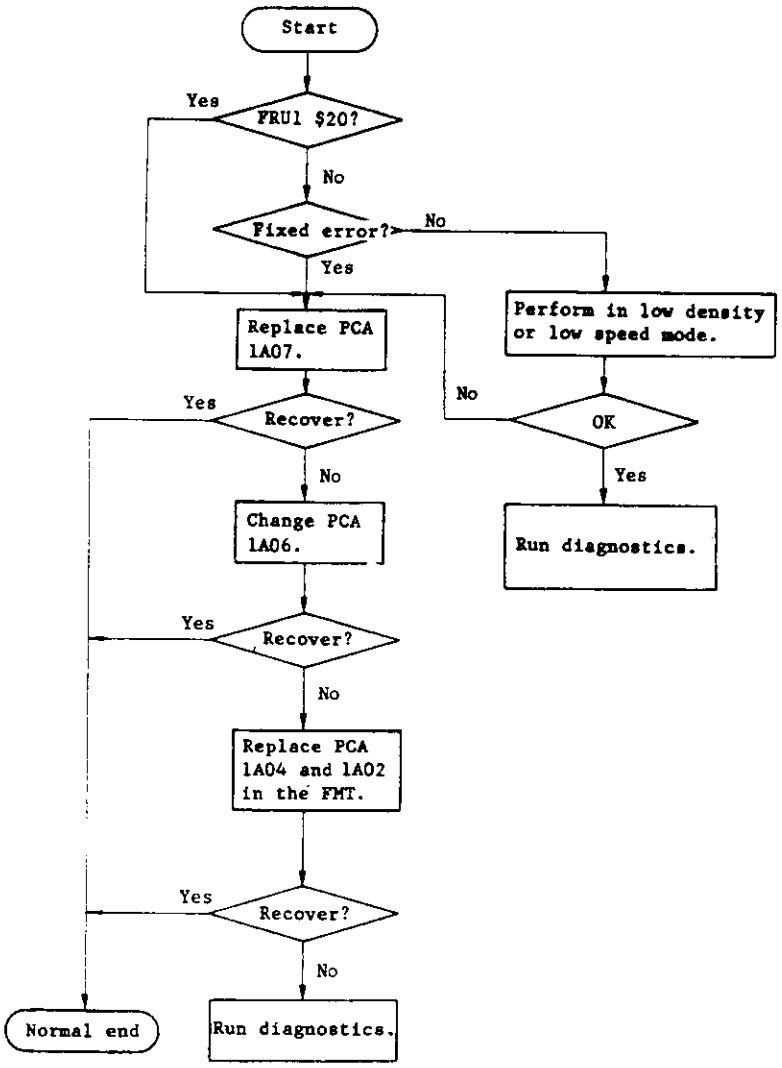
FRU1 (SB14) $21
FRU2 (SB15) The content of XCTL register

(1) In the write or loop-write-read command, this error will be set if the amount of data in the transfer buffer becomes less than 6 bytes (in 6250 BPI mode) or zero byte in 1600/800 BPI mode) before receiving stop signal.

(2) In the read or read backward command, this error will be set if transfer buffer becomes full during reading data.

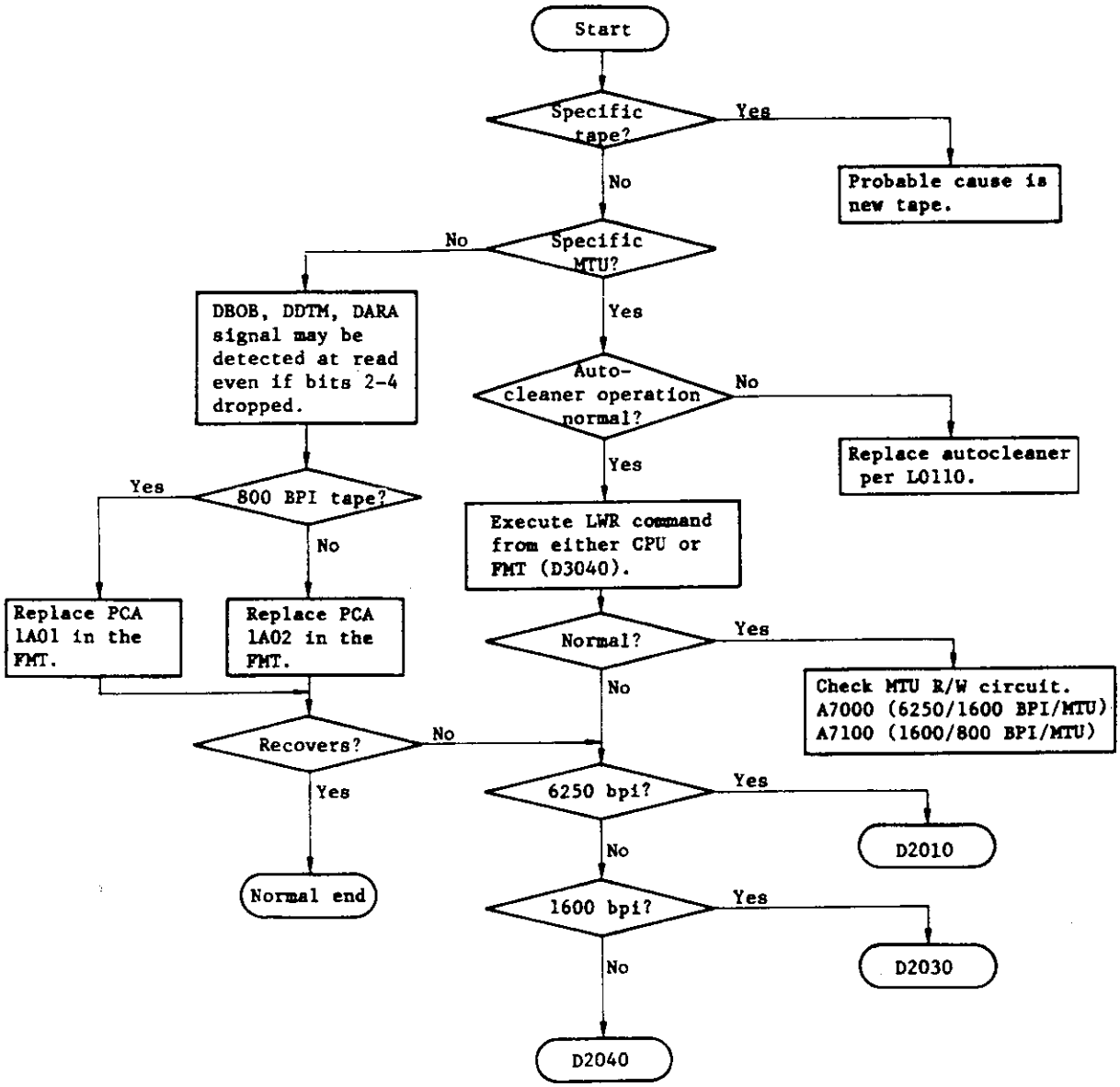
FRU1 (SB14) $20
FRU2 (SB15) The content of XCTL register

For failure in the data transfer sequence control circuit or the transfer buffer circuit, this error will be set. Transfer buffer does not become empty even after all read or write operations end.



D0060	20-Meter Check (Reject Code 025)

This check is generated when any data was not detected for more than 20 m at read command. (BOB, DTM, ARA, or NRZ data byte was not detected.)



Notes:

(1) DBOB = Detection of beginning of block.
(2) DARA = Detected automatic read amplification.
(3) DMT = Detected tape mark.

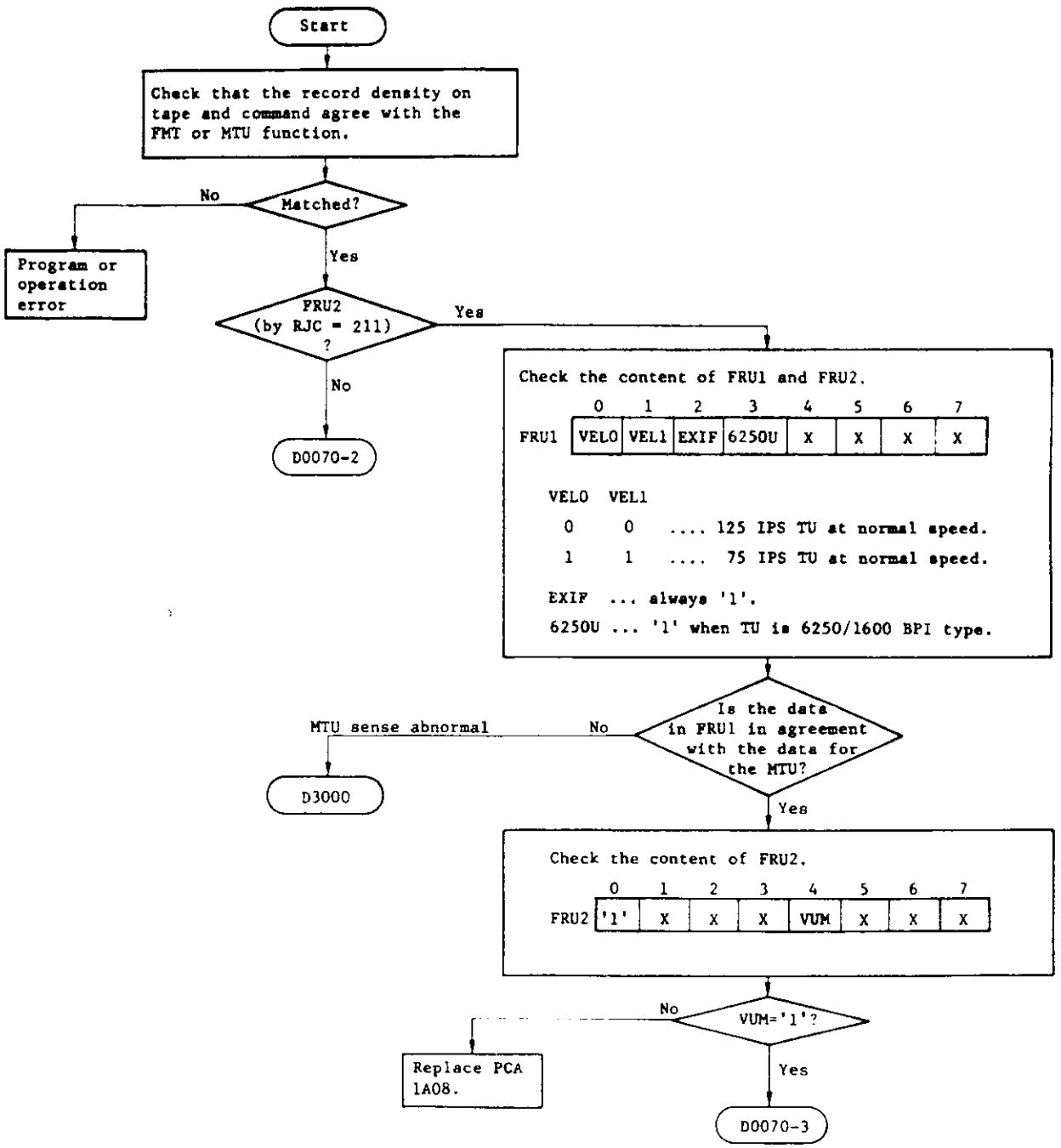
D0070-1	Not Capable (Reject Codes 011, 111, 211)

Not capable is generated:

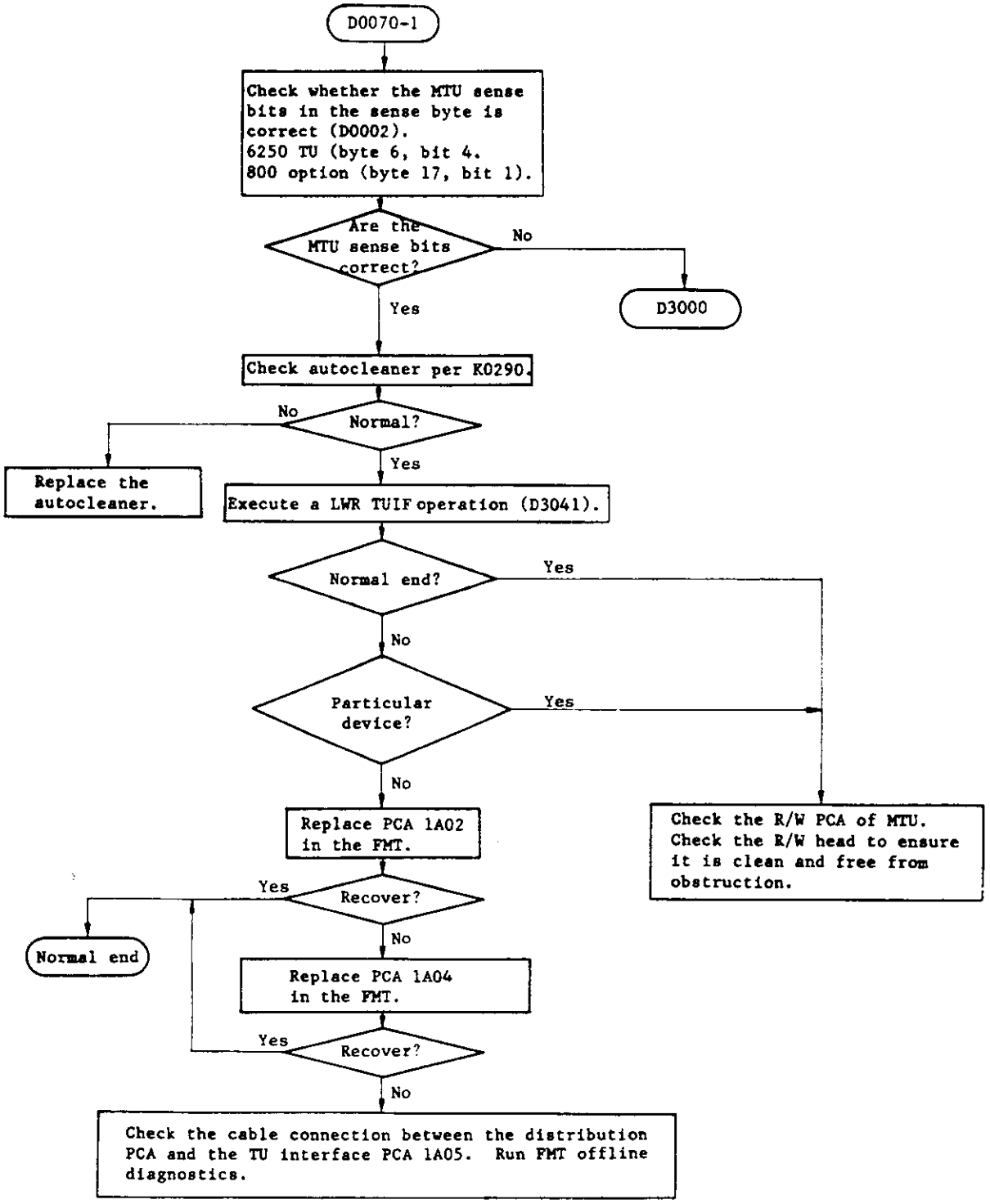
(1) If an attempt is made to read 800 BPI tape through the FMT or MTU without the 800 BPI feature or function, reject code 011 is issued.

(2) If an attempt is made to read 6250 BPI tape through the MTU without the 6250 BPI function, reject code 111 is issued.

(3) If the specification for the maximum possible processing speed of the demodulation circuit is not in agreement with that for the speed of the MTU. (In this case, FRU2 = 80 - FF) reject code 211 is issued.



D0070-2	Not Capable (Reject Codes 011, 111, 211)



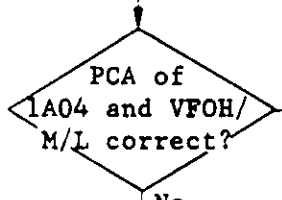
D0070-3	Not Capable (Reject Codes 011, 111, 211)

Check VFOH/M/L bit of FRU2.

	0	1	2	3	4	5	6	7
FRU1	VELO	VEL1	DXIF	6250U	X	VFOH	VFOM	VFOL

Allowable processing speed of VFO:

VFOH ... 200 IPS
VFOM ... 125 IPS
VFOL ... 75 IPS

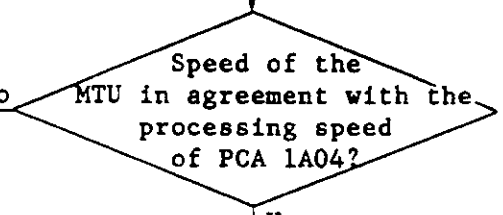


Yes

No

Replace PCA 1A04 in the FMT.

VFOH	VFOM	VFOL	Model
0	1	1	M2435L, 2436L/N
1	1	0	M2434L



No

Yes

Ensure that the MTU is correctly installed.

Replace PCA 1A05 in the FMT.

D1011	ROM Parity Error (Reject Code 002)

Start

Use ROM scan function with field tester as follows:

(1) Set ONL/OFL switch to OFL.

(2) Set switches S0 through S7 to $F4, then toggle the CNT. The ROM scan function begins.

(3) Set switches S0 through S7 to $A4, and lamps L0 through L11 will be in a half-lit condition if a ROM parity error has not occurred. When a ROM parity error occurs, microprocessor is halted immediately.

(4) Set switches S0 through S7 to $F0, then toggle the CNT to terminate the ROM scan function. Return the ONL/OFL switch to ONL after all troubleshooting.

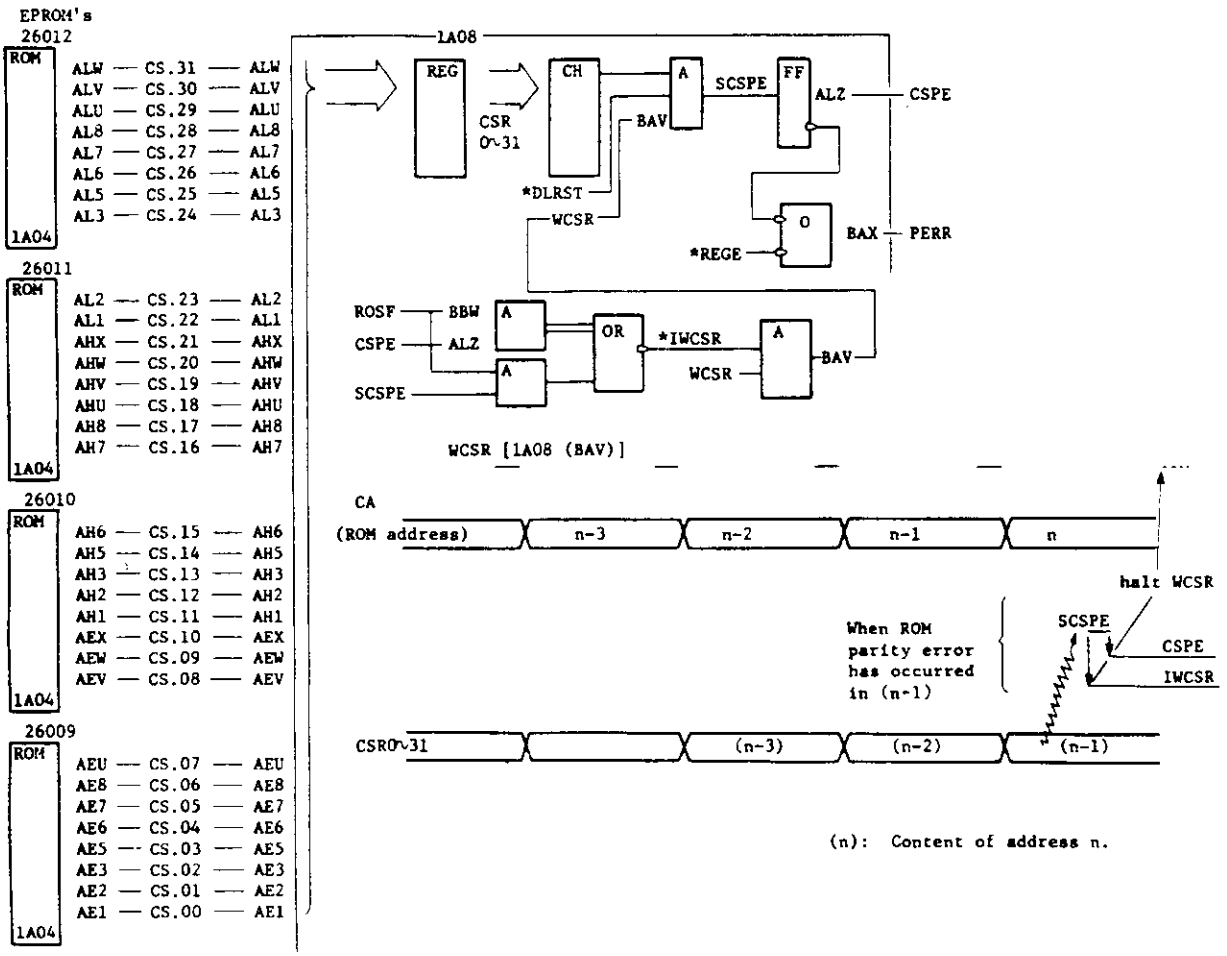
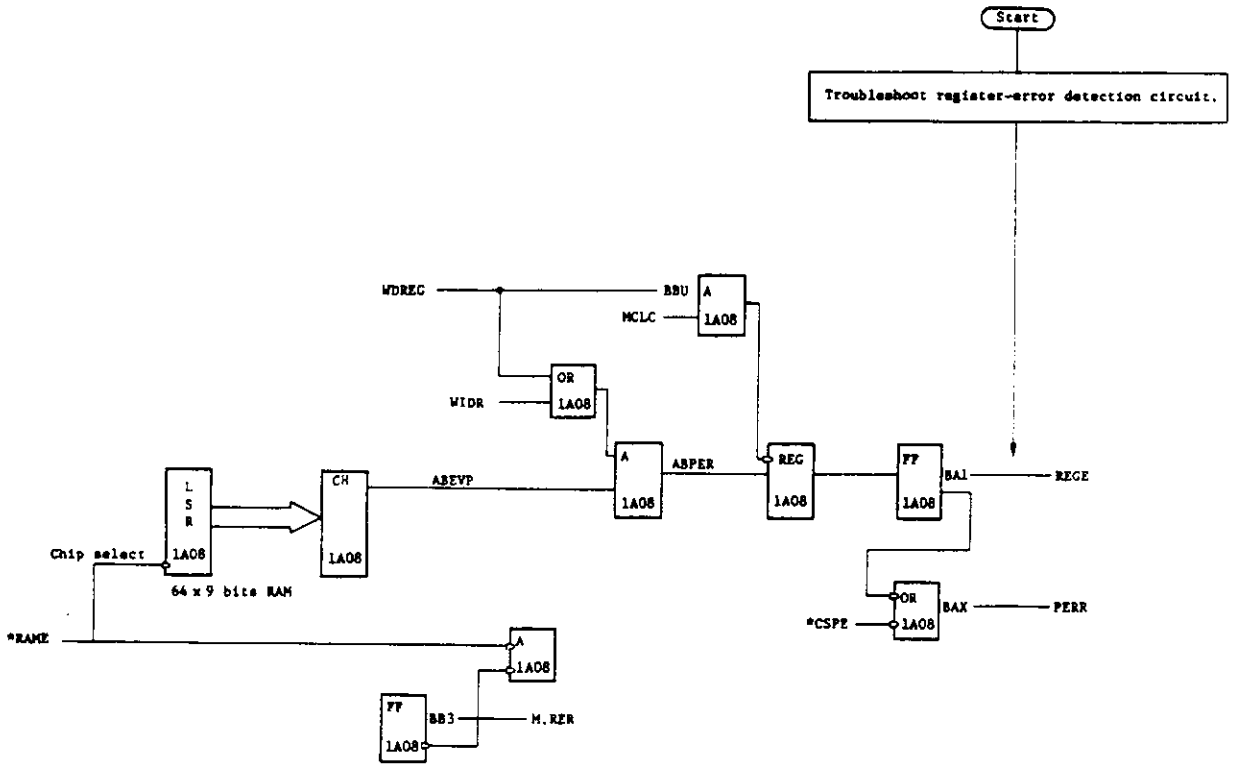


Figure D.2 ROM parity error troubleshooting

D1012	Register Parity Error (Reject Code 102)

When the microprocessor takes the data stored in register LSR (Local Storage Register) at register address 00-3F, the parity is checked if a M.RER signal has been set. If the parity is incorrect (even parity), the REGE signal is set.



D1220	Write Tape Mark Error - 1

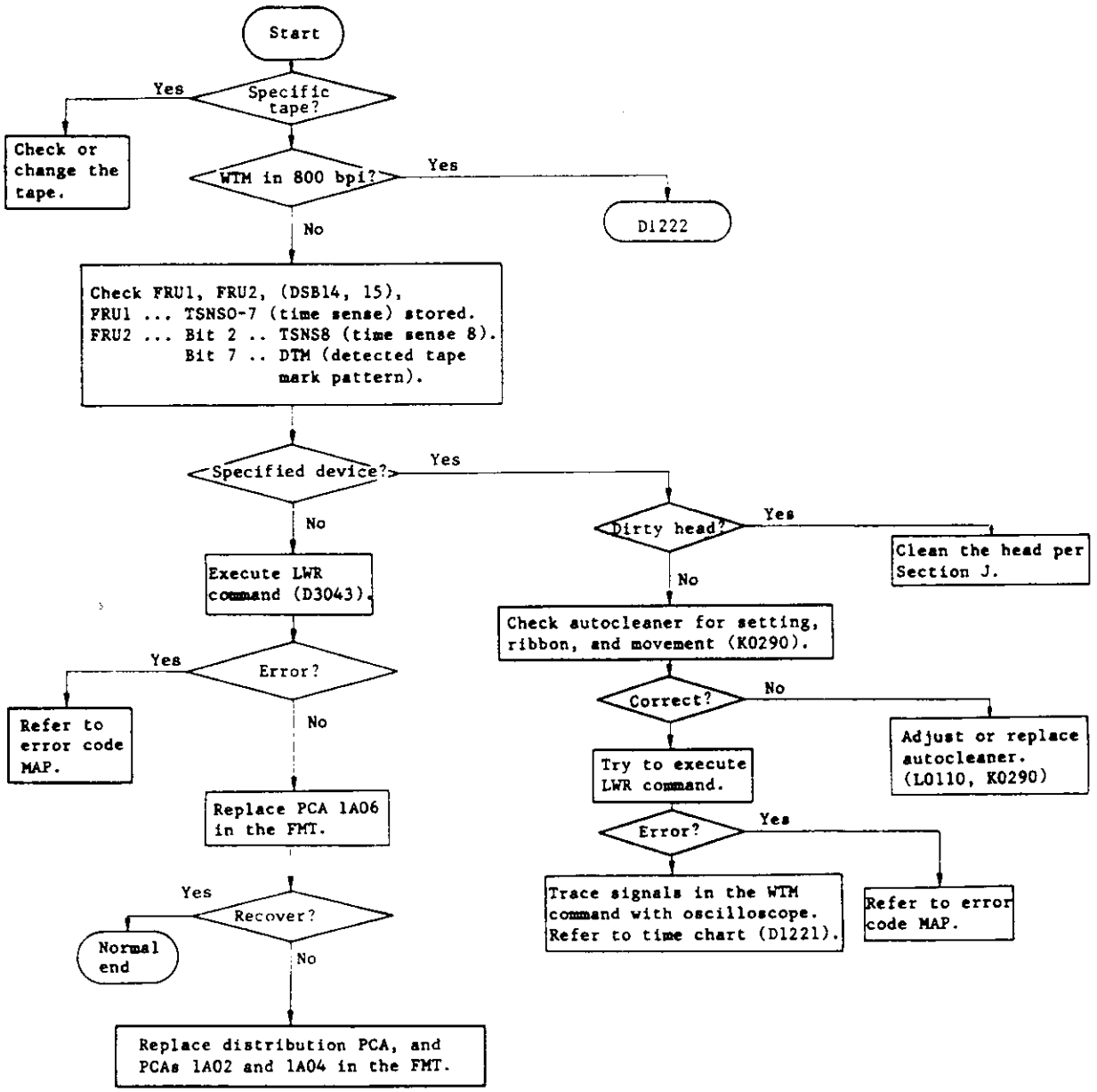
This error occurs when TM (Tape Mark) is written incorrectly as follows:

(1) When the TM pattern cannot be detected within the specified length from the end of recording the TM block in 6250/1600 bpi operation.

(2) When IBG cannot be detected within the specified length from the end of the TM block in 6250/1600 bpi operation.

(3) When the TM code cannot be detected in 800 bpi operation.

The contents of time sense are stored in FRU1 (DSB14) in 6250/1600 bpi.



D1221	Write Tape Mark Error - 2

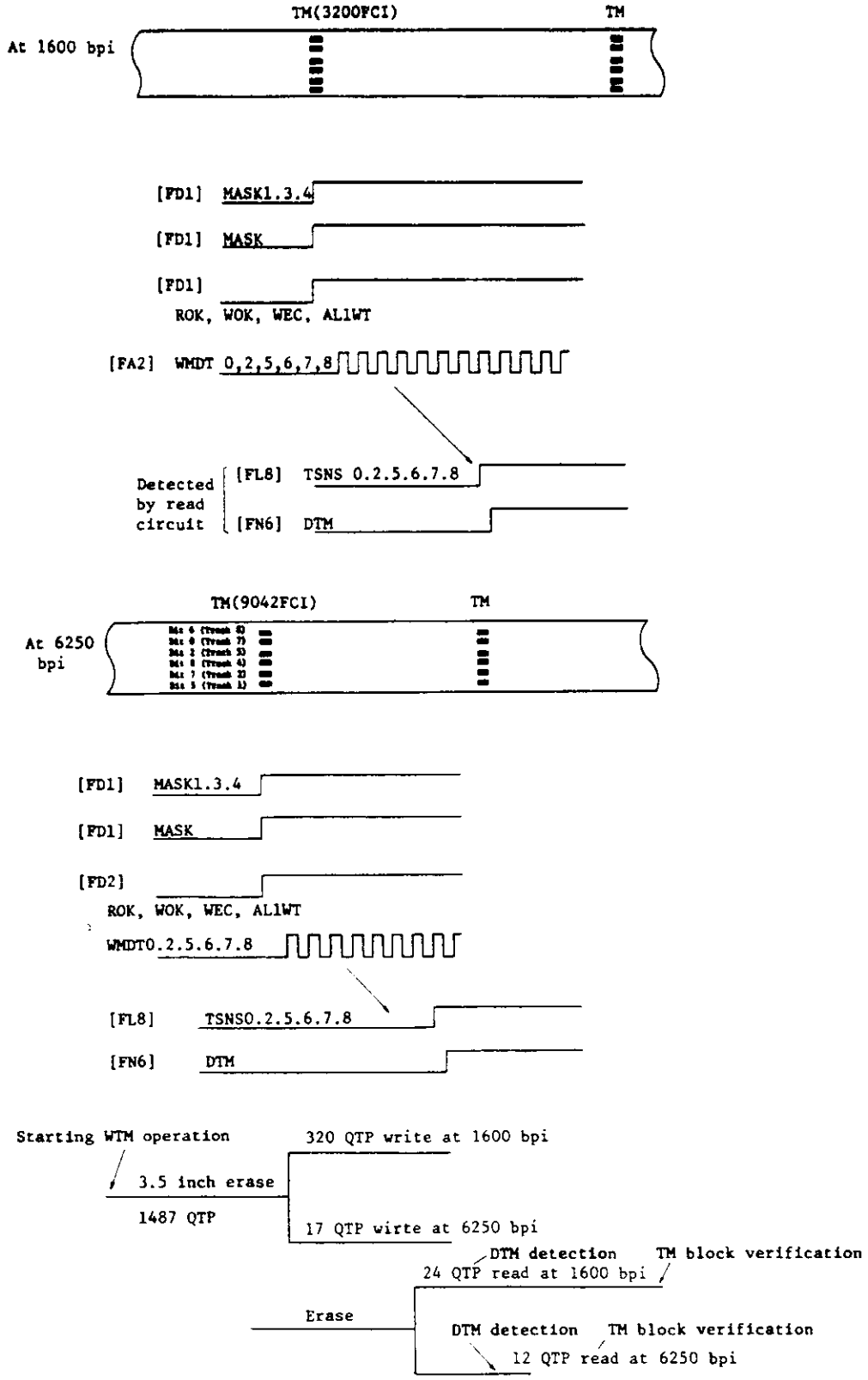
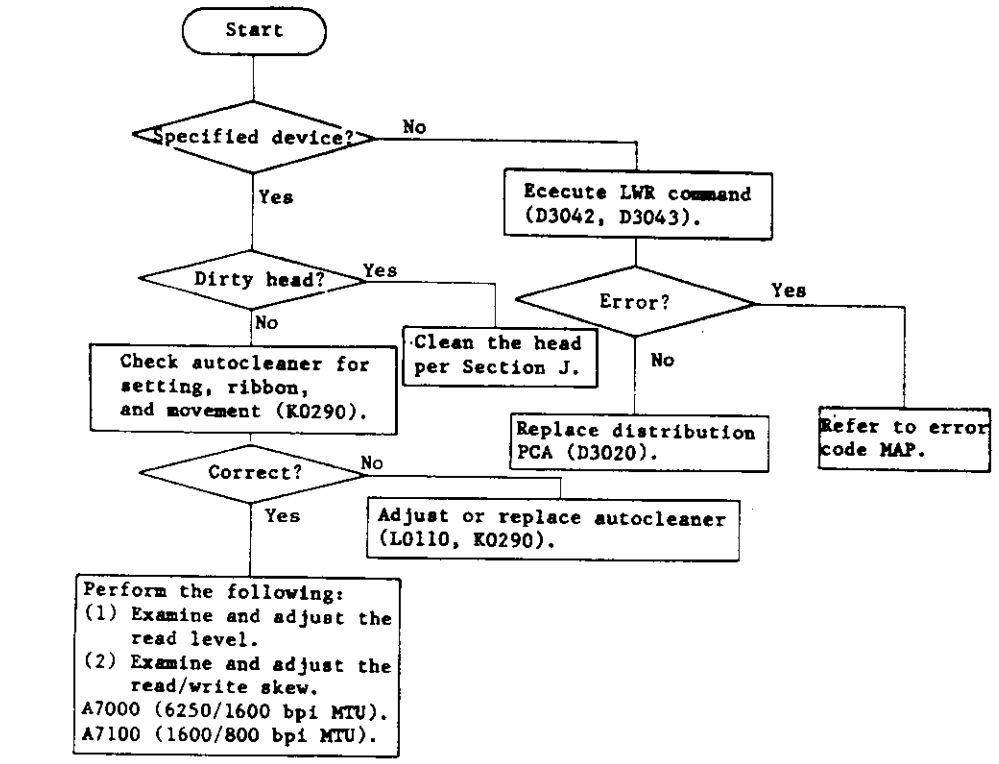
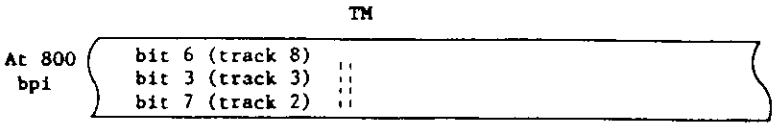


Figure D.3 Write tape mark error troubleshooting (6250 and 1600 bpi)

D1222	Write Tape Mark Error - 3





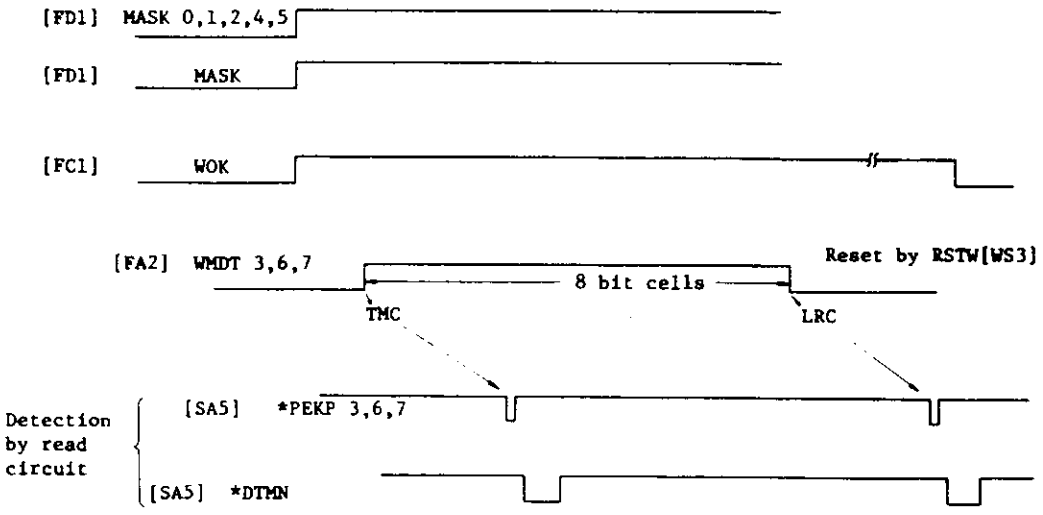


Figure D.4 Write tape mark error troubleshooting (800 bpi)

D1230	ID Burst Check - 1

ID burst check is generated when recording density identification (ID), ARA, and IVTM (ARA ID) are written incorrectly, as described below.

(1) ID burst could not be detected.

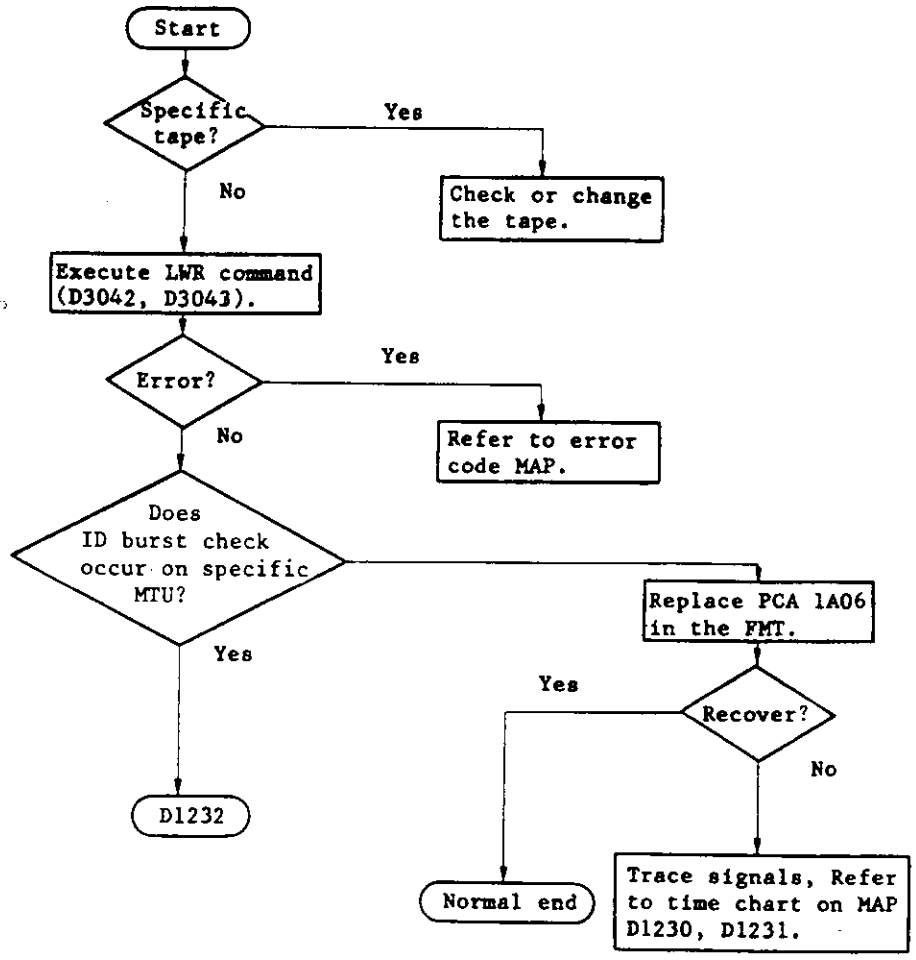
6250 bpi - track 6 (bit 1)
1600 bpi - track 4 (bit 8)

(2) ARA burst was written incorrectly (D1260).
SAGC check (sense byte 8, bit 4) is set.

(3) IVTM could not be detected.

The contents of time sense are stored in FRU1 (DSB14) and FRU2 (DSB15).

FRU1	bit 0 - TSNS0
	bit 1 - TSNS1
	. .
	. .
	. .
	bit 7 - TSNS7
FRU2	bit 1 - TSNS8



D1230	ID Burst Check - 1

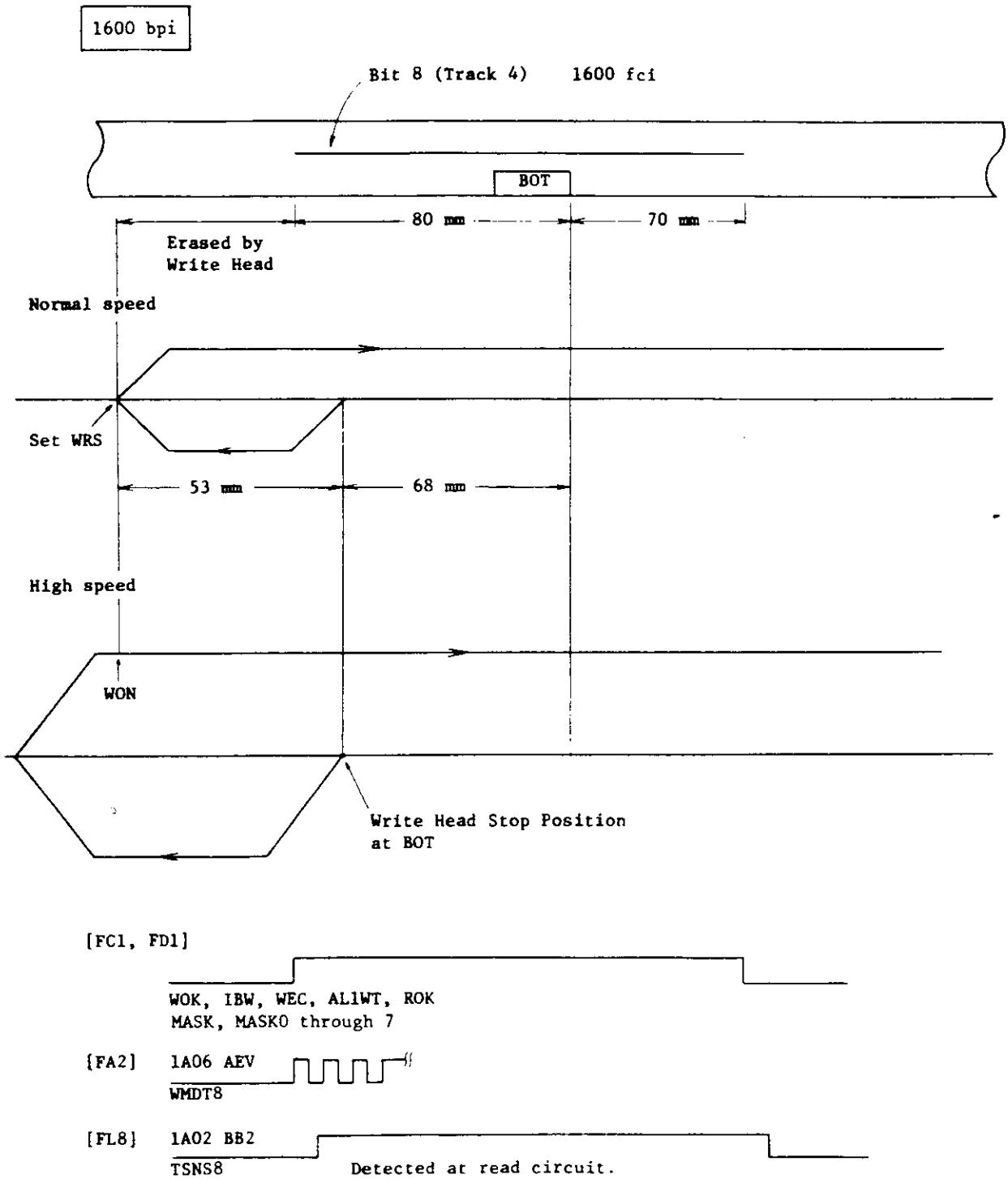


Figure D.5 ID burst check (1600 bpi)

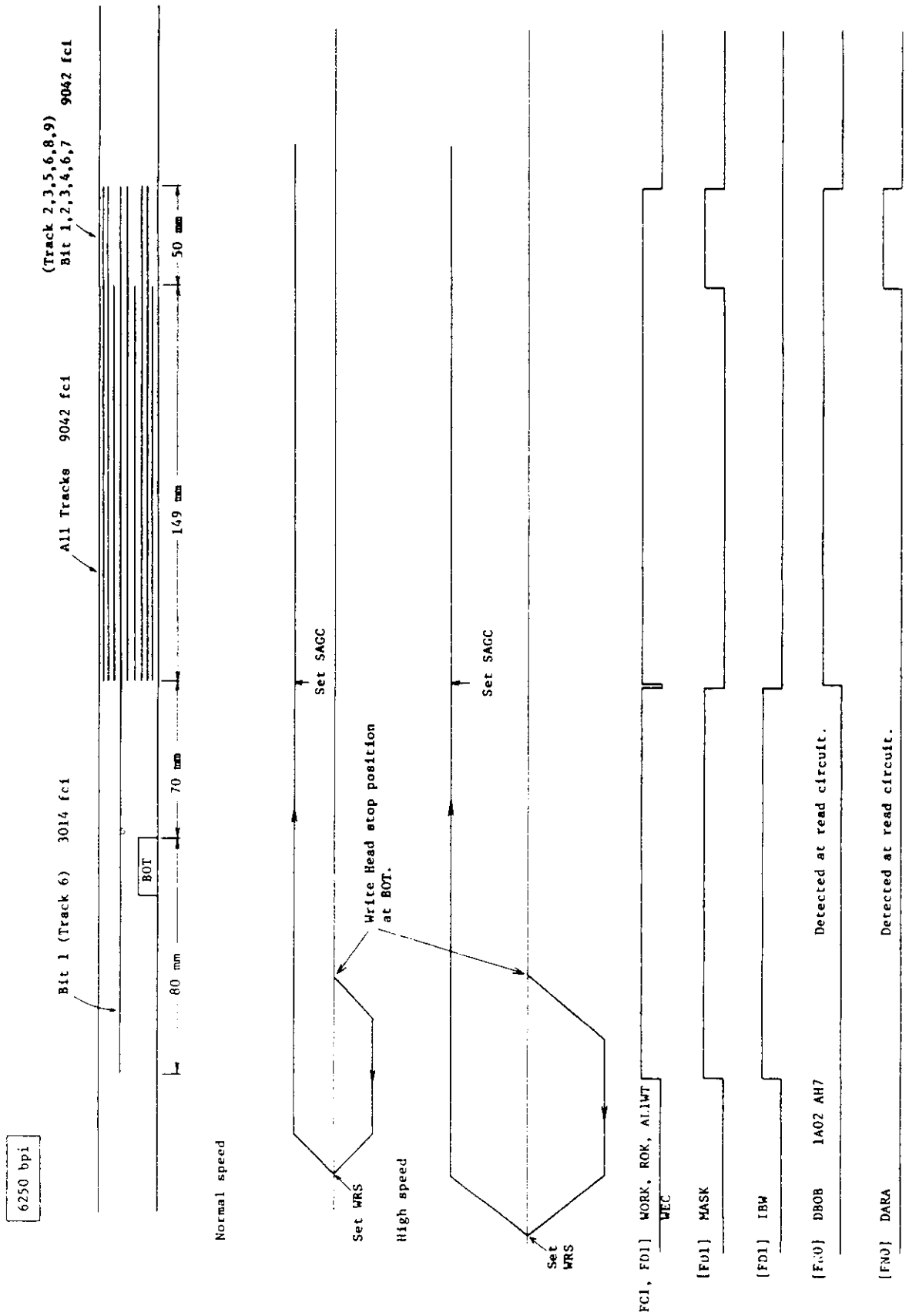
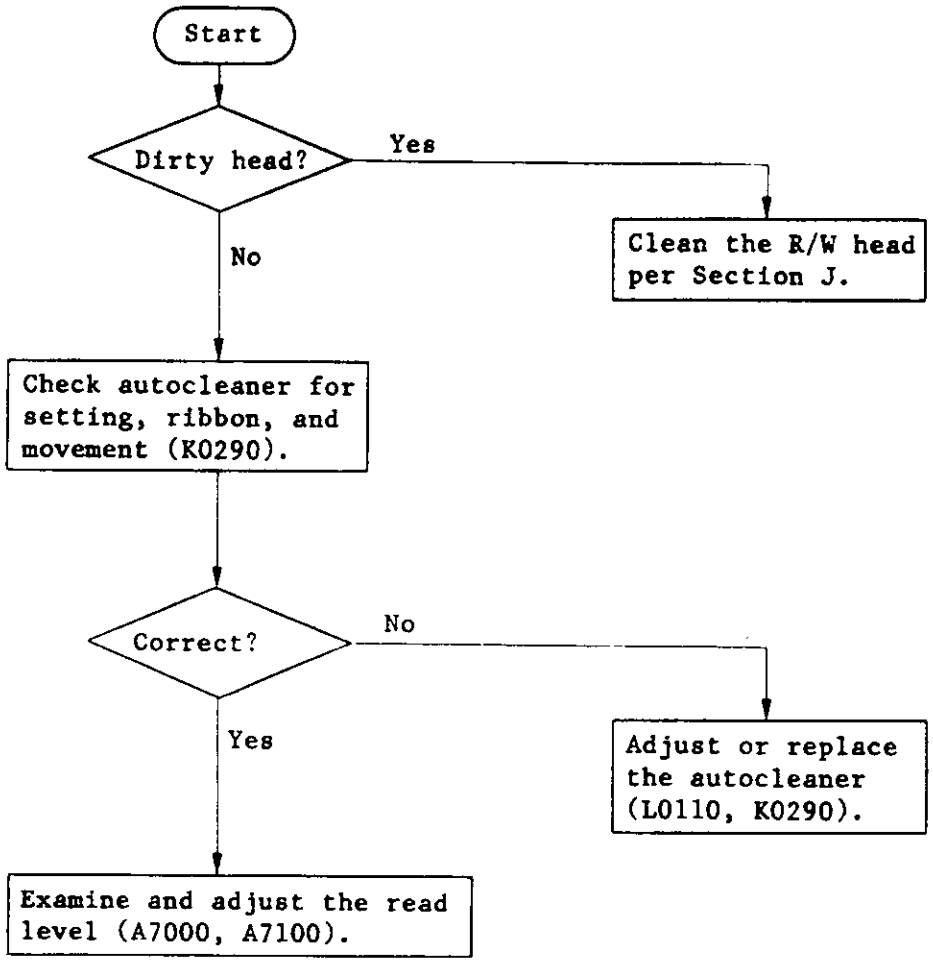


Figure D.6 ID burst check (6250 bpi)

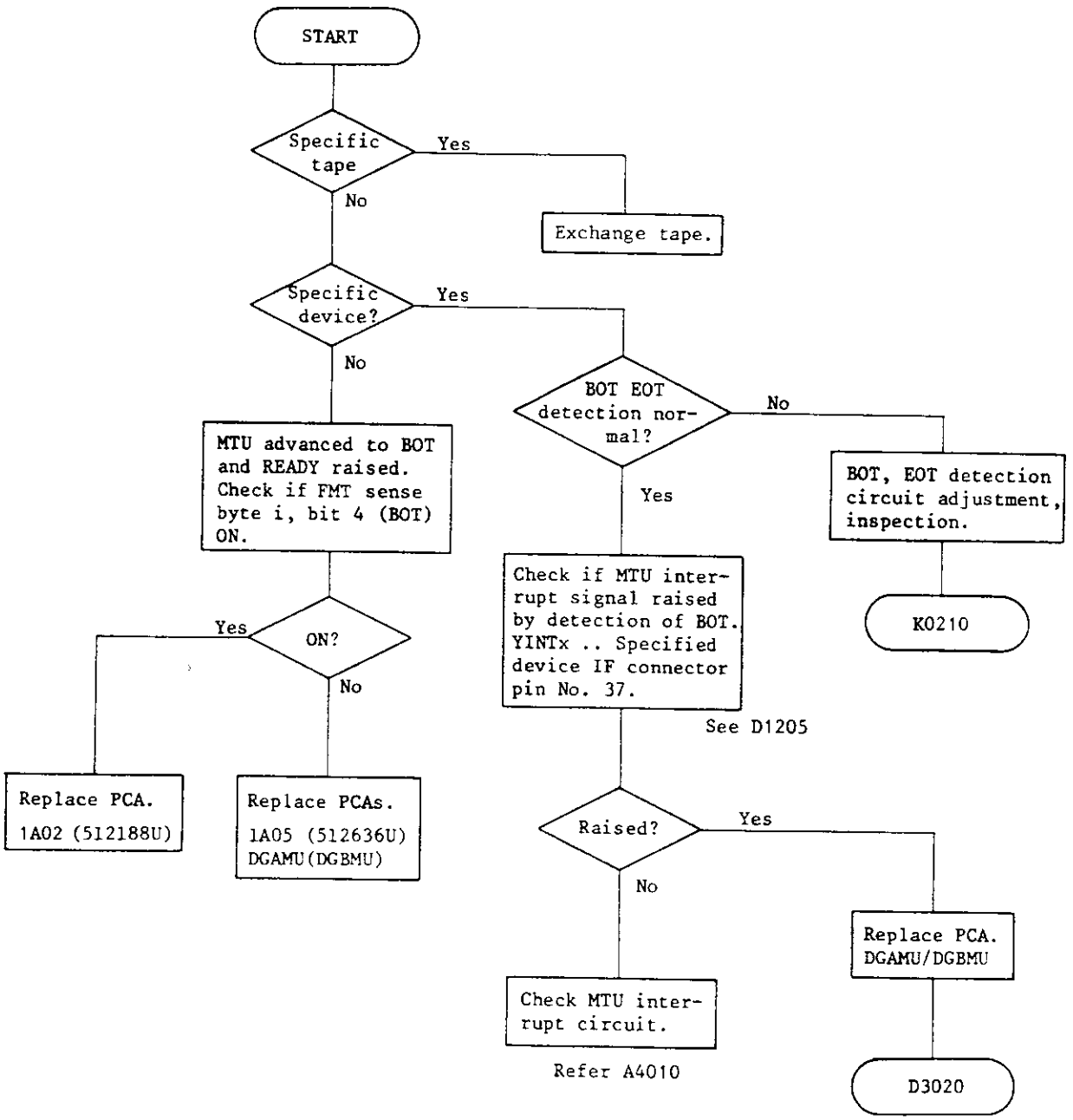
D1232	ID Burst Check - 3



D1240	Reject Code 115

An error will be generated if:

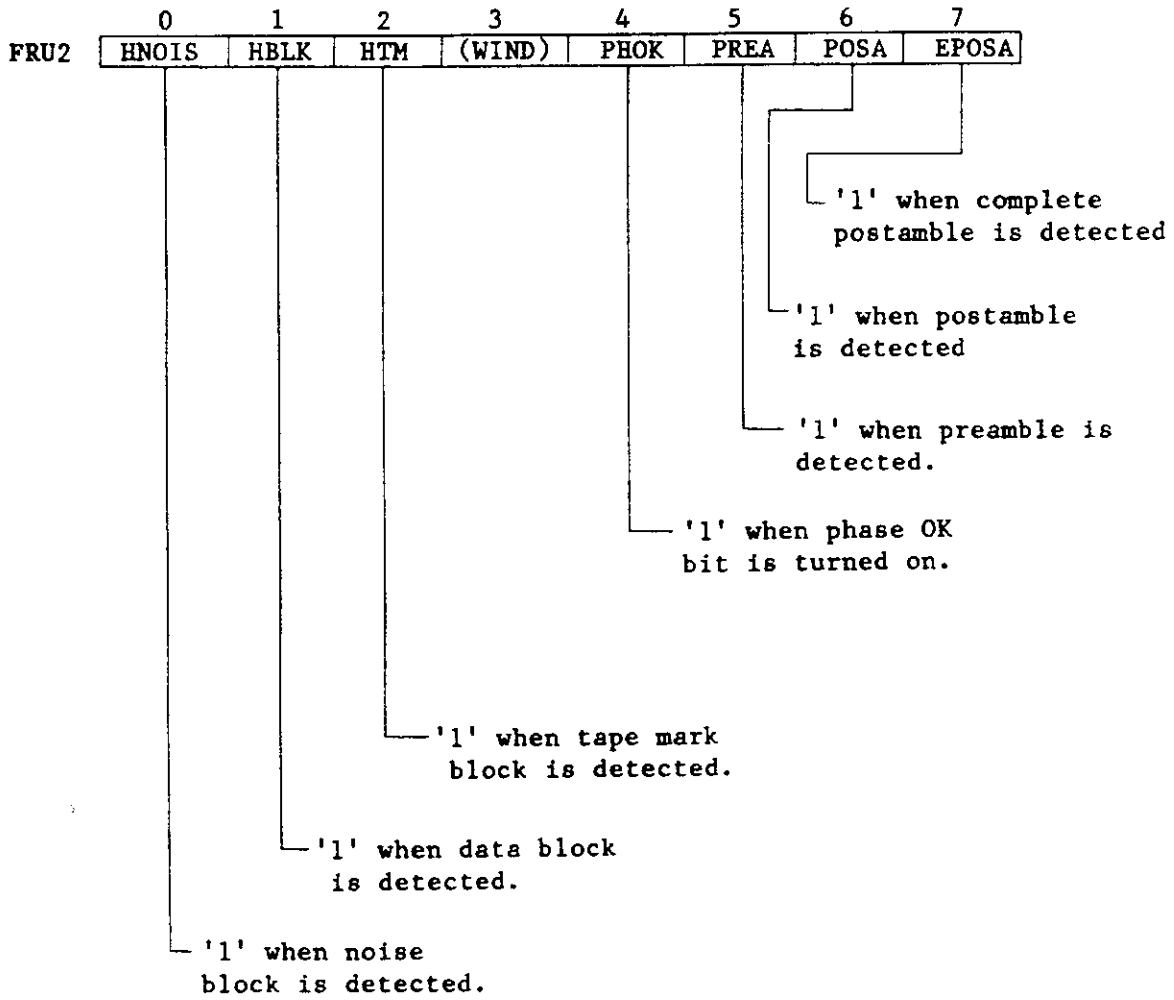
- o ARA (automatic read amplification) ID burst (IVTM) was detected, but (BOT) beginning of tape mark was not detected within the prescribed length during 6250 bpi backward operation.
- o ARA ID burst code was detected for 28 TP (6.7 mm).



D1250	IBG Detected

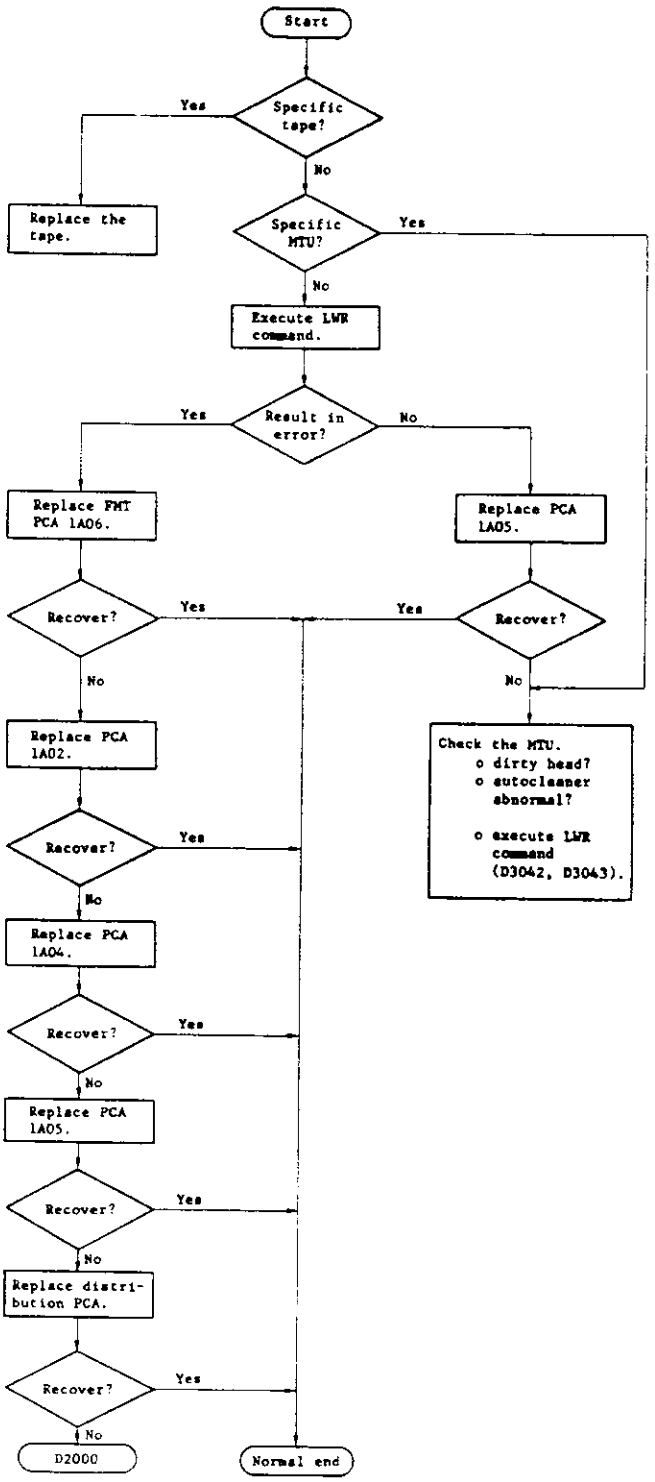
An error will be generated when an inter-block gap (IBG) is detected during write or loop wite-to read operation. The data check line bit is asserted in this case. EVC (DSB12, bit 1) may also be set in 6250/1600 bpi write operation. The following FRUs may be indicated on DSB 14, 15.

FRU1 (DSB14) $A8
FRU2 (DSB15) ..... Content of RDSNS register.



Notes:
(1) FRU = Field replaceable unit.

D1250	IBG Detected



Notes:

(1) IBG = Inter-block gap
(2) FRU = Field replaceable unit
(3) All PCAs in this troubleshooting flowchart are in the FMT.

D1255	IBG Not Detected (Reject Code 034)

An error will be generated when:

(1) Inter-block gap (IBG) is not detected within 44 cm from the point that automatic read amplification (ARA) burst was recognized in 6250 bpi read operation.

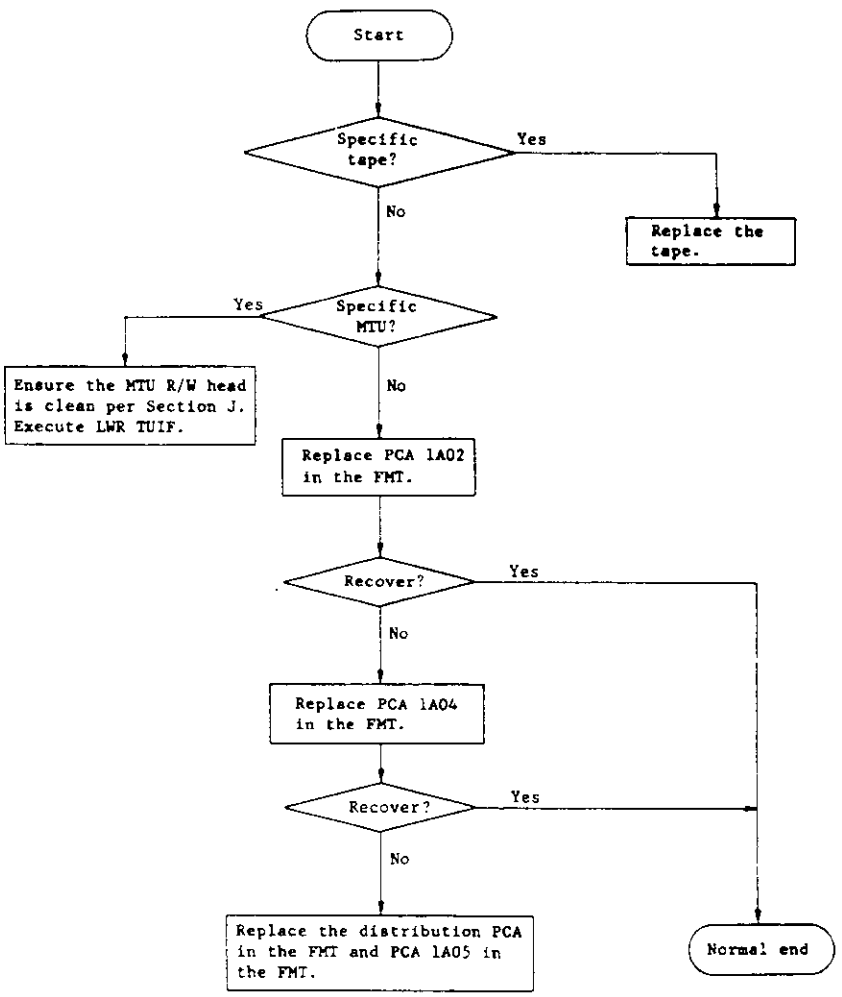
(2) IBG is not detected within 10 m from the pont ID burst was recognized in 1600 bpi read operation. Reject and operation incomplete lines are asserted. DSB14 and 15 give time sense information:

DSB14

P	7	6	5	4	3	2	1	0
0	TSNS 0	TSNS 1	TSNS 2	TSNS 3	TSNS 4	TSNS 5	TSNS 6	TSNS 7

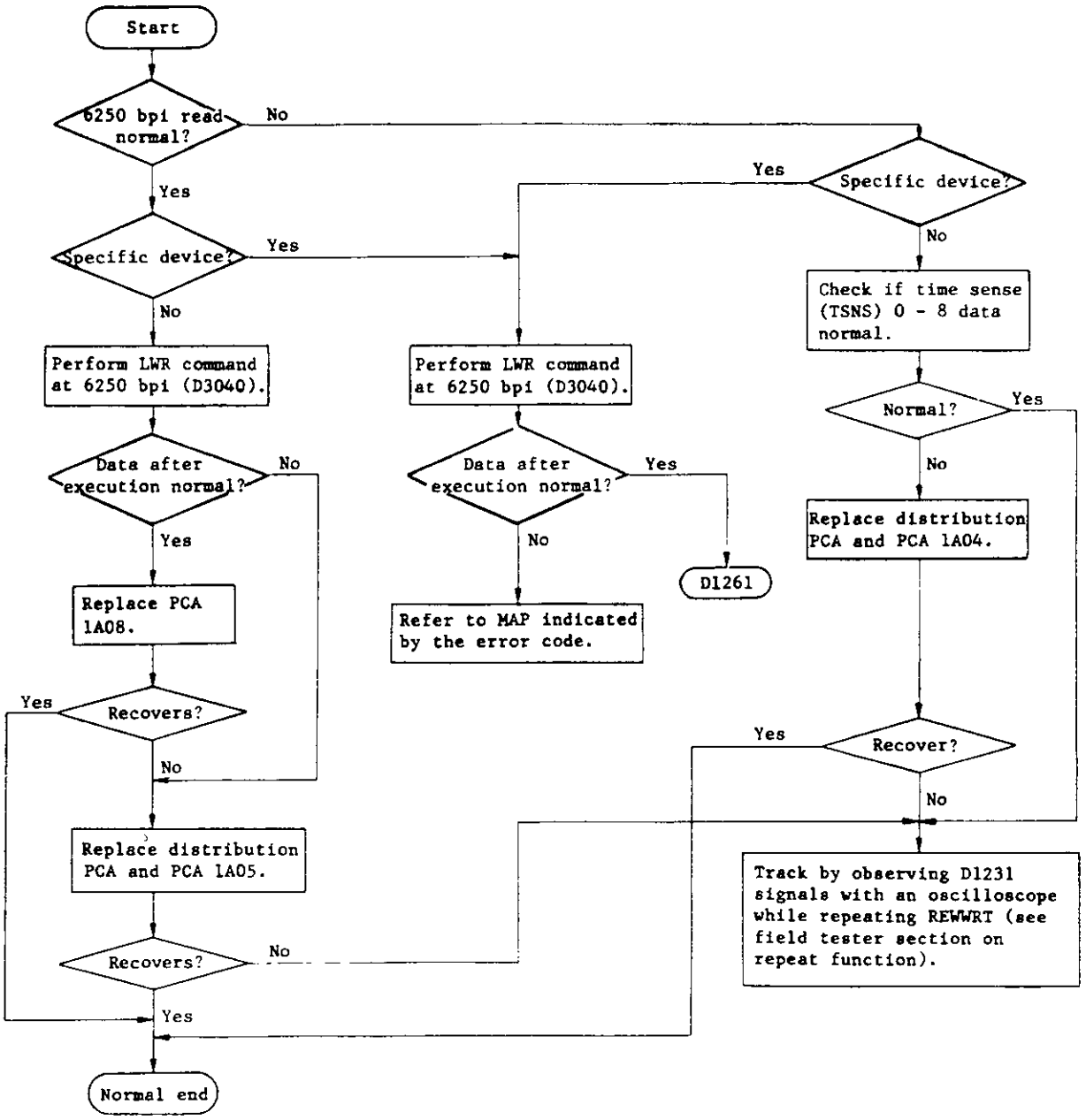
DSB15

P	7	6	5	4	3	2	1	0
			TSNS 8	DIBG	DNOIS	DBOB	DARA	DTM

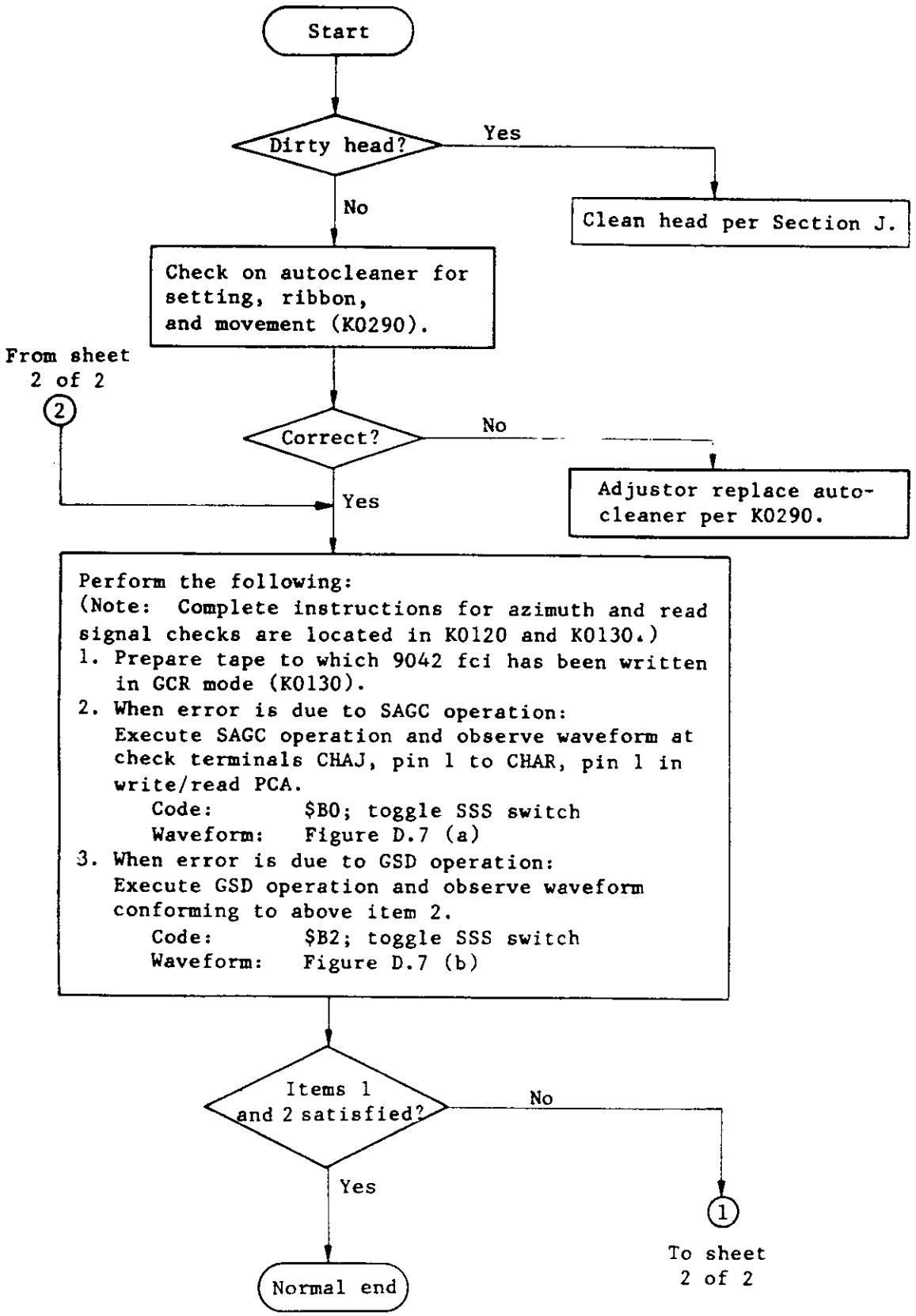


D1260	SAGC Check - 1

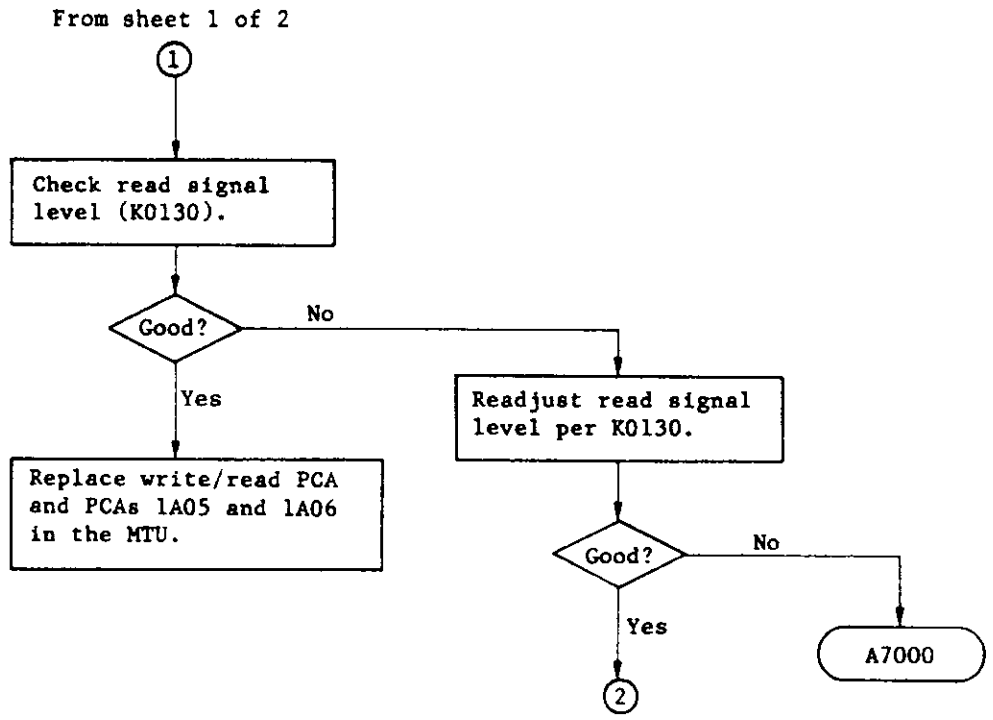
Self-adjust gain control (SAGC) check is generated when automatic read amplification (ARA) burst read or write was performed incorrectly during 6250 bpi operation.

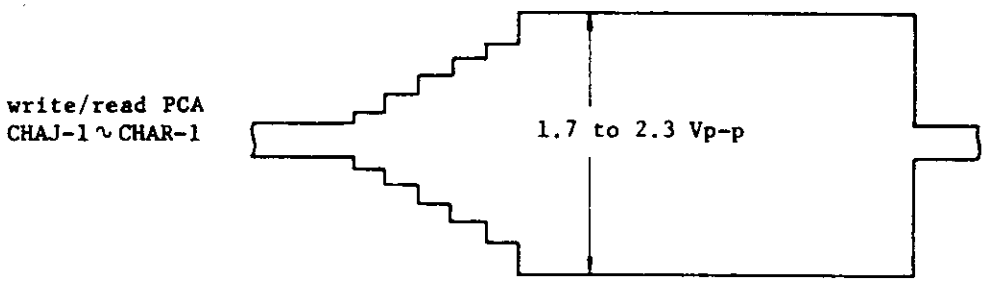


D1261	SAGC Check - 2

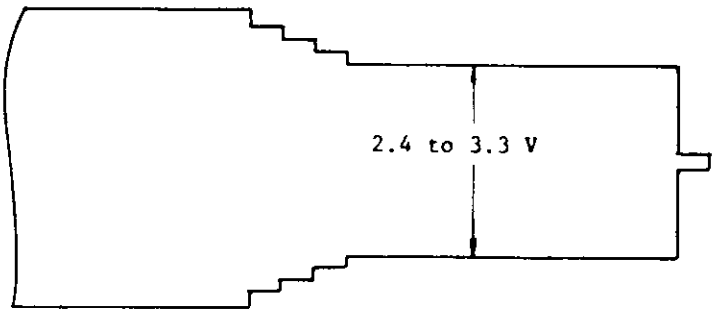


D1261	SAGC Check - 2





(a) SAGC waveform



(b) GSD waveform

Figure D.7 SAGC and GSD waveform

D1270	No Block Detected

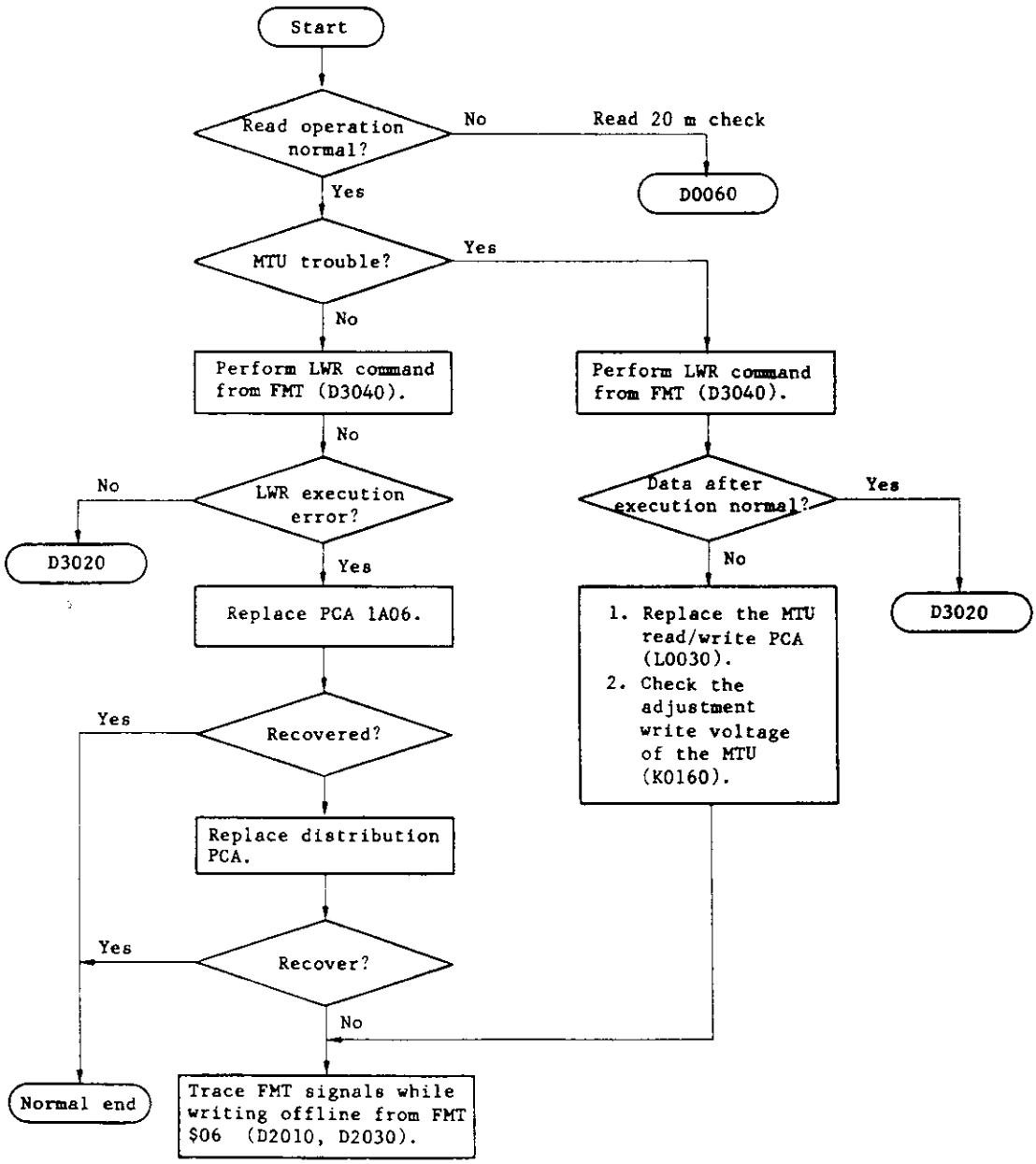
This error is generated when writing is started and data block cannot be detected within the prescribed length after the writing has ended (at write command). (Detected at 70 QTP.)

When DNIS (detection of noise pattern) signal continues as long as 46 bit cells in the 6250 bpi mode or 22 bit cells in the 1600 bpi mode, HNOIS signal is generated.

Detection of data block depends on whether HNOIS signal is generated.

DNOIS detection pattern at 6250/1600 bpi write

$0 \cdot 4 \cdot 6 + 1 \cdot 2 \cdot 8 + 3 \cdot 5 \cdot 7 + (0+4+6)(1+2+8)(3+5 \cdot 7)$

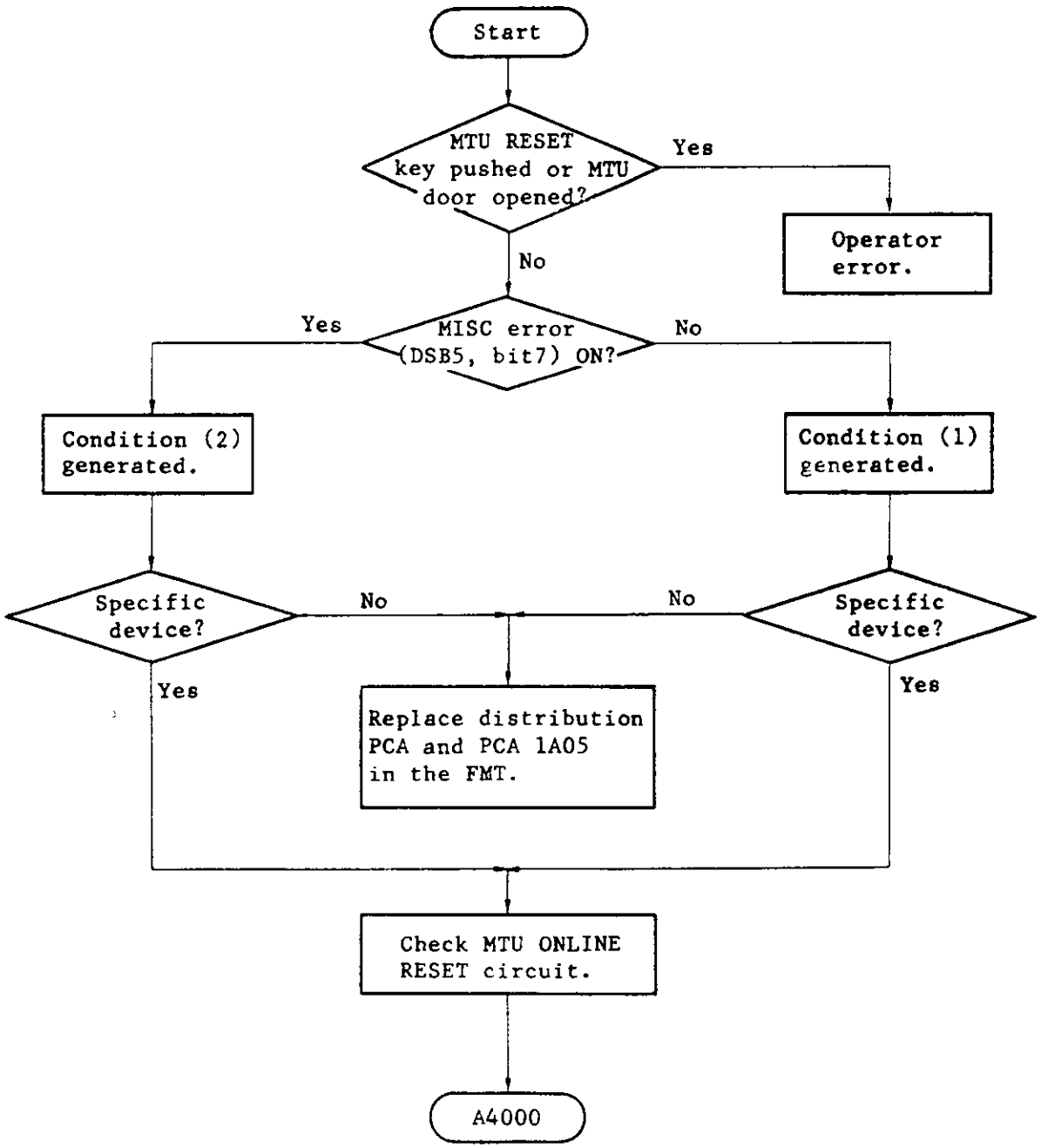


D1300	Reset Key (Reject Code 121)

This error is generated:

(1) When MTU RESET key is pushed mistakenly during MTU drive. (DSB3, bit 6, reset key is set.)
FRU1 (DSB14) 70

(2) When MTU door is opened inadvertently during operation. (DSB3, bit 6, reset key and DSB5, bit 7, miscellaneous error set.)
FRU1 (DSB14) 70

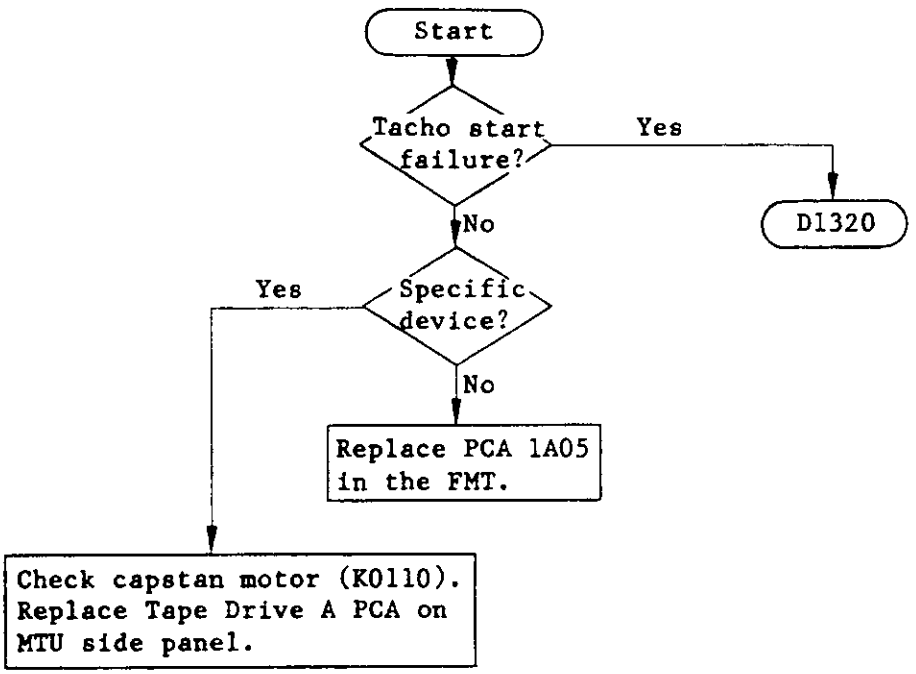


D1310	Reject Code 233

This error is generated when:

(1) The tape is operated more than the prescribed QTP (quarter tacho pulse) number in reverse direction at MTU starting.
- o FRU1 (sense byte 14) CC
- o FRU2 (sense byte 15) .... TQP count number (length of running of drive direction.)

(2) Error when operated 108TP in reverse direction.



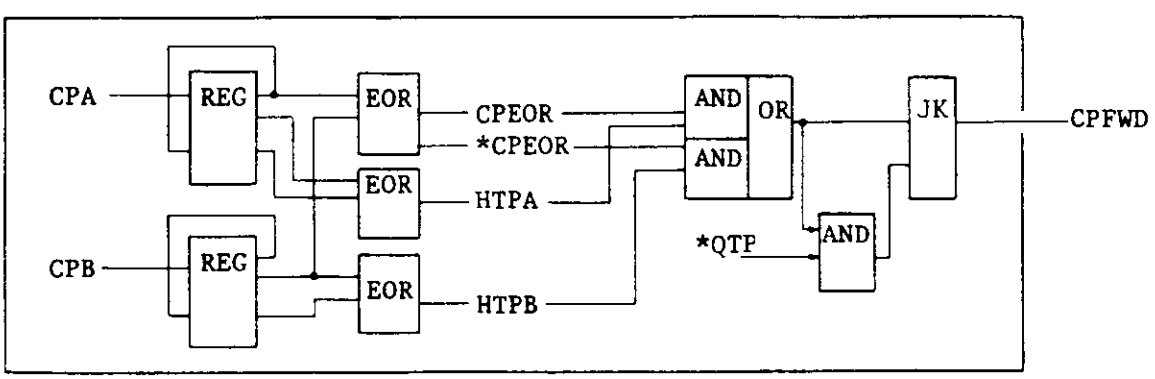


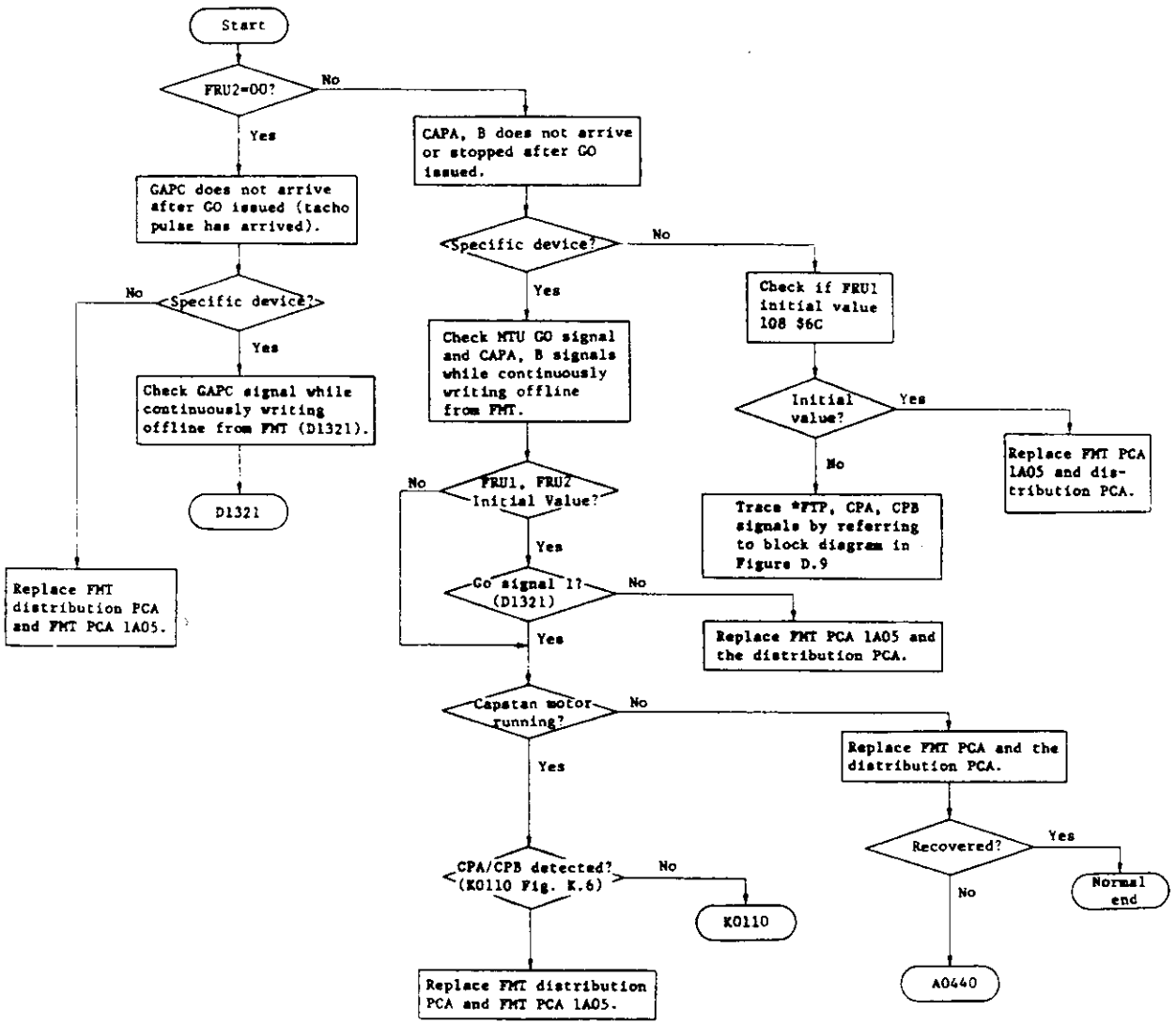
Figure D.8 Reject code 233 troubleshooting

D1320	Tacho Start Failure - 1 (Reject Codes 032, 012)

This error will be generated in the following cases:

(1) Reject code 032
When prescribed QTP length is not detected within the prescribed time after MTU start.
FRU1 (SB14) .... 108-QTP count total (drive direction and reverse direction)
FRU2 (DSB15) .... 20-drive direction QTP count

(2) Reject Code 012
when GAP CTL is not detected within prescribed time after MTU start.
FRU1 .... 108-QTP spacing
FRU2 00
Prescribed time .... 65 ms



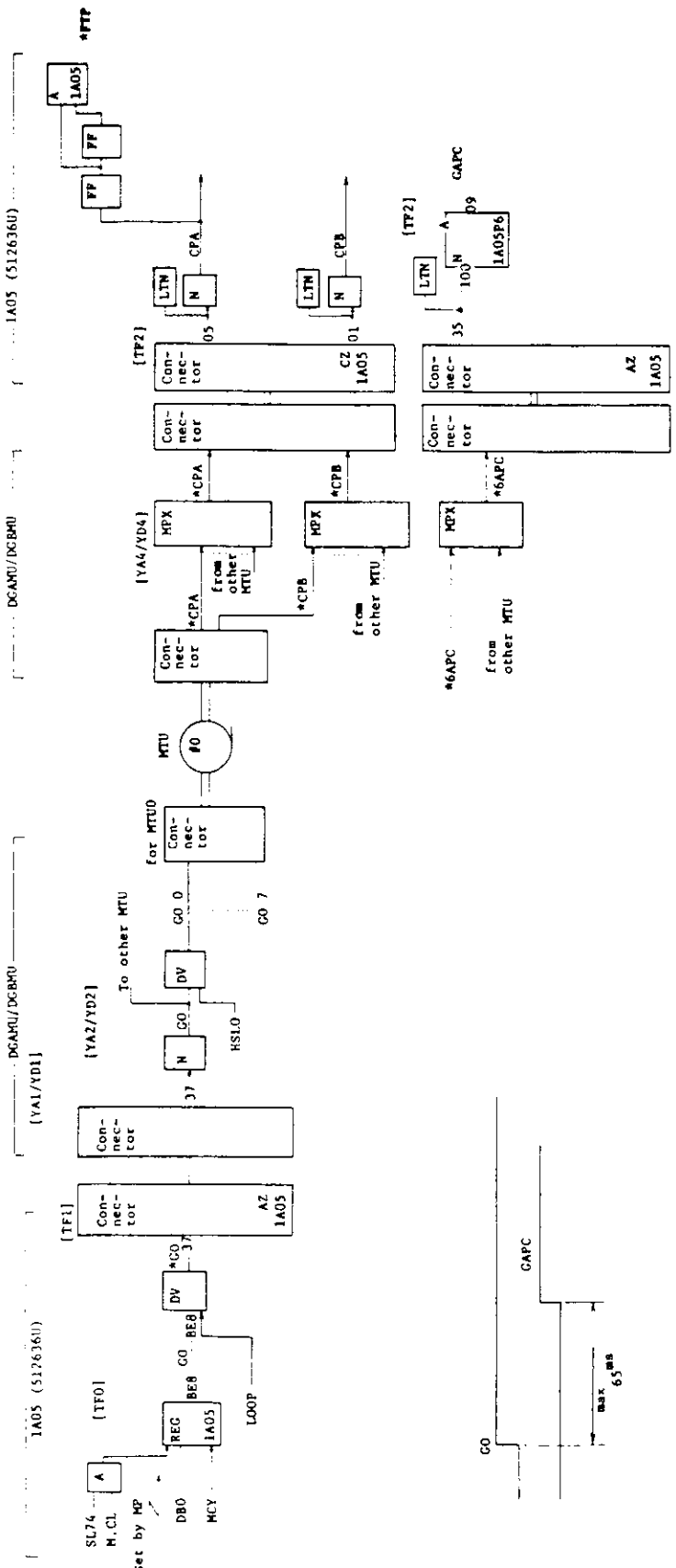
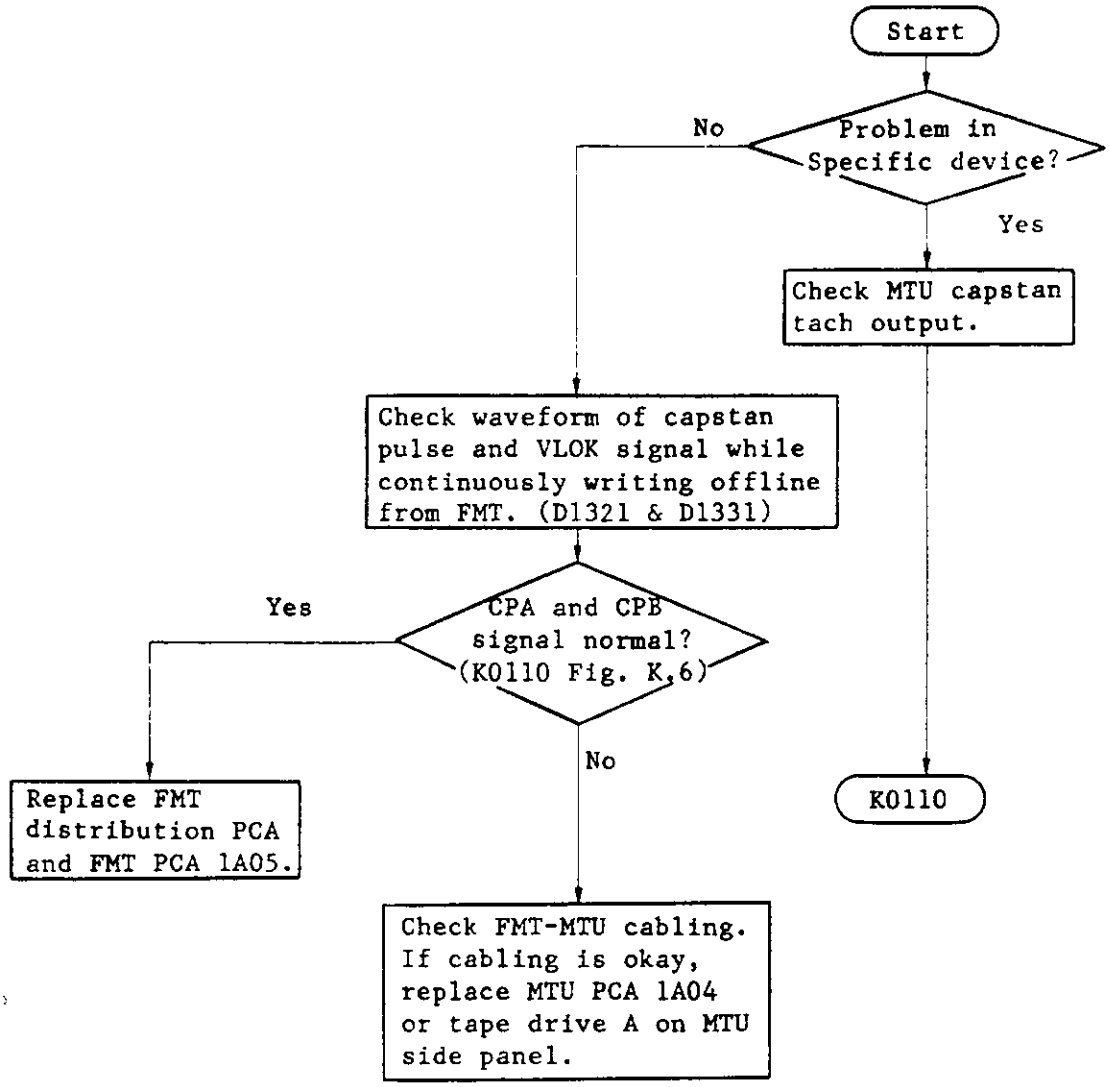


Figure D.9 Tacho start circuit

D1330	Velocity Check - 1 (Reject Code 112)

This error will be generated when velocity retry (over 16 times) has occurred during write operation. Velocity retry - DSB 12, bit 4. Write start was late because capstan speed was not within ±7.



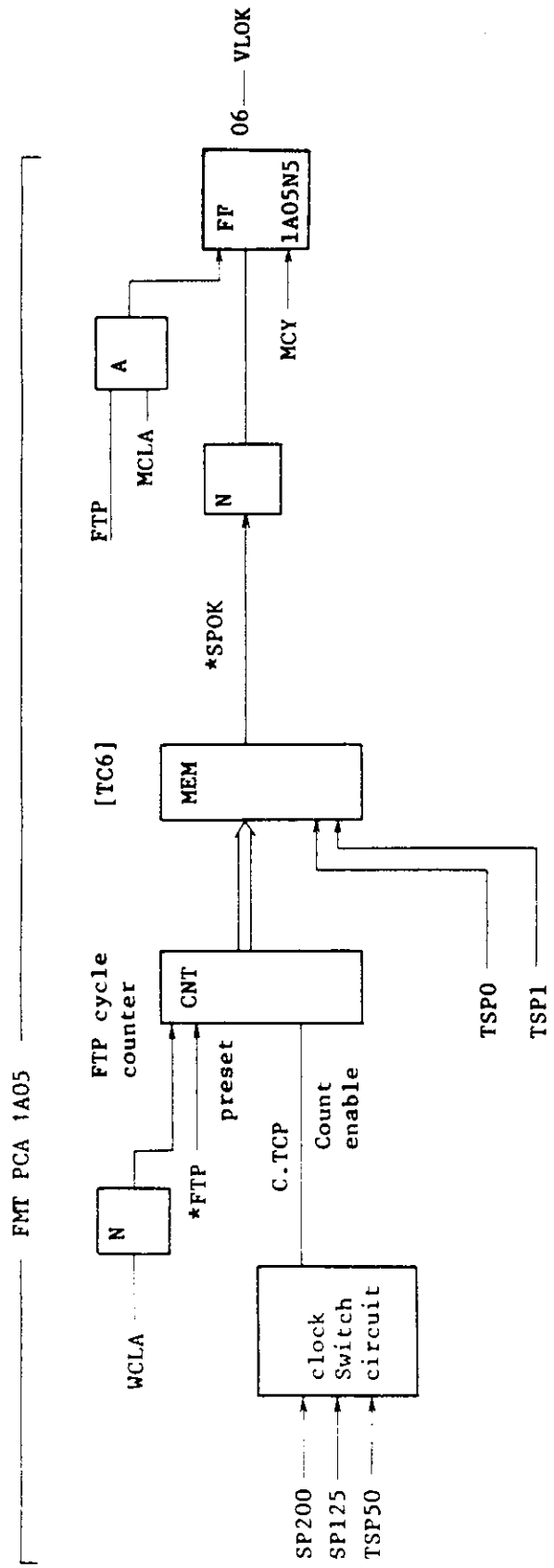
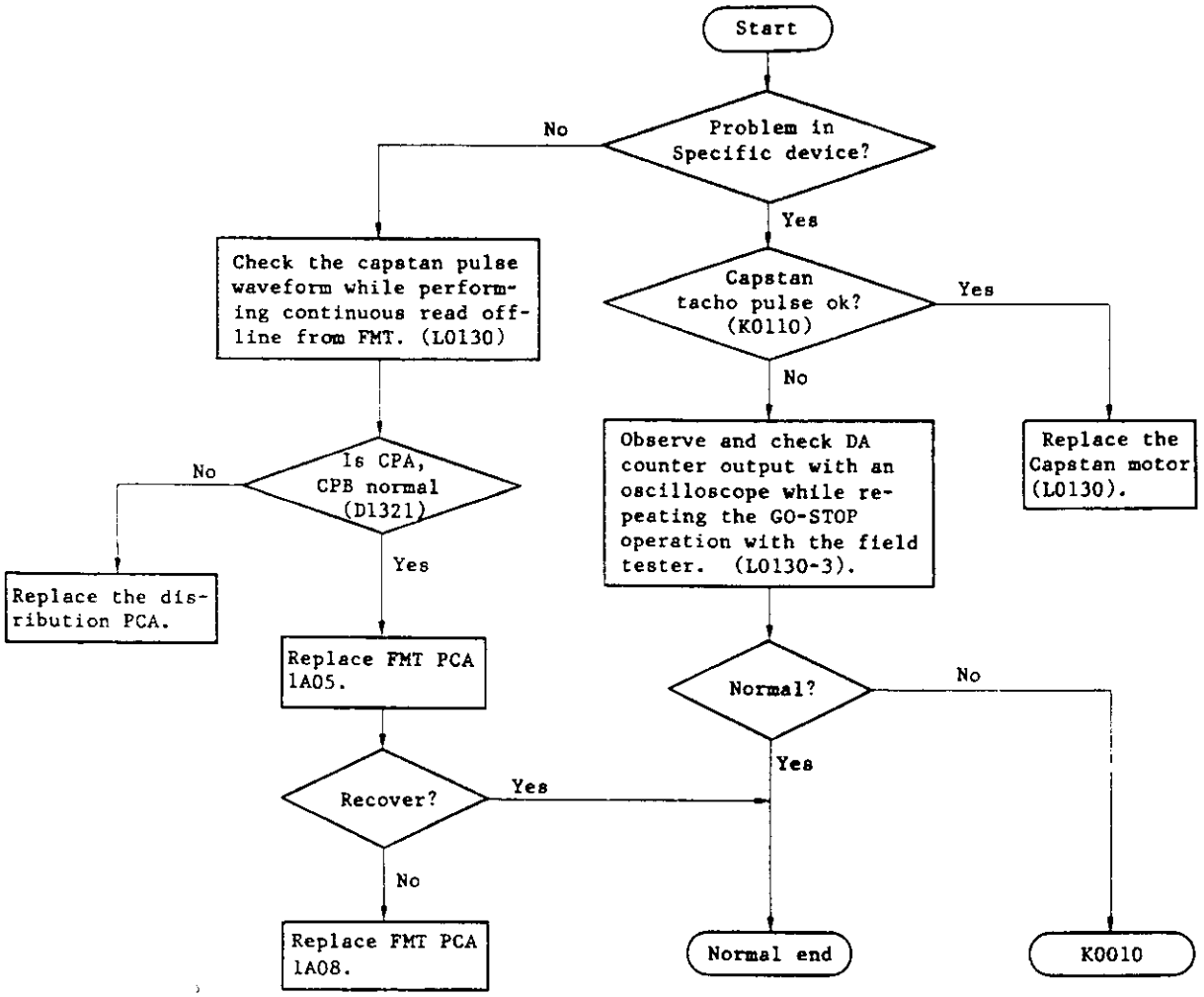


Figure D.10 Velocity check circuit

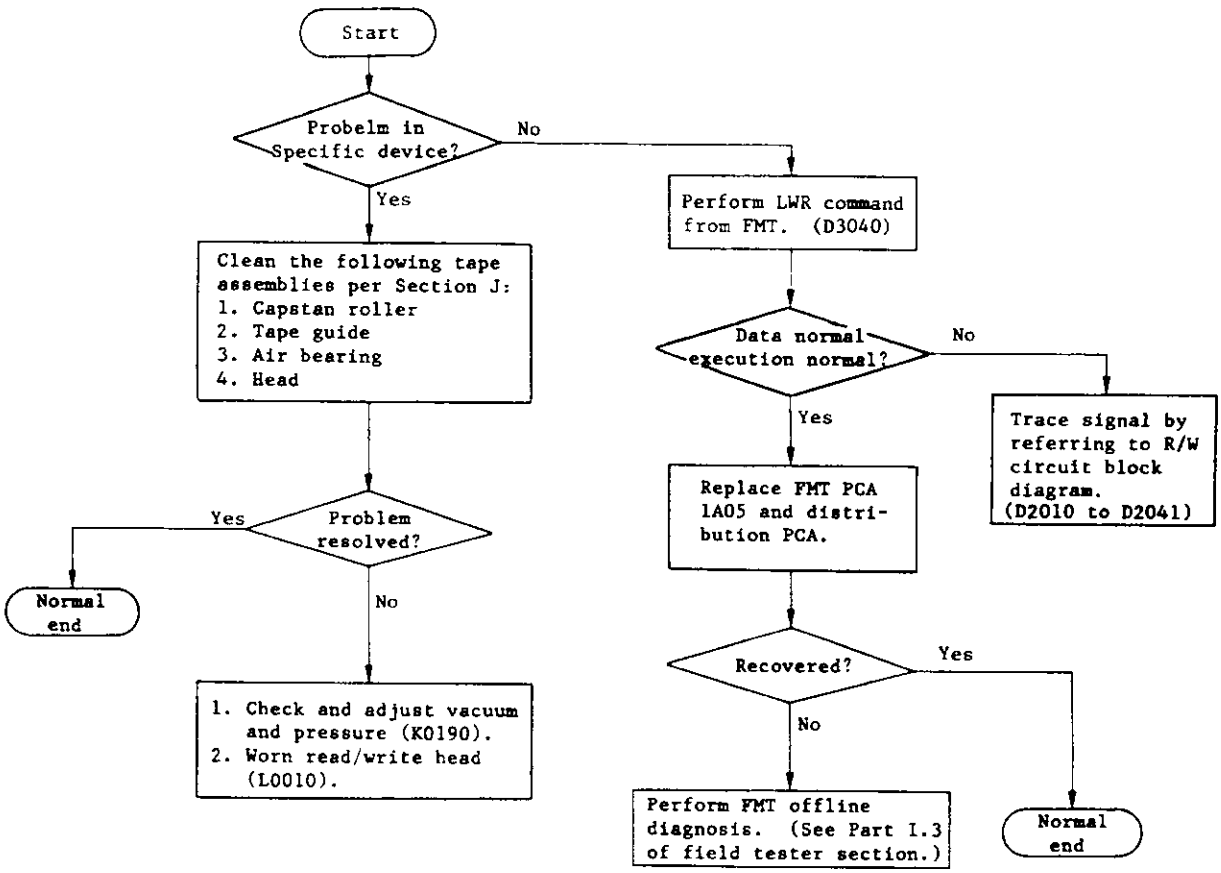
D1340	Velocity Error

Error Multiplex Byte 1, bit 1. Velocity error is generated when the designated capstan speed is exceeded during write operation.



D1350	Early Begin, Slow Begin, and Slow-End Read Back Check

- Early begin read back check (DSB11, bit 4)
  Error is generated in the following cases:
  (1) When data-byte (800 bpi) or DBOB pattern (1600/6250 bpi) is detected within time (a) (see Figure D.11) at write command execution. (Data is detected too early.)
  (2) When IBG is detected during writing (WOK signal on) at 800 bpi (IBG detected too early).
- Slow begin read back check (DSB11, bit 2)
  Error is generated when data-byte (800 bpi) or No. 5 pattern (1600/6250 bpi) is detected within time (b) (Figure D.11). (Data is detected too slow.)
- Slow end read back check (DSB11, bit 1)
  Error is generated when IBG is detected at over 70 QTP after block end detected after write end.



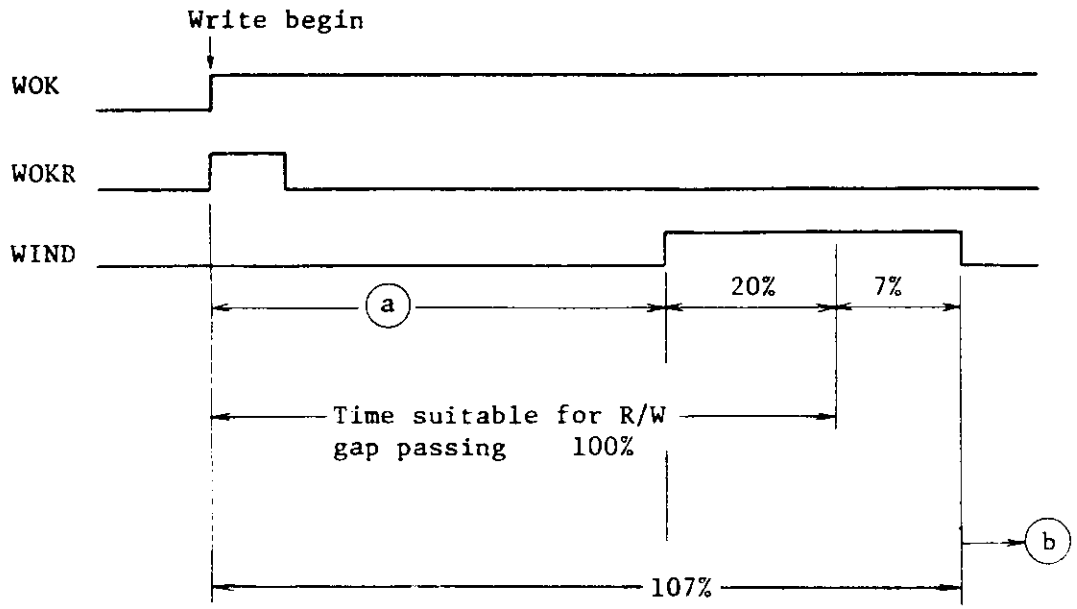


Figure D.11 Slip check timing

D1400	Status Command and Control Tag Response Check

The FMT uses three tag signal lines (Status tag, Control tag, and Go tag) to control the MTU. The FMT uses the status tag line in conjunction with the control tag line as a command tag line when both the status and the control tag lines are activated.

When the FMT uses the status tag, control tag, and command tag lines to control the MTU, the FMT receives a response from the MTU. When the response is not normal, the status tag response check, control tag response check, and command tag response check are set.

FRU1 (DSB14) ... Control data
(Content of DVBO register)
FRU2 (DSB15) ... Response data
(Content of DVBO register)

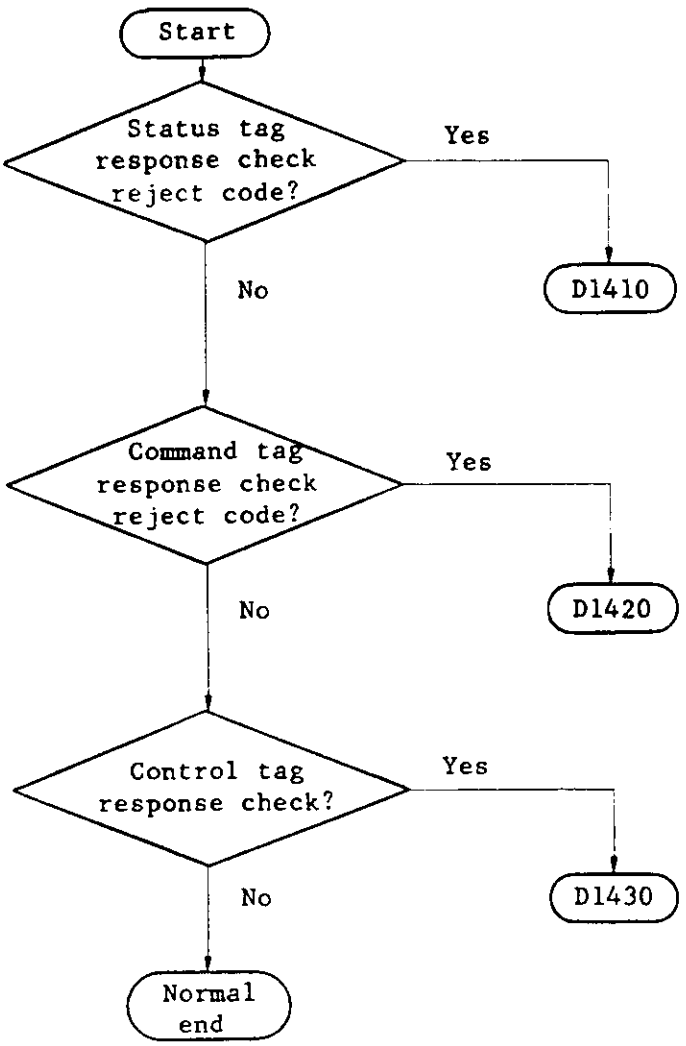
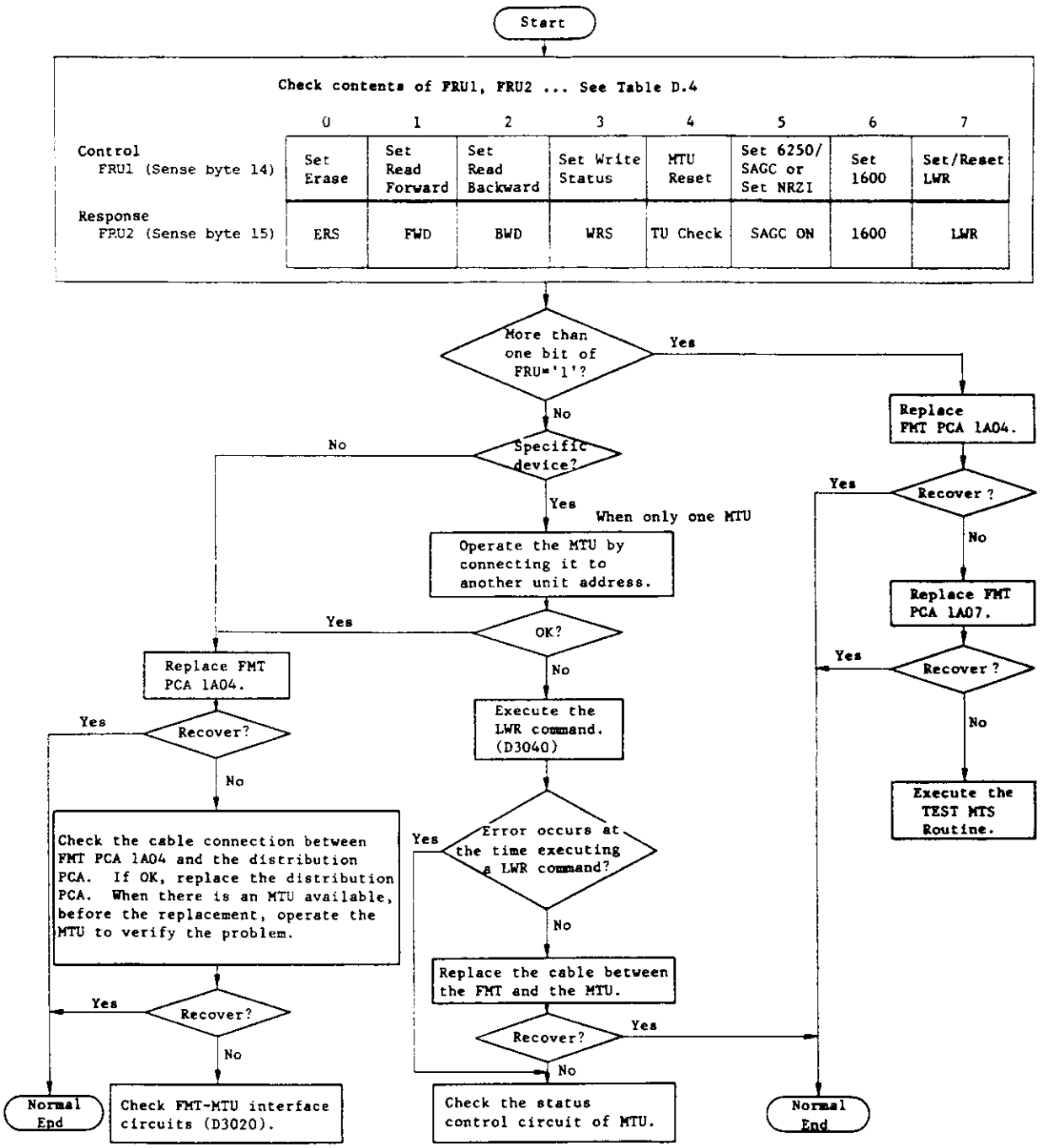


Table D.4 Response check with status tag control

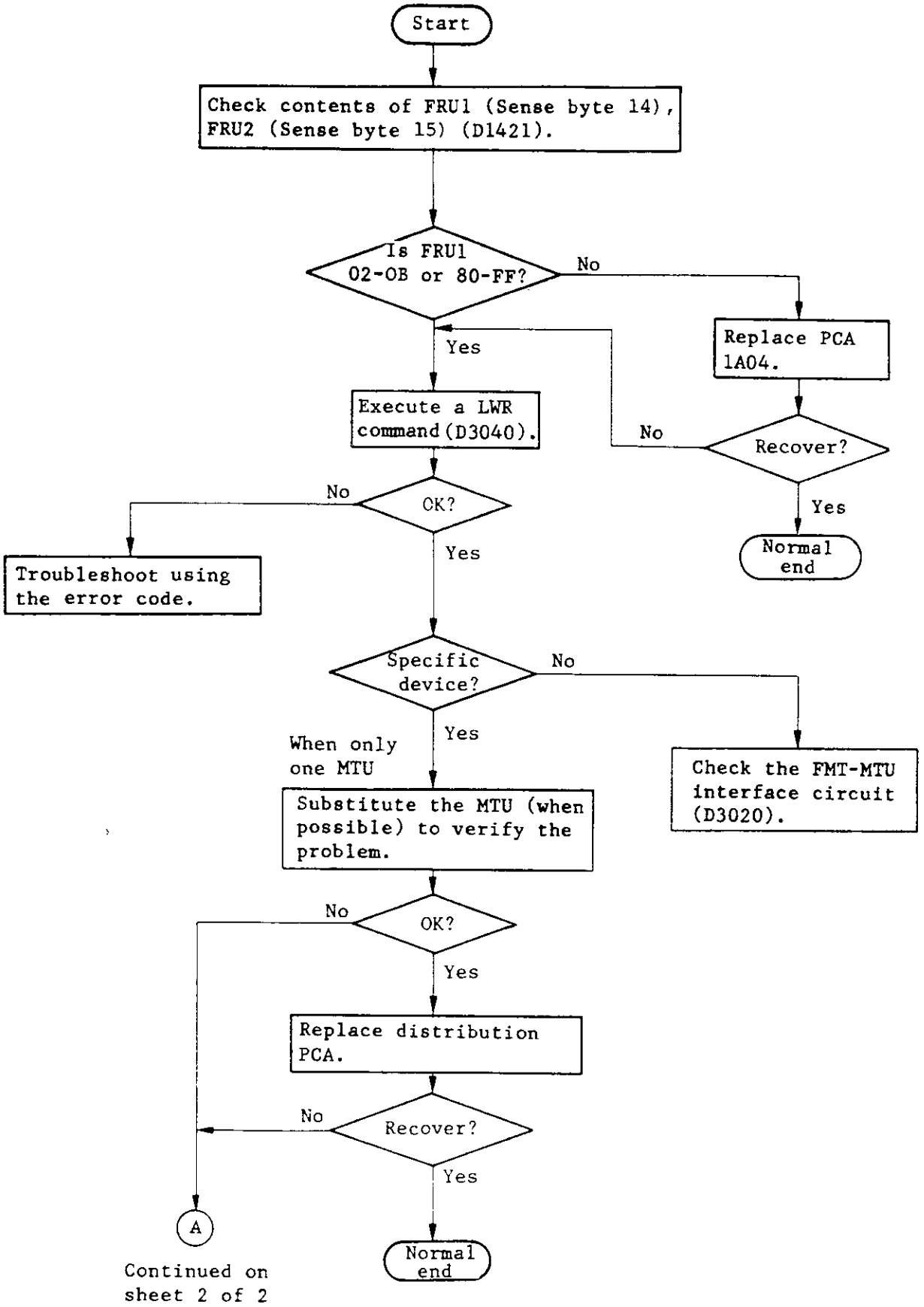
Control (FRU1) bit	Function	Response (FRU2) check	Time out
bit 0	Set ERASE ("1")	ERS=1, LWR=0 FWD=1, BWD=0	500 ms
bit 1	Set read forward ("1")	BWD=1, ERS=0 FWD=0 WR =0 LWR=0	500 ms
bit 2	Set read backward ("1")	BWD=1, ERS=0 FWD=0 WRS=0 LWR=0	500 ms
bit 3	Set read backward ("1")	ERS=1, BWD=0 FWD=1, LWR=0 WRS=1	500 ms
bit 4	Reset MTU ("1")	TU check = 0 (DVINT = 0)	10 μs (100 μs)
bit 5	Set GCR/NRZI ("1")	1600 = 0	13.6 ms
bit 6	Set PE ("1")	1600 = 1 SAGC = 0	13.6 ms
bit 7	Set LWR Reset LWR ("1")	LWR = 1 LWR = 0	13.6 ms

D1411	Status Tag Response Check = 2

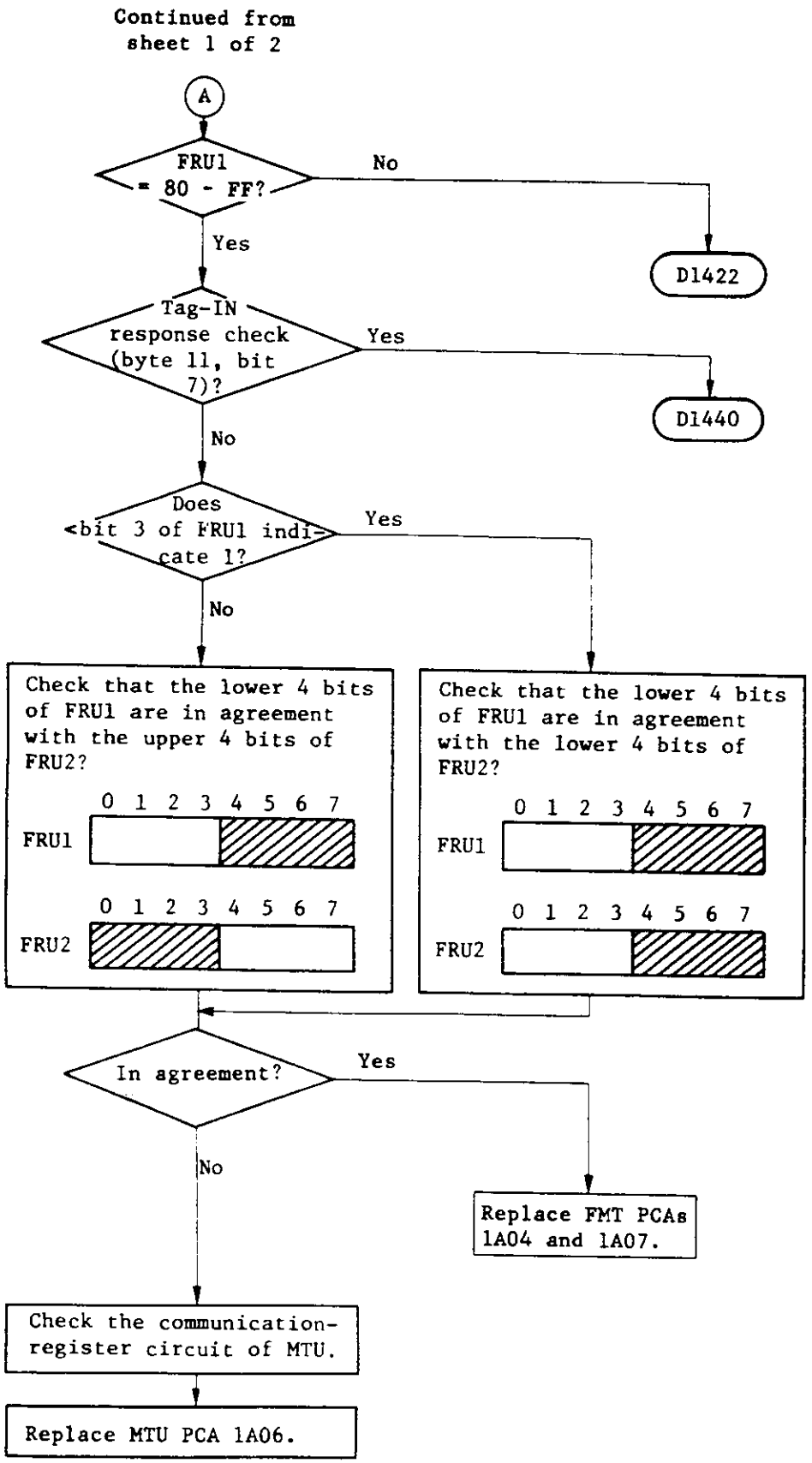


	0	1	2	3	4	5	6	7
Control FRU1 (Sense byte 14)	Set Erase	Set Read Forward	Set Read Backward	Set Write Status	MTU Reset	Set 6250/ SAGC or Set NRZI	Set 1600	Set/Reset LWR
Response FRU2 (Sense byte 15)	ERS	FWD	BWD	WRS	TU Check	SAGC ON	1600	LWR

D1420	Command Tag Response Check - 1



D1420	Command Tag Response Check - 1



FRU1 (Sense byte 22)

bit 0 1 2 3 4 5 6 7		Function	Response (FRU2)	Time out
0	2	Set streaming mode	Streaming mode = 1	1513 ms
0	3	Reset streaming mode	Streaming mode = 0	
0	4	Space file	READY = 0	
0	5	Backspace file	READY = 0	
0	6	(Spare)		
0	7	(Spare)		
0	8	Set LWR2	LWR2 = 1	13.6 ms
0	9	Reset LWR2	LWR2 = 0	
0	A	Set low slice	Low slice = 1	
0	B	Reset low slice	Low slice = 0	

FRU2 (Sense byte 23)

bit 0	1	2	3	4	5	6	7
Streaming feature	Skip file feature	(Spare)	Low sloce	Streaming mode	LWR2	Handler action	READY

FRU1 (Sense byte 22)

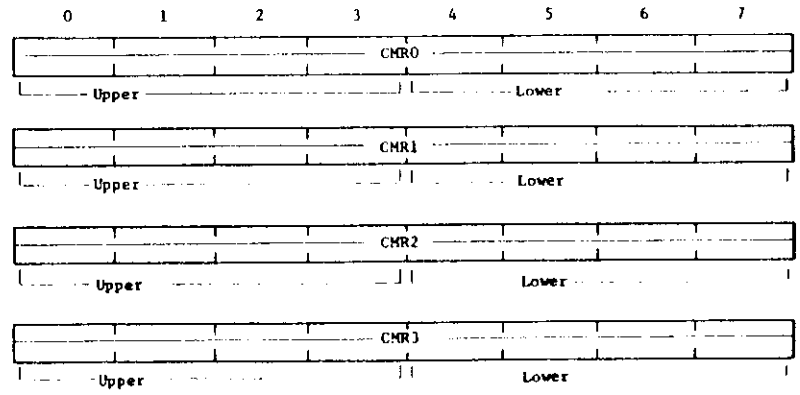
bit 0 1 2 3 4 5 6 7		Function
8	0 ∿ F	Set CMR0 upper
9	0 ∿ F	Set CMR0 lower
A	0 ∿ F	Set CMR1 upper
B	0 ∿ F	Set CMR1 lower
C	0 ∿ F	Set CMR2 upper
D	0 ∿ F	Set CMR2 lower
E	0 ∿ F	Set CMR3 upper
F	0 ∿ F	Set CMR3 lower

Response/Time out

The upper and lower values of CMR are in agreement with those intended to be set.

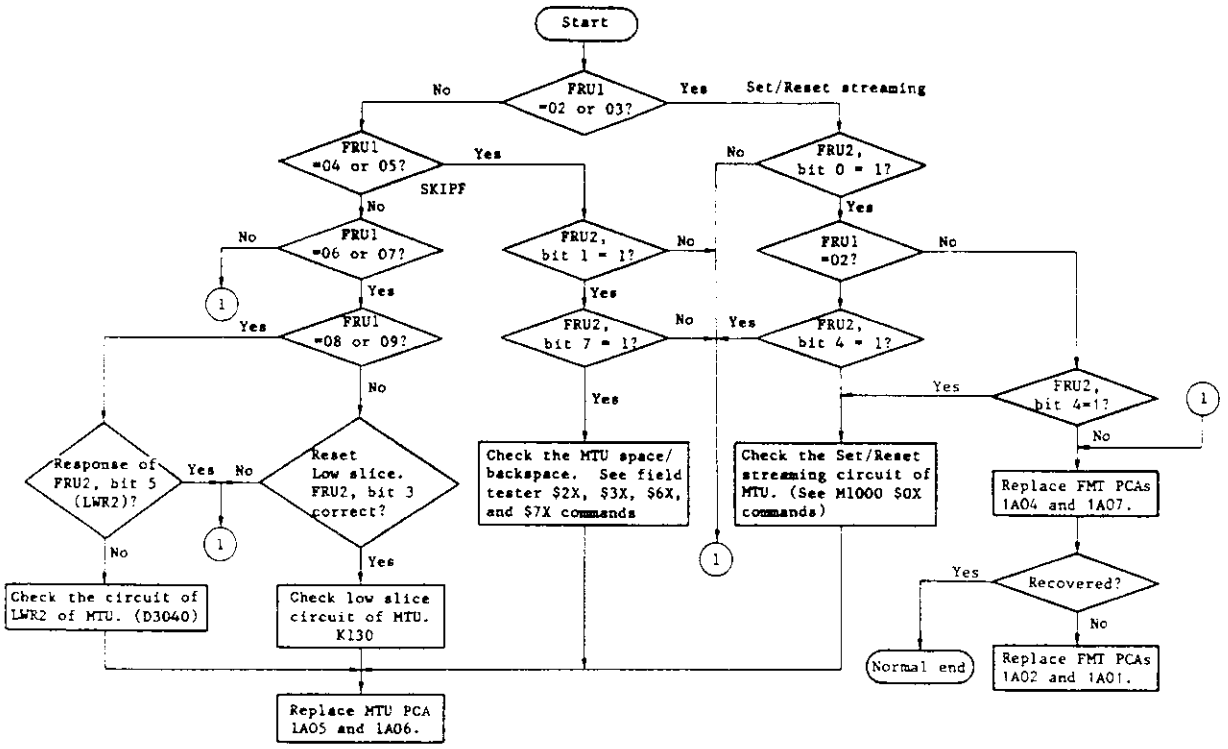
Time out = 700 μs

FRU2 (Sense byte 23)



CMR0 ∿ 3: Communication register 0 ∿ 3.

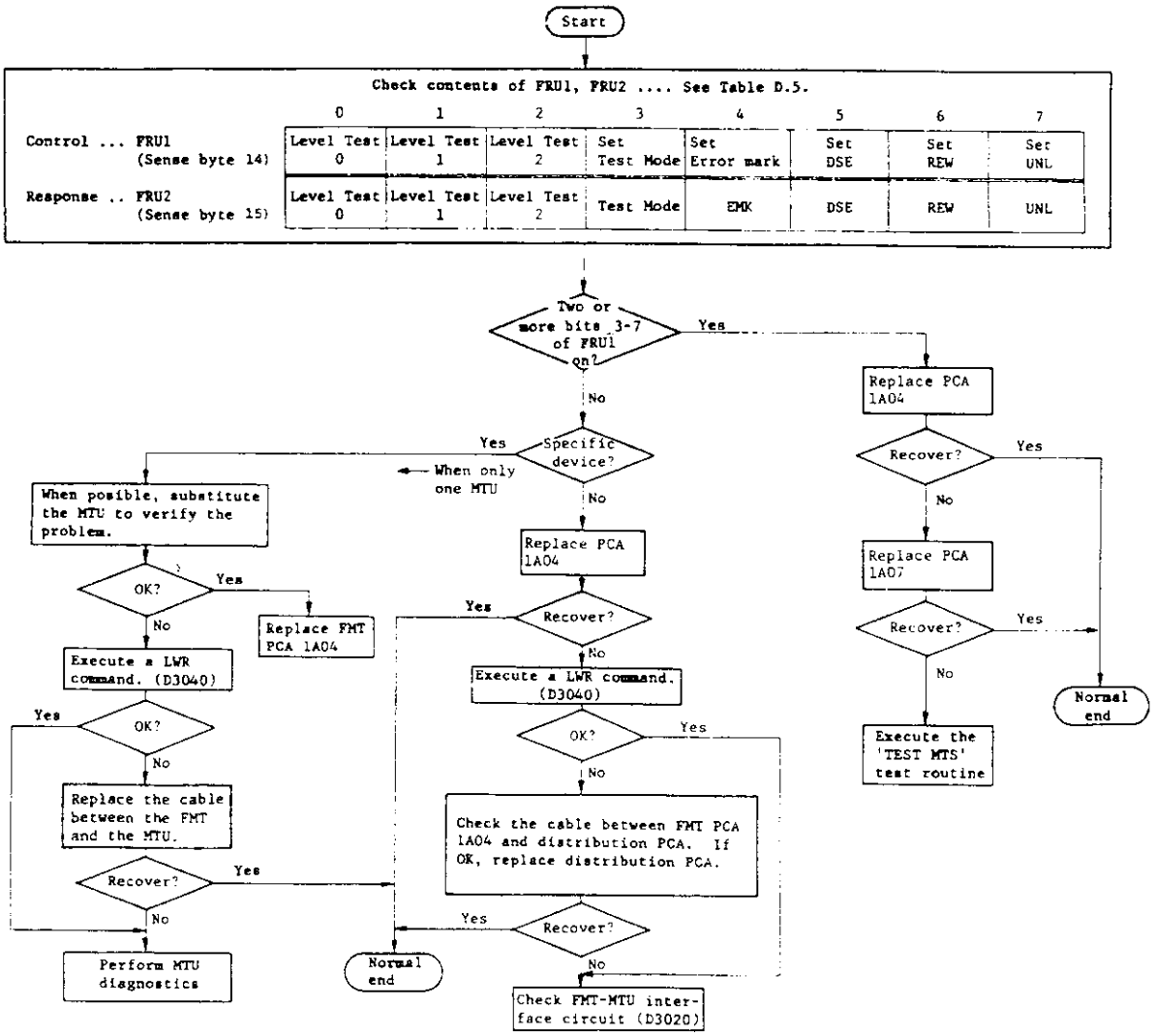
D1422	Command Tag Response Check - 3



D1430 Control Tag Response Check

Table D.5 Response check with Control Tag

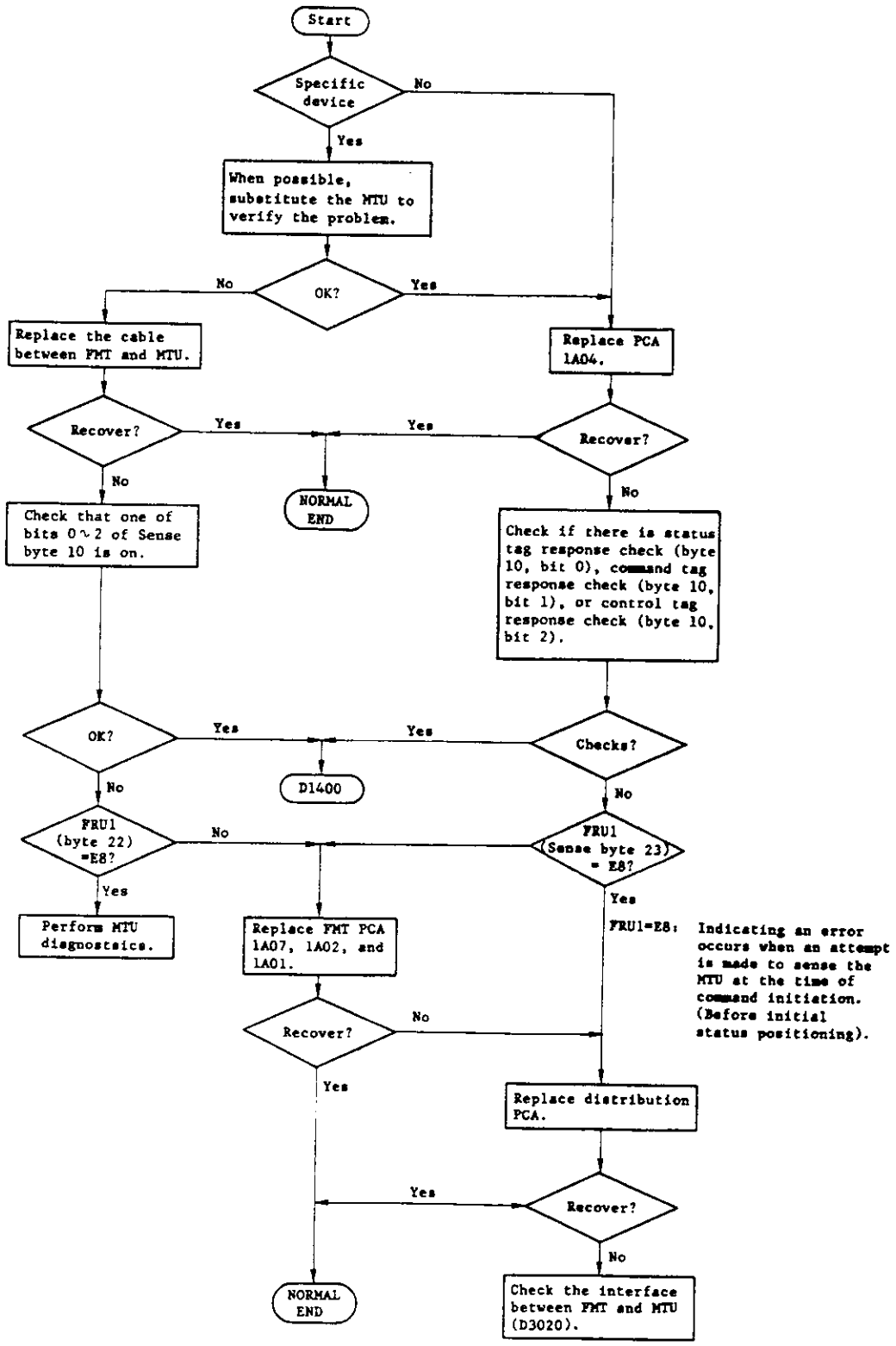
Control FRU1	Function	Response (FRU2)	Time out
bit 0 ~ bit 2	Level set	Level Test 0~2	500 ms
bit 3	Set Test-Mode	Test Mode	500 ms
bit 4	Set EMK	EMT = 1	500 ms
bit 5	Set DSE	DSE = 1 (also READY = 0)	500 ms
bit 6	Set REW	REW = 1 (also READY = 0)	500 ms
bit 7	Set UNL	UNL = 1 (also READY = 0)	500 ms



D1440	Tag In Check

Error is generate when TAG-IN signal response does not arrive from MTU within the prescribed time.

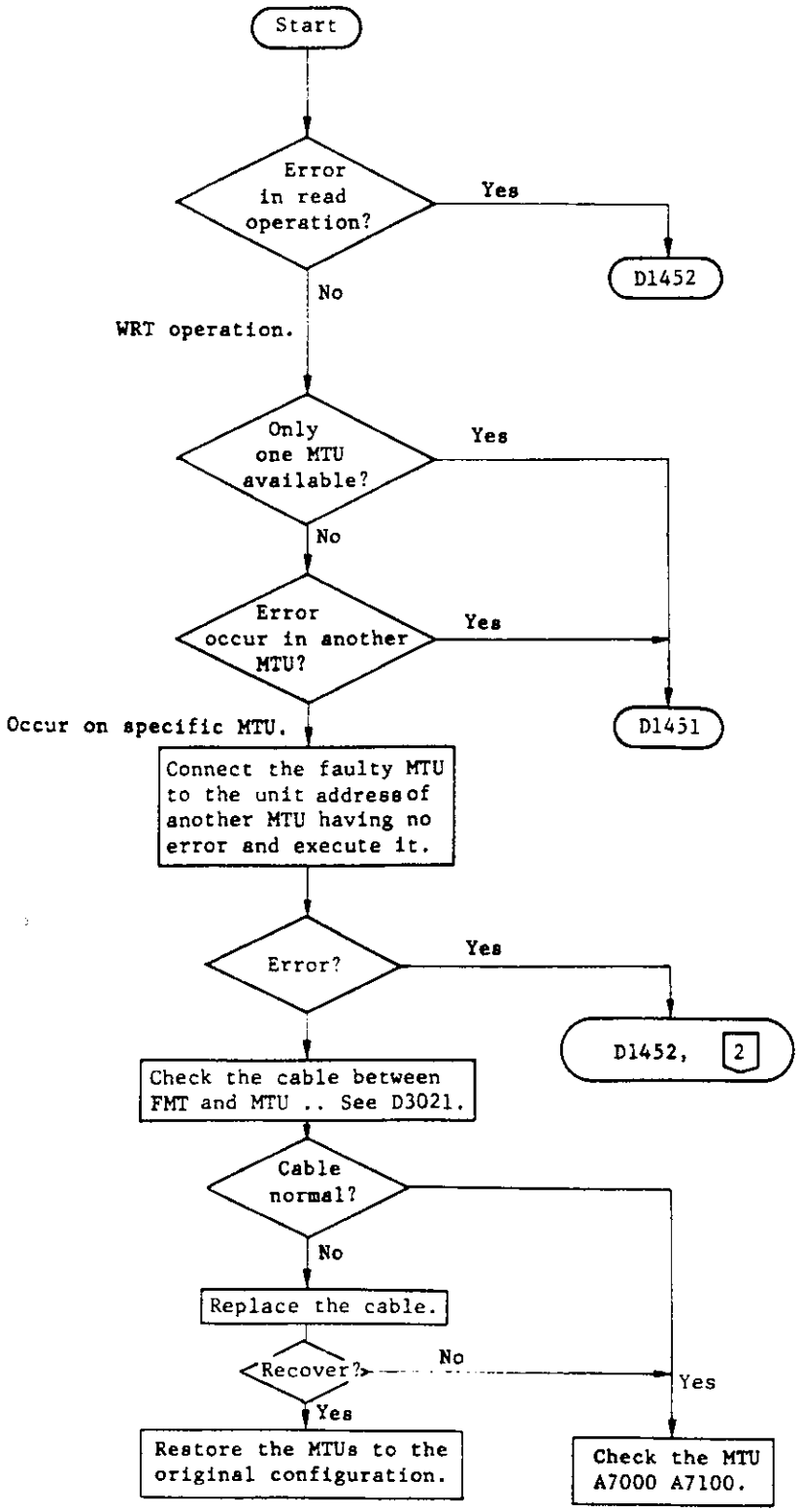
(Prescribed time = 3 through 7 μs)



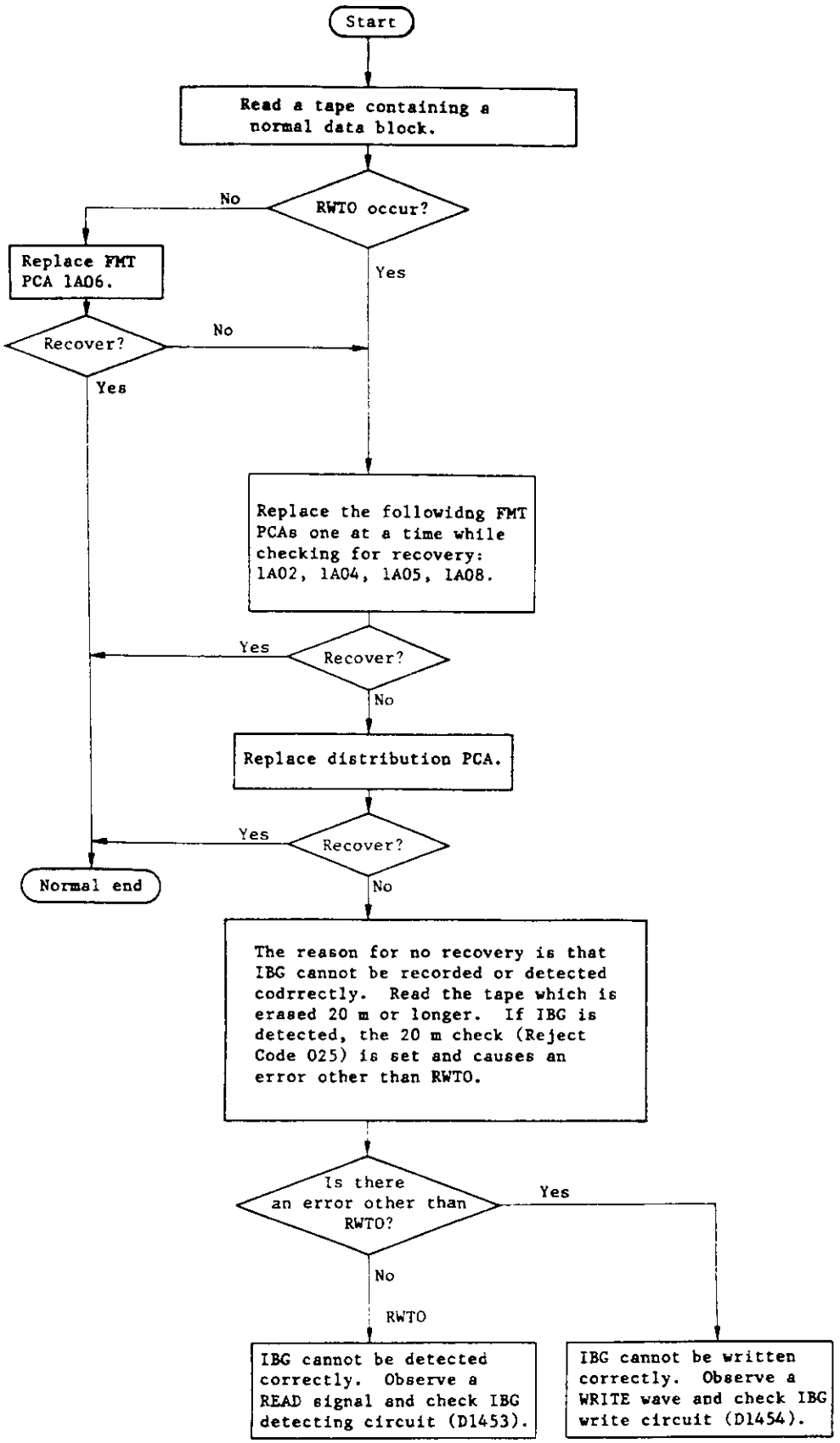
D1450	Read/Write Overrun - 1 (Reject Code 125)

Sets when the write and read operations of one data block are carried out over 15 m or the time interval equivalent to 15 m run. ..... RWTO

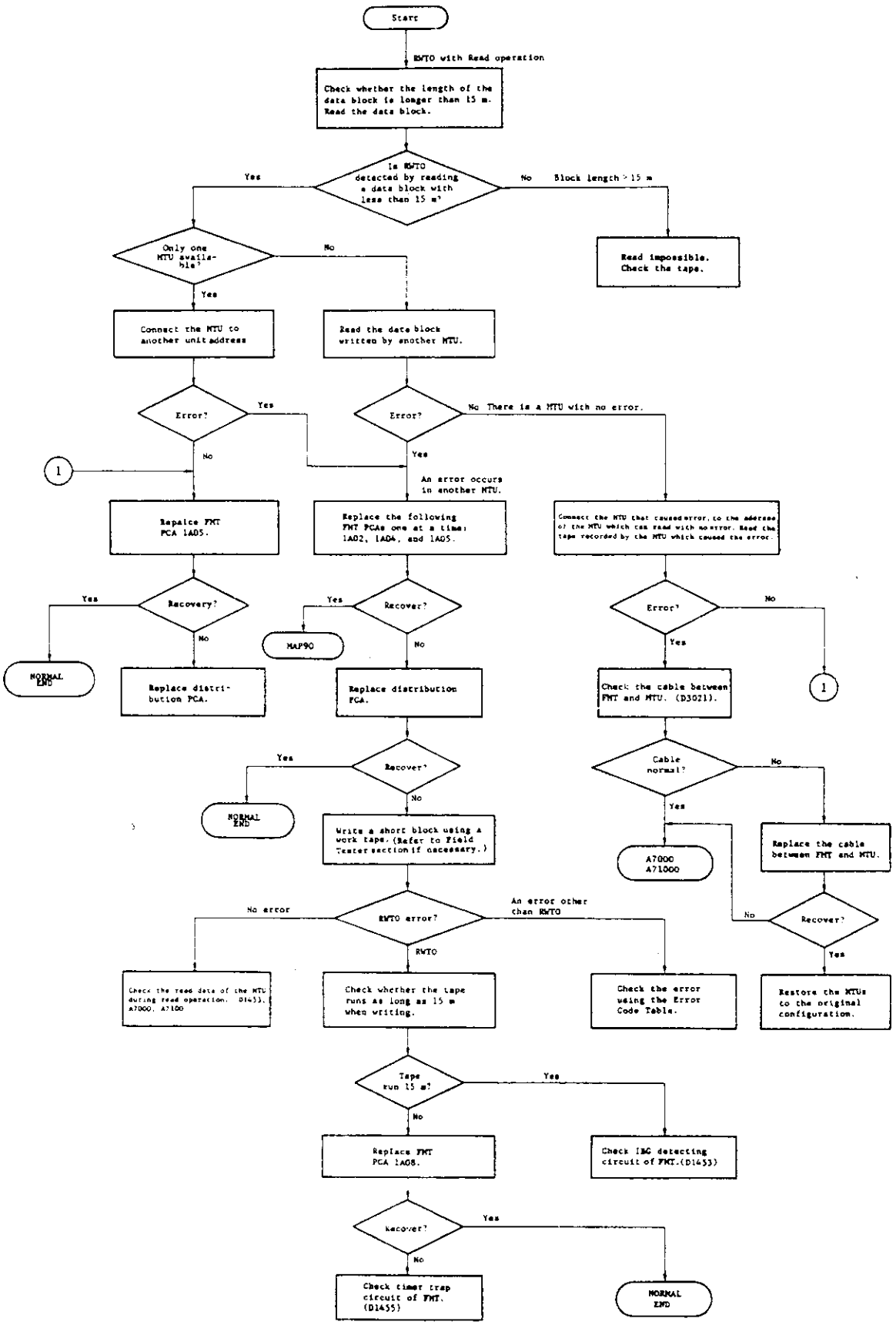
FRU1 (DSB14) = 77



D1451	Read/Write Overrun - 2



D1452	Read/Write Overrun - 3



D1453	Time Sense Decode Circuit

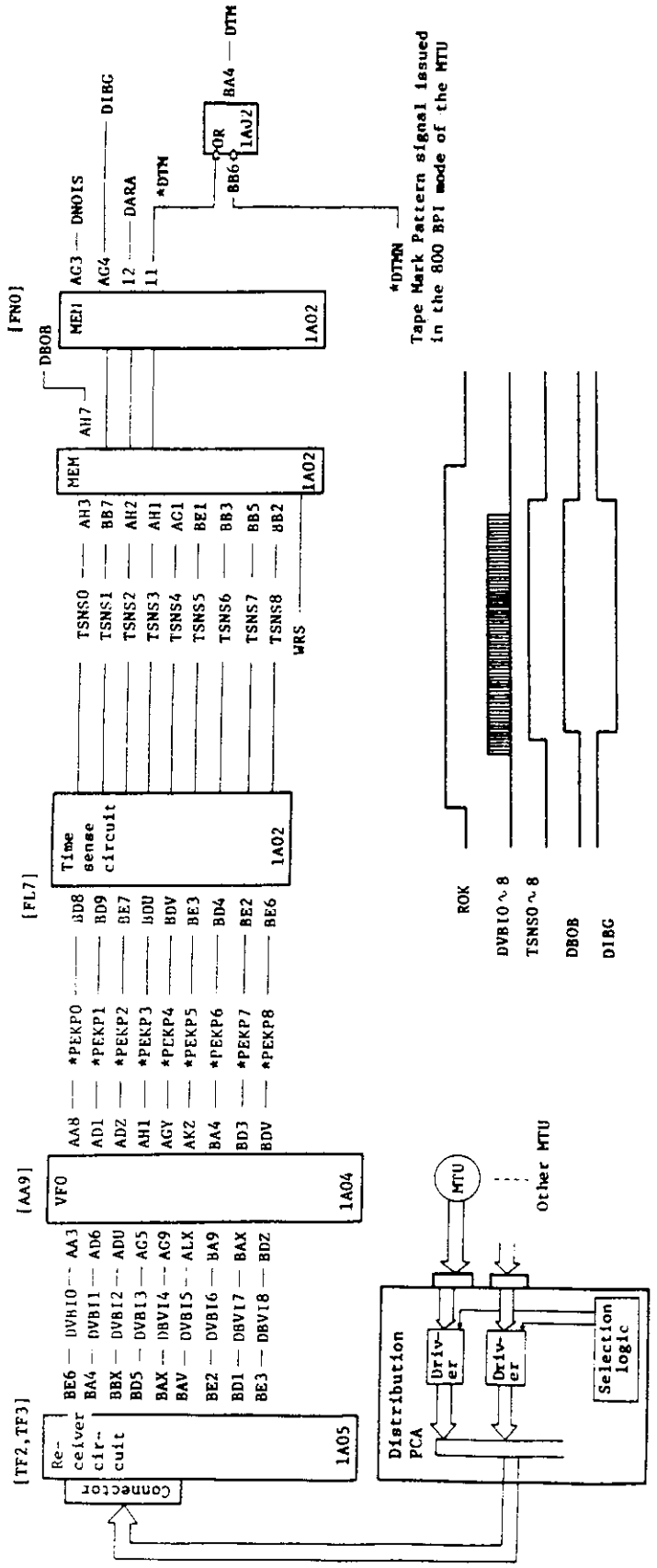


Figure D.12 Time sense decode circuit

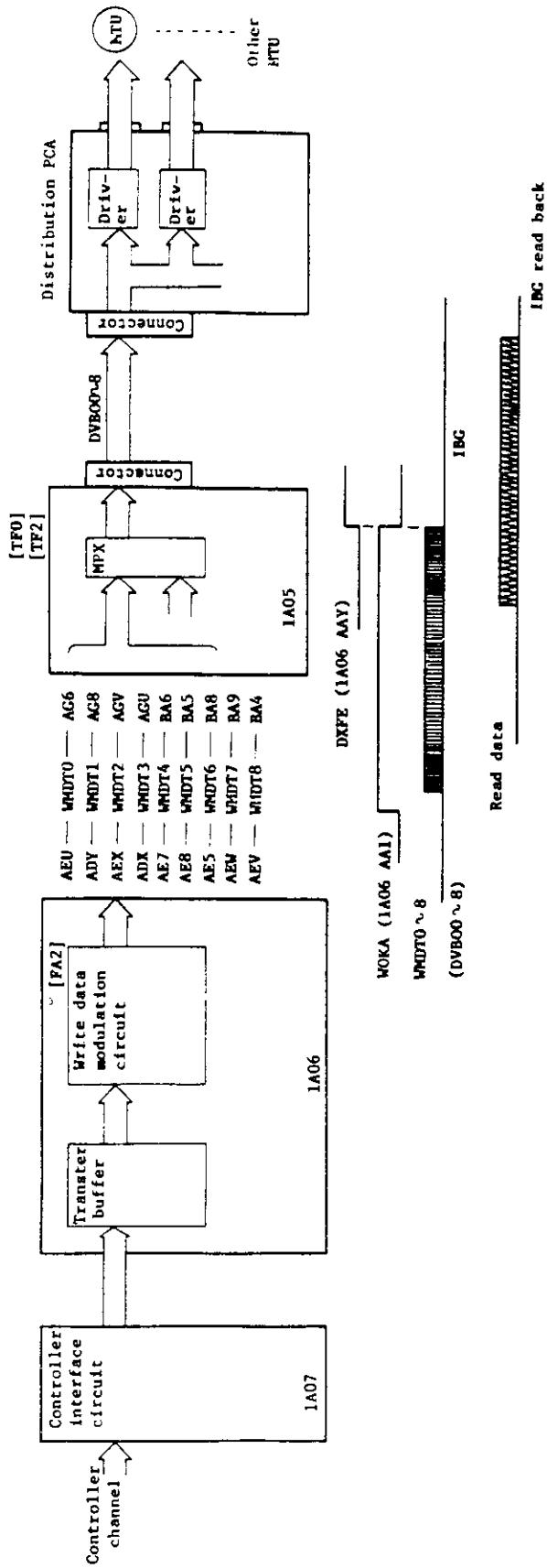


Figure D.13 Write data circuit

D1455	RWTO Trap

FTP pulses generated from CPA and CPB tach signal are counted by 16 bit counter. When the counter overflows (65536 count), TMINT signal is generated and a microprocessor trap occurs. If FTP signal has been generated correctly, the trap takes place after 8.23/4.94/3.09 seconds have elapsed in the 75/125/200 ips speed mode. GO signal to the MTU is turned off if IBG has been detected bebore the time elapse.

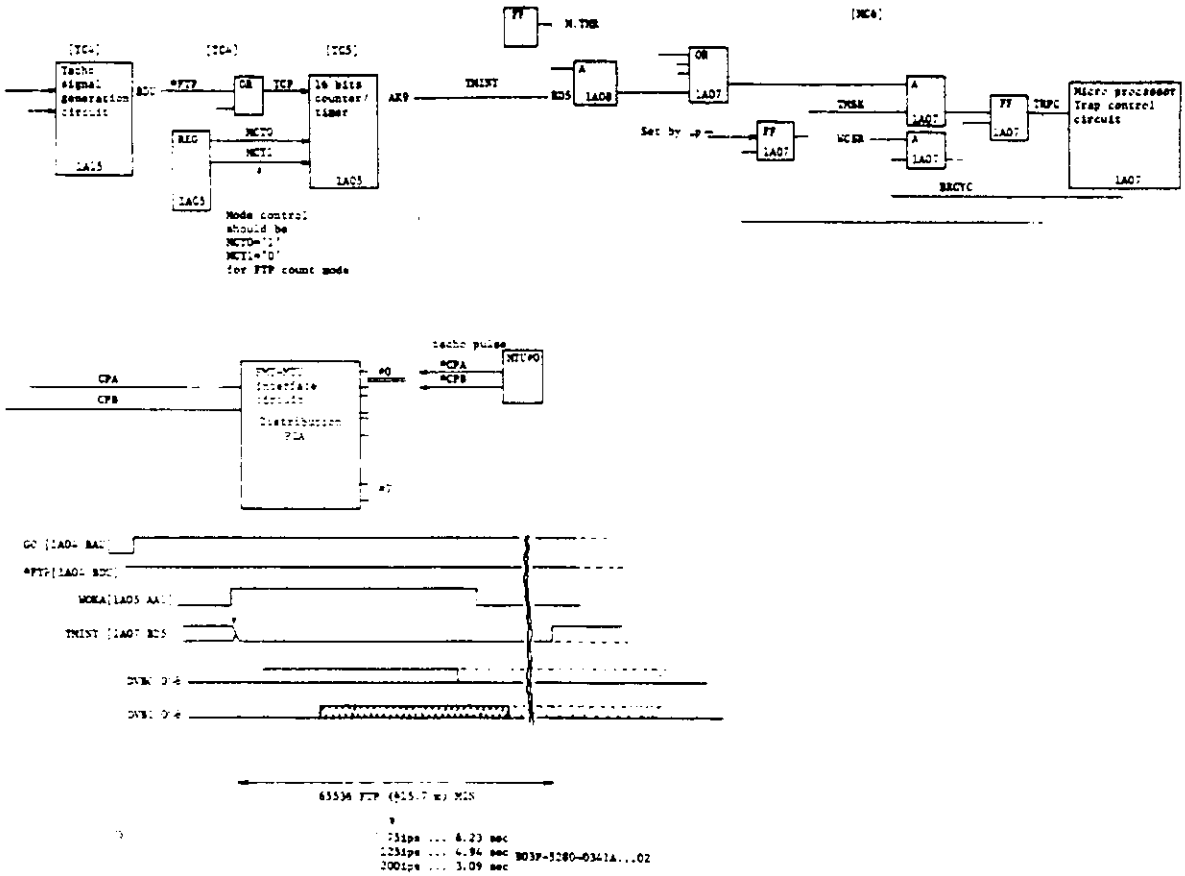
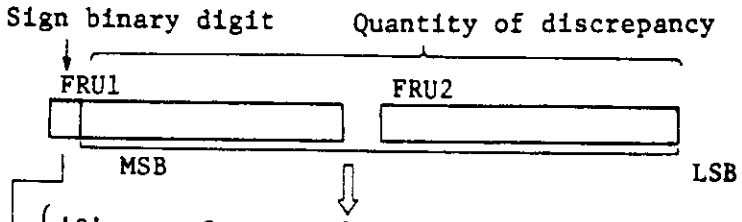


Figure D.14 RWTO trap

D1460	Missing Position - 1 (Reject Code 035)

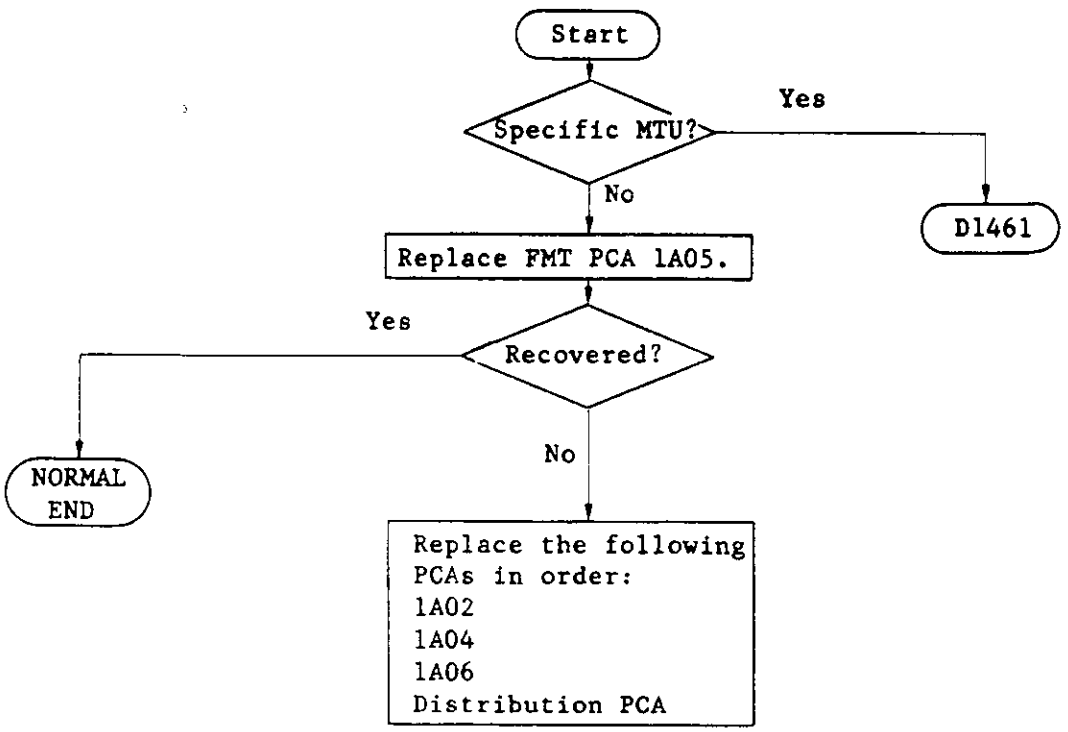
When a data check error is generated in write, Read or Read backward command operation, the information concerned with the length of block recorded in the operation is stored in communication register of MTU. For error recovery the Back Space command corresponding to the Read and Write command or the Space command corresponding to the Read Backward command is issued. The space length (associated with Space or Back Space command) is compared with the error block length stored in communication register. When the difference between the lengths is larger than the requirement, Reject Code 035 is generated.

FRU1 (DSB14) and FRU2 (DSB15) provide inforamtion of the length discrepancy.

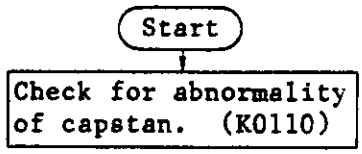


'0' .... Space or backspace more than the blocklength by described TP counts.

'1' .... Space or backspace less than the block length by described TP counts. (two's complement)



D1461	Missing Position - 2



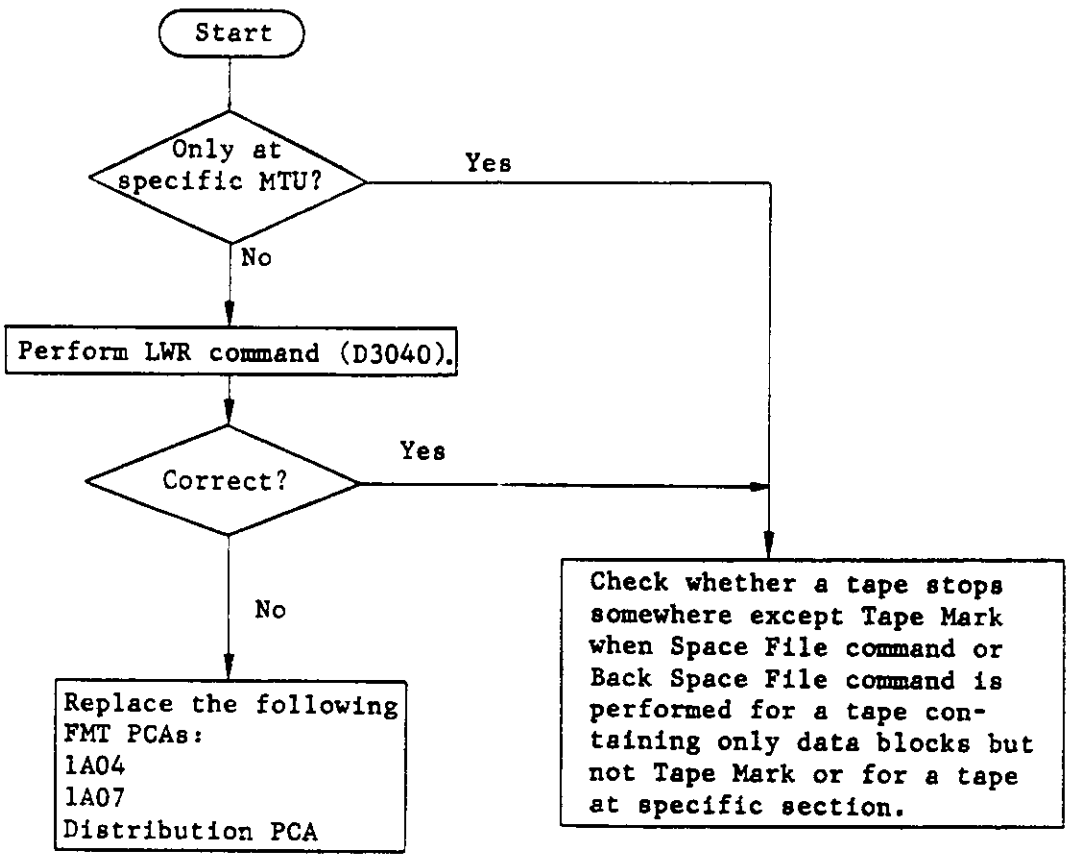
D1465	Missing Tape Mark (Reject Code 310)

After instructing MTU to search for Tape Mark Search in order to perform Space File or Back Space File command an error occurs:

1) When Tape Mark block cannot be detected correctly, though MTU enters ready status.
   (Bit 7 of TU sense byte, (Tape Mark) is 0.)

2) When MTU detects an interruption (except BOT detection and Tape overrun of the MTU).

Note: In this case, RWTO (Sense byte 11, bit 0) is also generated.



D2000	Data Check

Data check occurs when the followisng errors are detected:

(1) R/W and internal circuit error:

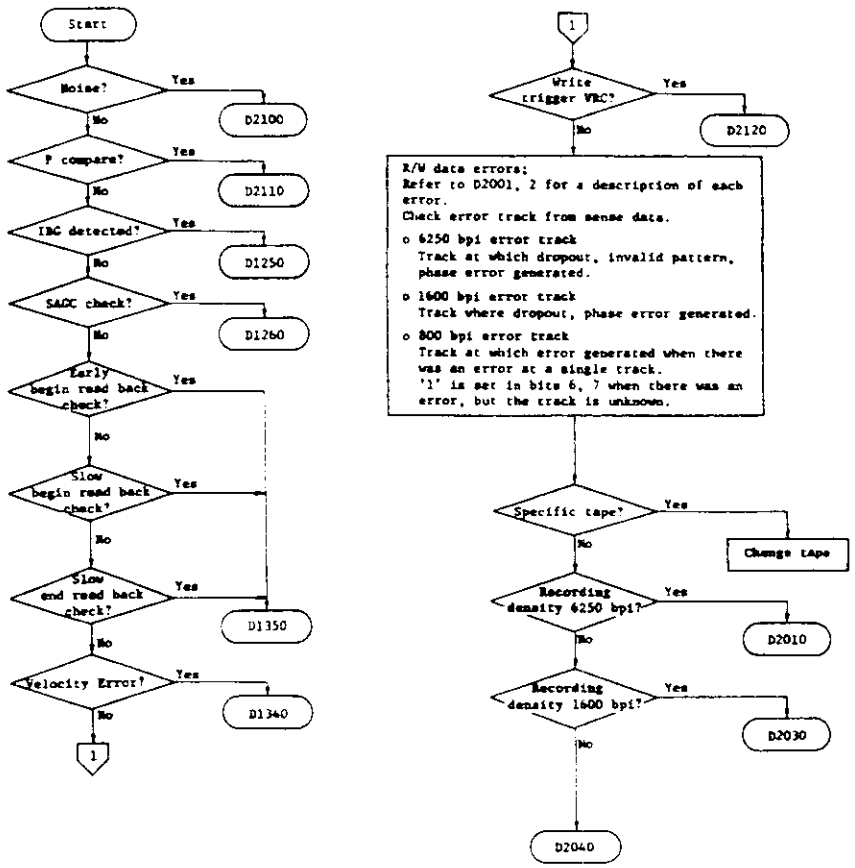
CRC error	MUX byte	1 - P
Uncorrectable error/skew error	byte	6
Partial Record	byte	5
Multiple track error/LRC error	byte	4
Miscellaneous Data error	byte	3
End of Data check/VRC error	byte	2

Details of Miscellaneous Data error

IBG Detected	DSB	11 - 7
Start Read check	DSB	- 6
CRC III check	DSB	- 5
SAGC check/Noise error	DSB	- 3
P compare	DSB	- 0
Skew error	DSB	12 - 3
Write Error Count Overflow	DSB	- 2
Envelope check	DSB	- 1
Write Trigger VRC	DSB	- 0

(2) Tape speed error

Early begin read back check	BSD	11 - 4
Slow begin read back check	BSD	11 - 2
Slow end read back check	BSD	11 - 1
Velocity error	MUX byte	1 - 1



D2001	Data Check Sense Byte Explanation - 1

- Uncorrectable error occurs:
  (1) When recoverable VRC error generated at read (read backward command).
  (2) When VRC error generated at write (LWR command). (May have CRC error set also.)

- Multiple track error/LRC error occurs:
  (1) When there is a pointer of 2 tracks or more at 6250 bpi write (LWR command).
  (2) When there is a pointer of 3 tracks or more at 6250 bpi read (read backward).
  (3) When there is a pointer of 2 tracks or more at 1600 bpi read (read backward).
  (4) When 800 bpi horizontal parity check error was generated. (Error Track may have been reset by RESYNC at 6250 bpi read operation.)

- Skew error occurs:
  (1) When excessive skew detected at 6250/1600 bpi read, read backward, write command.

6250 bpi write	RIC-ROC	2
1600 bpi write	RIC-ROC	14
6250 bpi read	RIC-ROC	30
1600 bpi read	RIC-ROC	15

  (2) When excessive skew detected at 800 bpi write, write tapemark command.

- End data check/CRC error occurs:
  (1) When postamble cannot be detected at 1600 bpi read operation. (No READEND)
  (2) When postamble is not all "1"s at 6250 bpi or not all "0"s at 1600 bpi.
  (3) When postamble is too long.

- Envelope check occurs:

  When dropout detected at 1600 bpi/6250 bpi write operation.

Notes:
  (1) Envelope check does not cause Data check at 6250 bpi operation.
  (2) Use D2010 - D2020 for 6250 bpi.
  (3) Use D2030 - D2032 for 1600 bpi.
  (4) Use D2040 - D2041 for 800 bpi.

D2002	Data Check Sense Byte Explanation - 2

- Start read check
  (1) When IBG is encountered before data detected after block is detected (at 6250/1600 bpi operation).
  (2) When data is not detected within the prescribed time after block is detected (at 6250/1600 bpi operation).

- Partial record
  When IBG encountered in data at 6250/1600 bpi.

- IBG detected
  When IBG is detected while reading data at 6250/1600 bpi write command.

- CRC error occurs:
  (1) When CRC is not normal pattern.
  (2) When CRC III error is set.

D2003	Explanation of CRC III Error

- CRC III error occurs:
  (1) When CRC-B byte and CRC-D byte match at 6250 bpi write (readcommand).
  (2) When CRC-C byte was incorrect pattern (at 6250 bpi read backward).
  (3) When CRC-B byte and CRC-C byte didn't match (at 1600/800 bpi write command).

-------- CRC error set --------

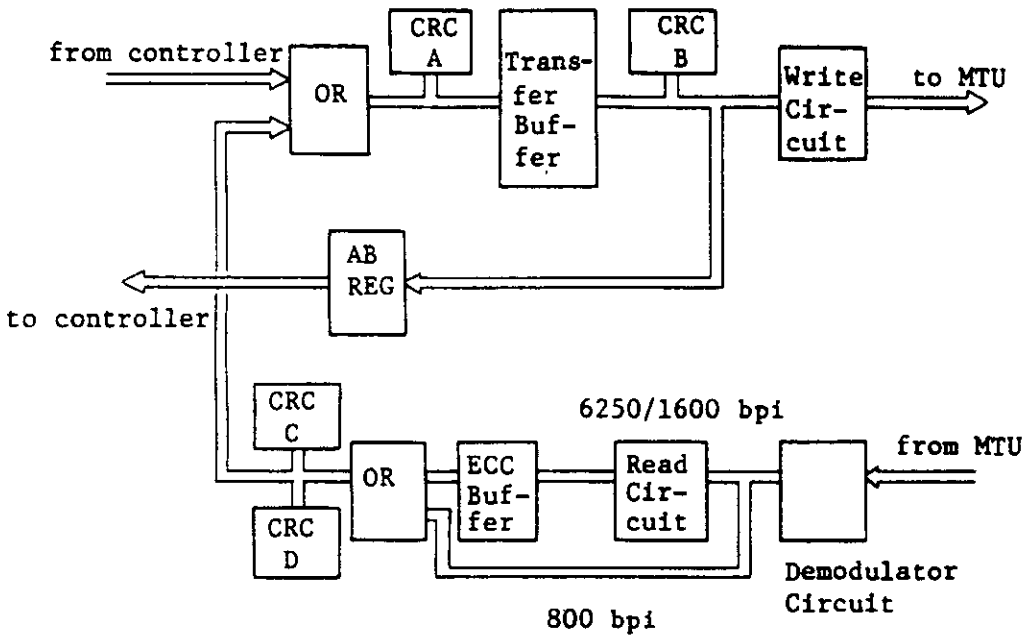


Figure D.15 CRC generation circuit

Mode	6250 bpi	1600/800 bpi	Sense
	A ≠ B	A ≠ B	P compare
	B ≠ D	B ≠ C	CRC III error
Read	A ≠ B	A ≠ B	P compare
	B ≠ D	-	CRC III error
Read backward	A ≠ B	A ≠ B	P compare
	C≠Match pattern	-	CRC III Error

- o CRCA : CRC pattern is generated from transfer buffer input.
- o CRCB : CRC pattern is generated from transfer buffer input.
- o CRCC : CRC pattern is generated from read data.
- o CRCD : Set CRC of read data at 6250 bpi.
- o When CRC III error or P Compare error is indicated (in the DSB11 FRU1 and FRU2 described below).

D2003	Explanation of CRC III Error

FRU1 (DSB14)

7	6	5	4	3	2	1	0
'0'	'0'	'0'	'1'	'0'	ABRPC	DBCK	(WVRC)

This code indicates that detailed CRC information was stored on FRU1, bit 4 - 7, and FRU2 successfully.

A/B register parity error.

Deskewing buffer check

FRU2 (DSB15)

7	6	5	4	3	2	1	0
*MCRC	*MCRCZ	EP/=CR	B=/D	B=/C	*MCRCC	A/=B	XBIC

Contents of CRCST register

- *MCRC (Not match CRC)
  "1" when CRC pattern generated as a result of read operation is not normal.

- *MCRCZ (Not match CRC zero)
  "1" when CRC pattern generated as a result of read operation is not all '0's.

- EP=/CR
  "1" when CRC pattern does not match EP (error pattern) register.
- B=/D
  "1" when CRCD does not match CRCB.

- B=/C
  "1" when CRCB does not match CRCC.

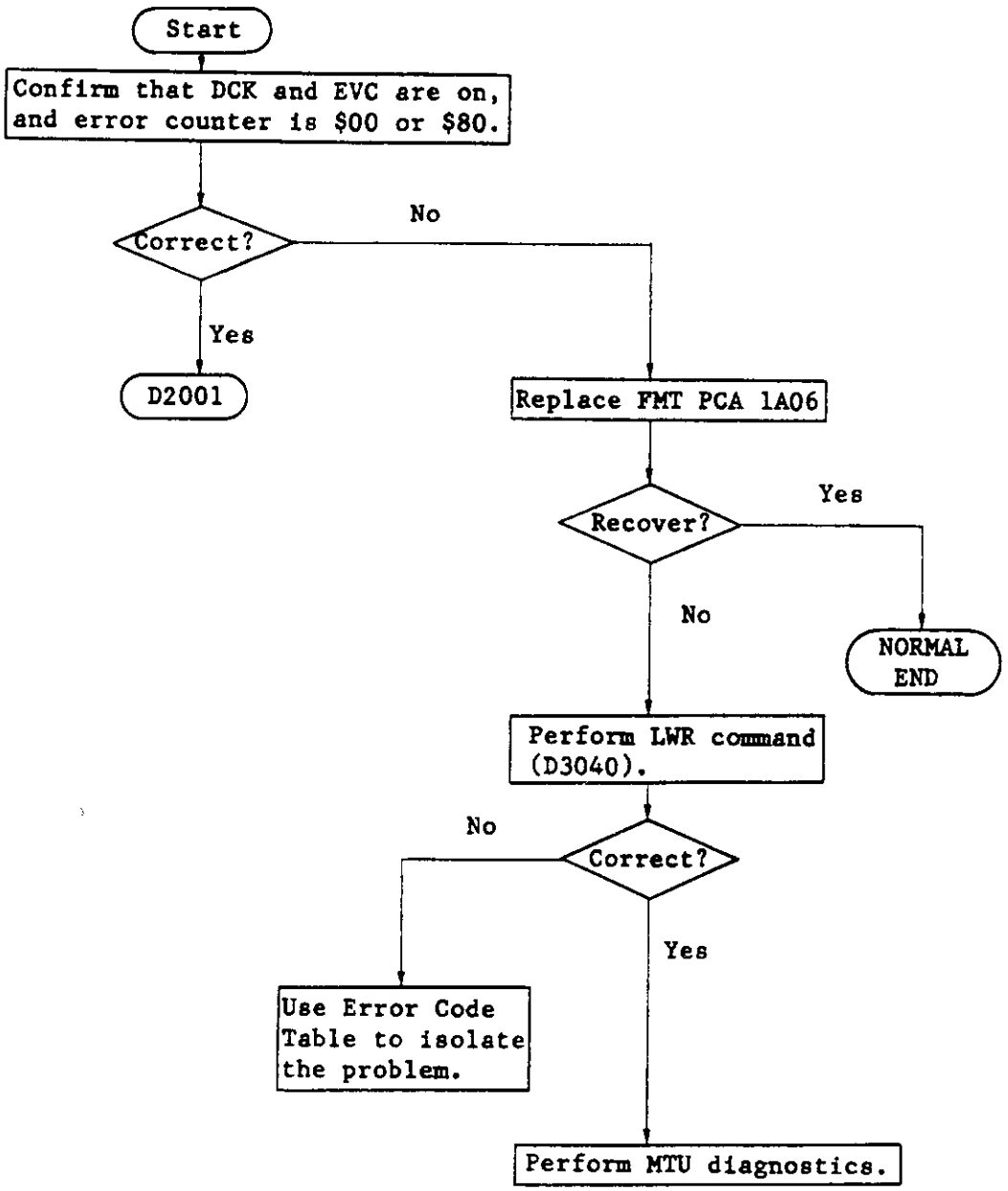
- *MCRCC (Not match CRCC)
  "1" when CRC pattern obtained from read data excluding CRC byte is not normal.

- A/=B
  "1" when CRCA does not match CRCB.

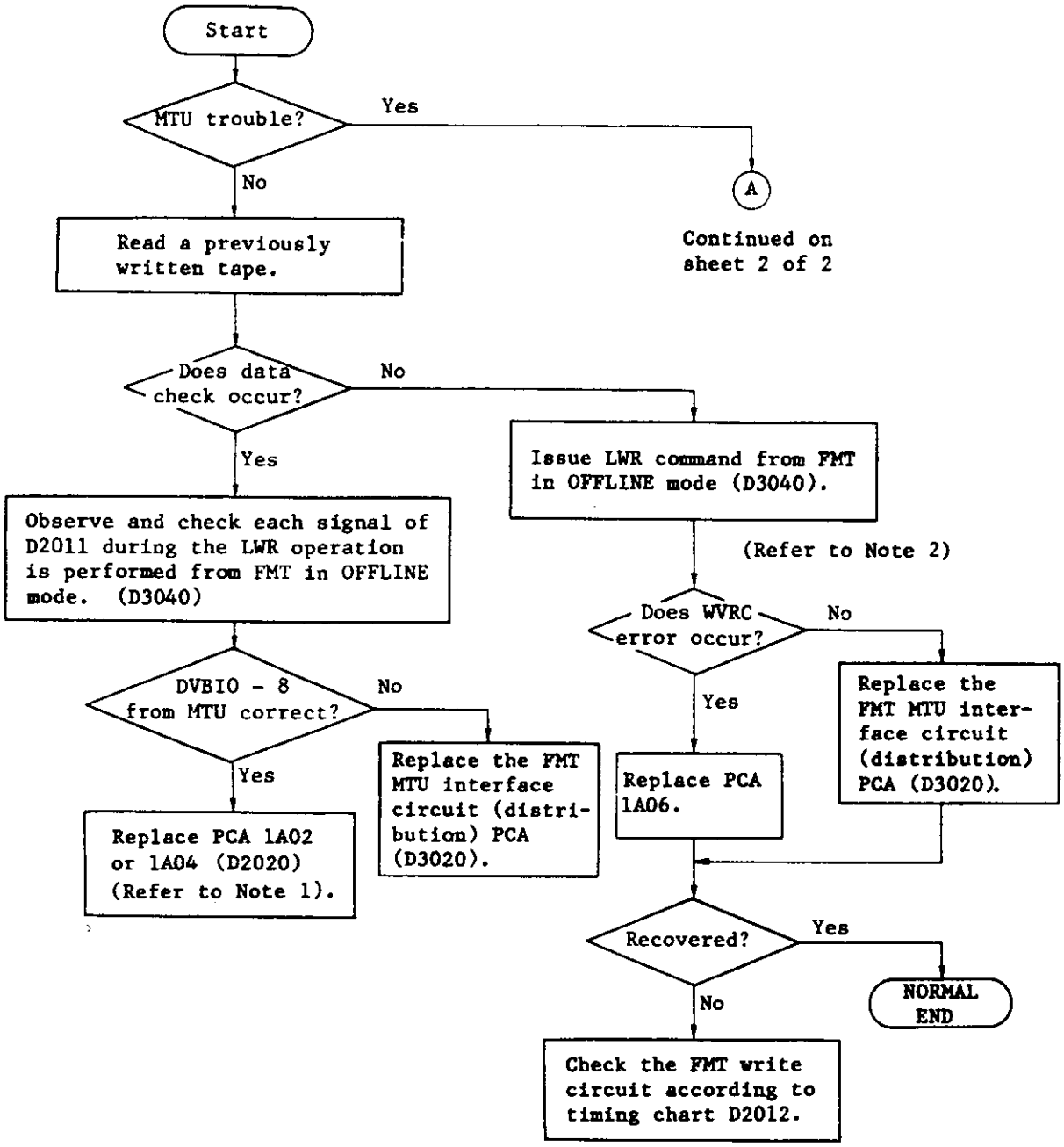
- XBIC
  Transfer buffer bus in check, "1" when illegal XFR Buffer input data is applied.

D2004	Error Count Overflow

The error counter is incremented if EVC (Envelope check: DSB12, bit 1) is generated as a result of performing the write operation in the 6250/1600 bpi mode. When performing write operation in 6250 bpi mode, if the error counter reaches $00 or $80, ECOVF (error counter overflow: DSB12, bit 2) is generated. ECOVF is generated each time 128 EVC errors are detected. The error counter is provided for each MTU.



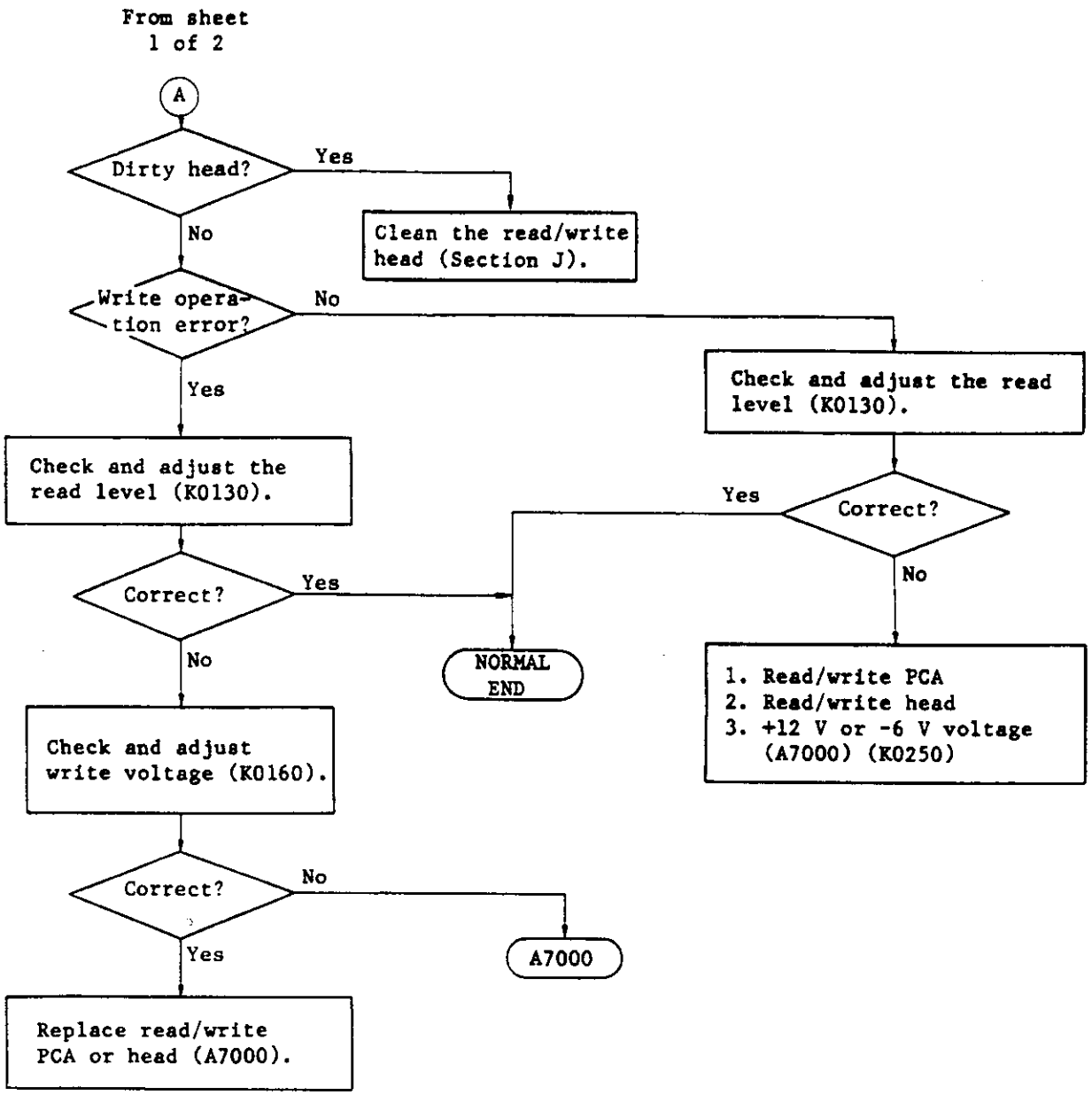
D2010	6250 bpi Data Check -1



Note 1: How to search error track:
(1) Place the FMT in offline mode and perform LWR command (D3040)
(2) After the LWR command is performed, an errored track can be checked by displaying the register at $22.

Note 2: How to search error:
(1) Display the contents of the register at $24.
(2) WVRC is bit 3.

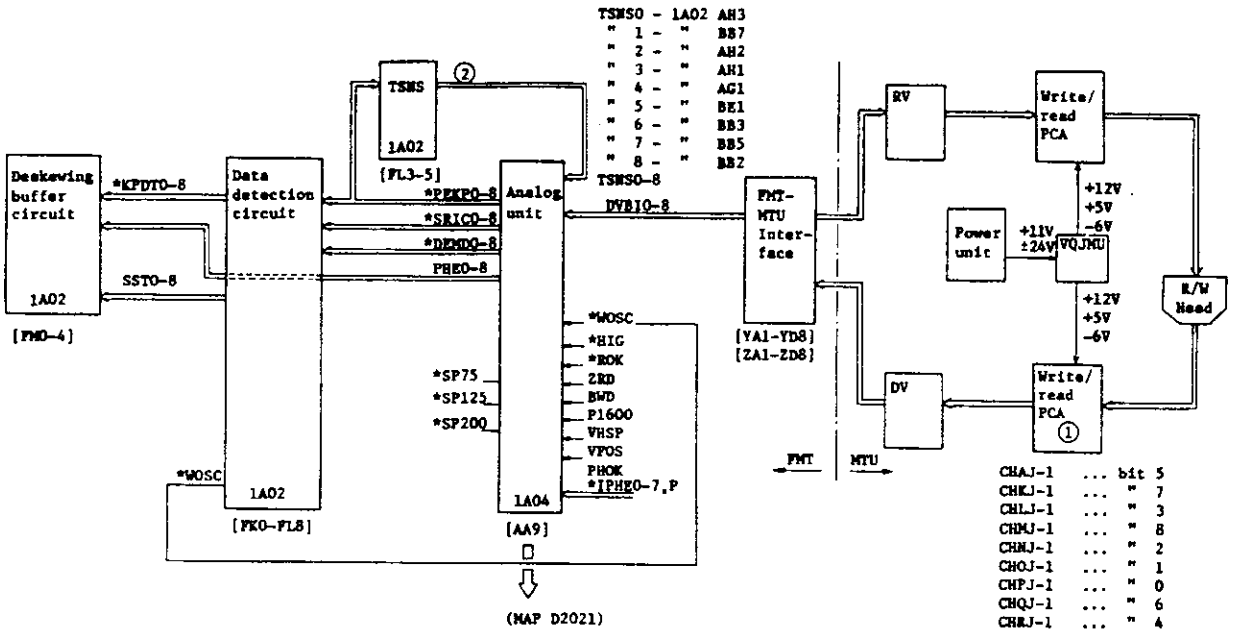
D2010	6250 bpi Data Check -1

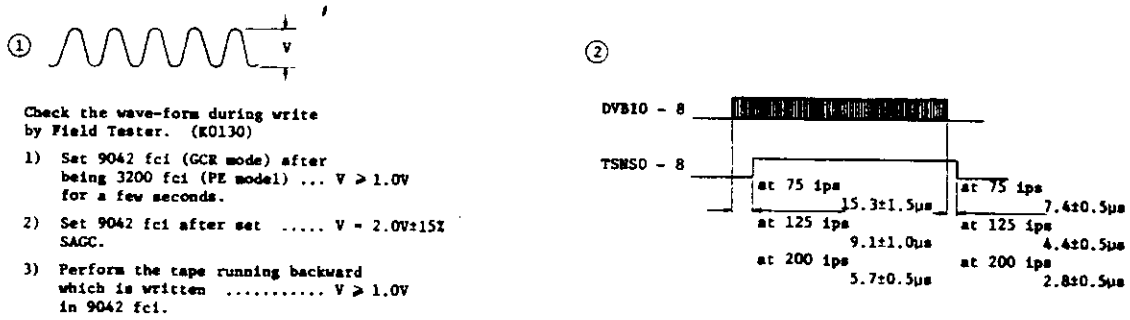


Note 1: How to search error track:
(1) Place the FMT in offline mode and perform LWR command (D3040)
(2) After the LWR command is performed, an errored track can be checked by displaying the register at $22.

Note 2: How to search error:
(1) Display the contents of the register at $24.
(2) WVRC is bit 3.

D2011	6250 bpi Data Check - 2





Check the wave-form during write by Field Tester. (K0130)

1) Set 9042 fci (GCR mode) after being 3200 fci (PE model) ... V ≥ 1.0V for a few seconds.

2) Set 9042 fci after set ..... V = 2.0V±15% SAGC.

3) Perform the tape running backward which is written ..... V ≥ 1.0V in 9042 fci.

Figure D.16 6250 bpi data check

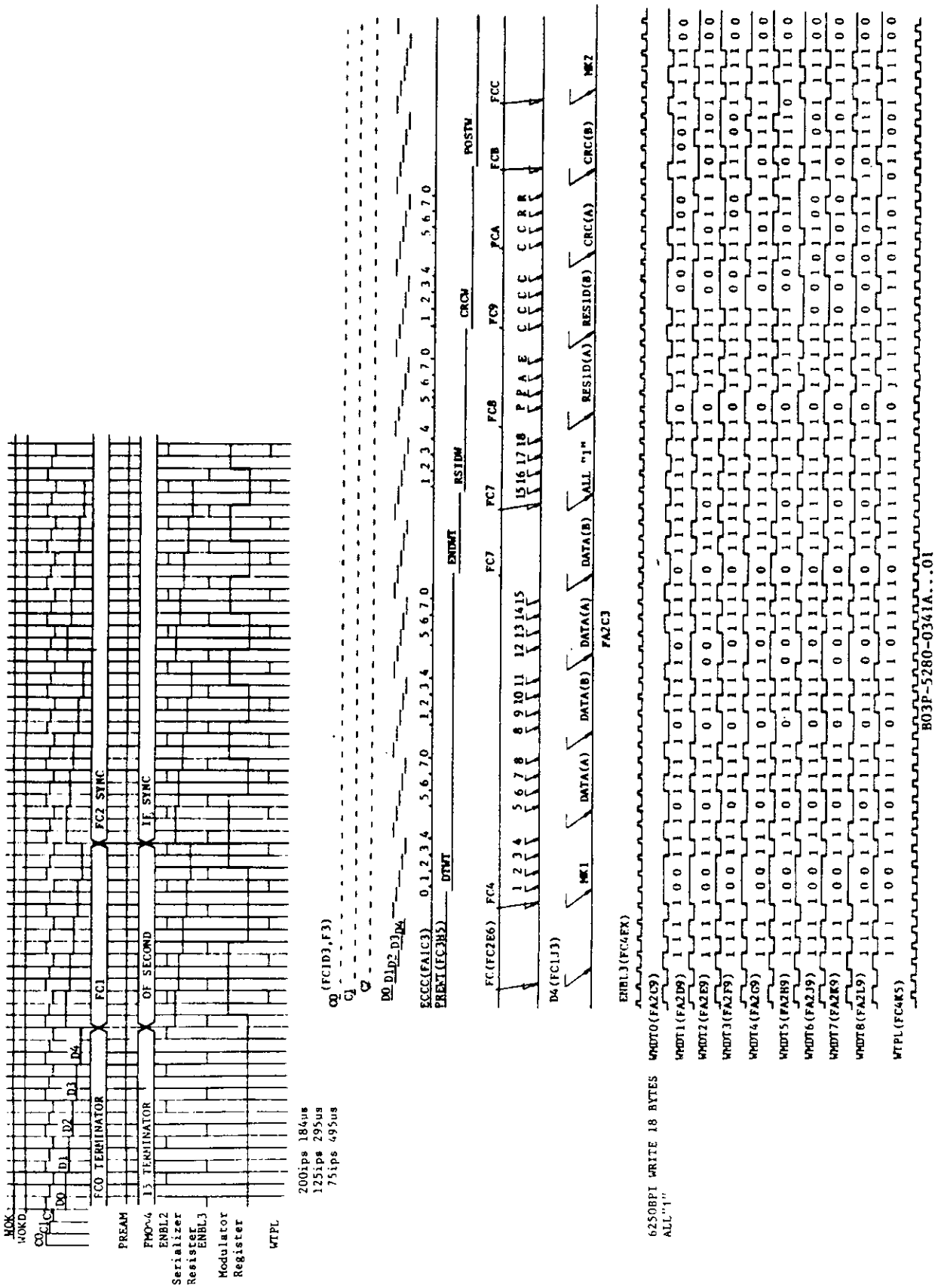


Figure D.17 6250 bpi write time chart

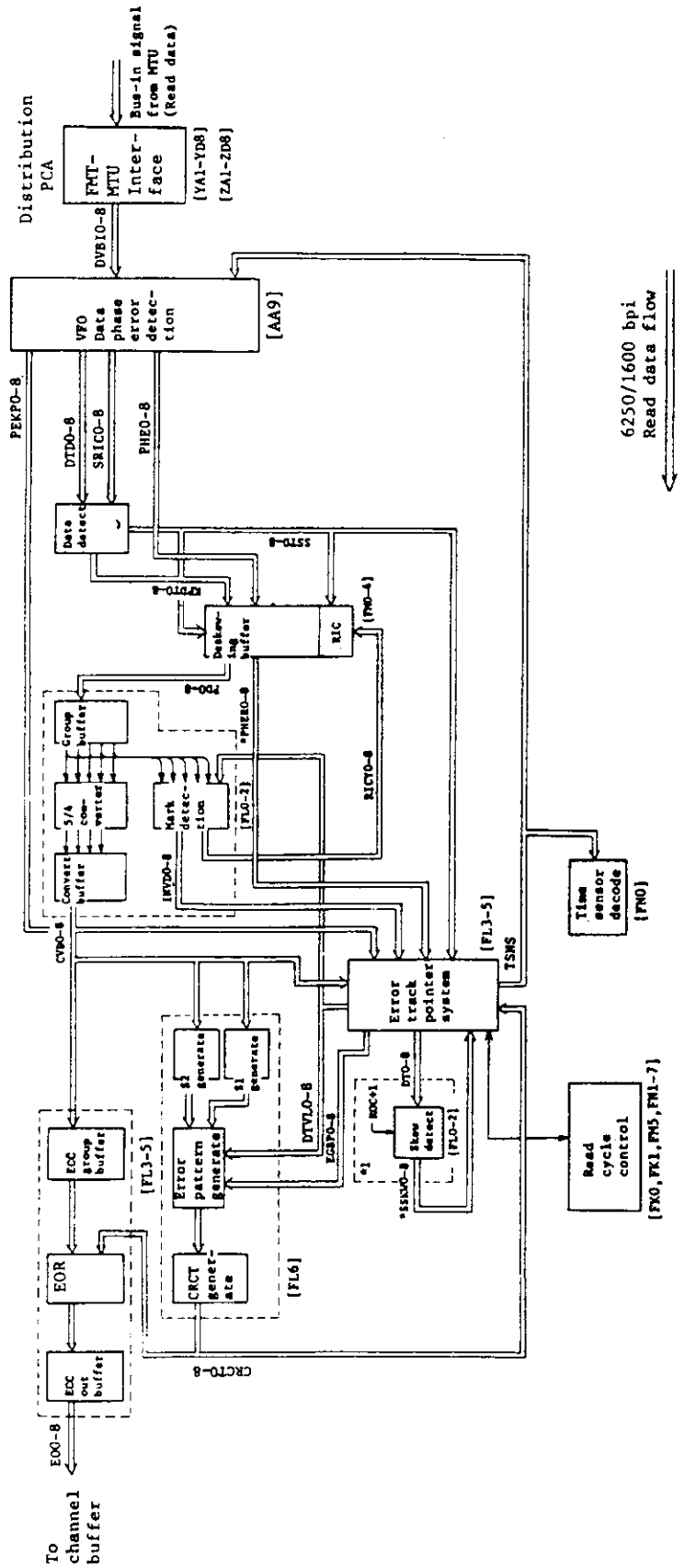
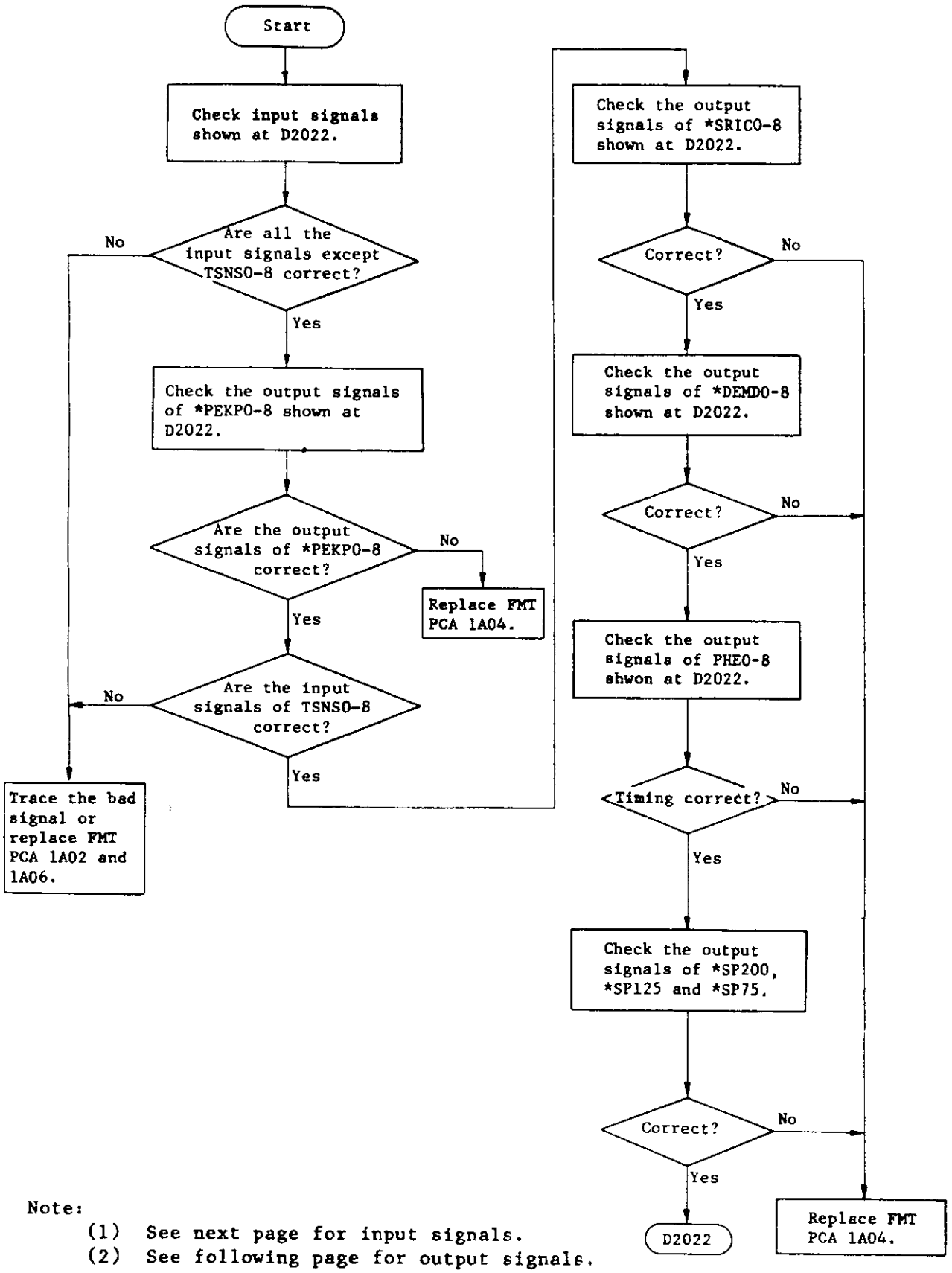


Figure D.18 Read data flow

D2021	Demodulation Circuit Trace Flow -1



Note:

(1) See next page for input signals.

(2) See following page for output signals.

Table D.6 Input signals

Item	Signal name	Contents	Bit									Reference
			0	1	2	3	4	5	6	7	8	
1	Peak signal (DVBIO-8)	Read peak position signal from MTU	AA3	AD6	ADU	AG5	AG9	ALX	GA9	BAX	BDZ	Figure D.19 Table D.8
2	Time sense (TSNSO-8)	VFO input changing signal	AAU	AAV	ADY	AHZ	AK1	AKV	BA6	BD5	BD6	Figure D.21
3	Error generated signal (IPHEO-8)	Read peak position signal from MTU	AB7	AD3	AEV	AH7	AHW	BB1	BB3	BE2	BEW	Ordinarily +2.4 V +5.0 V
4	Read OK (*ROK)	Read start signal signal from MTU	AL7									Figure D.21
5	Z read (*ROK)	Signal indicating 800 bpi	AK6									
6	Backward (BWD)	Signal indicating tape running direction	AL6									------
7	Write clock (*WOSC)	Clock signal of basic frequency	AKU									Figure D.20 Table D.8
8	VFO start (*VFOS)	Signal to reset VFO and start	AK8									Figure D.21
9	Speed signal (*HSP)	Signal indicating tape speed	AL3									
10	1600 signal (P1600)	Control signal indicating record density	AL5									
11	High gain signal (HIG)	Control signal indicating record density	BB5									Figure D.21 Table D.9
12	Phase OK (PHOK)	Signal to start data demodulation	AK4									Figure D.21

Table D.7 Output signals

Item	Signal name	Contents	Bit									Reference
			0	1	2	3	4	5	6	7	8	
1	Peak pulse (*PEKP0-8)	Rising and falling pulses of peak signl	AA8	AD1	ADZ	AH1	AGY	AKZ	BA4	BD3	BDW	Figure D.19
2	Read clock (*SRIC0-8)	Clock to get demodulation data	AA6	ABX	AD8	AEX	AGX	ALB	BBU	BZY	BDX	Figure D.22
3	Demodulation data (*DEMD0-8)	Data recognized with 1 and 0	AV3	AE6	ADV	AH5	AHU	AKY	BBU	BZY	BDX	Figure D.22
4	Phase error (PHE0-8)	Phase error detected signal	AA5	AAX	AEW	AG4	AGV	ALW	BA1	BD1	BD8	Figure D.23
5	*SP200 *SP125 *SP75	Signal indicating speed function of VFO	AE1 AK3 AK5									——

Table D.8 Cycle of T1 and T2

Record density	Tape speed	T1 and T2
6250 bpi	200 ips	555+ 100 ns
	125 ips	885+ 180 ns
	75 ips	1475+ 300 ns
	50 ips	220+ 0.5 μs
1600 bpi	200 ips	1.56+ 0.3 μs
	125 ips	2.50+ 0.5 μs
	75 ips	4.20+ 0.8 μs
	50 ips	6.25+ 1.3 μs

Table D.9 High gain

Record density	Write/read	*HIG
6250 bpi	Write	+2.4 ∿ +5.0 V
	Read	Figure D.23
1600 bpi	Write/read	+2.4 ∿ +5.0 V

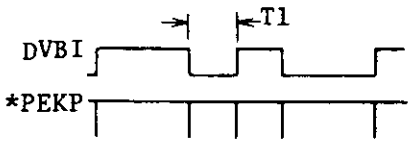


Figure D.19 DVBI and PEKP

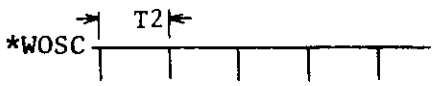


Figure D.20 WOSC

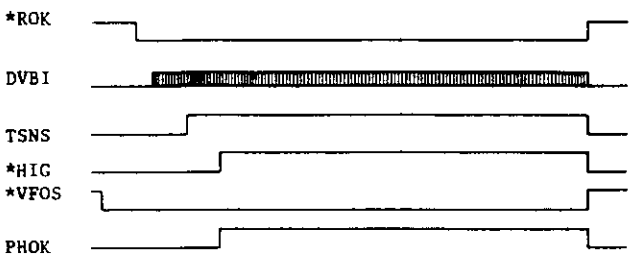


Figure D.21 Input timing

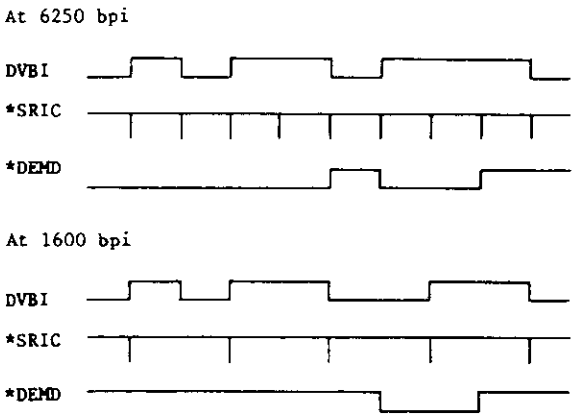


Figure D.22 Output timing

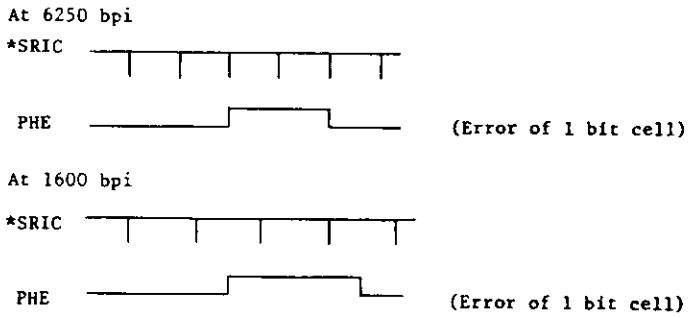
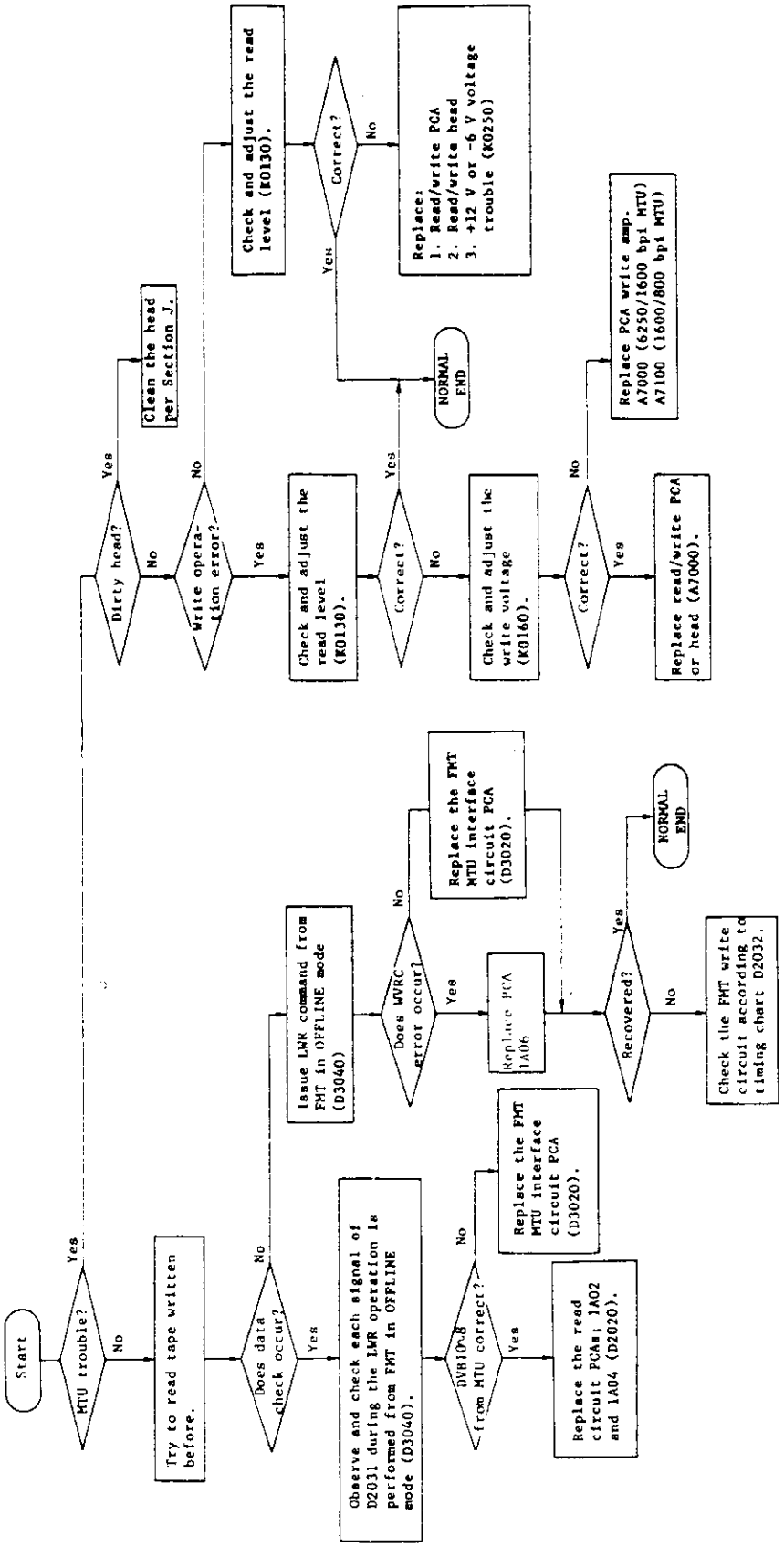


Figure D.23 PHE timing

D2030	1600 bpi Data Check - 1



D2031	1600 bpi Data Check - 2

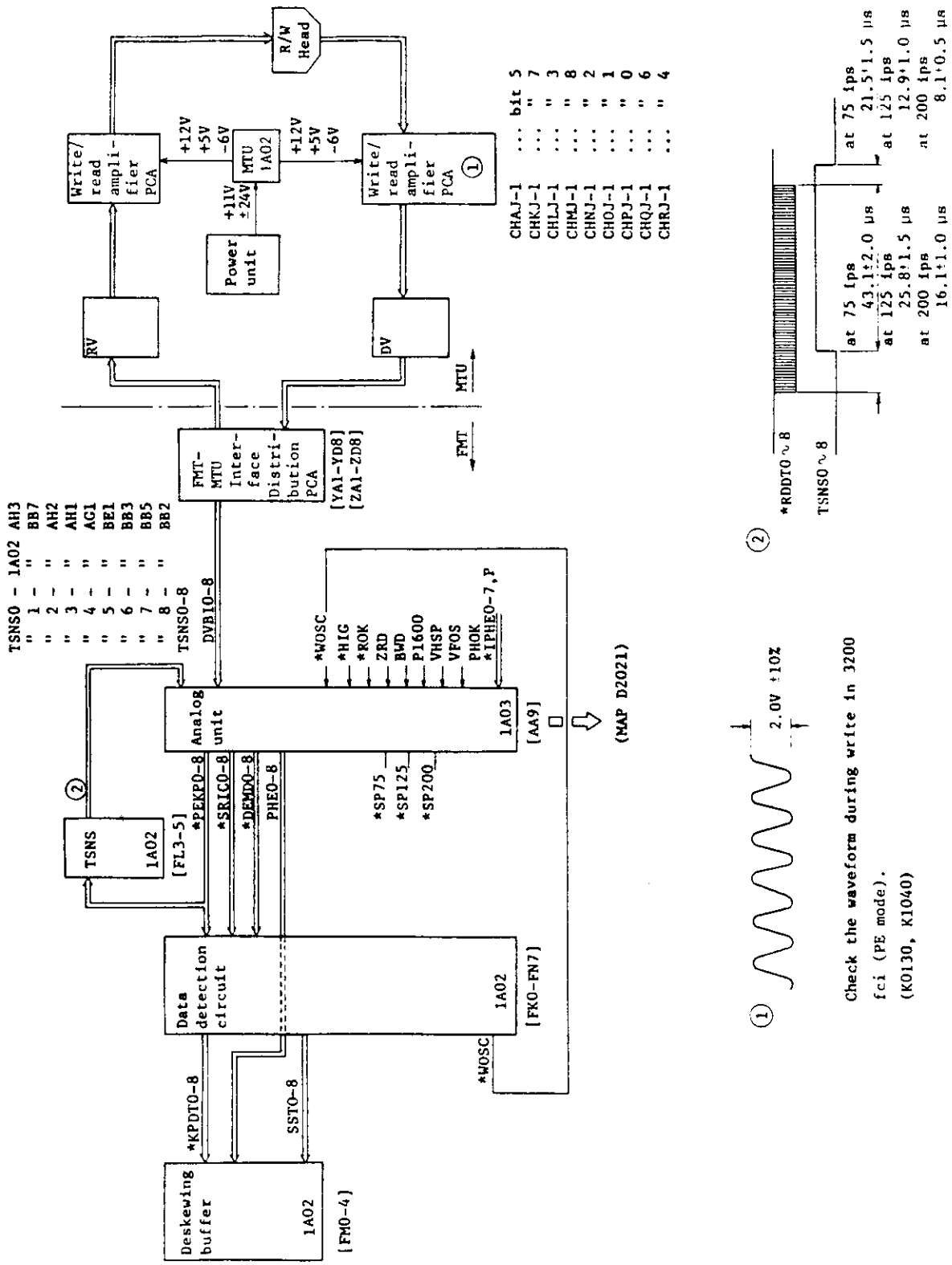


Figure D.24 1600 bpi data check circuit

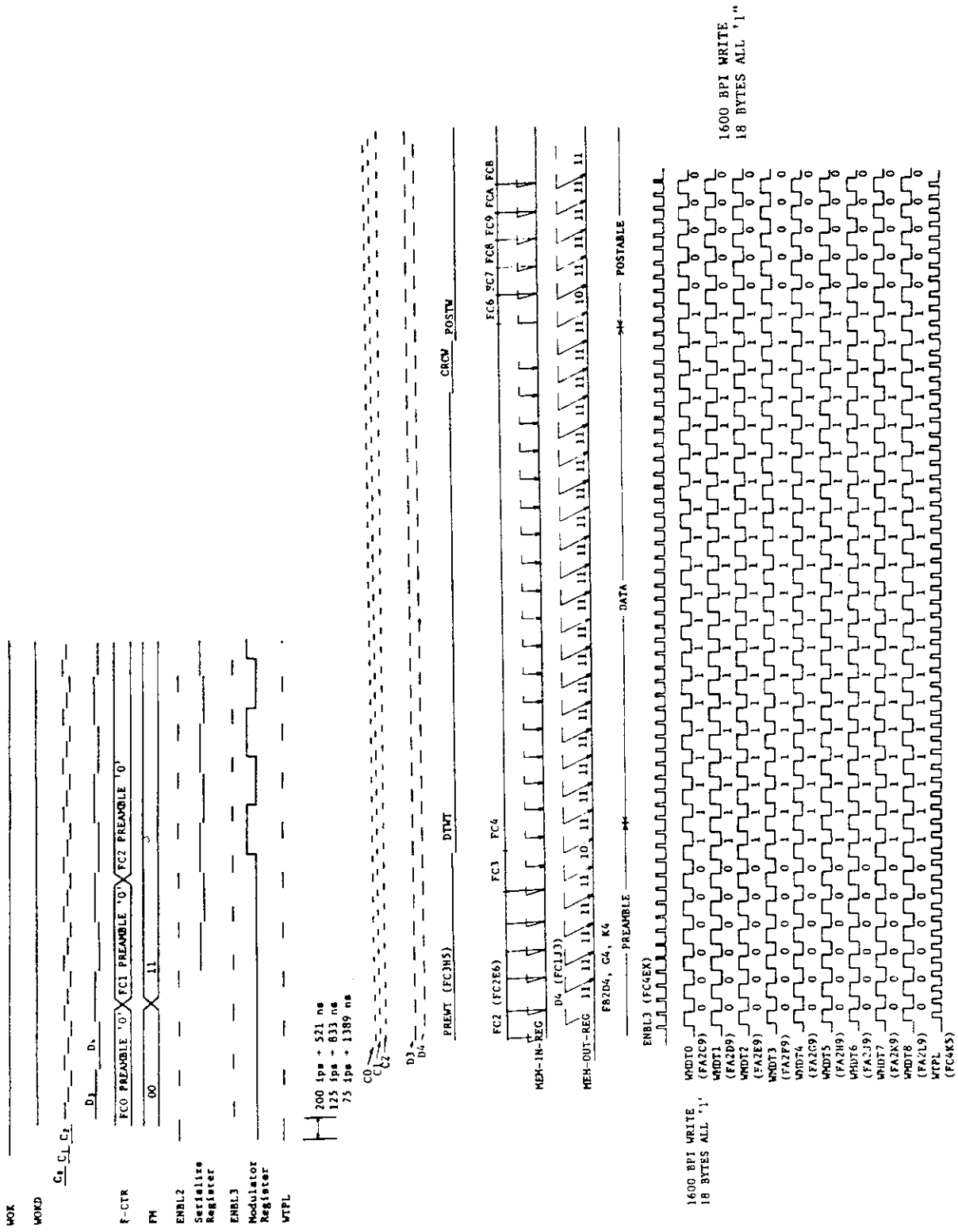
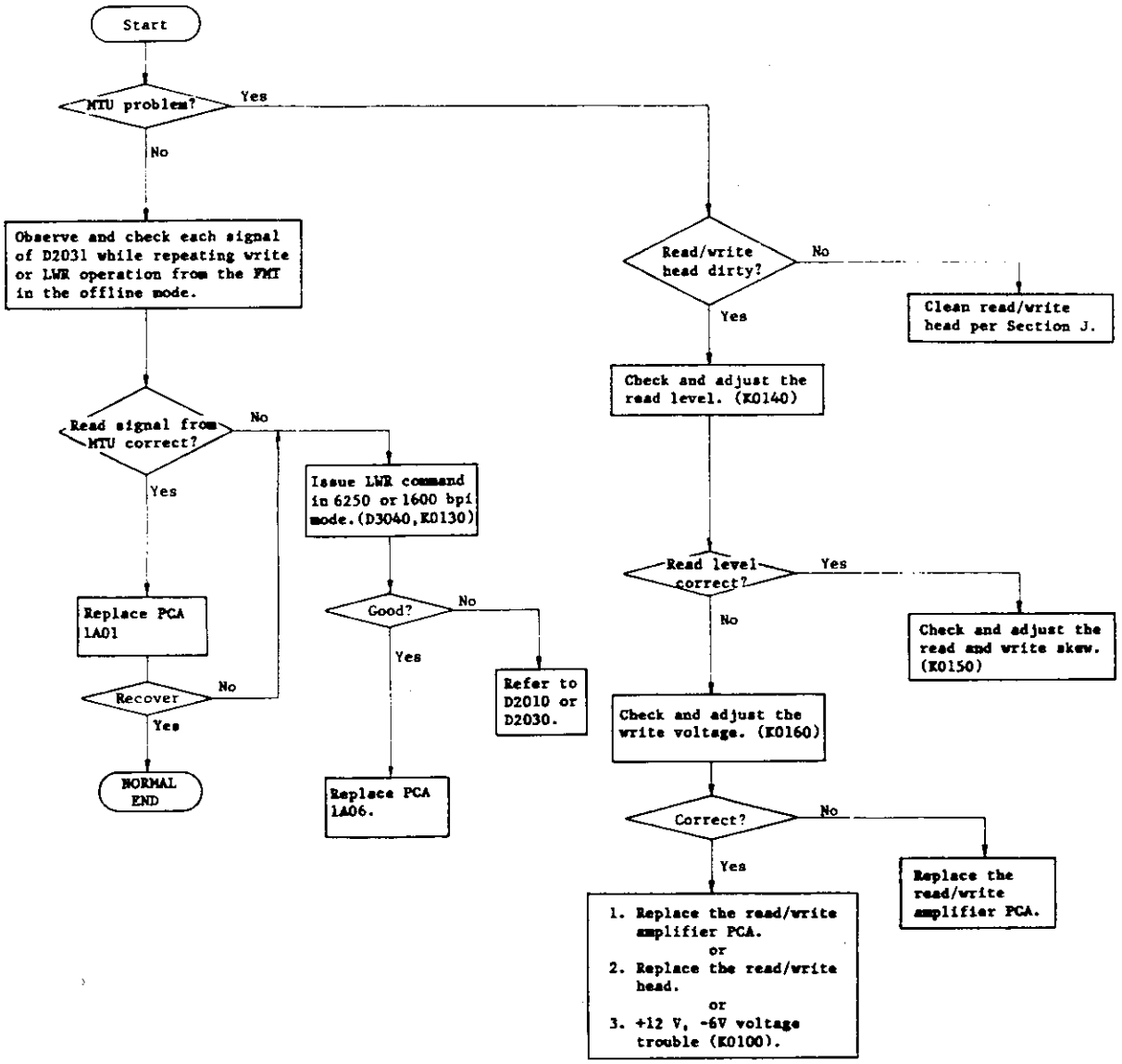


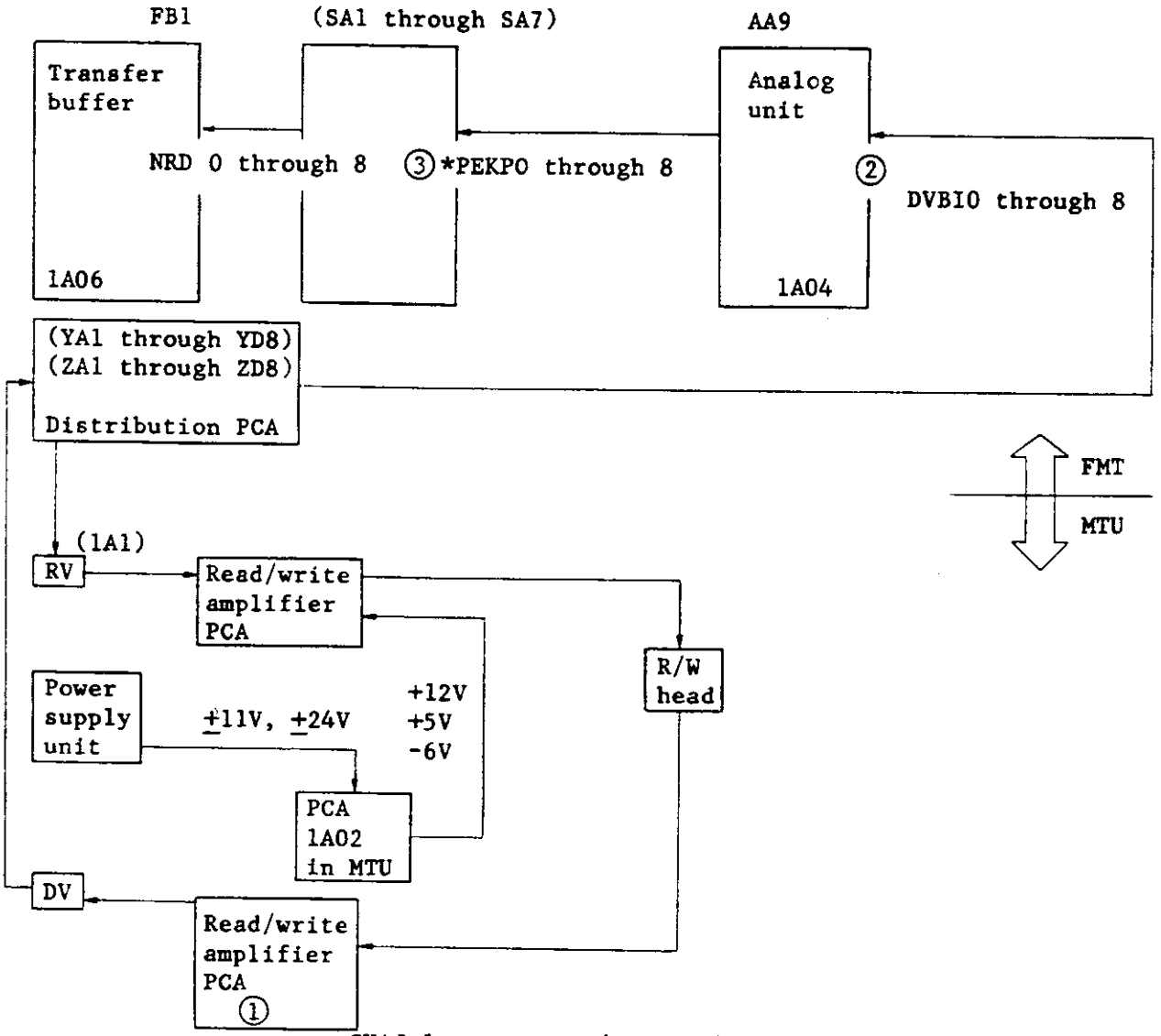
Figure D.25 1600 bpi write time chart

D2040	800 bpi Data Check - 1



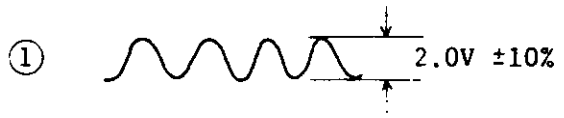
D2041	800 bpi Data Check - 2

Bit 0: 1A04 AA8	Bit 0: 1A04 AA3
Bit 1: 1A04 AD1	Bit 1: 1A04 AD6
Bit 2: 1A04 ADZ	Bit 2: 1A04 ADU
Bit 3: 1A04 AH1	Bit 3: 1A04 AG5
Bit 4: 1A04 AGY	Bit 4: 1A04 AG9
Bit 5: 1A04 AKZ	Bit 5: 1A04 ALX
Bit 6: 1A04 BA4	Bit 6: 1A04 BA9
Bit 7: 1A04 BD3	Bit 7: 1A04 BAX
Bit 8: 1A04 BDV	Bit 8: 1A04 BDZ



CHAJ-1 ... Bit 5 (Track 1)
CHKJ-1 ... Bit 7 (Track 2)
CHLJ-1 ... Bit 3 (Track 3)
CHMJ-1 ... Bit 8 (Track 4)
CHNJ-1 ... Bit 2 (Track 5)
CHOJ-1 ... Bit 1 (Track 6)
CHPJ-1 ... Bit 0 (Track 7)
CHQJ-1 ... Bit 6 (Track 8)
CHRJ-1 ... Bit 4 (Track 9)

D2041	800 bpi Data Check - 2



Observe the wave form while repeating the write operation in 800 fci (NRZI mode) from the field tester. (K0130)

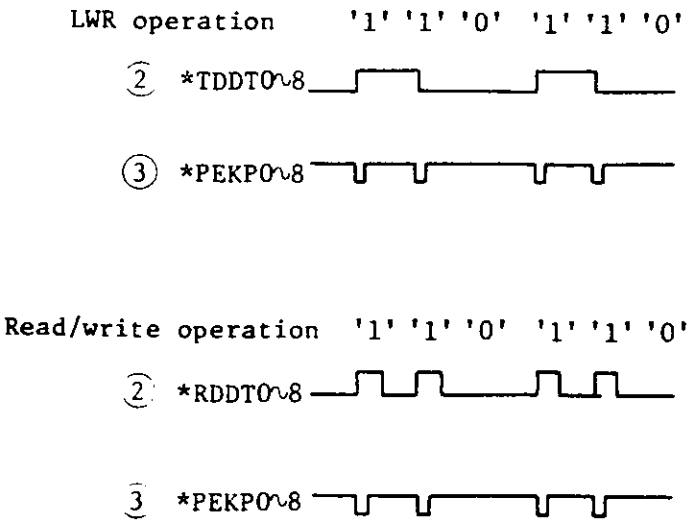
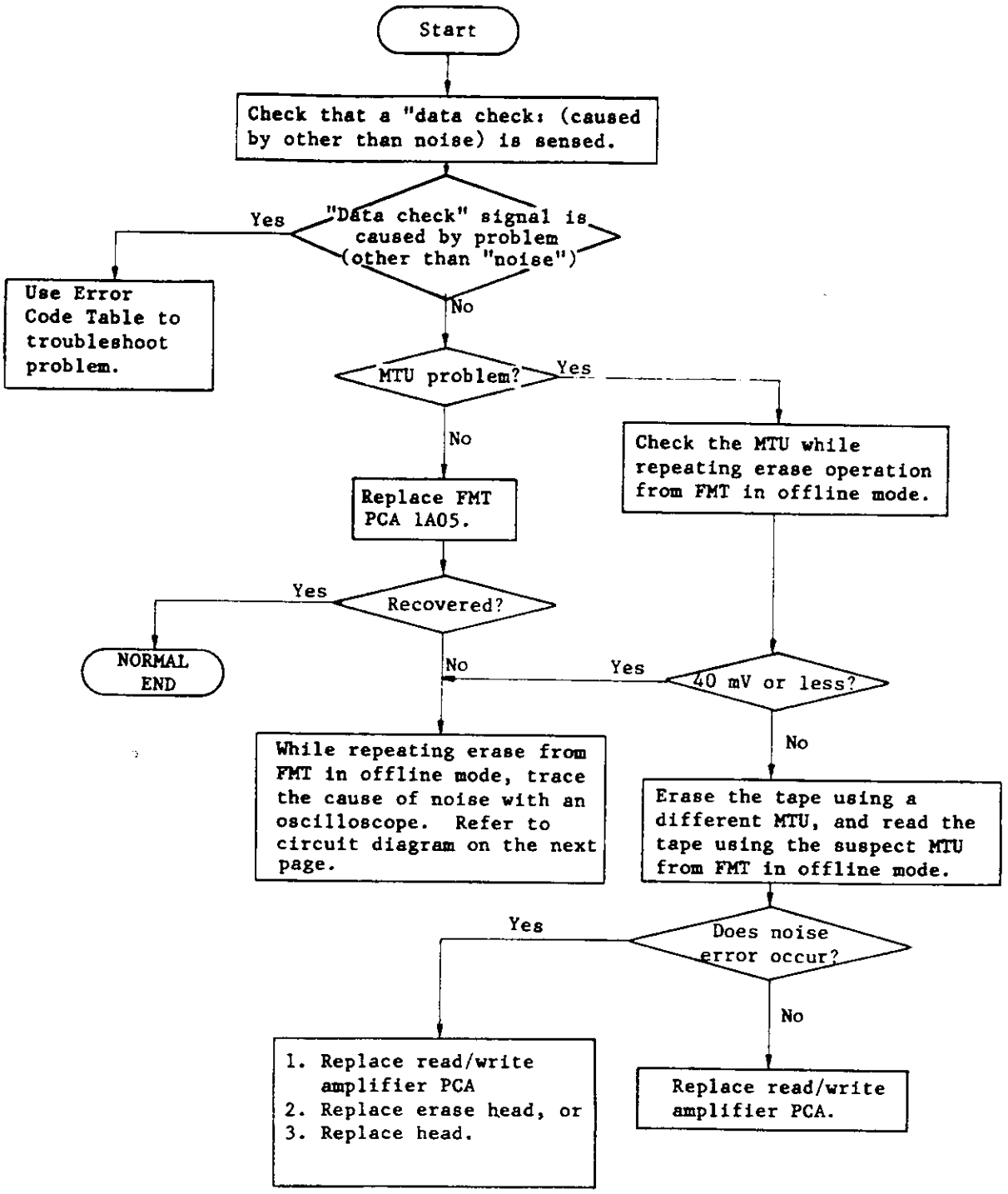


Figure D.26 800 bpi data check

D2100	Noise

Noise error occurs when:
(1) Data check is set to on during the read or read backward command.
(2) A noise block is detected read or read backward command.
(3) Data is detected during the erase, write tape mark, or write command.



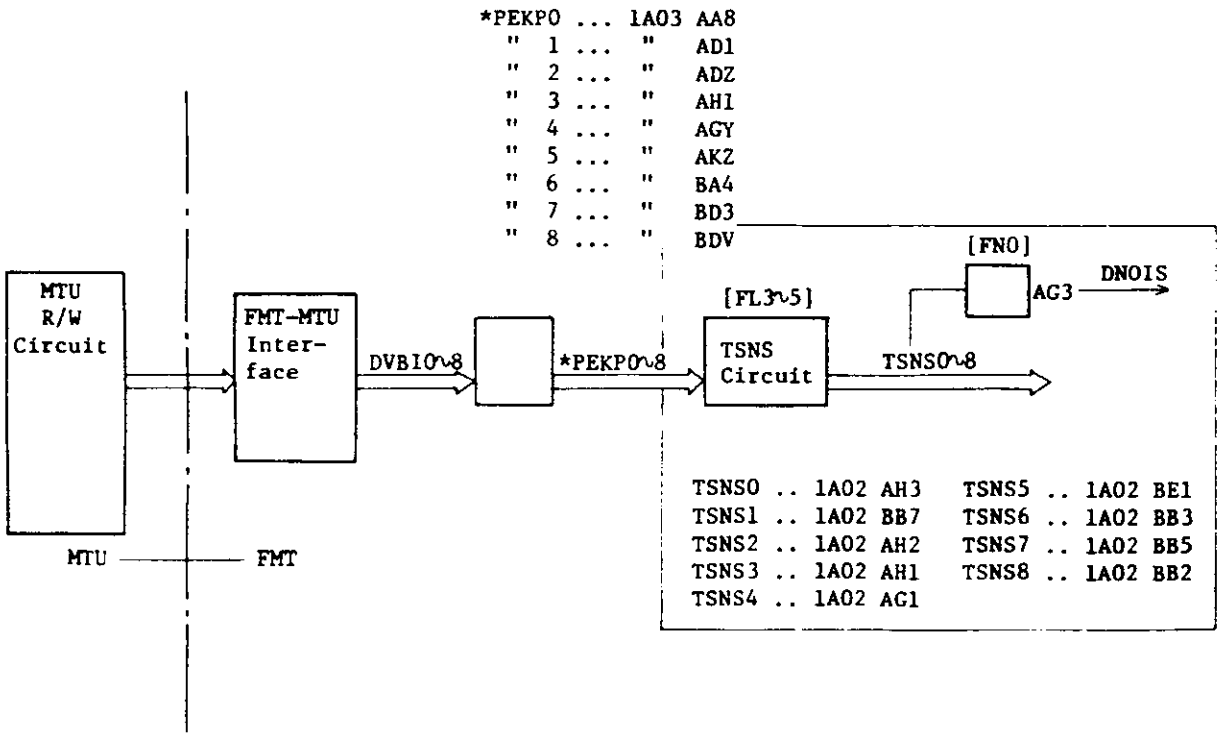


Figure D.27 Noise troubleshooting

D2110	P (Parity) Compare

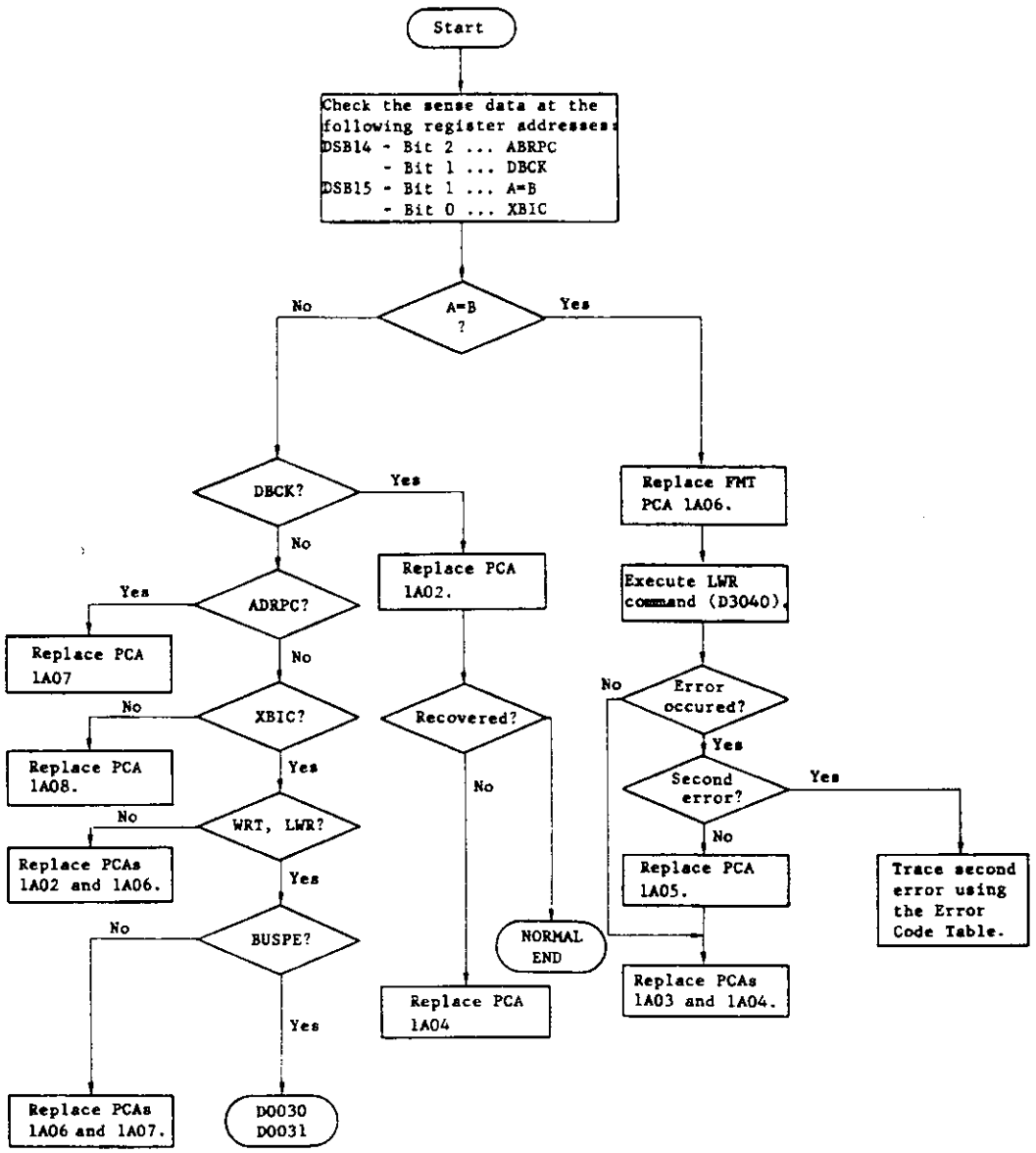
P compare means FMT parity check or compare check. P compare occurs in the following cases.

(1) Transfer buffer check (A≠B):
when the comparison between transfer buffer input and output data does not agree. (CRCA ≠ CRCB).

(2) Parity check transfer buffer (XBIC):
When a parity error is detected in the transfer buffer input data.

(3) A/B register error (ABRPC):
When a parity error is detected in the A/B register at read operation.

(4) Deskewing buffer check (DBCK):
When an error is detected in the ROC of deskewing buffer.

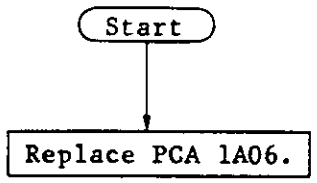


D2120	W-VRC Error

W-VRC error occurs when:

(1) Parity error occurs in WTD0 through 8 at write trigger VRC circuit. In this case, "IBG detected" is not set.

(2) Writing on creased tape. In this case, "IBG detected" is set.



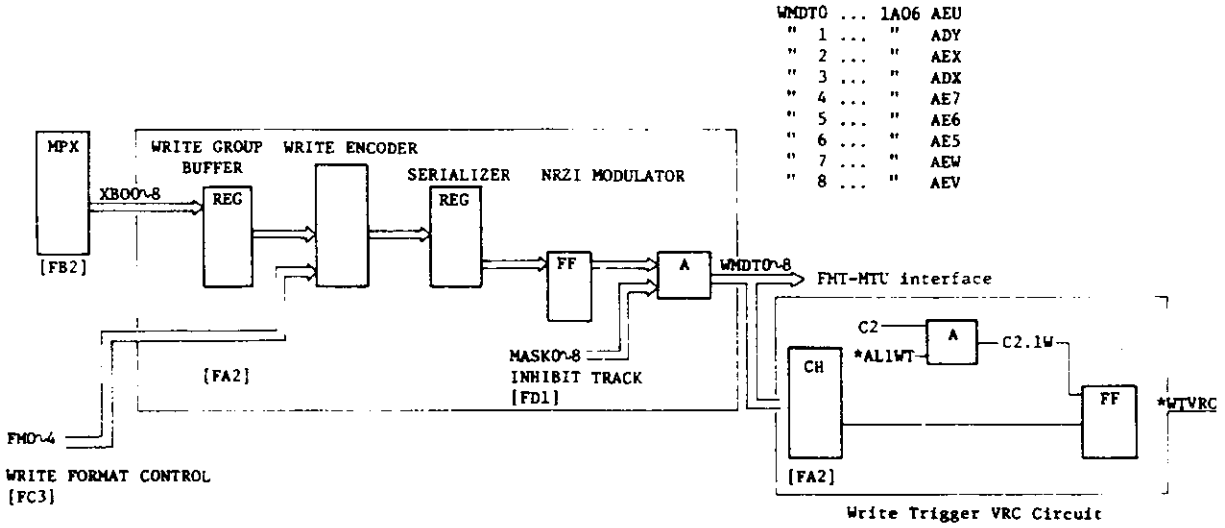


Figure D.28 Write trigger VRC circuit

D3000	MTU Sense Error

The MTU status (BWD, NOT-FP, TWA or BOT, WRS, ONL, READY, etc.) can be displayed on field tester.

MTU sense bytes representing the MTU status are listed in D3010.

To inspect TU (tape unit) sense bytes, use the instructions below:

(1) Set field tester ONL/OFL switch to OFL.
(2) Set FMT microprogram to the 'STEP' mode.

```
OFL

$E8, CNT      MP control 'STEP'
```

DBMPX (register address $74, bit 4) must be '0'.

```
$B2, CNT      register write
$dd, SSS
$72, SSS      Reg $74 - $00
```

Set DVA0-2, SLTAG bits (DVSEL register; $74)

```
$B2, CNT      register write
$dd, SSS
$72, SSS      Reg $72 - $dd
```

	0	1	2	3	4	5	6	7
dd:	0	0	0	1	0	DVA0	DVA1	DAV2
				STAG				MTU address

Content of DVSEL register may be checked. (D3010)

Lamp information to be indicated.

*DVENB and XCAL signals are multiplexed by MTXBO signal (Reg $77, bit 2).

DVSEL ($72)	L0	L1	L2	L3	L4	L5	L6	L7
	TAGI	C.CRY	*DVENB /XCAL	SLTAG	DVBSY	DVA0	DVA1	DVA2

Device busy is '1', if the MTU has been selected from another FMT, (2 FMT model).

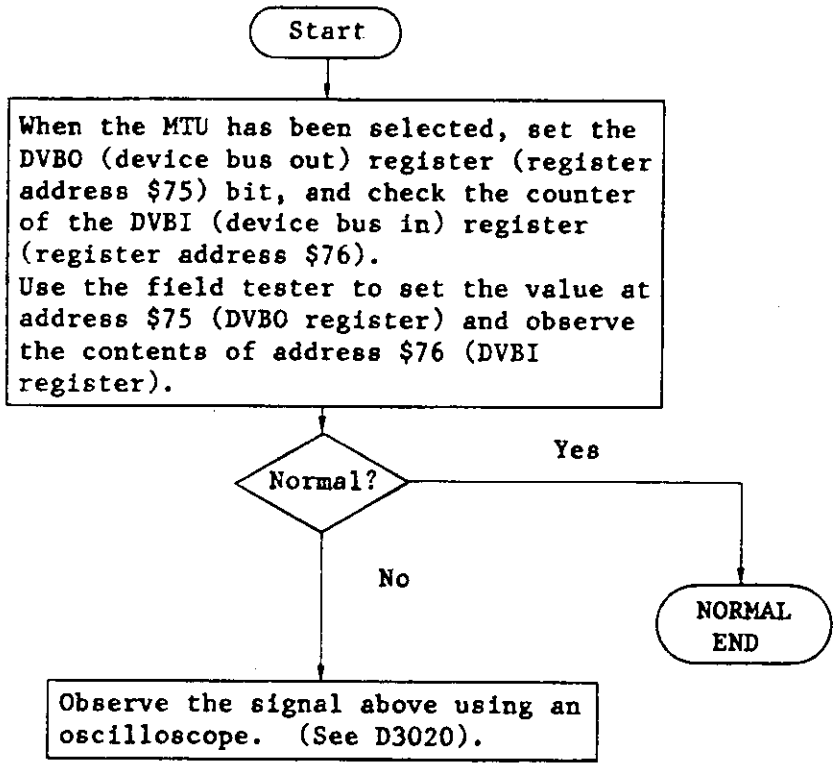
Not device enable '1' while the ENABLE switch on the FMT operator is set to on for the MTU selected. DVA0 through 2 bits displays the 'DISABLE' status. This bit is always '0' if there are no slave units.

Cross call. This bit should be '1' when subsystem is 2 FMT type.

Tag in. This bit is a parity bit for register DVBO.

Note: '1' means on or lit condition.

D3010	MTU Sense Bytes Configuration



MTU sense bytes

TU sense byte	0	1	2	3	4	5	6	7	8
Bus-out / bb: / Bus-in	$01 ($00)	$02	$04	$08	$10	$20	$40	$80	$41
Bit 0	BWD	New function	MISC error	VEL0	2^7	SAGC count 0	Read data 0	Error code 0	Handler erase current ON
Bit 1	NOT FP	Reset key	Tape loop alarm left	VEL1		SAGC count 1	Read data 1	Error code 1	Handler action
Bit 2	TWA	DSE	Tape loop alarm right	Ready hold	Tape unit unique ID low order	SAGC count 2	Read data 2	Error code 2	Handler backward status
Bit 3	BOT	7 tracks	ROM parity error	2^{12}		SAGC count 3	Read data 3	Error code 3	Handler write current ON
Bit 4	Write status	Test mode	Write circuit alarm	2^{11}		EC level 2^3	Read data 4	Error code 4	Handler 65% slices
Bit 5	ONLINE	Dual density	Fuse alarm	Tape unit unique ID high order		EC level 2^2	Read data 5	Error code 5	Handler overrun
Bit 6	TU CK	High density	Air bearing alarm			EC level 2^1	Read data 6	Error code 6	Handler PE mode
Bit 7	READY	6250	Load failure	2^8	2^0	EC level 2^0	Read data 7	Error code 7	Tape mark
Bit 8	TAG-IN	TAG-IN	TAG-IN	TAG-IN	TAG-IN	TAG-IN	Read data 8	TAG-IN	TAG-IN

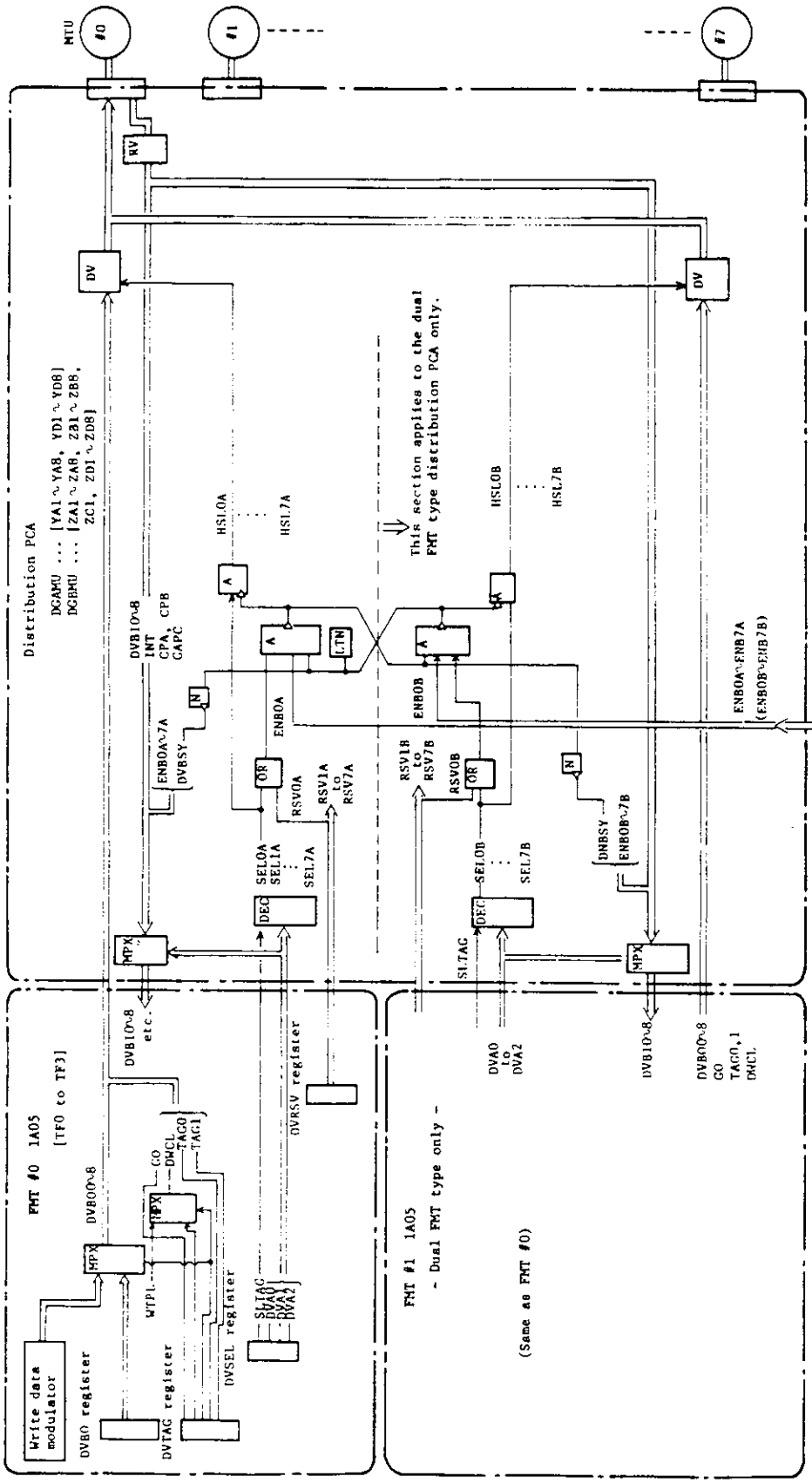


Figure D.29 FMT-MTU interface circuit

D3021	Investigation of the Cable between the FMT and the MTU

If a failure occurs in a specific MTU, check the cable between the FMT and the MTU.

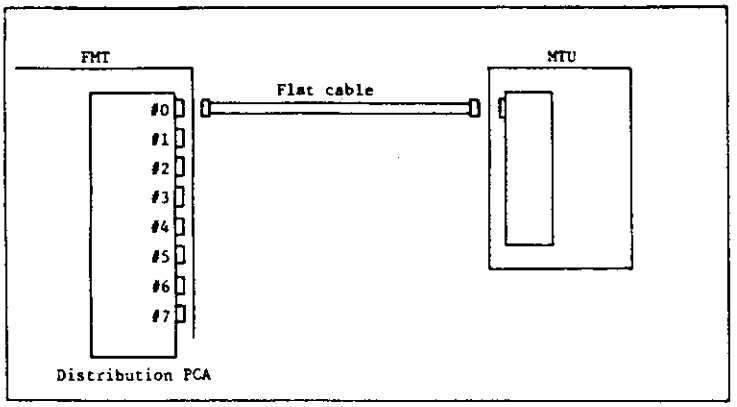
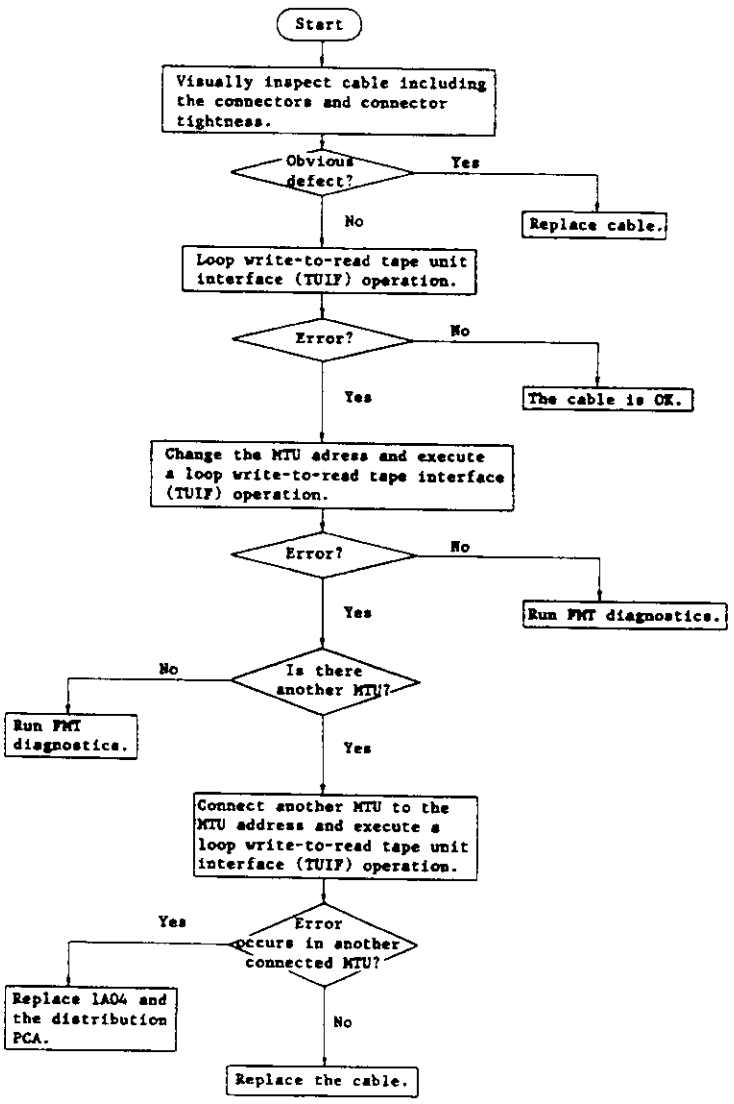


Figure D.30 FMT-MTU cable check



D3040	Loop Write-to-Read Command (LWR) Execution

Execute the loop write-to-read tape unit interface (LWR TUIF) operation offline from the FMT using the field tester, as follows:

(1) If the FMT is not connected with a field tester, proceed to step (2). If a field tester is connected, proceed to step (7).

(2) Set the field tester ONL/OFL switch of to OFL. Connect the field tester to 1A08 on the FMT.

(3) To execute system reset and lamp test, steps (4) to (5) should be performed; otherwise, proceed to step (7).

(4) Set field tester switches S0 to S7 to $F0. (Lamp test). L0 to L11 must all light or the field tester is not operating correctly.

(5) Toggle the CNT switch. (System reset).

(6) L8 (ERRF), L10 (PHLT), and L11 (PERR) should go off.

(7) To set a command code, the field tester is operated in the following sequence. When register address $3D is displayed in the register and command code is already set, this procedure may be omited.

S0 - S7	$B2
CNT-SW	ON
S0 - S7	$80 (LWR TUIF bit)
SSS-SW	ON
S0 - S7	$39 (SDIA1 Reg.)
SSS-SW	ON
S0 - S7	$B2
CNT-SW	ON
S0 - S7	$86 (6250 bpi) $46 (1600 bpi) $06 (800 bpi)
SSS-SW	ON
S0 - S7	$3D
SSS-SW	ON

(continued on sheet 2 of 2)

(8) To set a device address, the field tester is operated in the following sequence. When register address $3E is displayed in the register and the device address is set, this procedure may be omitted.

S0 - S7 $B2

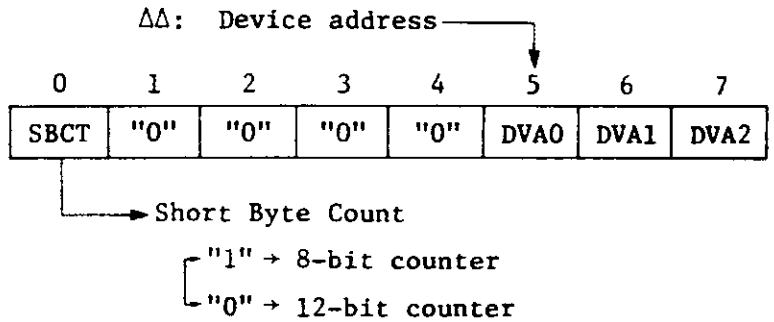
CNT-SW ONΔΔ

S0 - S7 $

SSS-SW ON

S0 - S7 $3E

SSS-SW ON



(9) To set the byte count, the field tester is oprated int eh following procedure. When register address $3F is displayed in the register and is already set at a predetermined byte count value, this procedure may be omitted.

S0 - S7 $B2

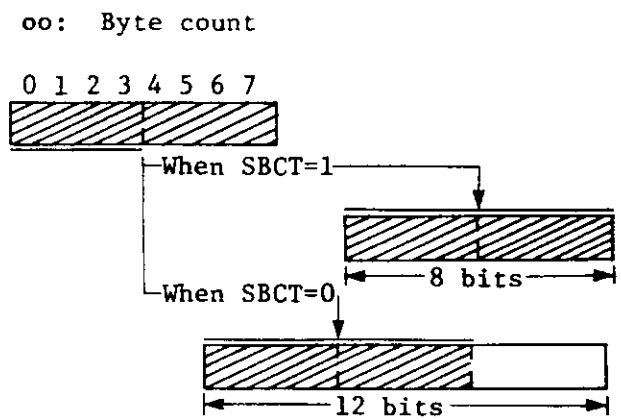
CNT-SW ON

S0 - S7 $00

SSS-SW ON

S0 - S7 $3F

SSS-SW ON



(continued on D3041)

(10) Preparation for executing an LWR TUIF operation is completed by performing steps (7) and (8). Various parameters are available for the execution of an LWR command. To modify the execution of the LWR TUIF using these parameters, registers the parameters into SDIA0 TUIF (address $38) to SDIA3 (address $38) and OFLCNT (address $3C). Refer to field tester section for operation instructions, if necessary.

When performing these operations, if there is doubt about the register contents, observe the contents of registers.

These registers are never reset except when the FMT is powered on.

(11) Execution of an LWR TUIF operation

An LWR TUIF operation is executed immediately when the SSS switch of field tester is toggled. When the 'REPEAT' parameter is designated, the executio of an LWR TUIF is repeated (without toggling the SSS switch) until 'REPEAT' parameter is reset, a stop condition is made by such parameter as 'UNIT-CHECK-STOP', or 'SINH' is indicated. If there is no 'REPEAT' parameter in the register, an LWR TUIF is executed when the SSS switch is toggled.

(12) Confirmation of the execution result

When the execution of an LWR TUIF results in an error, ERRF bit, L8 (L8 lamp is used when S0 to S7 are set to $80) lights. When this bit lights, it indicates that an error is contained in the END status of the executed command. This lamp remains lit from generation of the END status to the next command. The END status is stored in DSB register at address $0A.

(13) Sense byte

Since the sense data that indicates the cuase of error is stored in SB0 (address $20) to SB23 (address $2B) when the ERRF lights (when the UNIT CHECK of DSB register address $0A is set on), check the contents of these register through the register display function of field tester instead of issuing a sense command.

(14) Reject code

If REJECT signal is set, the reject code is stored in RJC (address $30).

D3042	LWR RW Operation

The LWR RW oepration allows the MTU to bypass write data at different points shown in Figure D.32, below. LWR RW operation is useful during MTU Read/Write fault isolation.

When a Read/Write problem occurs on a specific MTU, examine LWR RW operation. If LWR RW operation has resulted in succewss, the fault probably is in the Write/Read amplifier, Read/Write head, or in an amplifier/head adjustment refer to A7000, A7100.

If LWR RW operation has resulted in failure, LWR TUIF operation should be executed. Then the faulty PCA can be replaced.

To execute LWR TUIF operation with an MTU, procedure (1) - (6) in D3040 should be performed. To execute LWR RW operation, detailed procedures are described in D3043.

-- Restriction --

1) Reject Code 207 is set when the MTU detects BOT or is in the 800 bpi mode.
2) Executing LWR RW operation clears the SAGC-count of the MTU.

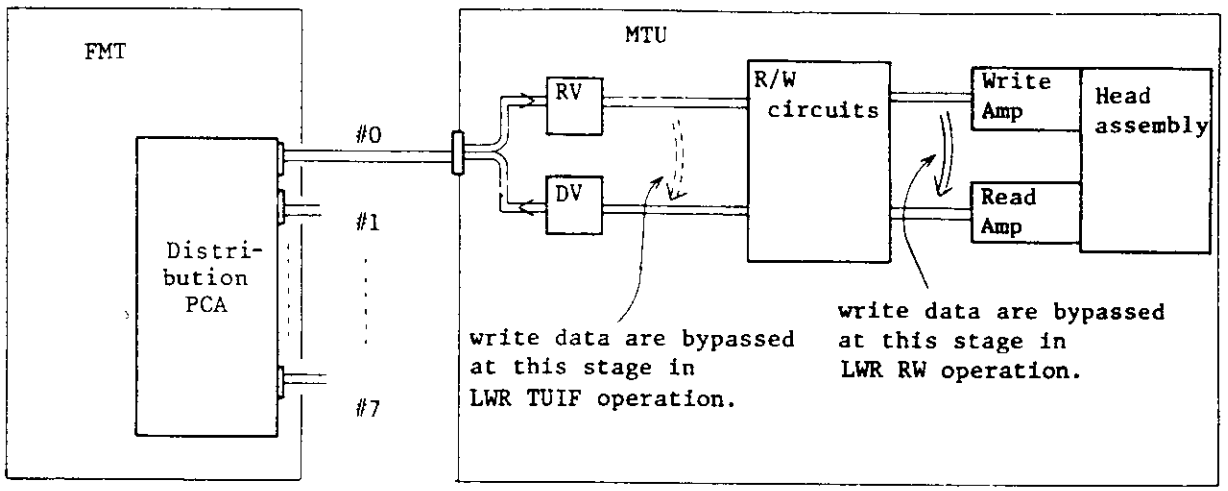


Figure D.31 LWR and LWR2

D3043	LWR RW Execution

Perform LWR RW execution as follows:

(1) Refer to Part I of this Maintenance Manual for information on the field tester, if necessary.

(2) Store the MTU address and byte count to OFLDVA, BCT register. See procedures (8) (9) in D3040.

```
OFLDVA = dd
BCT    = bb
```

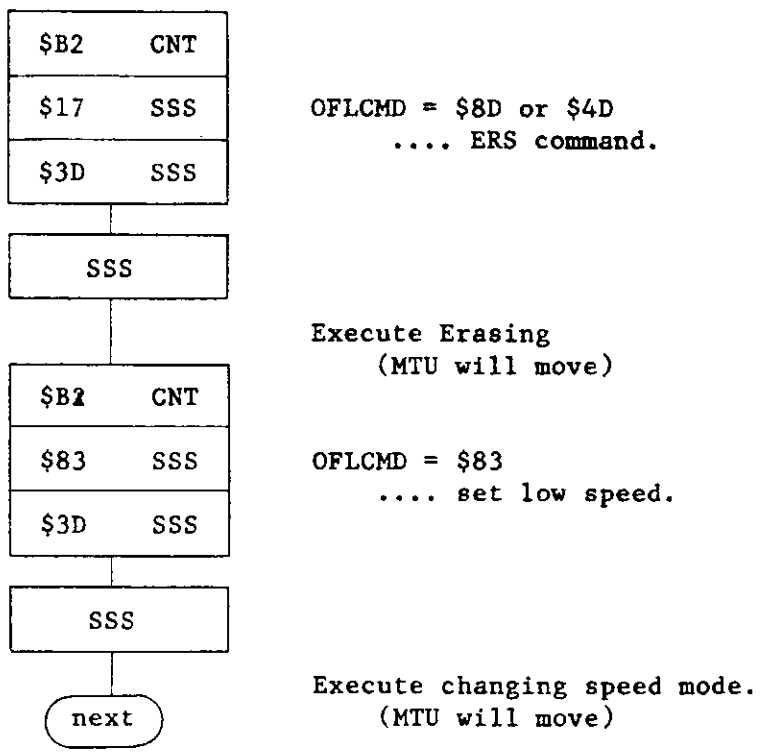
(3) Store the offline execution parameter to OFLCNT register. Here, parameter is all '0' (single command execution).

```
OFLCNT = 00
```

(4) To allow the MTU to move forward if the MTU is in the BOT detected status, issue WRT, WTM, or ERS command to the MTU.

(5) If a specific tape speed is to be tested set either the high-speed or low-speed command.

(6) If the MTU is in the BOT detected status, set density-select bit ('0' or '1').



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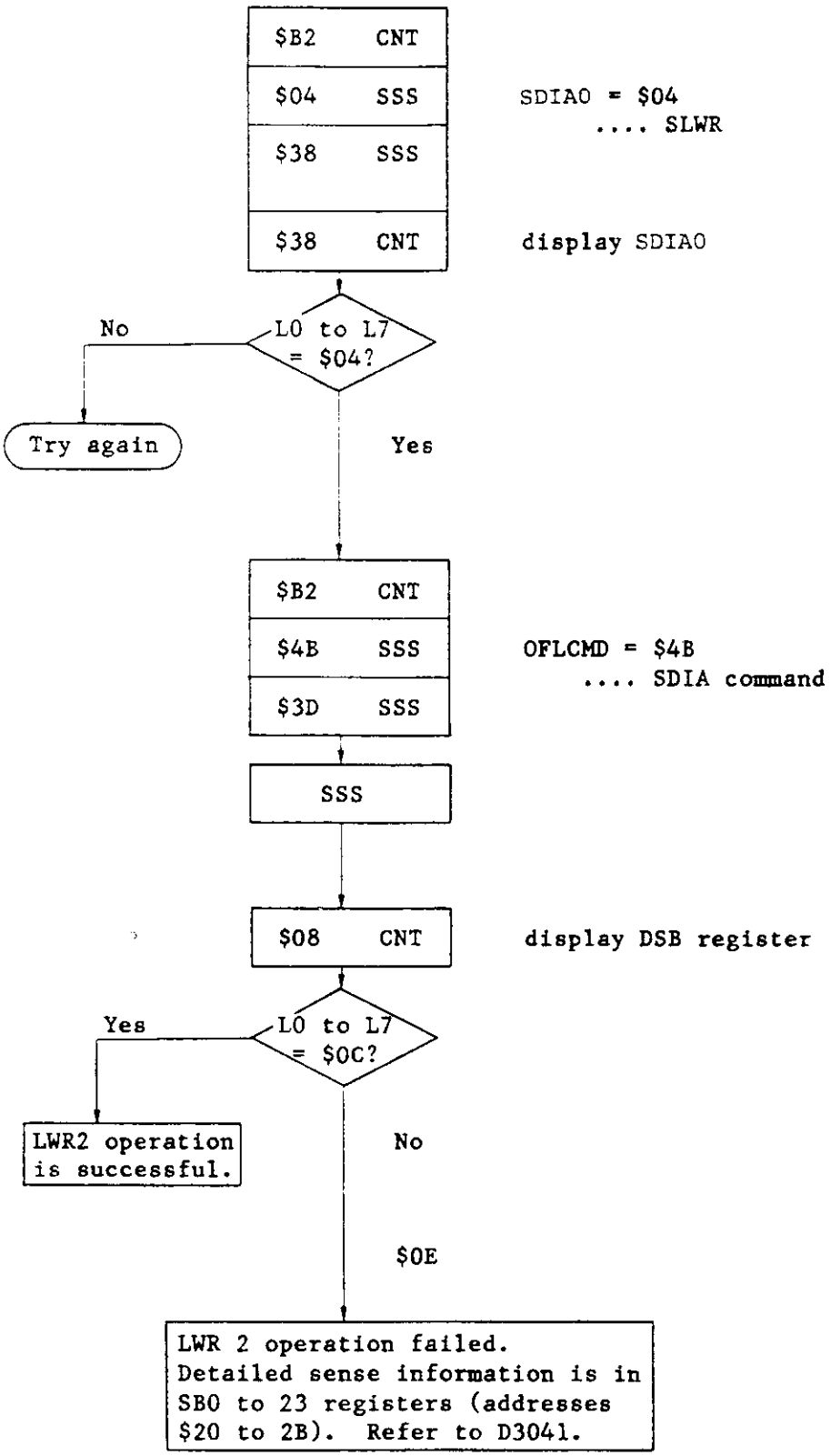
D3043	LWR RW Execution

(7) Store SLWR bit ($04) to SDIA0 register. Issue SDIA0 command.