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INSTRUCTION BOOK

TANDEM PROCESSING SUBSYSTEM (PROCESSOR)

PART OF

FLIGHT SEVICE AUTOMATION SYSTEM

VOLUME IV

CONTROLLED DOCUMENT

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TANDEM PROCESSING SUBSYSTEM

VOL 4

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TANDEM PROCESSING SUB SYSTEM

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VOLUME 4

Serial Number

014

TANDEM

NonStop II™
NonStop EXP™

Power Subsystem

Maintenance Manual

Part No. 82807

THIRD LEVEL

MAINTENANCE MANUAL

NonStop II AND NonStop TXP(TM)

POWER SUBSYSTEM

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TANDEM COMPUTERS INCORPORATED
2450 Walsh Avenue
Santa Clara, California 95050

Tandem Part No. 82807

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SECTION 1
INTRODUCTION

1.0 INTRODUCTION

This manual contains information necessary for the installation, troubleshooting, and field repair of the NonStop II/NonStop TXP Power Subsystem. The power subsystem includes the RFI filter, the AC power distribution module, the DC power supplies, battery supplies, and power distribution circuits for NonStop II and NonStop TXP systems.

1.1 REFERENCED DOCUMENTS

Refer to the following documents for detailed information not found in this manual:

a. NonStop II and NonStop TXP SITE PLANNING MANUAL (82853): This manual contains guidelines for preparing a site for the installation of a Tandem processing system.

b. NonStop II and NonStop TXP INSTALLATION GUIDE (82855): This manual contains information and instructions necessary for the installation of a Tandem processing system.

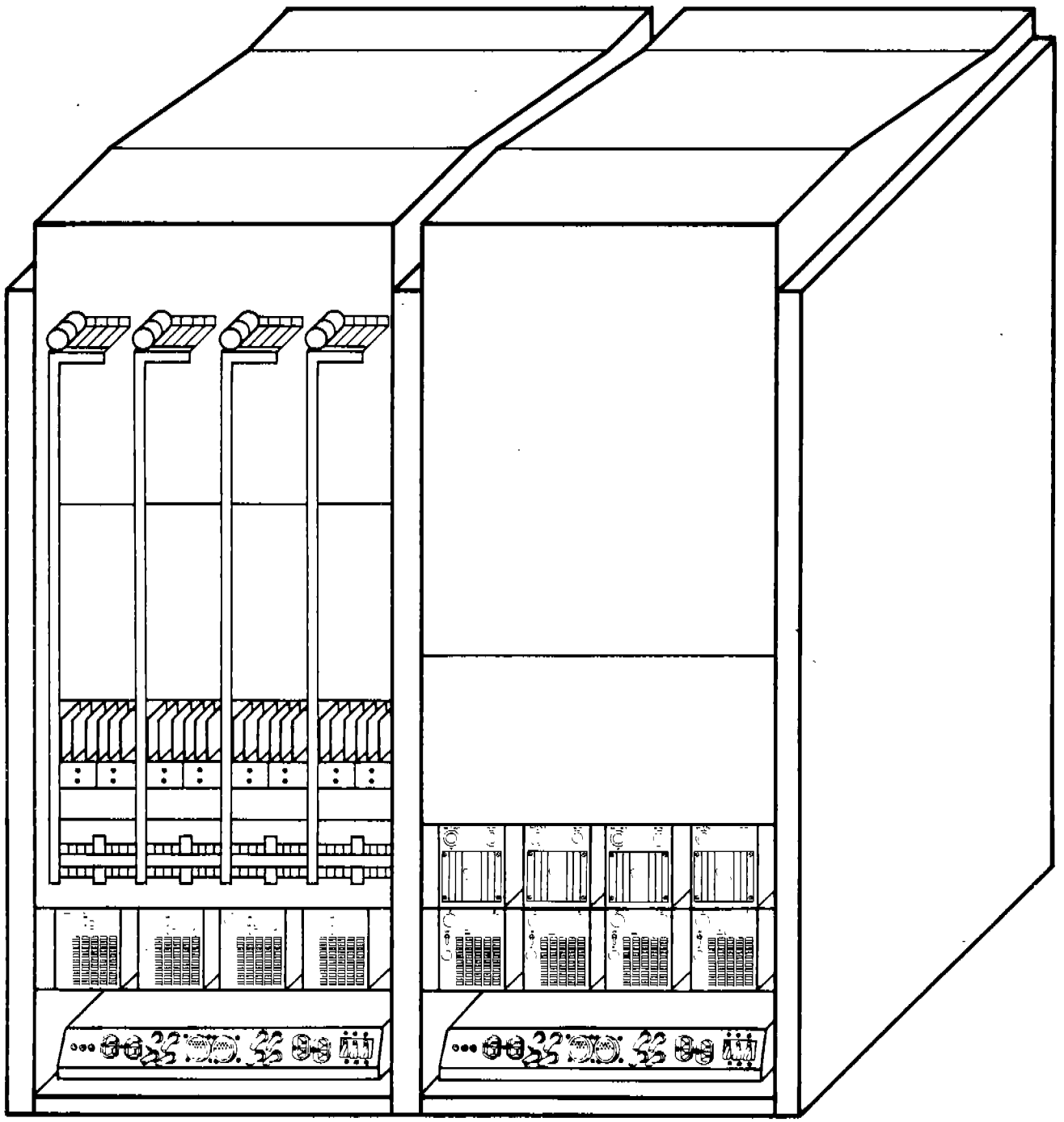

Figure 1-1 Power Subsystem Location

SECTION 2
PHYSICAL DESCRIPTION

2.0 PHYSICAL DESCRIPTION

The Power Subsystem for NonStop II/NonStop TXP processing systems consists of the RFI filter, the AC power distribution module, the DC power supplies, and the battery supplies.

For 60 Hz systems, each processor cabinet and most magnetic tape cabinets require an AC input. AC power is supplied to the system from the site power through the RFI (Radio Frequency Interference) filter mounted in front of the power distribution module. A dedicated AC power source with a 50 Amp breaker for each phase must be available for each cabinet that has a power distribution module. In addition, a shielded, unterminated 5-wire cable capable of handling 50 Amps must be supplied. The five wires are: one each for the three phases, one for neutral, and one for ground. It is the customer's responsibility to provide an electrician to connect the AC to the RFI filter. The Tandem customer engineer is responsible for specifying which phase is connected as A, B, and C. The output of the RFI filter is wired directly into the AC distribution module. Refer to paragraph 3.1 for a description of the phase distribution.

For 50 Hz systems, an AC input is required only for cabinets with isolation transformers (generally these are expansion cabinets and magnetic tape cabinets). No RFI filter is required for 50 Hz systems. Wiring is terminated in a junction box in the magnetic tape or the expansion cabinet. The output of the junction box is wired into the isolation transformers. The output of the isolation transformers is wired into the AC distribution modules in the processor and magnetic tape cabinets. An unterminated 5-wire cable capable of handling 25 Amps must be supplied.

Each processor cabinet and magnetic tape cabinet with battery supplies or DC supplies must have an AC power distribution module. The AC module contains circuit breakers, power outlets, an AC terminal block, and connectors for attaching DC supplies. AC power modules in tape cabinets are configured differently than in processor cabinets. Refer to paragraph 3.1 for AC module operation for both processor cabinets and magnetic tape cabinets.

Two DC voltage levels are required by the logic circuitry of the NonStop II and NonStop TXP systems. The processors, I/O device controllers, and the interprocessor bus for both systems require +5 volts. The memory circuits for NonStop II with 512 KB boards require both +5 volts and +12 volts. The memory circuits for NonStop II with 2 MB boards require only +5 volts. The memory circuits for NonStop TXP require only +5 volts.

POWER SUBSYSTEM
PHYSICAL DESCRIPTION

The necessary DC voltages for both systems are provided by processor power supplies, I/O-only power supplies, and battery supplies. The processor power supplies and the I/O-only power supplies are considered Interruptible Power Sources (IPS) and the battery supplies are considered Uninterruptible Power Sources (UPS).

Each processor has a dedicated processor power supply. In NonStop II systems the processor power supply can also provide power for I/O devices. In NonStop TXP systems the processor power supply is used exclusively to provide power to the processing unit. There is no backup power supply for a processor; redundancy at the processing unit level is obtained with multiple processing units.

The I/O-only power supply is used to supplement the +5-volt output of the processor supplies for I/O devices in a NonStop II system. In a NonStop TXP system, the I/O-only power supplies are used to power all I/O controllers. I/O board slots are provided with redundant power through current-sharing regulator circuits. If one supply fails, the other supply automatically assumes the full load.

Because the MOS memory for both NonStop II and NonStop TXP systems is volatile, electrical power must be maintained, even during a power failure. Battery supplies provide short term immunity to AC power loss. The batteries for NonStop II systems can supply DC power to the memory for eighty minutes to four hours, depending on the type and number of memory boards installed. The batteries for NonStop TXP systems can supply DC power to memory for three to nine hours, depending on the number of memory boards and the manufacturer of the RAM chips used on the boards.

In addition to the RFI filter (or isolation transformers), the AC module, and the DC supplies mentioned above, each NonStop II/NonStop TXP system contains several power distribution circuits. These include power buses, backplane power circuits, plenum diodes, power sense lines, power failure warning lines, and I/O power regulators. Refer to paragraph 2.5 for more detailed information about DC power distribution.

2.1 ELECTRICAL REQUIREMENTS

Computer systems require a supply of AC power that is continuous, stable, and free from electrical noise. The following material describes these requirements more fully, discusses potential problems, and makes general recommendations. Any electrical installation must comply with national and local electrical codes. A licensed electrical contractor should be employed to accomplish the wiring tasks involved.

The following system specifications will be used for all new system installations:

a. Maximum Allowable Sags (any or all phases):

   80% Nominal - 10 cycles
   50% Nominal - 2 1/2 cycles

b. Maximum Allowable Surges (any or all phases):

   130% Nominal - 1/2 cycle
   120% Nominal - 1 cycle
   115% Nominal - 30 cycles at 60 Hz; 25 cycles at 50 Hz

c. Maximum Allowable Interruptions (any or all phases):

   0% Nominal - 1/2 cycle

d. Maximum Allowable Steady State Power:

   +5% to -10% of rated voltages for the devices

e. Maximum Allowable Transients (nominal voltage = rms value):

   100 us pulse at 180% of nominal voltage
   1 ms pulse at 100% of nominal voltage
   8.33 ms pulse at 30% of nominal voltage
   0.1 sec pulse at 5% of nominal voltage

f. Maximum Allowable Frequency Deviation:

   +1.0 Hz to -1.0 Hz at 60 Hz

NOTE

These are general specifications for NonStop II and NonStop TXP system cabinets. Refer to the Site Planning Manual (82853) for individual device specifications and 50 Hz requirements.

2.1.1 Power Outages

The computer system application demands uninterrupted operation during brownouts or complete power outages. To provide this capability, each processor comes furnished with an uninterruptible power system (UPS). To be considered uninterruptible, a backup power system must be capable of switching into service automatically and instantaneously upon failure of the principal power source. Power interruptions no greater than 25 ms (.025 seconds) are transparent to the Tandem processing unit. While certain peripheral units, especially disc drives, are less tolerant of power interruptions, any resultant errors can normally be corrected by the Guardian Operating System as long as the processing units continue to run.

If power remains out for 25 ms, the power supply modules in the processing units warn the operating system that power loss is occurring. In response, the system stores in memory the information needed to resume the current process when power is restored and then becomes inactive. The processor includes MOS memory, which is volatile storage, and the DC power supply includes a battery pack (UPS) that keeps the memory viable for approximately eighty minutes to four hours (NonStop II) or three to nine hours (NonStop TXP) depending on the type and number of memory boards. When power is restored, the operating system resumes activity, reconstructs the processing environment that existed just before the outage, and the application can proceed.

If the uninterrupted operation is required even during prolonged power outages, the customer must install an auxiliary power generator of appropriate KVA rating or size.

2.1.2 Local Electrical Disturbances

Local disturbances of the line input such as fluctuating voltage levels, line transients (noise spikes), and the like may have unpredictable effects upon computer operation. Disturbances need to be determined by appropriate testing and periodic checks. To protect the system from extreme line transients, it may be necessary to install an isolation transformer on the system power input.

> CAUTION
>
> Abnormal voltage levels or voltage fluctuations can be damaging to both equipment and data. The line voltage should be checked thoroughly prior to system installation. Avoid typical sources of such disturbances as outlined in Table 2.1 by dedicating a power line to the computer room.

The electrical system should be adequately tested prior to system installation. If devices are present that might cause line transients or other disturbances, the customer may want to consider installing monitoring devices to determine whether or not a problem exists.

If disturbances occur, ensure that the computer system power panel (see paragraph 2.1.3) is connected to a feeder that supplies no other loads. In extreme cases, the use of line buffering units, such as static inverters and motor generator sets, may be necessary.

Table 2.1 Common Causes of Local Electrical Disturbances

CONDITION NUMBER	CONDITION
1	Overloading the power transformers and feeders.
2	Starting and stopping large electrical machinery, elevators, air conditioning motors, etc.
3	Injecting radio frequency energy into the power line with devices such as X-ray machines or arc welders.
4	Connecting equipment (such as keypunches, adding machines, coffee pots, vacuum cleaners, or other appliances that are electrically noisy) to the same power source as the computer system.

2.1.3 The Computer Power Panel

The Tandem system should receive AC power from a dedicated power panel located in or near the computer room. The size of the Tandem system dictates the rating of this power panel.

Ideally, this "computer power panel" should be fed directly and exclusively from a secondary (low voltage) service entrance. This scheme reduces the possibility of mutual interference between the Tandem system and other equipment due to electrical noise fed back into the power system. If this is not practical, the computer power panel should be fed directly from the main service panel as shown in Figure 2-1 (unless high voltage service requires a step-down transformer, in which case see Figure 2-2).

The least desirable arrangement - the one most prone to noise propagation - is one in which the computer power panel is fed by a circuit that feeds other loads.

2.1.4 Emergency Disconnect Switches

The National Electrical Code prescribes installing emergency disconnect switches that interrupt all electrical power (except that used for lighting) to the room and disable air conditioning, so that smoke or fire extinguishing agents are not exhausted from the room.

Disconnect switches should be placed near each exit door and should be conspicuously labelled. To prevent accidental shutdowns, these switches may be enclosed in the same manner as fire alarm switches.

2.1.5 Power Requirements for System Cabinets

The processor cabinets, magnetic tape cabinets, and any other system cabinets containing an AC Power Distribution Box, all require AC power inputs.

2.1.5.1 Circuit Breakers

The main circuit breakers in each system cabinet are rated at 40 amperes (20 amperes for most 50 Hz installations). Therefore, to comply with the electrical code, each AC power cable and corresponding circuit breaker in the customer's computer power panel must be 50 amperes or greater (25 amperes or greater for 50 Hz installations).

2.1.5.2 Customer-Supplied AC Power Cable

One shielded AC power cable, unterminated, must be supplied by the customer for each cabinet containing an AC Power Distribution Box. These cables are terminated inside the power distribution modules when the system is installed. This work must be performed by the customer's electrician in accordance with the appropriate power configuration for the particular line power available (refer to paragraph 2.1.5.3).

Because aluminum wiring does not make a reliable connection to the copper leads in the Tandem system, it is not recommended for use in the customer-supplied cables that connect the power panel with the processor cabinet.

2.1.5.3 Input Power Configurations

For installations in the United States and Canada, 120/208 volt, 3-phase, 60 Hz power is required. This must be a wye (star) connected, five-wire system as shown in Figure 2-1. Figure 2-2 shows connections for a primary (high-voltage) service entrance.

Phase balancing should be ±5% using the following formula:

$$\% \text{ Variance} = \frac{3 \times (\text{maximum voltage} - \text{minimum voltage})}{\text{voltage phase A} + \text{voltage phase B} + \text{voltage phase C}}$$

The nondomestic power services that are normally available for computer sites are 220/380 volt, 3-phase, 50 Hz and 240/415 volt, 3-phase, 50 Hz. Figure 2-3 shows the power panel connections required. Isolation transformers are included in Tandem systems built for nondomestic installation (refer to Appendix B.)

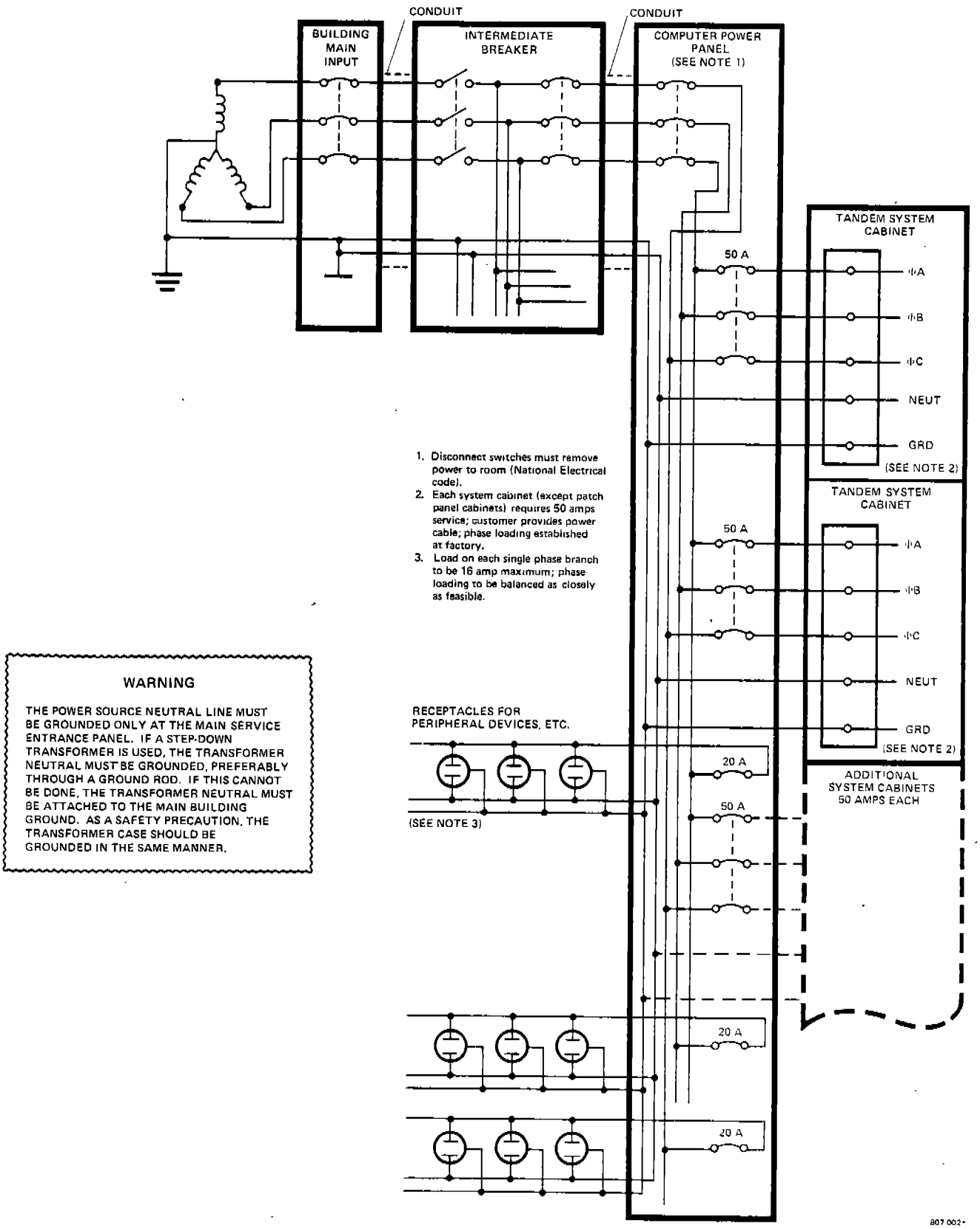

Figure 2-1 120/208 Volt, 3-Phase, 5-Wire Connections

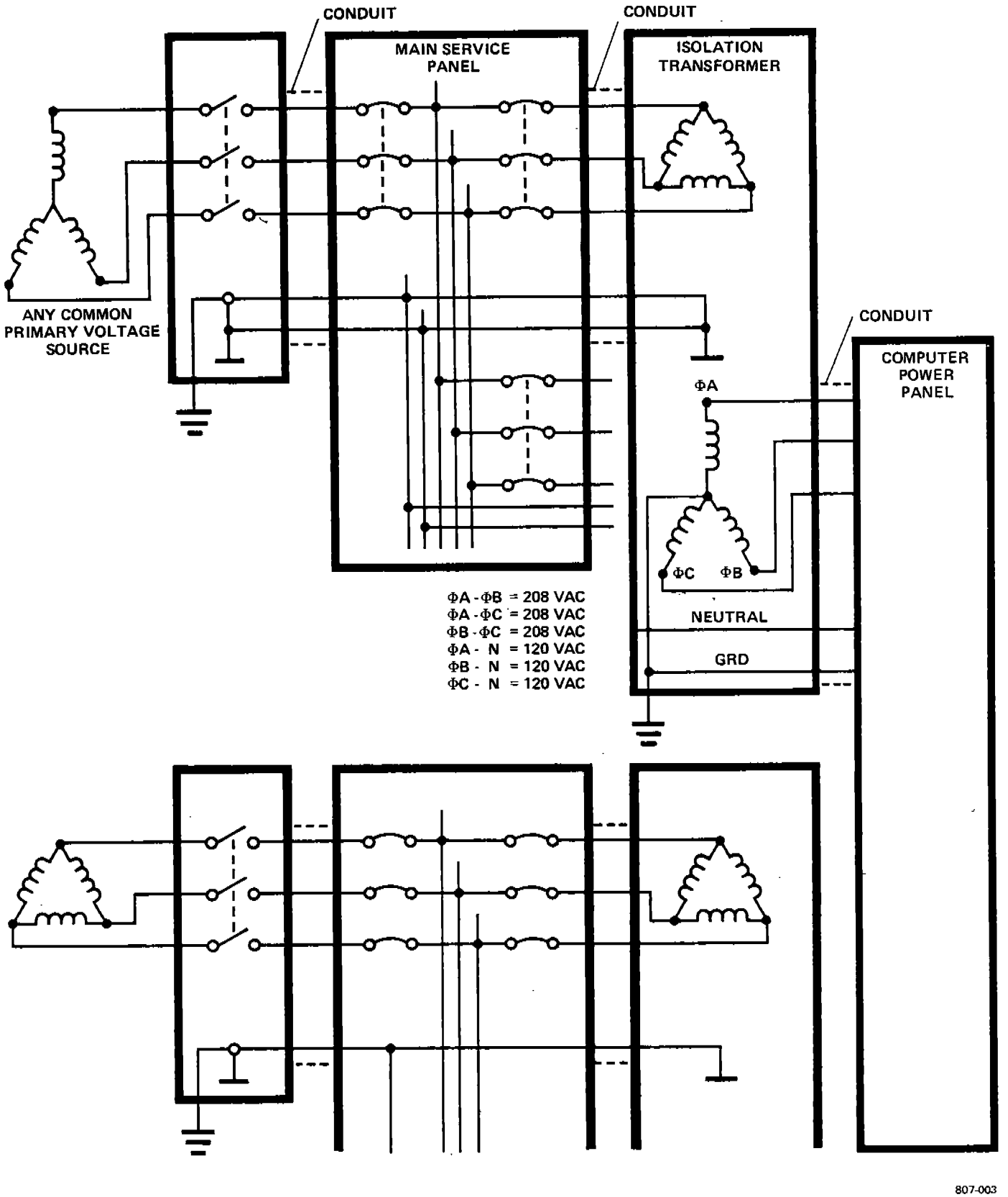

Figure 2-2 Primary Service Voltage, Delta, or Wye Connections

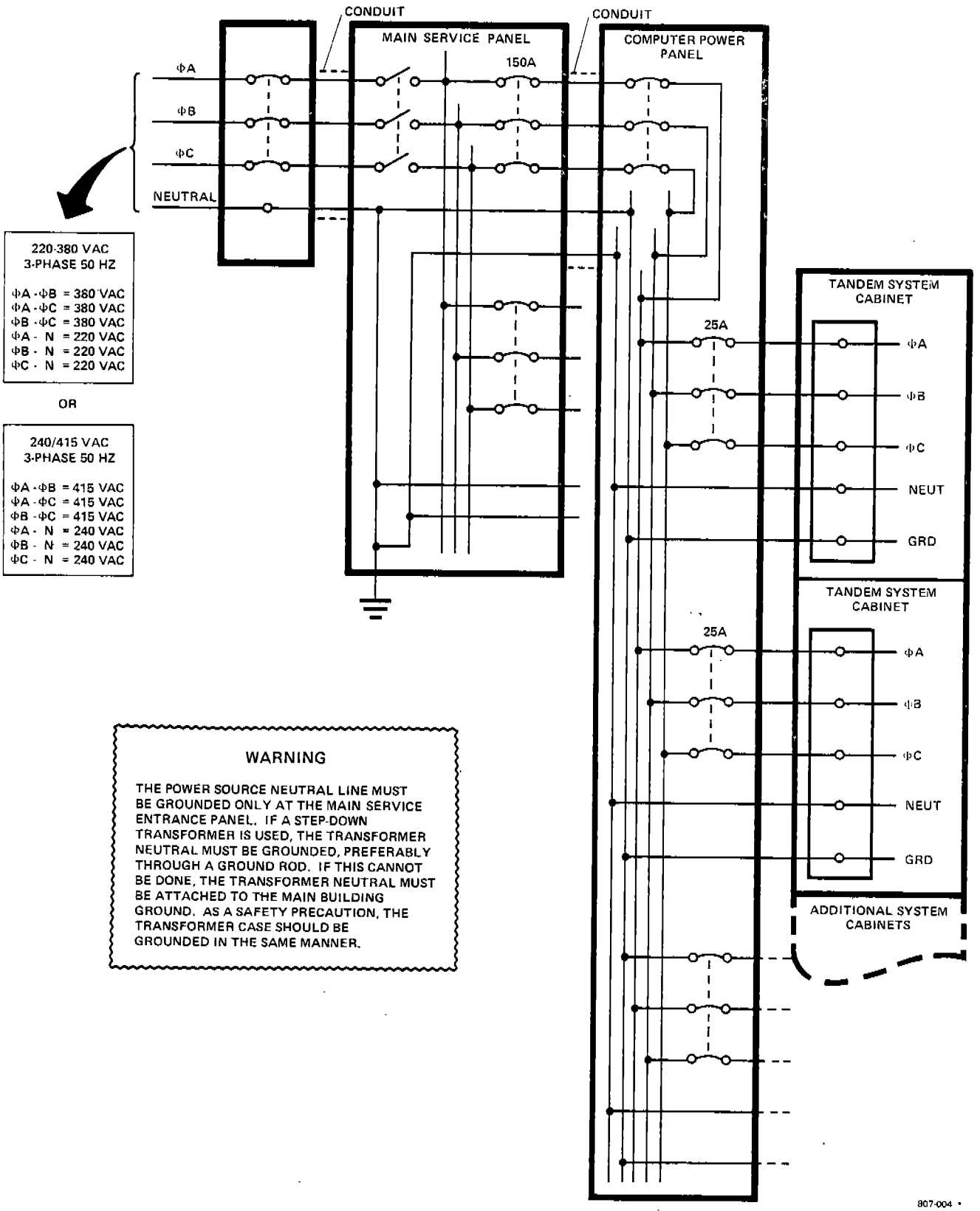

Figure 2-3 220/380 and 240/415 Volt, 3-Phase, 50 Hz Connections

2.1.6 Ground Requirements

Proper power system grounding is essential to both computer system operation and personnel safety. Without exception, conduit grounds are not acceptable. Continuous copper wire ground of appropriate size (as determined by NEC electrical codes) must be carried from the power panel to the system itself to ensure solid ground.

> **WARNING**
>
> It is essential that the computer power panel be properly grounded by adhering to the requirements described in Table 2.2.

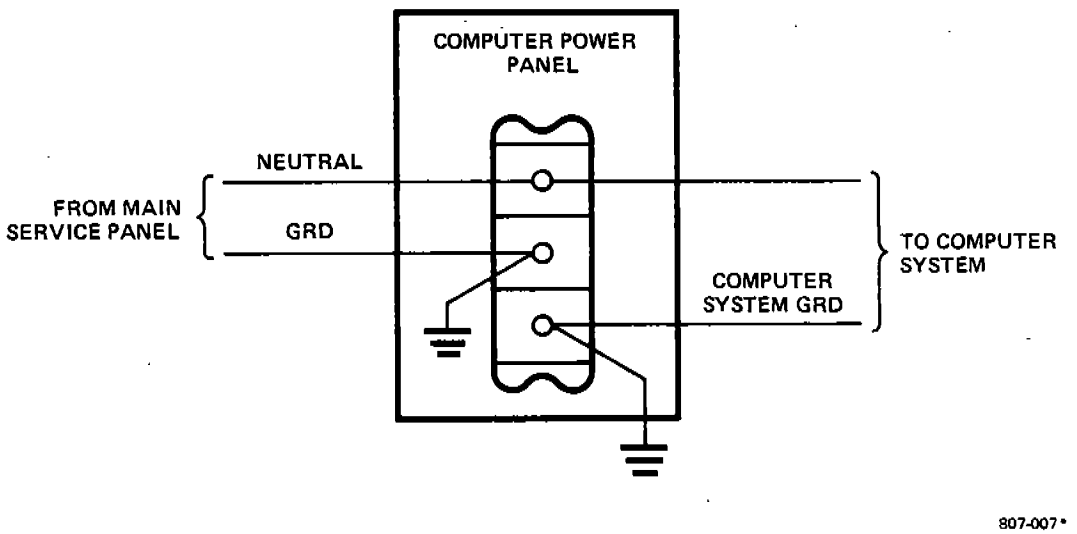

Figure 2-4 Alternate Ground for Processing System

Table 2.2 Ground Requirements

REQ. NO.	REQUIREMENT
1	The main service entrance panel should be grounded in accordance with the National Electrical Code, which requires that the ground present less than 25 ohms impedance through the range of DC to 10 MHz, measured to an array of test electrodes driven into the earth ground as specified by the National Electrical Code.
2	If the computer power panel is fed directly from the main service entrance panel, a ground wire (green) must be installed between the two panels. This ground wire must have at least double the current-carrying capacity as the conductor wires. When the distance between the two panels exceeds 100 feet, the ground wire size should be increased to the next larger gauge.
3	If, after 1 and 2 above are satisfied, the computer power panel ground does not meet the same NEC specification stated in requirement 1, a separate ground must be furnished. To meet code requirements, this newly established ground must not be connected to the existing building power source ground; instead it must be connected to an isolated terminal within the computer power panel (refer to Figure 2-4 on previous page). When this expedient is necessary, all computer equipment must then use this isolated ground.

WARNING

The power source neutral line must be grounded only at the main service entrance panel. If a step-down transformer is used, the transformer neutral must be grounded, preferably through a ground rod. If this cannot be done, the transformer neutral must be attached to the main building ground. As a safety precaution, the transformer case should be grounded in the same manner.

2.2 OPERATING ENVIRONMENT

The acceptable limits of humidity for a typical Tandem system are:

Relative Humidity: 42% to 70% noncondensing

The optimum operating humidity for a Tandem system is:

Relative Humidity: 50% (± 3%) noncondensing

The rate of change in Relative Humidity should be no more than ± 5% per hour.

The acceptable temperature limits for a typical Tandem system are:

Temperature: 60 to 85 degrees F
15 to 29 degrees C

The optimum operating temperature for a Tandem system is:

Temperature: 72 degrees F (± 3 degrees)
22 degrees C (± 1 degree)

The rate of temperature change should be no more than ± 5 degrees F (± 2 degrees C) per hour.

Because the Power subsystem resides in the system cabinets, the environmental requirements are the same as for the system as a whole. For more detailed information on system environmental considerations, refer to the SITE PLANNING MANUAL (82853), Section 2.

2.3 SWITCHES AND INDICATORS

The following paragraphs describe the switches and indicators located on the supplies in the NonStop II/NonStop TXP power subsystem. For more detailed information on setting the switches, refer to paragraph 4.1.

2.3.1 AC Distribution Module Switches

The AC power distribution module has six switches or circuit breakers, CB1-CB6, on the front panel (as seen from the rear of the cabinet). The circuit breakers allow distribution of AC power to the DC supplies, battery supplies, cooling fans, or power receptacles (refer to paragraph 2.4 for AC power distribution details). CB1, CB2, and CB3 are toggle switches and CB4, CB5, and CB6 are push button circuit breakers. The toggle switches, in the ON position, allow AC power distribution to the DC supplies, power receptacles, and fans. The push button circuit breakers, when pushed in, also allow power to the power receptacles or fans, but these circuit breakers pop out if an overload condition occurs. Refer to Figure A-1 for switch location diagram.

2.3.2 Processor Power Supply Switches and Indicators

The 7900 processor power supply has two switches on the front panel. The switch on the left is the AC ON/OFF switch and the switch on the right is the DC ON/OFF switch. The AC switch, when in the ON position, allows 115 V or 230 V of AC voltage from the AC power distribution module to power the processor supply. The DC switch, when in the ON position, allows the 48 volt battery back-up power from the UPS modules to be provided to the power supply so that it is available to power the 5 volt, 18 amp and 12/15 volt supplies in the event of an AC power failure. (Normally the 12/15 volt supply is adjusted to +12 volts for use with 512 KB memory boards in NonStop II systems.)

The processor power supply has three indicators on the front panel. Table 2.3 describes the meaning of the indicators. These indicators extinguish if the required voltage is not present. Refer to Figure A-1 for switch indicator location diagram.

Table 2.3 Processor Power Supply Indicators

INDICATOR	MEANING
5 100	Indicates that +5 volts/100 amps is present, but not necessarily adjusted.
5 18	Indicates that +5 volts/18 amps is present, but not necessarily adjusted.
12 15	Indicated that +12 or +15 volts is present, but not necessarily adjusted.

2.3.3 I/O-Only Power Supply Switch and Indicator

The 7301 I/O-only power supply has one switch on the rear panel, the AC ON/OFF switch. The AC switch, when in the ON position, allows 115 V or 230 V of AC voltage from the AC power distribution module to power the I/O-only power supply.

The I/O-only power supply has one indicator on the rear panel. This indicator, when lit, indicates that +5 volts/100 amps is present, but not necessarily adjusted. Refer to Figure A-1 for switch and indicator location diagram.

2.3.4 Battery Supply Switches and Indicators

The 7303 battery supply has two switches on the front panel. The switch on the left is the AC ON/OFF switch and the right is the TEST ON/OFF switch. The AC switch, when in the ON postion, allows 115 V or 230 V of AC voltage from the AC power distribution module to power the unit, which in turn charges the batteries. The TEST switch, when in the ON position, allows a visual measurement of the battery voltage. (A voltmeter may be used to make a direct measurement of the battery voltage at the red (TP1) and black (TP2) jacks on the front of the battery supply.)

There are 24 LED indicators on the front panel of the UPS battery supply that display the battery voltage and charge current of the battery pack while AC power is applied to the UPS unit. The 12 LEDs in the top row indicate the charge current and the 12 LEDs in the bottom row indicate the battery voltage. Figure 2-5 shows the acceptable limits of the voltage and current ranges. Refer to Figure A-1 for switch and indicator location diagram.

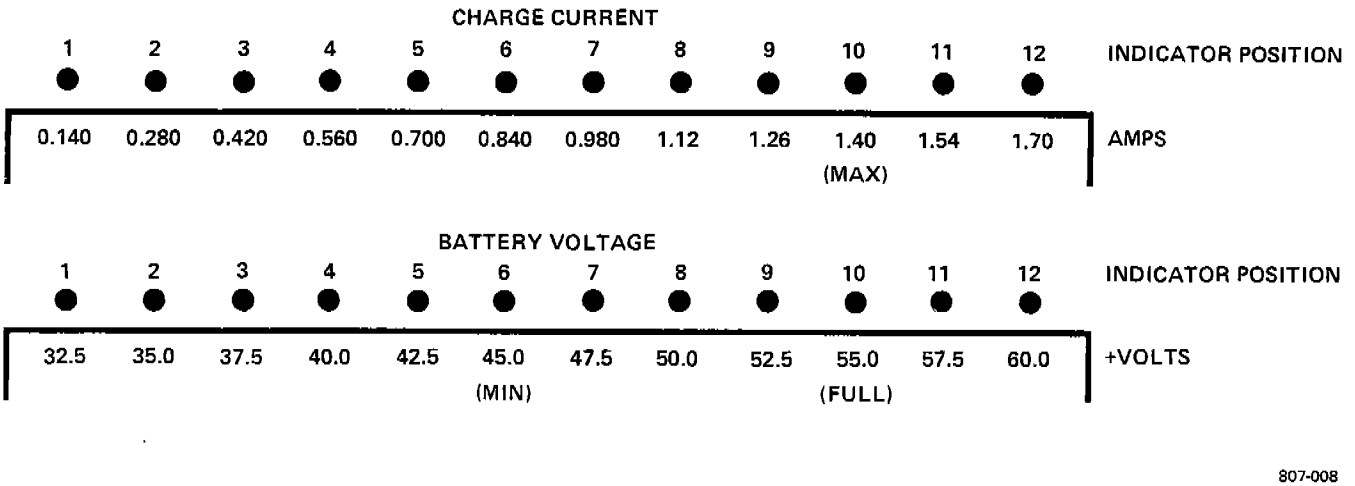

Figure 2-5 Battery Supply Indicator Ranges

2.3.5 I/O Regulator Assembly Switch and Indicator

The I/O regulator assembly, located at the bottom of each I/O board slot, has one switch at the outer edge of the board. The switch, in the UP position, allows the regulated +5 volts to be supplied to the I/O slot.

A red LED (Light Emitting Diode), when lit, indicates that power is being supplied to the I/O slot. When the switch is in the DOWN postion, power is removed from the I/O slot. If the I/O slot is empty, the LED may be lit when the switch is in the DOWN postion because no power is being drawn by an I/O board. Refer to Figure A-1 for switch and indicator location diagram.

2.4 AC POWER DISTRIBUTION

AC power from the computer room power panel must be supplied by the customer. The power panel must be a dedicated AC power source with three 50 Amp breakers (25 Amp for 50 Hz systems) for each cabinet that has a power distribution module. A shielded five wire cable (with ring lugs for #10 studs) of sufficient current carrying capability to handle 50 amps must be supplied by the customer. The five wires are: one each for the three phases, one for neutral, and one for ground. The electrician must connect the AC cable to the RFI filter mounted in front of the power distribution module. The customer engineer must specify which phase will be connected as phase A, B, and C (refer to paragraph 4.4 for phase balancing information). The output of the RFI filter is wired directly into the AC distribution module. The following paragraphs describe the phase distribution from the AC distribution module.

2.4.1 Processor or I/O-Only Cabinet (60 Hz)

The following is a description of the AC phase distribution in a 60 Hz processor or I/O-only cabinet. Figure 2-6 shows the 60 Hz AC power distribution module for a processor or I/O-only cabinet.

Phase A goes to circuit breaker "CB1" then to:

a. CPU power supply for Processor 0 via cable "AC0" and for Processor 3 via cable "AC3".

b. One-half of a 20 amp power receptacle, designated "P8", available for magnetic tape unit power via "CB4".

c. Two of four plenum cooling fans via "CB4" and cable marked "Fan Power".

Phase B goes to circuit breaker "CB2" then to:

a. CPU power supply for Processor 2 via cable "AC2".

b. One-half of a 20 amp power receptacle, designated "P8", available for magnetic tape unit power via "CB5".

c. One of four plenum cooling fans via "CB5" and cable marked "Fan Power".

Phase C goes to circuit breaker "CB3" then to:

a. CPU power supply for Processor 1 via cable "AC1".

b. A 15 amp power receptacle, designated "P7", available for test equipment via "CB6".

c. One of four plenum cooling fans via "CB6" and cable marked "Fan Power".

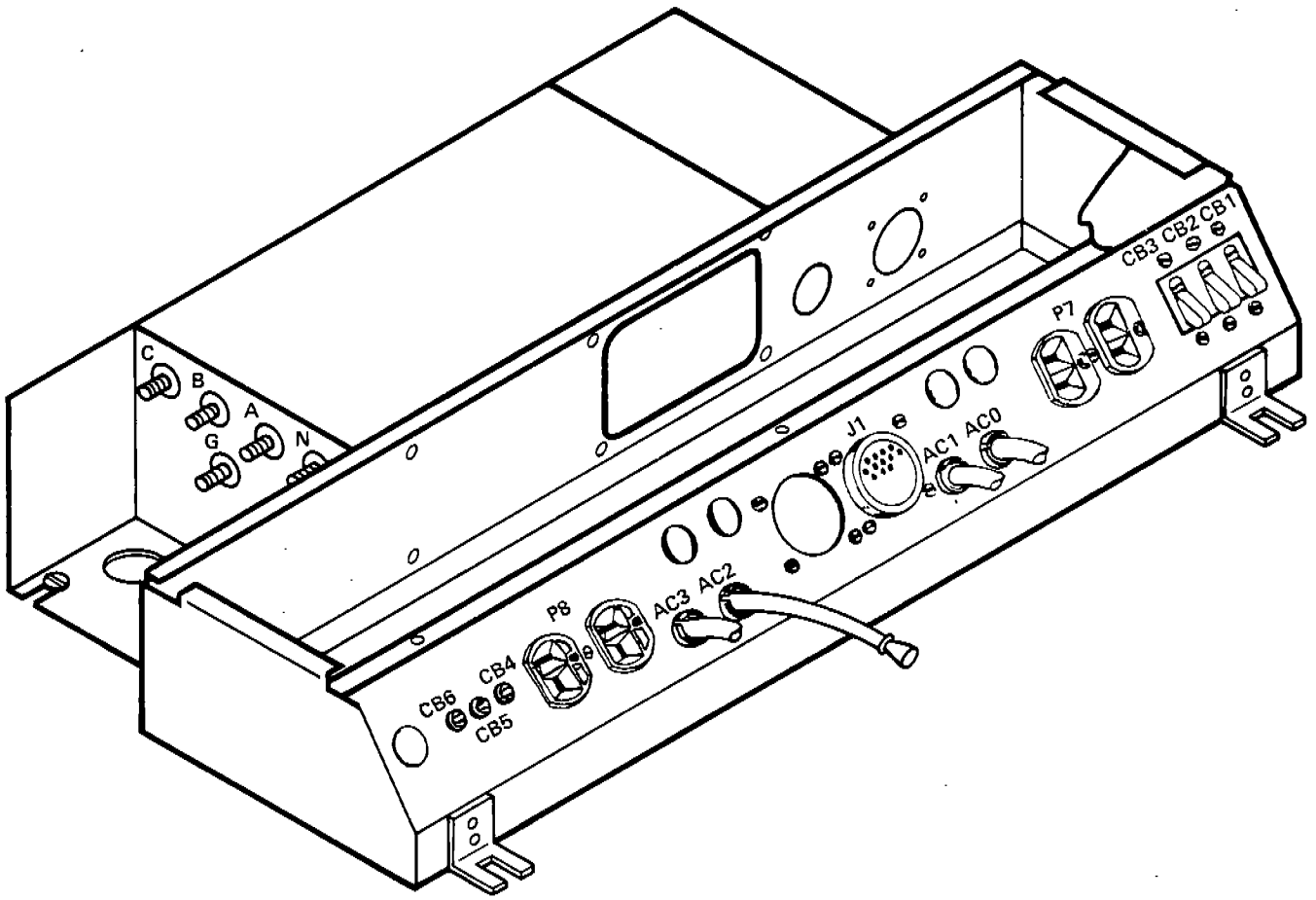

Figure 2-6 60 Hz Processor AC Power Distribution Module

2.4.2 Magnetic Tape, Expansion, or Patch Panel Cabinet (60 Hz)

The following is a description of the 60 Hz AC phase distribution in a magnetic tape, expansion, or 7105 patch panel cabinet. Figure 2-8 shows the 60 Hz AC power distribution module for a magnetic tape, expansion, or patch panel cabinet.

Phase A goes to circuit breaker "CB1" then to:

a. I/O-only supply or UPS 0 via cable "AC0".

b. I/O-only supply or UPS 3 via cable "AC3".

c. One-half of a 20 amp power receptacle, designated "P8", available for magnetic tape unit power via "CB4".

Phase B goes to circuit breaker "CB2" then to:

a. I/O-only supply or UPS 2 via cable "AC2".

b. I/O-only supply or UPS 5 via cable "AC5".

c. I/O-only supply or UPS 7 via cable "AC7".

d. One-half of a 20 amp power receptacle, designated "P8", available for magnetic tape unit power via "CB5".

Phase C goes to circuit breaker "CB3" then to:

a. I/O-only supply or UPS 1 via cable "AC1".

b. I/O-only supply or UPS 4 via cable "AC4".

c. I/O-only supply or UPS 6 via cable "AC6".

d. A 15 amp power receptacle, designated "P7", available for test equipment via "CB6".

Circuit breakers CB1 through CB6 for both types of distribution module are rated as follows:

For 102/208 volts @ 60 HZ:

a. CB1 through CB3 are rated 40 amps.

b. CB4 and CB5 are rated 20 amps.

c. CB6 is rated 15 amps.

For 220/380 volts @ 50 HZ:

a. CB1 through CB3 are rated 20 amps.

b. CB4 and CB6 are rated 15 amps.

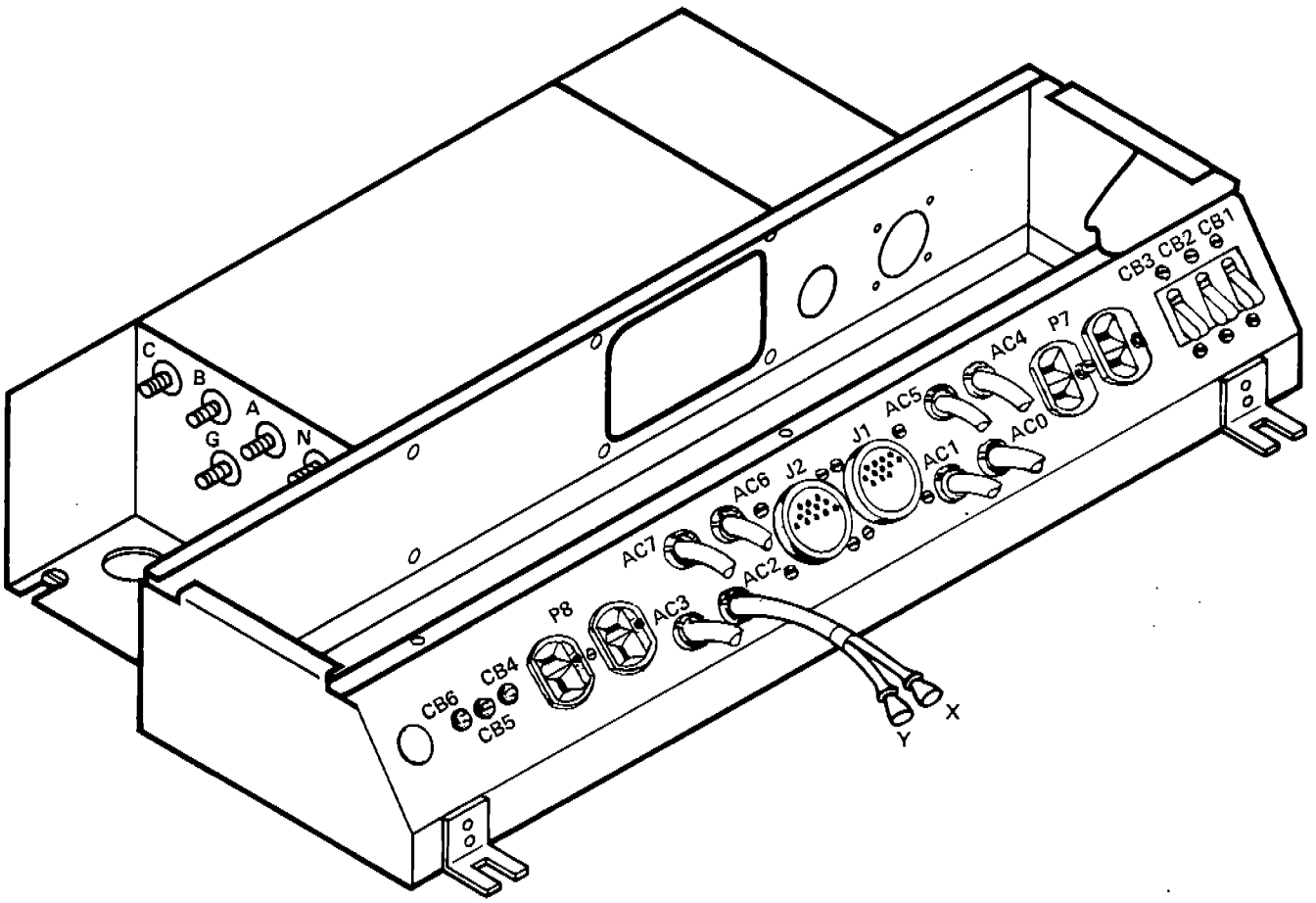

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Figure 2-7 60 Hz Magnetic Tape AC Power Distribution Module

2.5 DC POWER DISTRIBUTION

There are three types of DC power sources used in a NonStop II or NonStop TXP processing system. The DC power sources are:

a. Processor Power Supplies which provide:

   +5 volts at 100 amps used for the CPU and I/O controllers.
   +5 volts at 17.5 amps memory voltage (UPS).
   +12 volts at 4 amps memory voltage (UPS).

NOTE

For NonStop TXP processors, the +5 volt/100 amps is used exclusively for the CPU and the +12 volts memory voltage is not used.

b. I/O-Only Power Supplies which provide:

   +5.7 volts at 100 amps used for the I/O controllers.

c. Uninterruptable Power Sources (UPS) or Battery Supplies which provide:

   +48 volts used by the processor power supply during a power failure to supply the +5 and +12 memory voltages.

In addition to the three types of DC power supplies, there are several other DC power distribution circuits in the power subsystem. These circuits include:

a. I/O (Horizontal) Bus

b. Processor Power (Vertical) Bus

c. Backplane Power Circuits

d. Plenum Diodes

e. Power Sense Lines

f. Power Fail Warning Lines

g. I/O Regulators.

Refer to Figure A-2 for DC power distribution location diagram.

2.5.1 Processor Power Distribution

The processor power supply is used to supply voltage to the main processor, memory, and I/O controllers. The processor supply must be located directly below the processor that it supplies. This ensures an orderly configuration and allows the cables to be kept short to reduce power losses.

The processor power supply draws AC power from the AC distribution module through J3. J3 also provides the +48 volts used by the power supply to keep the +5 and +12 UPS voltage on during a power failure.

The +5 volts/100 amps (IPS) is supplied through J2. The +5 volts/17.5 amps (UPS) and +12 volts/4 amps memory voltages are supplied through J1.

The +5 volts/100 amps from J2 splits into two paths. One path goes to the plenum diode then to the 5I tab of the vertical bus, and from the vertical bus to the CPU backplane. The other path goes to one of the V-tabs of the horizontal bus, and then to one side of the I/O regulator that supplies +5 volts to the I/O controller slots. Since the path going to the CPU backplane must be at +5 volts and the path going to the I/O regulators must be at approximately +5.7 volts, the plenum diode is used to drop approximately .7 volts, allowing the +5 volts/100 amps output of the power supply and the horizontal bus bar to be at +5.7 volts, while +5 volts is supplied to the vertical bus bar.

Refer to Figure A-2 for processor power supply location.

2.5.2 I/O-Only Power Distribution

The I/O-only power supply is used to supply power to the I/O card cage when the configuration requires more power than can be supplied by the CPU power supplies (or in the case of NonStop TXP processors, all I/O devices are supplied exclusively by I/O-only supplies) and for backup if one of the other supplies fails. The I/O-only power supply can be located in any cabinet type with an AC distribution module and power supply racks. Because of power loss in cabling, the I/O power supply must reside in the same or adjacent cabinet to the card cage it supplies.

The I/O-only power supply gets AC power from the AC distribution module through J3. J1 is the input for the voltage sense lines. The +5.7 volts/100 amps is supplied from J2. The cable from J2 goes to the V-tab of the horizontal bus where power is required to augment the processor supplies (NonStop II only).

Refer to Figure A-2 for I/O-only power supply location.

2.5.3 UPS (Battery Supply) Distribution

The UPS supplies power to the processor power supply to keep memory voltages on during a power failure. The UPS can be located in any cabinet that has an AC distribution module and power supply racks, except a processor or I/O-only cabinet. The UPS supplies +48 volts to the processor supplies to be used during power failure.

The UPS (battery supply) receives power from the AC distribution through one of the AC0 through AC7 cables, depending on placement in the supply rack. If in the lower rack, AC0 through AC3 are used. If in the upper rack, AC4 through AC7 are used. This power comes in through J1 of the UPS box. The +48 volts goes out through J2 to the distribution module through the same cable as the AC input. It then goes out J1 or J2 of the distribution module to J1 of the processor distribution module. If the UPS is connected to AC0 through AC3, J1 is used as the output. If it is connected to AC4 through AC7, then J2 is used as the output. Table 2.4 shows how the tape cabinet distribution module battery cables correspond to the processor distribution module cables.

Table 2.4 Magnetic Tape to Processor PDM Correspondence

MAGNETIC TAPE PDM CABLES	CORRESPOND TO PROCESSOR PDM CABLE
AC0 and AC4	AC0 (CPU 0, 4, 8, or 12)
AC1 and AC5	AC1 (CPU 1, 5, 9, or 13)
AC2 and AC6	AC2 (CPU 2, 6, 10, or 14)
AC3 and AC7	AC3 (CPU 3, 7, 11, or 15)

Refer to Figure A-2 for UPS (battery supply) location.

2.5.4 I/O (Horizontal) Bus

The I/O power bus (horizontal bus bar) is a laminated bar made up of nine flat bus layers separated by insulating material. This provides eight power buses and one ground plane. The bus is divided into eight sections, each consisting of two large tabs (ground and +5 volts) to which the power supply is connected and eight smaller tabs (one for each of the eight +5 volt buses) that supply the I/O board slots.

The horizontal bus distributes the +5.7 volts/100 amps to the I/O backplane. The large tabs along the top of the bus connect the power supplies grounds to the bus. The large tabs along the bottom labeled V1 through V8 connect the +5.7 volts from the CPU and I/O-only supplies. The small tabs labeled V1 through V8 distribute the power to the regulators that supply power to the I/O controller slots. The large V-tabs are common to its corresponding small V-tab inside the bus. The even numbered V-tabs connect the processor supplies to the bus. The odd numbered V-tabs connect any I/O supplies that are needed.

Red wires connect the bus V-tabs to the regulators. The two wires for each controller slot must go to two different V-tab connections to provide backup power. When the power supply voltages are properly adjusted, equal current is drawn from each of the two V-tabs. The voltage of approximately +5.7 at the V-tabs is regulated to +5.05 and supplied to each controller slot. The bottom pot on each regulator is used to adjust the voltage output of each regulator. The top pot, for adjusting the current limit, is FACTORY SET and should NEVER be adjusted in the field.

Refer to Figure A-2 for I/O (horizontal) bus location.

2.5.5 Processor Power (Vertical) Bus

The processor power bus (vertical bus bar) is a laminated bar made up of five flat bus strip layers, separated by insulating material, used to transfer power from the processor power supply to the CPU backplane (refer to Figure A-2). The buses are:

a. 5I - This is the +5 volt 100 amps and comes from the plenum diode.

b. 5U - This is the +5 volts uninterruptable power and comes from J1 of the processor supply.

c. VM - This is the +12 volts uninterruptable power for memory and comes from J1 of the processor supply.

d. G1 - Ground plane for the +5 volts 100 amps.

e. G2 - Ground plane for the +5 and +12 uninterruptible supplies.

2.5.6 Backplane Power Circuits

The backplane circuits for each processor are located on the lower backplane board for that processor. The power circuits consist of printed circuit buses that receive power from the processor power bus and distribute power to the connectors into which the processors are plugged.

The backplane power circuits for each block of six I/O slots are located on the lower backplane board for that block. The power circuits distribute +5 volts from the CPU or I/O supply to each card slot.

Refer to Figure A-2 for backplane power circuit location.

2.5.7 Plenum Diodes

For each processing unit and processor power supply installed in a processor cabinet, a diode is installed on a large heat sink in the cooling air plenum just below the I/O card cage. The plenum diode is required to compensate for the voltage drop of the power regulator circuits (I/O board slots). The +5 volt output from the processor power supply is applied to the processor backplane via the I/O power bus and the power switching circuits (refer to paragraph 2.5.10), producing a voltage level to the processor backplane of exactly +5.05 volts. The plenum diodes cause the voltage level to the I/O backplane to be the same as that applied to the processor backplane through the power regulators.

Refer to Figure A-2 for plenum diode location.

2.5.8 Power Sense Lines

The power sense lines provide the voltage regulators in the power supply with an indication of the voltage level at the backplane. The power sense lines also allow compensation for voltage dropped across the plenum diodes and along the length of the vertical bus. These lines extend from J1 of the power supply to the backplane through connector P3.

Refer to Figure A-2 for power sense line location.

2.5.9 Power Fail Warning Lines

The power failure warning lines provide the CPU and the Guardian Operating System with an indication that the AC power input to the power supply has stopped. When the AC power stops, the DC power is lost if AC power is not restored within 25 ms. The power supply has a large capacitive storage capability and can maintain DC power for 25 ms after an AC power failure. The power failure warning occurs 17 ms after the initial loss of AC power. An 8-ms period allows the operating system time to perform a power fail routine, storing in memory the information required to resume the current operation when power is restored. The battery supply then takes over and can operate for 80 minutes to four hours (NonStop II) or three to nine hours (NonStop TXP) depending on the type and number of memory boards. When power is restored, the operating system is reactivated, reconstructing the processing environment that existed just before the failure, and the application resumes.

The power failure warning lines extend from J1 of the power supply to the backplane through connector P2 and are routed along the vertical bus with the power sense lines.

Refer to Figure A-2 for power fail warning line location.

2.5.10 I/O Regulators

The I/O regulator receives inputs from two separate V-tabs on the horizontal bus bar. The output of the I/O regulator powers one I/O controller board. The I/O regulator draws current equally from the two V-tabs and regulates the two +5.7-volt sources to +5.05 volts at the I/O controller board input. If one of the +5.7-volt sources fails, the I/O regulator automatically draws all the required output current from the remaining +5.7-volt source, keeping the input voltage at the I/O controller card slot at +5.05 VDC.

Refer to Figure A-2 for I/O regulator location.

SECTION 3
FUNCTIONAL DESCRIPTION

3.0 FUNCTIONAL DESCRIPTION

The power subsystem configuration, shown in Figure 3-1, has the following attributes:

a. Separate power supply for each processor module.

b. Separate uninterruptible power source (battery supply) for each semiconductor memory processor.

c. Power switching between two independent power sources for I/O controllers and IPB controllers.

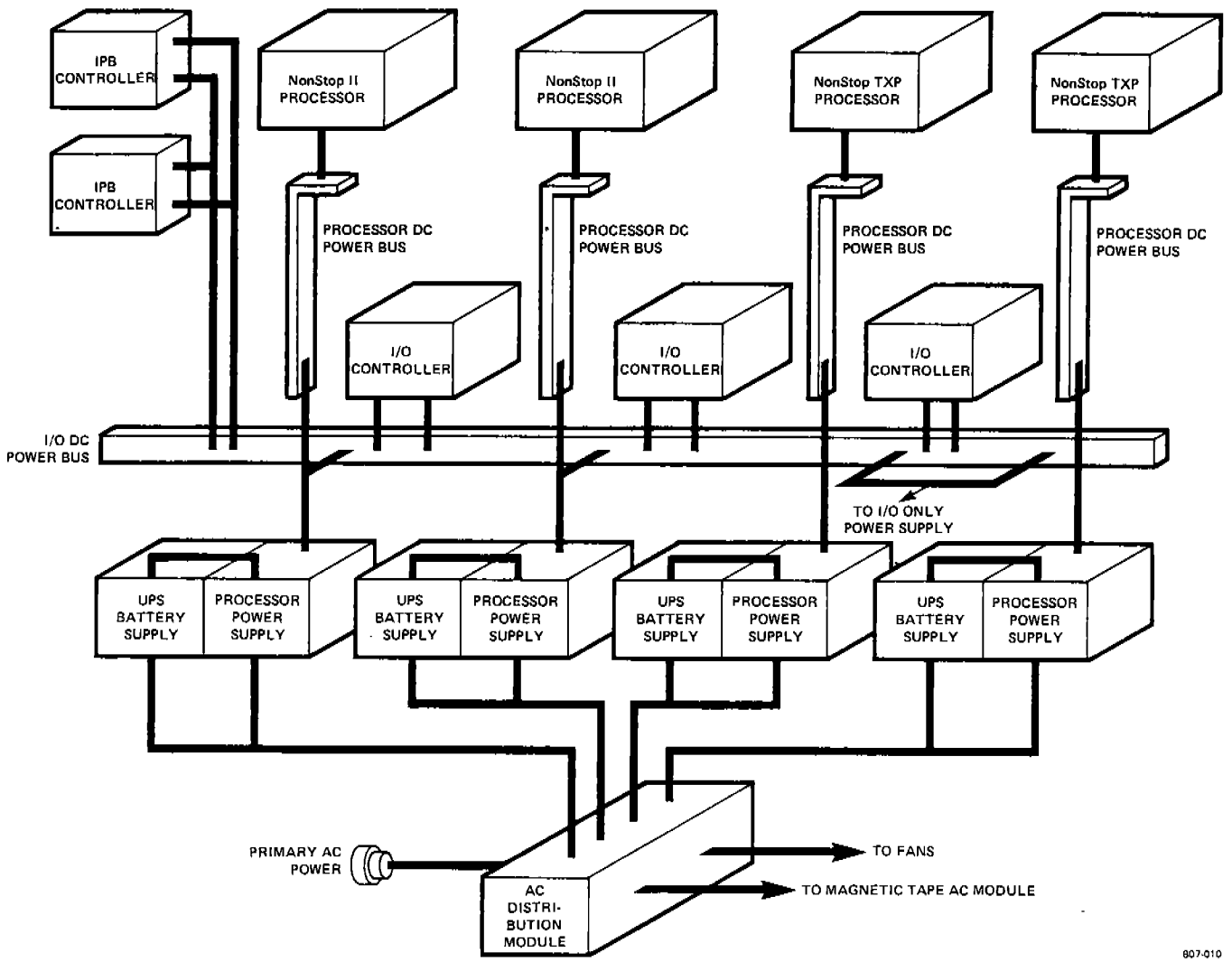


Figure 3-1 Power Subsystem Configuration

3.1 OPERATIONAL DESCRIPTION

AC power is distributed to the IPS (Interruptable Power Source) DC power supplies, the UPS (Uninterruptable Power Source) battery supplies, the fans, and the magnetic tape unit by the AC distribution module. Figure 3-2 shows the block diagrams for both the 60 Hz processor AC power distribution module and the 60 Hz magnetic tape AC power distribution module. Refer to paragraph 4.4.2 for 50 Hz phase information. Primary AC power can be any one of the following:

a. 120/208 VAC, 3 phase, 60 Hz

b. 220/380 VAC, 3 phase, 50 Hz

c. 240/415 VAC, 3 phase, 50 Hz

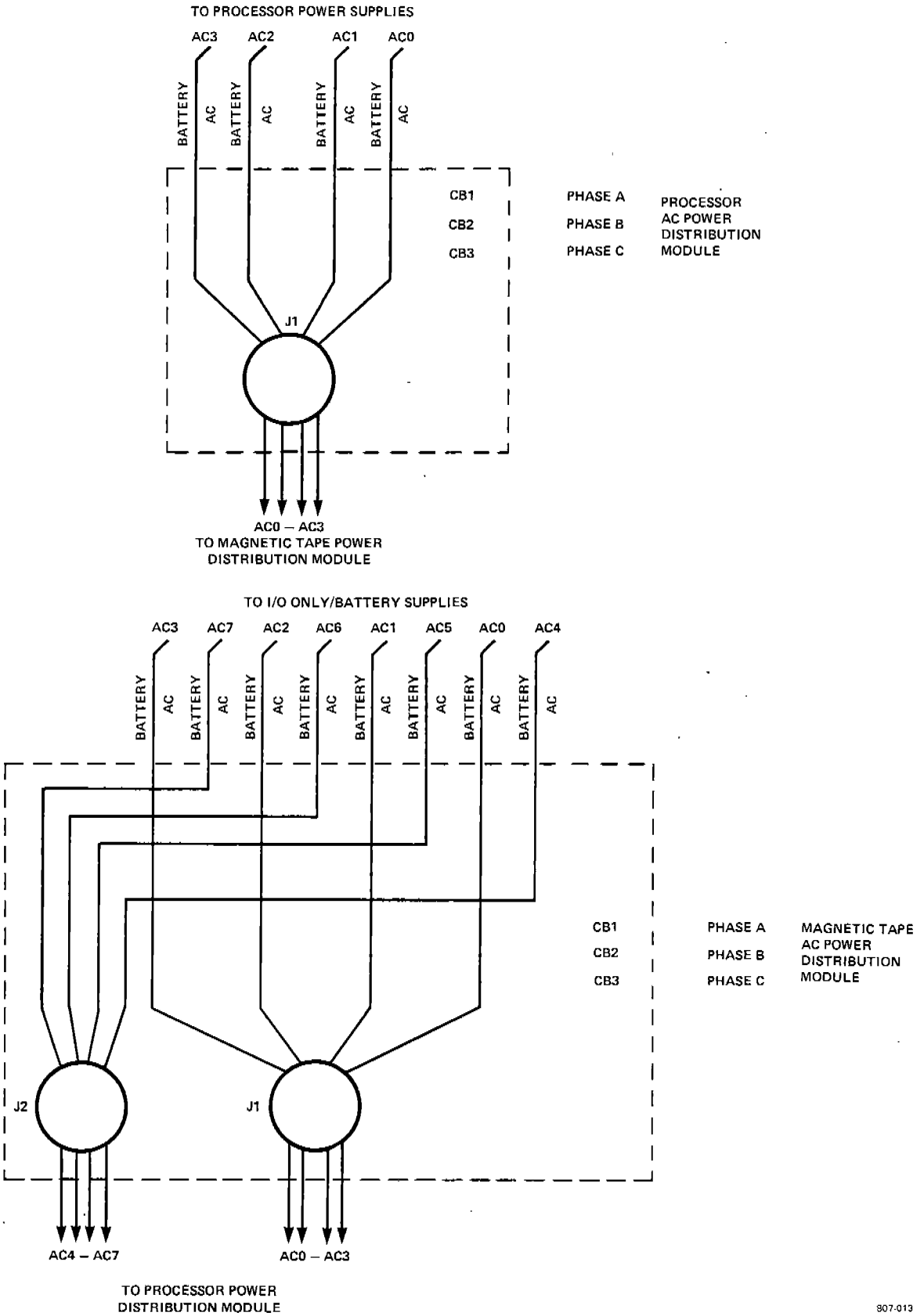


Figure 3-2 60 Hz AC Power Distribution Module Block Diagram

The DC voltages provided by the IPS processor power supply are:

a. +5 VDC UPS @ 100 Amps

b. +5 VDC IPS @ 18 Amps

c. +12 VDC UPS @ 4 Amps (used for NonStop II only)

DC power is delivered from the processor power supply to each processor via a processor (vertical) power bus, consisting of five individual buses laminated together to form a single unit. The bus delivers +5 VDC IPS, +5 VDC UPS, +12 VDC UPS, DC ground, and memory ground to the processor. Refer to Figure 3-3 for processor power supply block diagram.

A single I/O (horizontal) power bus delivers DC power from the +5 VDC IPS I/O-only supply to the I/O controllers. The bus consists of nine individual buses that are laminated together to form a single unit. Voltage is supplied to the bus from each I/O-only power supply. Voltage tabs along the bus allow the I/O controllers and IPB controllers to be electrically distributed among the power modules.

3.1.1 I/O Power Regulators

Local voltage for the I/O controller modules is regulated by the I/O regulator card on the I/O lower backplane. Each I/O regulator delivers the regulated 5 volts to one I/O slot. The current required by an I/O controller module is drawn equally from two power modules (one processor power supply and one I/O only power supply). In the event of a failure of either power module, the full load current is drawn from the operational module.

3.1.2 IPB, Control Panel, and PMI DC Power

An I/O power regulator furnishes redundant DC power to each IPB, control panel, and PMI in the same manner that power is supplied to an I/O controller slot. The I/O regulator cards for this purpose are located on the right side of the processor cabinet card cage.

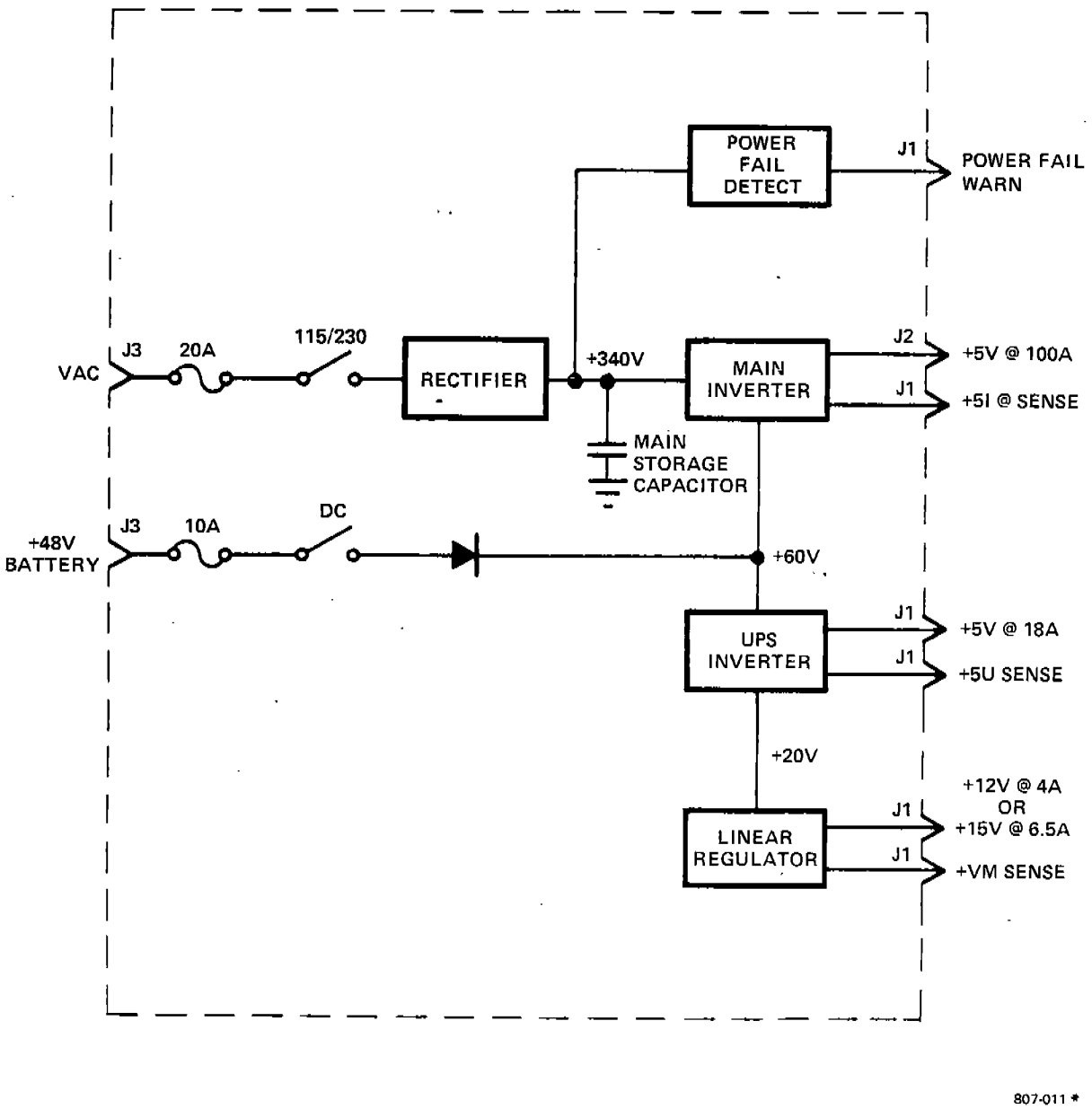


Figure 3-3 IPS Processor Power Supply Block Diagram

3.1.3 Uninterruptible Power Supply (UPS)

This feature is used to preserve semiconductor memory data during AC power outages. The UPS voltages are:

a. +5 VDC @ 18 Amps

b. +12 VDC @ 4 Amps (NonStop II only)

These voltages are sustained, in the event of an AC power failure, by the UPS battery supply. During normal operation, the charge on the batteries is maintained by a battery charger contained in the battery supply housing. Refer to Figure 3-4 for battery supply block diagram.

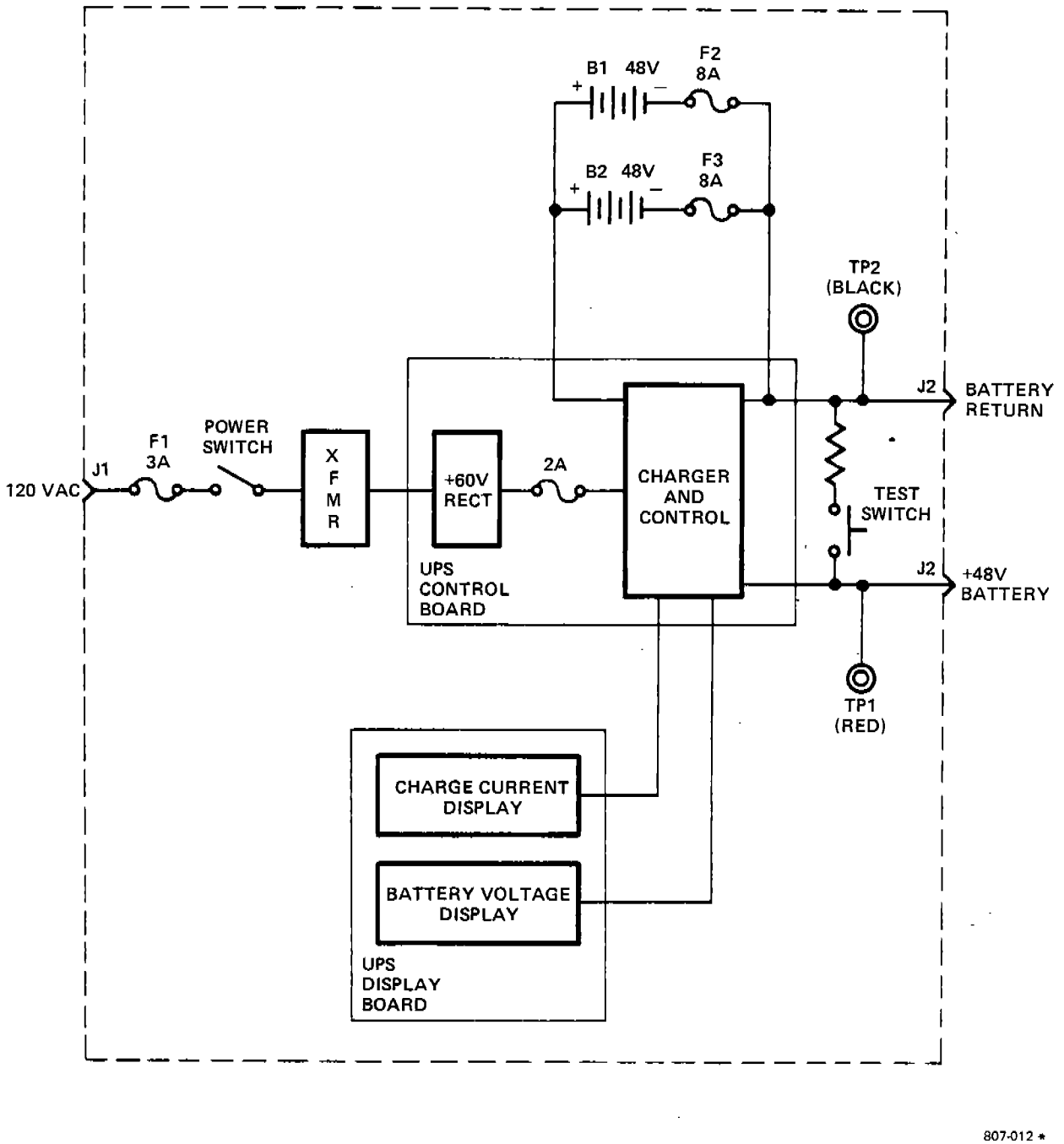


Figure 3-4 UPS Battery Supply Block Diagram

SECTION 4
INSTALLATION

4.0 INSTALLATION

The following paragraphs contain information necessary for the installation of power subsystem components in a NonStop II or NonStop TXP processing system. Included are switch setting details, installation procedures for new devices, phase balancing, and load calculation instructions. The RFI filter, AC power distribution module, and I/O regulator assemblies are normally installed at the factory and require no installation at the customer site.

4.1 SWITCH SETTINGS

The following paragraphs describe the switch settings for normal operation of the AC power distribution module, the DC power supplies (both processor and I/O-only supplies), battery supplies, and the I/O regulator card.

4.1.1 AC Power Distribution Module Circuit Breakers

The AC power distribution module has six switches or circuit breakers, CB1-CB6, on the front panel (as seen from the rear of the cabinet). The circuit breakers allow distribution of AC power to the DC supplies, battery supplies, cooling fans, or power receptacles (refer to paragraph 2.4 for AC power distribution details). CB1, CB2, and CB3 are toggle switches and CB4, CB5, and CB6 are push button circuit breakers. The toggle switches, in the ON position, allow AC power distribution to the DC supplies, power receptacles, and fans. The push button circuit breakers, when pushed in, also allow power to the power receptacles or fans, but these circuit breakers pop out if an overload condition occurs. Refer to Figure 4-1 for circuit breaker location diagram.

During normal operation, the toggle switches must be in the ON position and the push button circuit breakers must be pushed in.

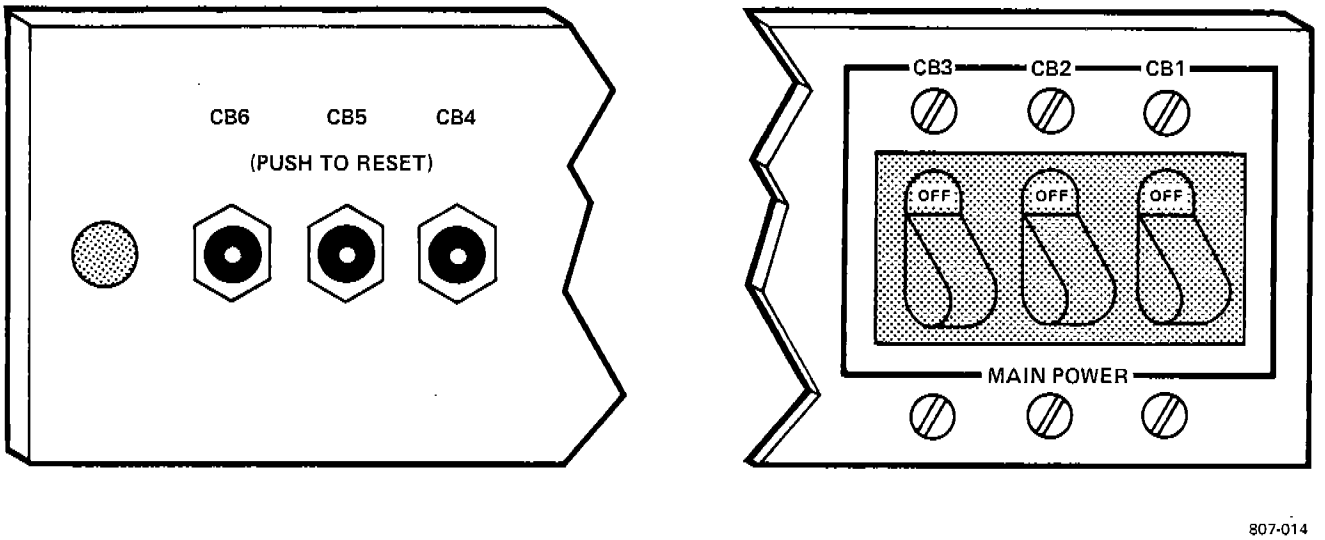


Figure 4-1 AC Power Distribution Module Circuit Breakers

4.1.2 Processor Power Supply Switches

The 7900 processor power supply has two switches on the front panel. The switch on the left is the AC ON/OFF switch and the switch on the right is the DC ON/OFF switch. The AC switch, when in the ON position, allows 115 V or 230 V of AC voltage from the AC power distribution module to power the processor supply. The DC switch, when in the ON position, allows the 48 volt battery back-up power from the UPS modules to be provided to the power supply so that it is available to power the 5 volt, 18 amp and the 12/15 volt supplies in the event of a power failure. Refer to Figure 4-3 for switch location diagram.

During normal operation, both the AC and DC switches must be in the ON position.

4.1.3 I/O-Only Power Supply Switch

The 7301 I/O-only power supply has one switch on the rear panel, the AC ON/OFF switch. The AC switch, when in the ON position, allows 115 V or 230 V of AC voltage from the AC power distribution module to power the I/O-only power supply. Refer to Figure 4-4 for switch location diagram.

During normal operation, the AC switch on the I/O-only power supply must be in the ON position.

4.1.4 Battery Supply Switches

The 7303 battery supply has two switches on the front panel. The switch on the left is the AC ON/OFF switch and the right is the TEST ON/OFF switch. The AC switch, when in the ON postion, allows 115 V or 230 V of AC voltage from the AC power distribution module to power the unit, which in turn charges the batteries. The TEST switch, when in the ON position, tests the battery charger and the relative condition of the batteries. The RED/BLACK test points on the front panel allow direct measurement of the battery voltage. Refer to Figure 4-6 for switch location diagram.

During normal operation, the AC ON/OF switch must be in the ON position. The TEST switch must be in the OFF position during normal operation. Refer to paragraph 4.2.3 for a description of the TEST switch use.

> CAUTION
>
> Do NOT hold the TEST switch in the ON position for over 5 seconds, because this may damage the battery supply.

4.1.5 I/O Regulator Assembly Switch

The I/O regulator assembly, located at the bottom of each I/O board slot, has one switch at the outer edge of the board. The switch, in the UP position, allows the regulated +5 volts to be supplied to the I/O slot. A red LED (Light Emitting Diode), when lit, indicates that power is being supplied to the I/O slot. When the switch is in the DOWN postion, power is removed from the I/O slot. If the I/O slot is empty, the LED may be lit when the switch is in the DOWN postion because no power is being drawn by an I/O board. Refer to Figure 4-2 for switch location diagram.

During normal operation, the switch must be in the UP position.

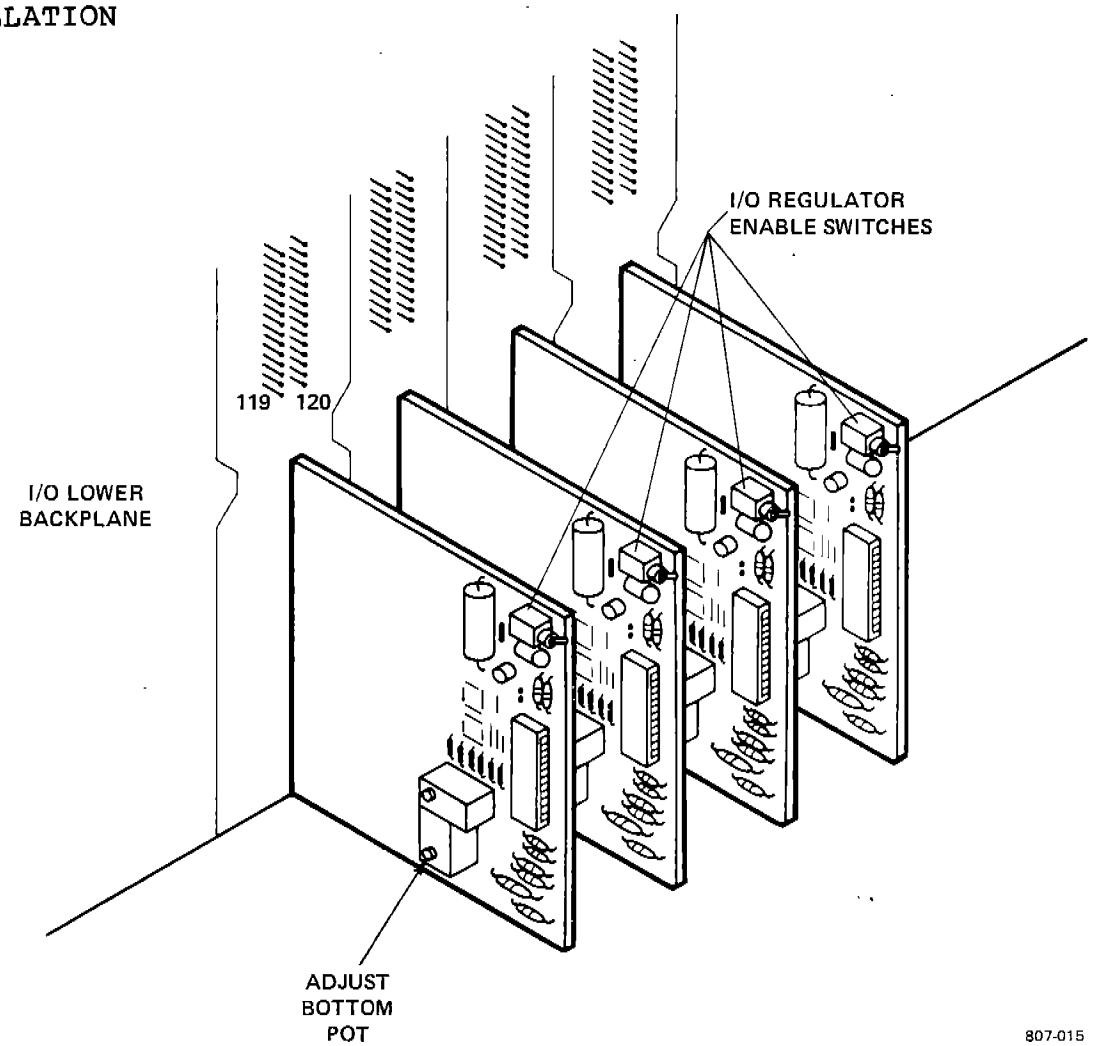


Figure 4-2 I/O Regulator Assembly Switch Location

4.2 INSTALLING NEW POWER SUPPLIES

The installation of processor power supplies, I/O power supplies, and battery supplies is subject to various conventions and restrictions. The following paragraphs describe the procedures and restrictions for installing the power supplies.

4.2.1 Processor Power Supply Installation

The processor power supply is always housed in the same cabinet and directly below the processing unit. This ensures an orderly configuration and allows the cables that connect the supply to the power buses to be kept short, reducing power losses. Mounting racks for four power supplies in the processor cabinet are located just above the AC power module. Figure 4-3 shows the placement of the power supplies in the processor cabinet (view is from the rear of the cabinet).

Normally, the processor power supplies for a new system are installed at the factory and require no installation at the customer site except voltage checks. When add-on processors are installed in a cabinet, however, the power supplies for those processors must also be installed. To install a new processor power supply, refer to Figure 4-3 and perform the following steps:

a. Place the processor power supply on the rack in the processor cabinet and slide the supply into the cabinet, ensuring that no cables or wires are resting on the rack.

b. Connect the appropriate AC cable from the AC power module to J3 on the back of the power supply and connect the DC cables to J1 and J2.

c. Switch on the AC and DC switches on the front of the processor power supply.

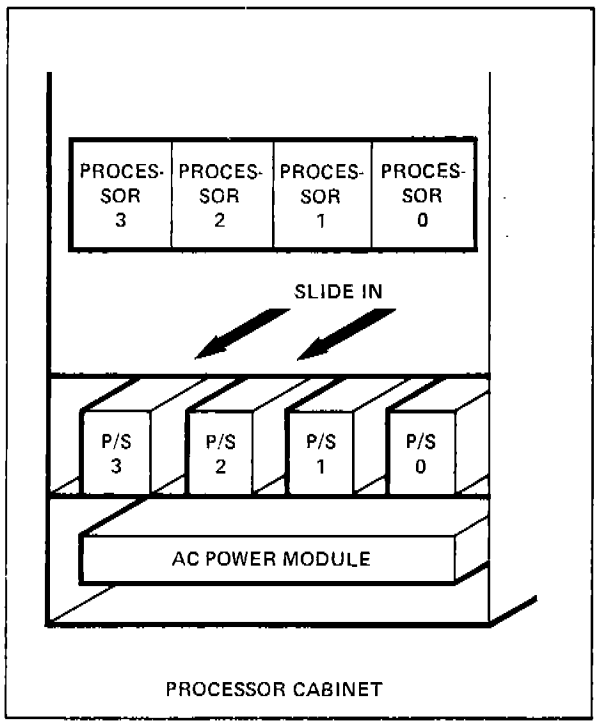
d. Check voltages and adjust, if necessary, to within the limits specified in Table 4.1. Refer to Figure 4-3 for adjustment location.

NOTE

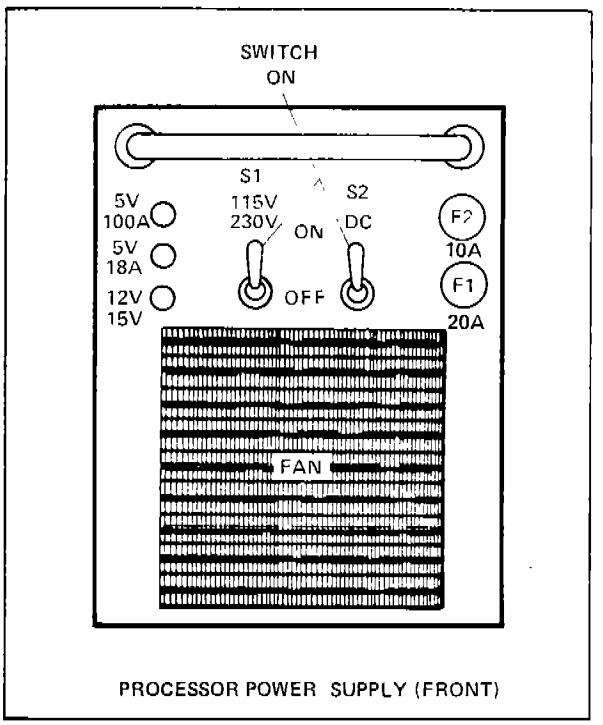
All measurements should be taken at the vertical power bus to allow for line drops.

Table 4.1 Processor Power Supply Voltages

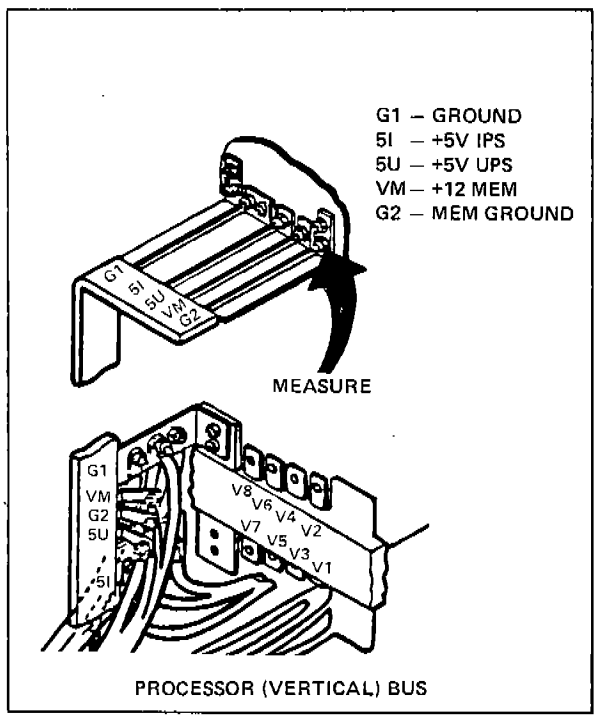
SUPPLY	BUS TABS	ADJUSTMENT LIMITS
5V/100A	5I/G1	5.05 ±.01 VDC
5V/18A	5U/G2	5.05 ±.01 VDC
12V/15V	VM/G2	12.05 ±.01 VDC



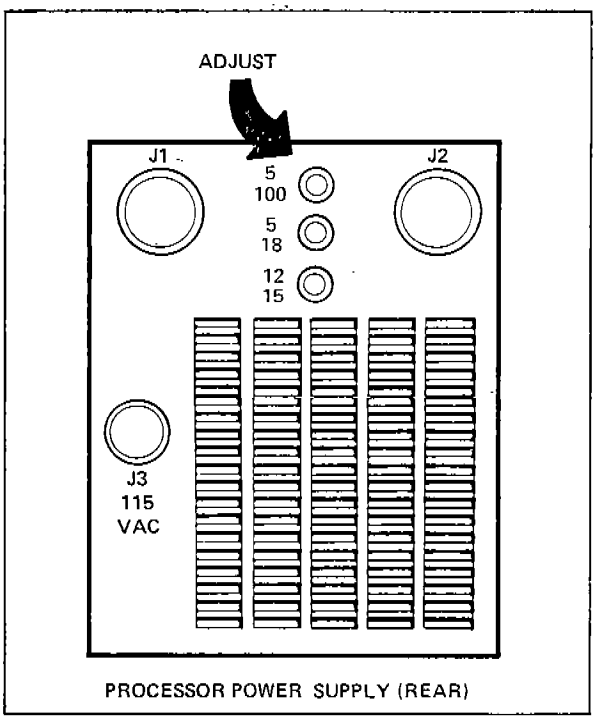
SLIDE THE PROCESSOR POWER SUPPLY INTO THE CABINET AND CONNECT CABLES TO J1, J2 AND J3.



SWITCH AC AND DC POWER ON.



MEASURE DC VOLTAGES ON THE VERTICAL BUS (5I AND 5U = 5.05± 0.01 V AND VM = 12.05± 0.01 V).



ADJUST VOLTAGES ON THE REAR OF THE PROCESSOR POWER SUPPLY, IF NECESSARY.

807-016

Figure 4-3 Processor Power Supply Installation

4.2.2 I/O-Only Power Supply Installation

An I/O-only power supply can be installed in a processor cabinet if space is available, in an I/O-only cabinet, in a patch panel cabinet, in a system expansion cabinet, or in a magnetic tape drive cabinet.

Magnetic tape cabinets, 7105 patch panel cabinets, and 7107 system expansion cabinets can contain up to two levels of mounting racks to accommodate up to four I/O-only power supplies and four battery supplies. I/O-only power supplies are normally mounted on the lower rack to facilitate cable routing. If only I/O-only supplies are to be used, up to six supplies may be installed in a cabinet.

NOTE

The 5106 Magnetic Tape Drive cabinet does not have provisions to store I/O-only power supplies.

7121 I/O-only cabinets contain only one mounting rack and can accommodate up to four I/O-only power supplies.

NOTE

If I/O power supplies are to be mounted in a a patch panel cabinet, AC power distribution module and power supply racks must be specified for the cabinet at the time of order. All I/O power supplies must be mounted in the cabinet that they service or in a directly adjacent cabinet.

I/O voltage sense and 5 volt auxiliary cables are used to connect J1 and J2 of the I/O-only power supply to the vertical and horizontal bus bars. Refer to Table 4.2 for cable part numbers.

Table 4.2 I/O-Only Power Supply Cables

PART NUMBER	DESCRIPTION
51930	J1 I/O Voltage Sense Cable, 19 inches
51931	J2 5V Power Auxiliary Cable, 21 inches

To install a new I/O-only power supply, refer to Figure 4-4 and perform the following steps:

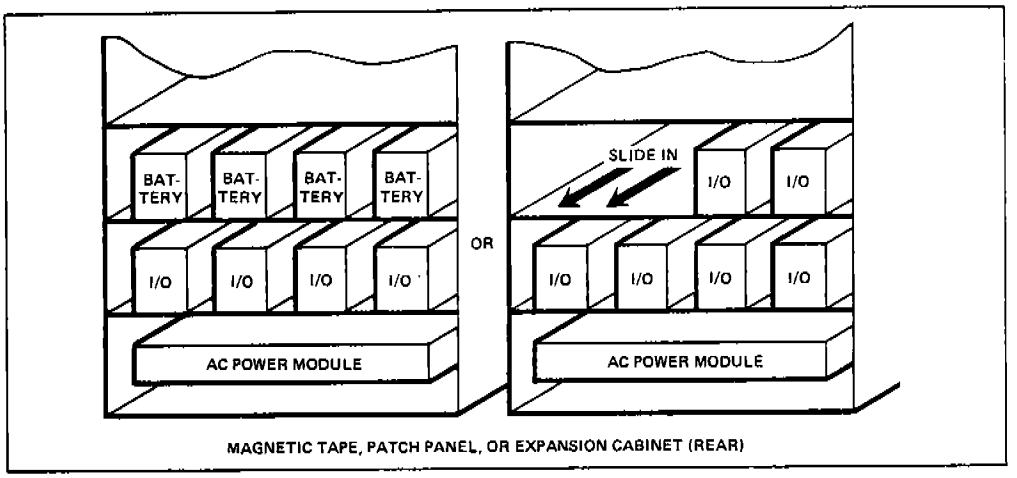
a. Place the I/O-only power supply on the rack in the cabinet and slide the supply into the cabinet, ensuring that no cables or wires are resting on the rack.

b. Connect the appropriate AC cable from the AC power module to J3 on the back of the power supply and connect the DC cables to J1 and J2.

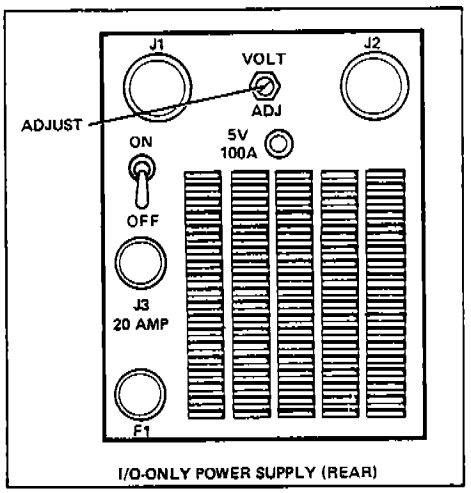
c. Switch on the AC switch on the back of the I/O-only power supply.

d. Check voltage at the appropriate V-tab on the horizontal bus bar and adjust, if necessary, to 5.7 ±.10 volts. Refer to Figure 4-4 for adjustment location.

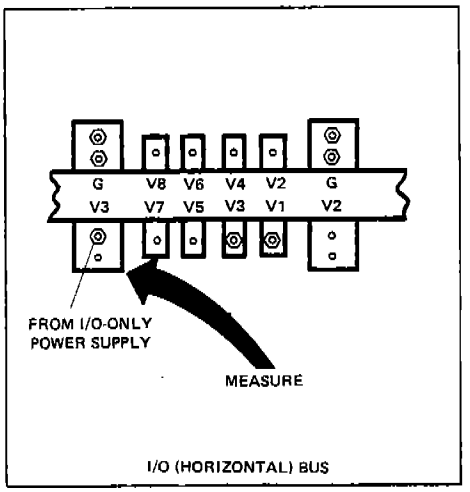
e. Measure the output of the I/O power regulators between pin 120 ("+" lead) and pin 108 (ground lead) on the I/O lower backplane. The output should be 5.05 ±.02 volts. If adjustment is necessary, adjust the bottom pot on the I/O regulator card. (The top pot is for current limit and is to be adjusted at the factory only.)



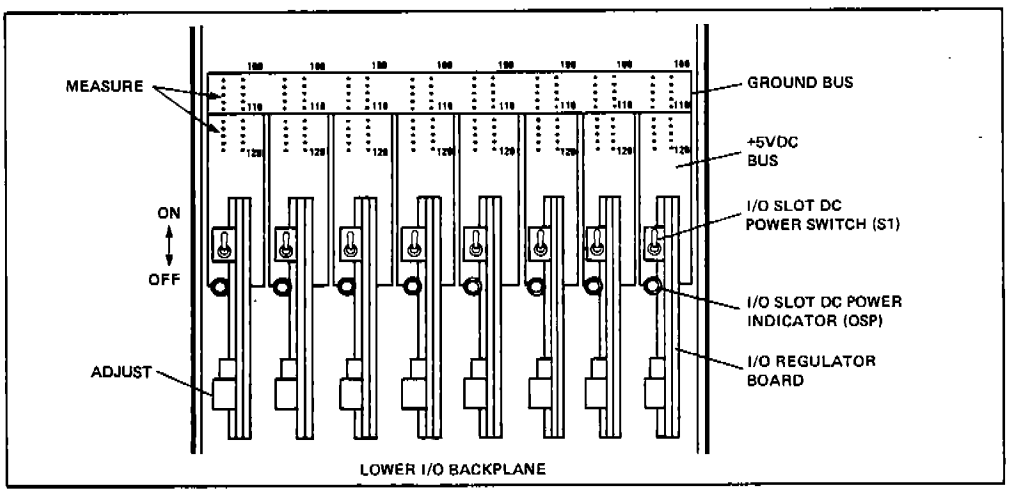
SLIDE THE I/O-ONLY POWER SUPPLY INTO THE CABINET.



CONNECT CABLES, SWITCH POWER ON, AND ADJUST VOLTAGE, IF NECESSARY,



WHILE MEASURING AT V-TAB ON THE I/O BUS FOR 5.7± 0.10 VOLTS.



MEASURE AT P/N 120 OF THE I/O LOWER BACKPLANE FOR 5.05 ± .02 VOLTS AND ADJUST LOWER POT ON THE I/O REGULATOR BOARD, IF NECESSARY.

807-017

Figure 4-4 I/O-Only Power Supply Installation

4.2.3 Battery Supply Installation

Battery supplies can be mounted in magnetic tape cabinets, system expansion cabinets, or patch panel cabinets.

NOTE

> If battery supplies are to be mounted in a patch panel cabinet, a magnetic tape AC power distribution module and power supply racks must be specified for the cabinet at the time of order.

The battery supplies back up the processor power supplies through the magnetic tape and processor AC power modules. Figure 4-5 shows the AC power distribution to and from the battery supplies. A cabinet with a magnetic tape AC power distribution module can house up to eight battery supplies, providing backup power to up to two processor cabinets. Battery supply DC power cables of various lengths are available to connect J2 on the magnetic tape AC power module to J1 on the processor AC power module. Table 4.3 describes the cable lengths and part numbers.

Table 4.3 Battery Supply DC Power Cables

PART NUMBER	DESCRIPTION
52284	UPS DC Power Cable, 42 inches
52575	UPS DC Power Cable, 126 inches
52576	UPS DC Power Cable, 164 inches
52577	UPS DC Power Cable, 205 inches

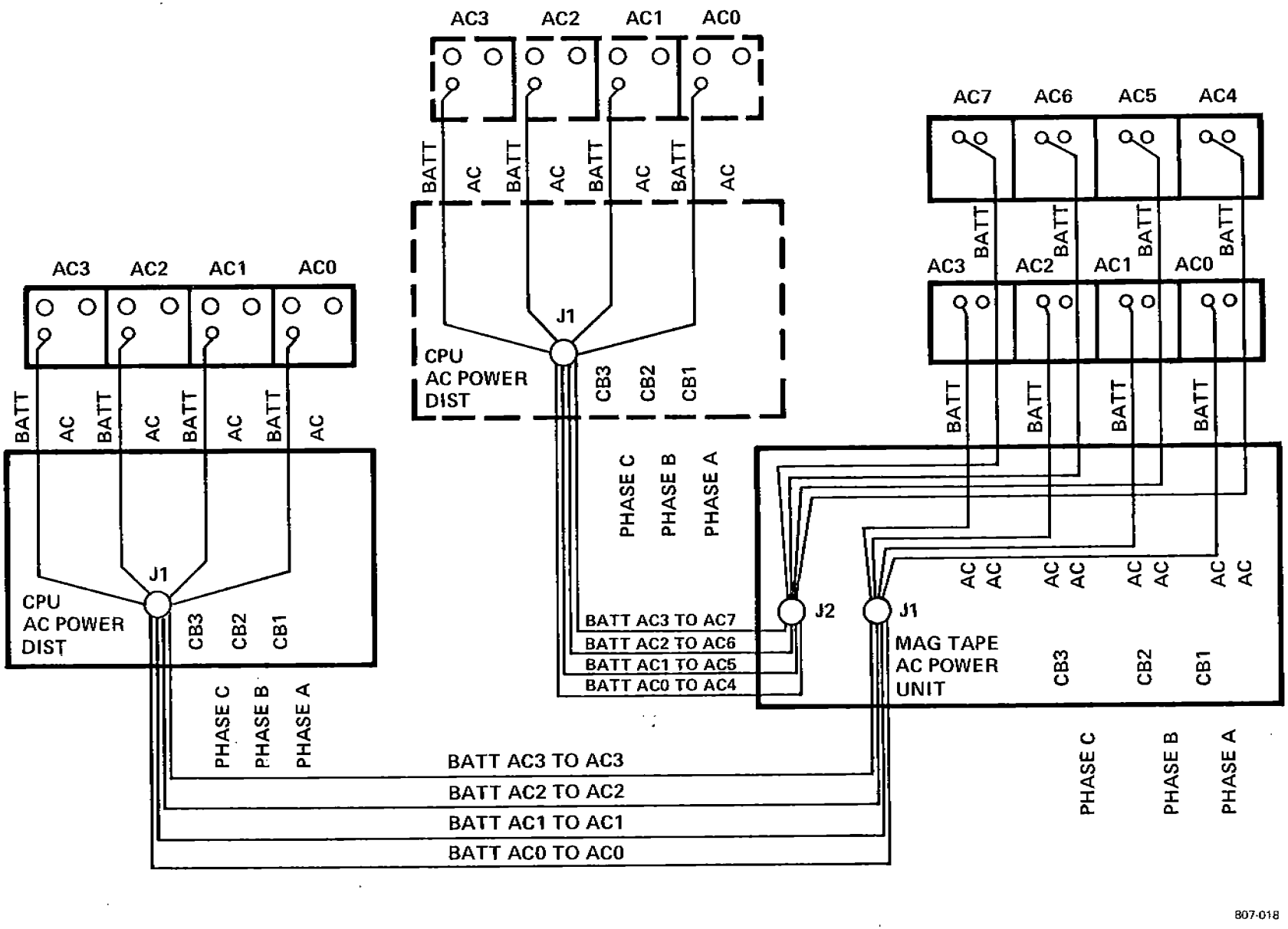


Figure 4-5 Battery Supply AC Distribution

Battery supplies are shipped with the battery packs and battery cases packed separately. The supplies must be assembled during installation. If shipped with a system, the battery cases are mounted in a cabinet and the battery packs are packed in a box. To assemble the battery supplies, refer to Figure 4-6 and perform the following steps:

a. Remove the screws from the battery case and open the cover.

b. Lower the battery pack into the case and snap the plastic shield into place.

c. Connect leads J5 and J6 to the connectors on the PCB in the battery case.

d. Replace the cover and secure with the screws.

To install the UPS battery supply in a cabinet, refer to Figure 4-7 and perform the following steps:

a. Place the UPS battery supply from the front on the rack and slide the supply back into the cabinet, ensuring that no cables or wires are resting on the rack.

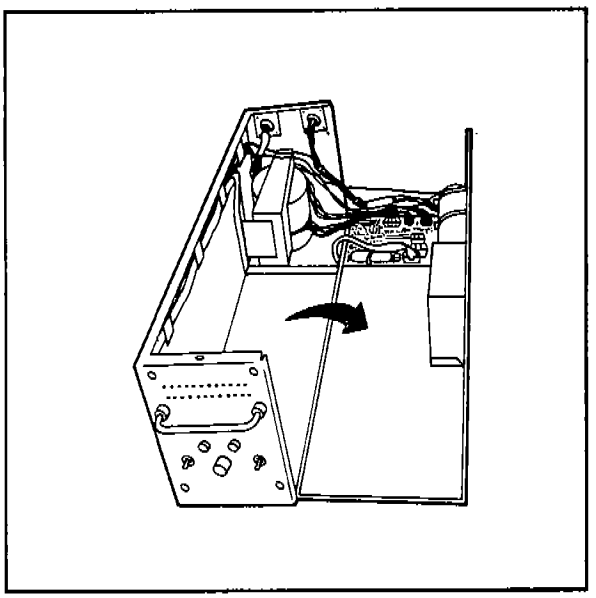
NOTE

In a magnetic tape cabinet, if both I/O power supplies and battery supplies are used, the battery supplies are normally mounted on the upper rack to facilitate cable routing.

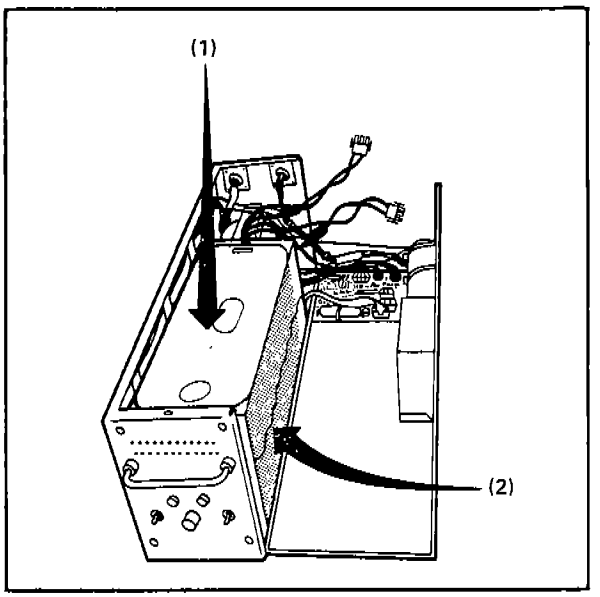
b. Connect cables to J1 and J2 on the rear of the supply.

c. Switch on the power switch on the front of the UPS supply.

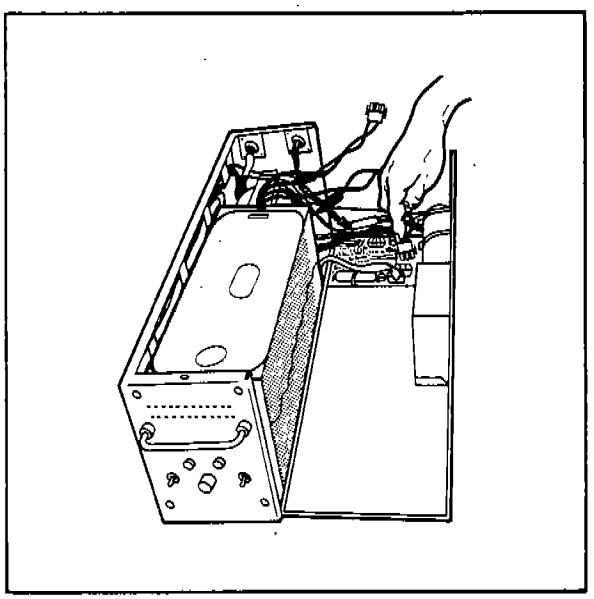
d. Verify proper operation of the UPS battery supply by turning off the AC power switch on the processor supply (supported by the replacement UPS supply) and checking for the proper memory voltages on the vertical bus (refer to Table 4.1 for memory voltage limits).



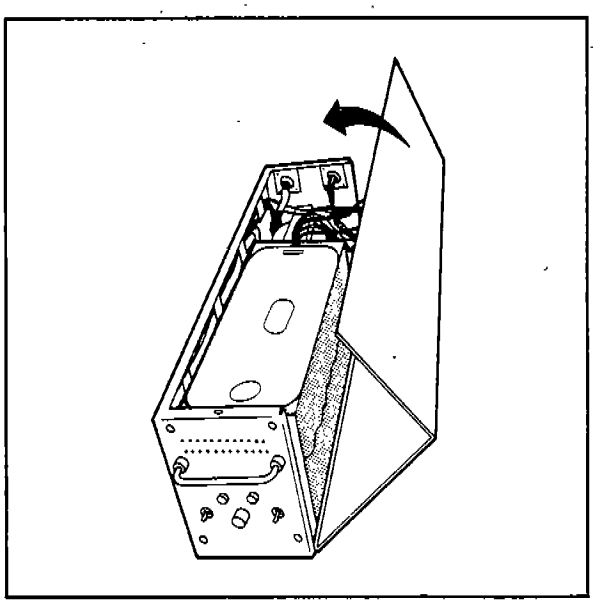
REMOVE SCREWS AND OPEN COVER OF BATTERY PACK CASE.



(1) LOWER BATTERY PACK INTO CASE AND
(2) SNAP PLASTIC SHIELD INTO PLACE.



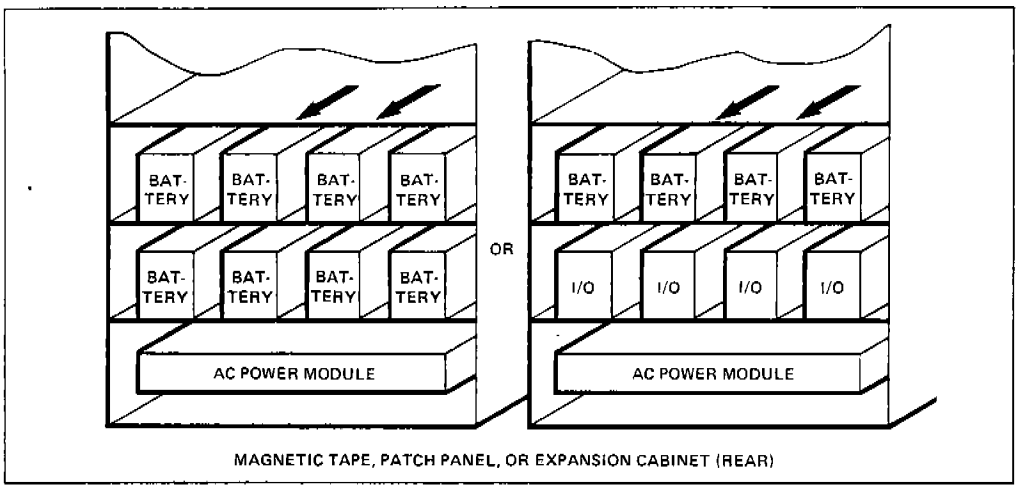
CONNECT LEADS TO J5 AND J6 ON PCB.



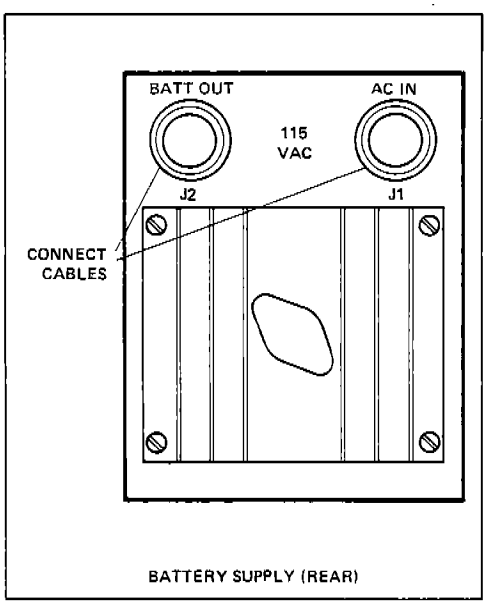
REPLACE COVER AND SECURE WITH SCREWS.

807-026*

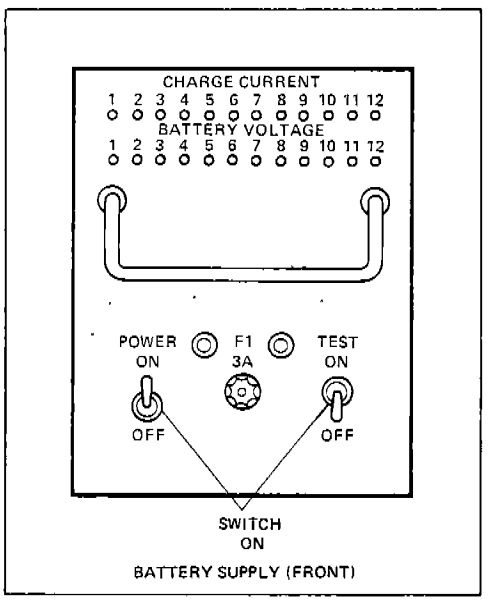
Figure 4-6 Battery Supply Assembly



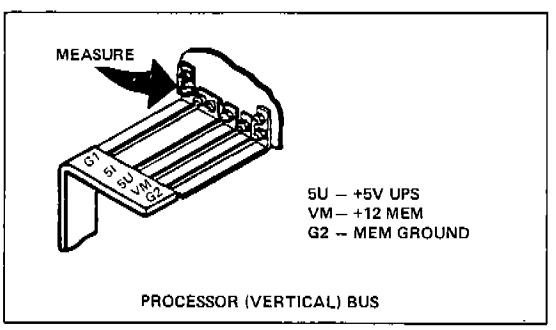
SLIDE THE BATTERY SUPPLY INTO THE CABINET.



CONNECT CABLES TO J1 AND J2.



SWITCH POWER ON.



VERIFY MEMORY VOLTAGES ON THE PROCESSOR BUS WITH PROCESSOR SUPPLY POWER SWITCHED OFF.

807-019

Figure 4-7. Battery Supply Installation

4.3 DC POWER LOAD CALCULATION

In order to ensure problem-free operation of a NonStop II or NonStop TXP processing system and to calculate the number of I/O power supplies needed, the amount of current drawn for each power supply must be calculated. This is accomplished by calculating the total current each V-tab is supplying to the I/O card cage and the IPB/PMI regulators. Since the regulator gets half of its power from two different V-tabs, the total of each V-tab is divided by two. This gives the actual current drawn from each supply by the controllers and the IPB/PMI regulators. If the power supply is a processor supply (even V-tabs), 60 amps must be added to the actual current to get the total current drawn from each supply (60 amps is the amount that each processor draws).

Use the following equations to calculate the actual and total current:

$$TV \div 2 = AV$$

$$AV + PA = TA$$

Where:

TV = Total V-tab amps.

AV = Actual V-tab amps per supply.

PA = Procesor amps (60).

TA = Total power supply amps.

This equation gives the amps per supply for normal (no failure) operation.

The following is an example of a DC load calculation:

For:

SLOT NUMBER	V-TABS	AMPS
1	2/1	9.2
2	2/1	6.2
3	2/1	8.0
5	2/3	8.2
6	2/3	6.8
7	4/3	8.4
8	4/3	8.4
9	4/3	8.0
10	4/1	8.0
11	4/1	8.0
12	4/1	8.0
17	6/3	8.2
18	6/3	6.8
19	1/3	6.2
IPB/PMI	2/4	5.0

Actual V-tab current equals:

V-TAB	TV AMPS	DIVIDED BY	AV AMPS
1	53.6	2	26.8
2	43.4	2	21.7
3	61.0	2	30.5
4	53.8	2	26.9
6	15.0	2	7.5

Total power supply current equals:

V-TAB	AV AMPS	PLUS PA	TA AMPS
2	21.7	60	81.7
4	26.9	60	86.9
6	7.5	60	67.5

To find the total amps for each supply during any single supply failure, add half the total V-tab amps for each controller slot connected to the failing supply to the total amps (TA) of the backup supplies.

For example:

In the previous example, if the supply connected to V-tab 1 fails, V-2 supply equals 93.4 amps, V-3 supply equals 33.6 amps, V-4 supply equals 98.9 amps, and V-6 stays at 67.5 amps (V-6 is not a backup for V-1).

4.4 PHASE LOAD BALANCING

Current loading in the mainframe must be evenly distributed over the three phases to ensure the proper load balance of the overall system. The following paragraphs describe the requirements for phase load balancing in 60 Hz and 50 Hz systems. Also included are reproducible worksheets to be filled out for each cabinet or configuration.

4.4.1 60 Hz Phase Load Balancing

The maximum current load allowed on each phase for a 60 Hz system is 30 amps. Table 4.4 lists the maximum current requirements for supplies, tape drives, and cooling fans that load the AC phases in a 60 Hz system.

Table 4.4 Maximum Current Requirements (60 Hz)

DEVICE TYPE	MAXIMUM CURRENT
7900 Processor Power Supply	14 Amps
7301 I/O-Only Power Supply	11.5 Amps
7303 UPS Battery Supply (60 Hz)	2 Amps
5103 Magnetic Tape Drive	3.6 Amps
5104 Magnetic Tape Drive	6.5 Amps
5109 Magnetic Tape Drive	2.7 Amps
Plenum Cooling Fan	.5 Amps

Figures 4-8 and 4-9 are examples of the AC power phase assignment worksheet for 60 Hz processor and magnetic tape power distribution modules. Pages 4-21/22 and 4-23/24 are reproducible copies of the 60 Hz worksheets that can be removed from the manual and copied for use in determining the phase balancing configuration for each cabinet.

AC POWER ASSIGNMENTS – 60 HZ CPU OR I/O CABINET
(STANDARD PHASE SEQUENCE)

EXAMPLE	–	EXAMPLE
CONFIGURED BY	DATE	CABINET NUMBER
–	–	–
CUSTOMER	SYSTEM NUMBER	REV.

PHASE/CONNECTOR ASSIGNMENTS (REAR VIEW)

CABINET NUMBER 3

CABINET TYPE:
CPU ☒
I/O ☐

CPU P/S

AC3 phA	AC2 phB	AC1 phC	AC0 phA

MAGNETIC TAPE OUTLETS: P8-1 = phA = CB1 & CB4; P8-2 = phB = CB2 & CB5
SERVICE OUTLETS: phC = CB3, CB6 (FOR TEST EQUIPMENT ONLY)

CONFIGURABLE ITEM ASSIGNMENTS

PHASE A		PHASE B		PHASE C	
ITEM	MAX AMPS	ITEM	MAX AMPS	ITEM	MAX AMPS
P8-1		P8-2 5103 MT	3.6	AC1 CPU P/S	14
AC0 CPU P/S	14	AC2 CPU P/S	14		
AC3 CPU P/S	14				
phA TOTAL = 28 AMPS		phB TOTAL = 17.6 AMPS		phC TOTAL = 14 AMPS	

MAXIMUM CURRENT ALLOWED ON ANY PHASE = 30 AMPS.
BALANCE TO MINIMIZE LOADING DIFFERENCES BETWEEN PHASES.

807-028

Figure 4-8 60 Hz Processor PDM Phase Worksheet Example

AC POWER ASSIGNMENTS – 60 HZ MAG TAPE, EXPANSION OR PATCH PANEL CABINET (STANDARD PHASE SEQUENCE)

EXAMPLE	–	EXAMPLE
CONFIGURED BY	DATE	CABINET NUMBER
–	–	–
CUSTOMER	SYSTEM NUMBER	REV.

PHASE/CONNECTOR ASSIGNMENTS (REAR VIEW)

CABINET NUMBER 2

CABINET TYPE:
- EXPANSION ☐
- PATCH PANEL ☐
- MAG TAPE ☒

UPS

AC7 phB J2-UPS	AC6 phC J2-UPS	AC5 phB J2-UPS	AC4 phC J2-UPS
AC3 phA J1-UPS	AC2 phB J1-UPS	AC1 phC J1-UPS	AC0 phA J1-UPS

I/O P/S

MAGNETIC TAPE OUTLETS: P8-1 = phA = CB1 & CB4; P8-2 = phB = CB2 & CB5
SERVICE OUTLETS: phC = CB3, CB6 (FOR TEST EQUIPMENT ONLY)

CONFIGURABLE ITEM ASSIGNMENTS

PHASE A		PHASE B		PHASE C	
ITEM	MAX AMPS	ITEM	MAX AMPS	ITEM	MAX AMPS
P8-1		P8-2 5109 MT	2.7	AC1 I/O P/S	11.5
AC0 I/O P/S	11.5	AC2 I/O P/S	11.5	AC4 UPS	1.2
AC3 I/O P/S	11.5	AC5 UPS	1.2	AC6 UPS	1.2
		AC7 UPS	1.2		
phA TOTAL = 23 AMPS		phB TOTAL = 16.6 AMPS		phC TOTAL = 14.9 AMPS	

MAXIMUM CURRENT ALLOWED ON ANY PHASE = 30 AMPS.
BALANCE TO MINIMIZE LOADING DIFFERENCES BETWEEN PHASES.

807-029

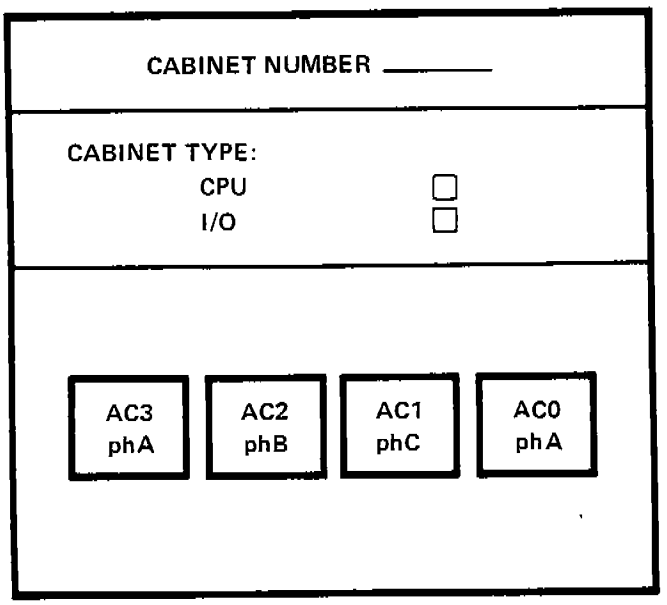
Figure 4-9 60 Hz Magnetic Tape PDM Phase Worksheet Example

AC POWER ASSIGNMENTS – 60 HZ CPU OR I/O CABINET
(STANDARD PHASE SEQUENCE)

CONFIGURED BY _____ DATE _____ CABINET NUMBER _____

CUSTOMER _____ SYSTEM NUMBER _____ REV. _____

PHASE/CONNECTOR ASSIGNMENTS (REAR VIEW)



MAGNETIC TAPE OUTLETS: P8-1 = phA = CB1 & CB4; P8-2 = phB = CB2 & CB5
SERVICE OUTLETS: phC = CB3, CB6 (FOR TEST EQUIPMENT ONLY)

CONFIGURABLE ITEM ASSIGNMENTS

PHASE A		PHASE B		PHASE C	
ITEM	MAX AMPS	ITEM	MAX AMPS	ITEM	MAX AMPS
P8-1 AC0 AC3		P8-2 AC2		AC1	
phA TOTAL = ____ AMPS		phB TOTAL = ____ AMPS		phC TOTAL = ____ AMPS	

MAXIMUM CURRENT ALLOWED ON ANY PHASE = 30 AMPS.
BALANCE TO MINIMIZE LOADING DIFFERENCES BETWEEN PHASES.

807-030

AC POWER ASSIGNMENTS – 60 HZ MAG TAPE, EXPANSION OR PATCH PANEL CABINET (STANDARD PHASE SEQUENCE)

CONFIGURED BY _____ DATE _____ CABINET NUMBER _____

CUSTOMER _____ SYSTEM NUMBER _____ REV. _____

PHASE/CONNECTOR ASSIGNMENTS (REAR VIEW)

CABINET NUMBER _____

CABINET TYPE:

- EXPANSION ☐
- PATCH PANEL ☐
- MAG TAPE ☐

AC7 phB J2-UPS	AC6 phC J2-UPS	AC5 phB J2-UPS	AC4 phC J2-UPS
AC3 phA J1-UPS	AC2 phB J1-UPS	AC1 phC J1-UPS	AC0 phA J1-UPS

MAGNETIC TAPE OUTLETS: P8-1 = phA = CB1 & CB4; P8-2 = phB = CB2 & CB5
SERVICE OUTLETS: phC = CB3, CB6 (FOR TEST EQUIPMENT ONLY)

CONFIGURABLE ITEM ASSIGNMENTS

PHASE A		PHASE B		PHASE C	
ITEM	MAX AMPS	ITEM	MAX AMPS	ITEM	MAX AMPS
P8-1 AC0 AC3		P8-2 AC2 AC5 AC7		AC1 AC4 AC6	
phA TOTAL = ____ AMPS		phB TOTAL = ____ AMPS		phC TOTAL = ____ AMPS	

MAXIMUM CURRENT ALLOWED ON ANY PHASE = 30 AMPS.
BALANCE TO MINIMIZE LOADING DIFFERENCES BETWEEN PHASES.

807-031

4.4.2 50 Hz Phase Load Balancing

The maximum current load allowed on each phase for a 50 Hz system is 22.7 amps. Table 4.5 lists the maximum current requirements for supplies, tape drives, and cooling fans that load the AC phases in a 50 Hz system.

Table 4.5 Maximum Current Requirements (50 Hz)

DEVICE TYPE	MAXIMUM CURRENT
7900 Processor Power Supply	7 Amps
7301 I/O-Only Power Supply	6 Amps
7303A UPS Battery Supply (50 Hz)	.6 Amps
5103 Magnetic Tape Drive	2 Amps
5104 Magnetic Tape Drive	3.4 Amps
5109 Magnetic Tape Drive	1.5 Amps
Plenum Cooling Fan	.25 Amps

For 50 Hz systems the phase assignments in processor cabinets are determined by the AC power cable used to interconnect the processor cabinet power distribution module to the isolation transformers located in the magnetic tape or expansion cabinet. The short power cables are 80 inches long (sufficient to connect the isolation transformers to a processor power distribution module to an adjacent cabinet). The long cables are 142 inches long in order to connect to the second cabinet down the line from a set of isolation transformers. Pages 4-27/28 and 4-29/30 are reproducible copies of the 50 Hz worksheets that can be removed from the manual and copied for use in determining the phase balancing configuration for each cabinet.

AC POWER ASSIGNMENTS – 50 HZ, 1 OR 2 CABINET CONFIGURATIONS (STANDARD PHASE SEQUENCE)

CONFIGURED BY _____ DATE _____ CABINET NUMBER _____

CUSTOMER _____ SYSTEM NUMBER _____ REV. _____

PHASE/CONNECTOR ASSIGNMENTS (REAR VIEW)

CABINET "A", NO. _____

CABINET TYPE:
- CPU ☐
- I/O ☐
- NONE ☐

AC POWER CABLE:
- SHORT (80") – 52711*
- LONG (142") – 45342*

AC3 phA	AC2 phB	AC1 phC	AC0 phA

CABINET "B", NO. _____

CABINET TYPE:
- EXPANSION ☐
- PATCH PANEL ☐
- MAG TAPE ☐

AC7 phB J1-UPS	AC6 phC J1-UPS	AC5 phB J1-UPS	AC4 phC J1-UPS
AC3 phA J2-UPS	AC2 phB J2-UPS	AC1 phC J2-UPS	AC0 phA J2-UPS

MAGNETIC TAPE OUTLETS: P8-1 = phA = CB1 & CB4; P8-2 = phB = CB2 & CB5
SERVICE OUTLETS: phC = CB3, CB6 (FOR TEST EQUIPMENT ONLY)

CONFIGURABLE ITEM ASSIGNMENTS

PHASE A		PHASE B		PHASE C	
ITEM	MAX AMPS	ITEM	MAX AMPS	ITEM	MAX AMPS
A – AC0 A – AC3 A – P8-1 B – AC0 B – AC3 B – P8-1		A – AC2 A – P8-2 B – AC2 B – AC5 B – AC7 B – P8-2		A – AC1 B – AC1 B – AC4 B – AC6	
phA TOTAL = ____ AMPS		phB TOTAL = ____ AMPS		phC TOTAL = ____ AMPS	

MAXIMUM CURRENT ALLOWED ON ANY PHASE = 22.7 AMPS.
BALANCE TO MINIMIZE LOADING DIFFERENCES BETWEEN PHASES.

* Tabulated Drawing Number 49048

807-032

AC POWER ASSIGNMENTS – 50 HZ, 1 OR 2 CABINET CONFIGURATIONS (ROTATED PHASE SEQUENCE)

CONFIGURED BY _____ DATE _____ CABINET NUMBER _____

CUSTOMER _____ SYSTEM NUMBER _____ REV. _____

PHASE/CONNECTOR ASSIGNMENTS (REAR VIEW)

CABINET "A", NO. _____

CABINET TYPE:
- CPU ☐
- I/O ☐
- NONE ☐

AC POWER CABLE:
- SHORT (80") – 46000*
- LONG (142") – 46019*

AC3 phB	AC2 phC	AC1 phA	AC0 phB

CABINET "B", NO. _____

CABINET TYPE:
- EXPANSION ☐
- PATCH PANEL ☐
- MAG TAPE ☐

AC7 phB J1-UPS	AC6 phC J1-UPS	AC5 phB J1-UPS	AC4 phC J1-UPS
AC3 phA J2-UPS	AC2 phB J2-UPS	AC1 phC J2-UPS	AC0 phA J2-UPS

CABINET "A": phA = CB3 & CB6; phB = CB1, CB4 & P8-1; phC = CB2, CB5 & P8-2
CABINET "B": phA = CB1, CB4 & P8-1; phB = CB2, CB5 & P8-2; phC = CB3 & CB6
MAGNETIC TAPE OUTLETS: P8-1 & P8-2
SERVICE OUTLETS: P7 (FOR TEST EQUIPMENT ONLY)

CONFIGURABLE ITEM ASSIGNMENTS

PHASE A		PHASE B		PHASE C	
ITEM	MAX AMPS	ITEM	MAX AMPS	ITEM	MAX AMPS
A – AC1 B – AC0 B – AC3 B – P8-1		A – AC0 A – AC3 A – P8-1 B – AC2 B – AC5 B – AC7 B – P8-2		A – AC2 A – P8-2 B – AC1 B – AC4 B – AC6	
phA TOTAL = ____ AMPS		phB TOTAL = ____ AMPS		phC TOTAL = ____ AMPS	

MAXIMUM CURRENT ALLOWED ON ANY PHASE = 22.7 AMPS.
BALANCE TO MINIMIZE LOADING DIFFERENCES BETWEEN PHASES.

* Tabulated Drawing Number 46029

807-033

SECTION 5
CORRECTIVE MAINTENANCE

5.0 CORRECTIVE MAINTENANCE

Field repair of the power subsystem is normally accomplished by replacing the defective unit. The only exception is field replacement of some fuses, cables, and batteries. Refer to Table 8.1 for a list of field replaceable spare parts.

5.1 TROUBLESHOOTING

The following paragraphs describe troubleshooting suggestions for the power subsystem supplies.

5.1.1 IPS DC Power Supply Troubleshooting

Table 5.1 describes the troubleshooting procedure for the IPS DC power supplies (processor or I/O-only supplies).

Table 5.1 IPS Power Supply Troubleshooting Chart

INDICATION	POSSIBLE PROBLEM
5/100 LED not lit	LED expired No 5/100 output
No 5/100 output	No AC power; check CB1-3 on AC module; check F1 Loss of +300 V to inverter; check fuse F1 on 52770 board Bad output cable; replace J2 Overvoltage crowbar fired; check sense lines or bad supply
5/100 LED flashing (1 Hz rate)	Excessive load (PS in current limit); recalculate load Power supply current limits too early; bad supply

Table 5.1 IPS Power Supply Troubleshooting Chart (Cont'd)

INDICATION	POSSIBLE PROBLEM
5/100 output too low	Adjust 5/100 potentiometer Sense lines disconnected or loose
5/100 output too high	Adjust 5/100 potentiometer
Periodical loss of 5/100 output	Fan bad; thermal switch on heat sink open Overcurrent condition being detected by power supply
No 5/18; 5/100 OK	Fuse f2 (52770 board) open Overvoltage crowbar fired; turn PS AC and DC switches OFF and ON to reset crowbar Excessive load; PS in current limit Bad output cable; replace J2 PS current limit too early; bad supply
5/18 output too low	Sense lines disconnected or loose Adjust 5/18 potentiometer
5/18 output too high	Adjust 5/18 potentiometer
No 12/15 output other outputs OK	Excessive load; remove J2 Overvoltage crowbar fired; adjust 12/15 potentiometer below 13 volts to recover Power supply in current limit; check sense lines

5.1.2 UPS Battery Supply Troubleshooting

The following are troubleshooting hints for the UPS battery supply:

a. Field replacement of the UPS control board (51560) is not recommended, because a number of factory adjustments are required.

b. Relay K1 on the UPS control board is set to drop out when battery voltage is below 39 volts, disconnecting the battery from the load to prevent deep discharge. If the battery voltage is between zero volts and 36 volts, the UPS control board is not responding properly to low battery voltage and the battery may not recover from deep discharge. Replacement of the complete UPS supply is recommended.

c. If the backup time of the UPS supply appears significantly lower than normal, a fuse in one of the two battery pack wires may be open or a battery pack may have discharged past the point that the internal battery charger can recharge it. Check the fuse; if the fuse is not open, replace the defective battery pack.

5.2 REMOVAL AND REPLACEMENT PROCEDURES

The following paragraphs describe the removal and replacement procedures for the various assemblies that comprise the power subsystem. Included are procedures for removing and replacing the RFI filter, AC distribution module, and IPS and UPS powers supplies. Also included are unpacking and packaging instructions for replacement parts and defective parts, and instructions for completing documentation used in reshipping.

5.2.1 Removal Procedures

Paragraphs 5.2.1.1 through 5.2.1.5 describe the removal procedures for the RFI filter, the AC power distribution module, the plenum diode assemblies, the IPS DC power supplies, and the UPS battery supplies.

5.2.1.1 RFI Filter Removal

To remove the RFI filter from the system cabinet, perform the following steps:

a. Turn off the external AC power source to the system cabinet at the computer room power panel.

b. Disconnect and slide forward any DC power supplies that are covering the RFI filter (refer to paragraph 5.2.1.4 for power supply removal procedure).

c. Remove the screws from the input ("field wiring") end of the RFI filter and remove the cover.

d. Have an electrician disconnect the site AC cable from the RFI filter input.

e. Remove the screws from the top of the AC distribution module cover and remove the cover.

f. Remove the two screws attaching the AC distribution module to the cabinet base and the hold-down screws at each end of the filter.

g. Lift the AC module/RFI filter assembly out of the cabinet.

h. Remove the screws from the output end of the filter and remove the cover.

i. Disconnect the wires attaching the filter to the AC module.

j. Remove the screws that attach the RFI filter to the AC distribution module and remove the RFI filter.

5.2.1.2 AC Distribution Module Removal

To remove the AC distribution module from the system cabinet, perform the following steps:

a. Turn off the external AC power source to the system cabinet at the computer room power panel.

b. Disconnect and slide forward any DC power supplies that are covering the RFI filter (refer to paragraph 5.2.1.4 for power supply removal procedure).

c. Remove the screws from the top of the AC distribution module cover and remove the cover.

d. Detach the wires between the RFI filter and the AC module at the filter and remove the four screws that attach the RFI filter to the AC distribution module.

e. Disconnect the GRN/YEL ground wire from the cabinet frame ground point.

f. Remove the two screws attaching the AC distribution module to the system cabinet.

g. Lift the AC distribution module out of the system cabinet from the rear of the cabinet.

5.2.1.3 Plenum Diode Assembly Removal

To remove the plenum diode assembly from the system cabinet, perform the following steps:

a. Turn off the DC power supply for the defective diode assembly.

b. Disconnect the diode cable assembly from J2 on the CPU power supply and slide the power supply forward so that the plenum diode is accessible (refer to paragraph 5.2.1.4 for power supply removal procedure).

NOTE

Save all hardware for attaching the replacement diode.

c. Remove the power connections to the vertical bus. First remove the three black wires labeled 5, 6, and 7 (attached at G1). Then remove the two long red wires labeled 9 (attached at 5I).

d. Remove the two short red wires labeled 3 and 4 from the horizontal bus.

e. Remove the four screws (two top and two bottom) that hold the assembly in place and remove the assembly.

5.2.1.4 IPS (Processor or I/O-Only) DC Power Supply Removal

To remove the IPS DC power supply from the system cabinet, perform the following steps:

a. Switch off the AC and DC switches for 7900 processor supply or the AC switch for 7301 I/O-only supply. (Switches are located on the front of the 7900 supply and on the rear of the 7301 supply.)

b. Remove the cables from J1, J2, and J3 on the rear of the supply.

c. Slide the IPS power supply forward and remove from the cabinet.

5.2.1.5 UPS Battery Supply Removal

To remove the UPS battery supply from the system cabinet, perform the following steps:

a. Switch off the power switch on the front of the UPS battery supply.

b. Remove the cables from J1 and J2 on the rear of the supply.

c. Slide the UPS battery supply forward and remove from the cabinet.

5.2.2 Unpacking Replacement Units

After receiving a replacement for any unit in the power subsytem, perform the following inspection:

a. Open the shipping container and remove the unit from the packing material. (Save the packing material for reshipping the defective unit.)

b. Inspect the unit to ensure that there is no physical damage.

5.2.3 Replacement Procedures

Paragraphs 5.2.3.1 through 5.2.3.5 describe the replacement procedures for the RFI filter, the AC power distribution module, the plenum diodes, the IPS DC power supplies, and the UPS battery supplies.

5.2.3.1 RFI Filter Replacement

To replace the RFI filter in the system cabinet, perform the following steps:

a. Remove the screws from the ends of the replacement RFI filter and remove the end covers.

b. After the defective RFI filter has been removed (paragraph 5.2.1.1), put the replacement unit in place in front of the AC power distribution module. (The top cover of the AC module should already be removed.)

c. Attach the RFI filter to the AC distribution module using the four screws removed in paragraph 5.2.1.1, step j.

d. Connect the wires from the AC power distribution module to the connectors at the RFI filter output. The wires are labled (FL1N, FL1A, FL1B, etc.) to indicate where they are attached. Refer to Figure 5-1 for wire attachment diagram.

e. Replace the cover at the output end of the filter.

f. Place the AC module/RFI filter assembly in the cabinet.

g. Replace the two screws attaching the AC module to the cabinet base and replace the hold-down screws at both ends of the replacement filter.

h. Have an electrician reconnect the site AC cable to the RFI filter input (as shown in Figure 5-2).

i. Replace the RFI filter input cover and AC module cover.

j. Slide the DC power supplies back into place and reconnect the J1, J2, and J3 cables.

k. Turn on the external AC power to the system cabinet and turn on the AC power switch on the DC supplies.

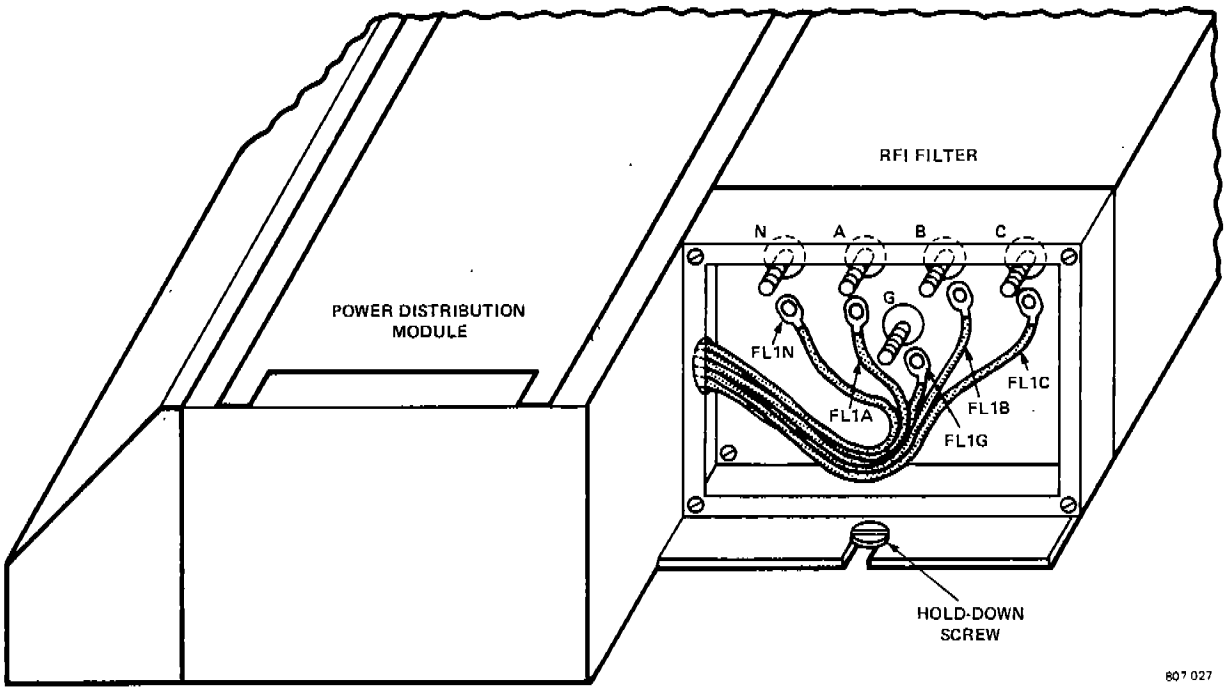


Figure 5-1 RFI Filter to PDM Wire Attachment

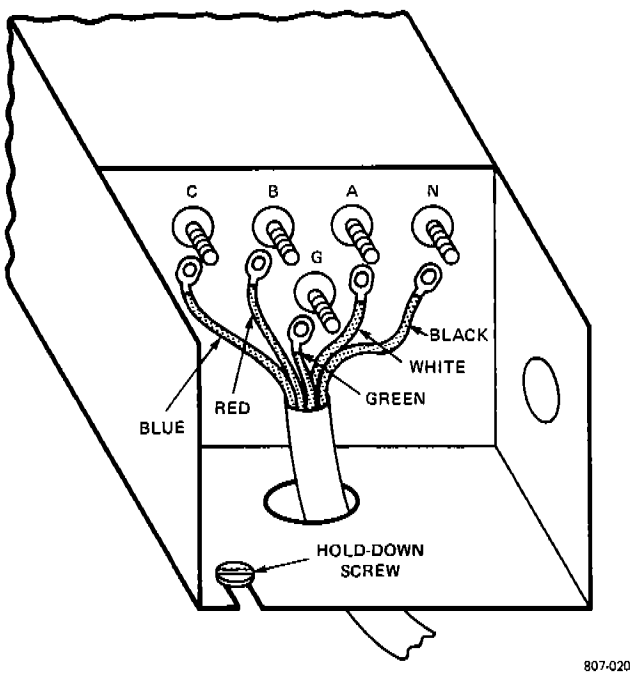


Figure 5-2 RFI Filter to External AC Wire Attachment

5.2.3.2 AC Power Distribution Module Replacement

To replace the AC power distribution module in the system cabinet, perform the following steps:

a. Remove the screws from the top of the replacement AC power distribution module and remove the cover.

b. Set the replacement AC power distribution module in place behind the RFI filter. (The top cover of the RFI filter should already be removed.)

c. Replace the two screws that attach the module to the system cabinet.

d. Attach the RFI filter to the AC distribution module using the four screws removed in paragraph 5.2.1.2, step d.

e. Connect the wires from the AC module to the output connectors of the RFI filter and connect the GRN/YEL ground wire to the frame ground point. Refer to Figure 5-1 for wire attachment diagram.

f. Replace RFI filter cover and AC module cover.

g. Slide the DC power supplies back into place and reconnect the J1, J2, and J3 cables.

h. Turn on the external AC power to the system cabinet and turn on the AC power switch on the DC supplies.

5.2.3.3 Plenum Diode Replacement

To replace the plenum diode assembly in the system cabinet, perform the following steps:

a. Hold the diode assembly in place in the cabinet and replace the the four screws (two top and two bottom) that hold the assembly in place.

b. Connect the two short red wires labeled 3 and 4 to the even-numbered tab on the bottom half of the horizontal bus.

c. Connect the two long red wires labeled 9 to 5I on the vertical bus. Then connect the three black wires labeled 5, 6, and 7 to G1 on the vertical bus.

c. Slide the DC power supply back into place under the diode assembly and reconnect the J2, connector.

d. Turn on the DC power supply.

5.2.3.4 IPS (Processor or I/O-Only) DC Power Supply Replacement

To replace the IPS DC power supply in the system cabinet, perform the following steps:

a. Place the IPS power supply in the system cabinet on the rack and slide the supply back into the cabinet, ensuring that no cables or wires are resting on the rack.

b. Connect cable to J1, J2, and J3 on the back of the supply.

c. Switch on the AC and DC switches on 7900 processor supply or the AC switch on 7301 I/O-only supply. (Switches are located on the front of the 7900 supply and on the rear of the 7301 supply.)

d. Check voltage(s) and adjust if necessary (refer paragraph 4.2 for adjustment procedure).

5.2.3.5 UPS Battery Supply Replacement

To replace the UPS battery supply in the magnetic tape cabinet, perform the following steps:

a. Place the UPS battery supply in the magnetic tape cabinet on the rack and slide the supply back into the cabinet, ensuring that no cables or wires are resting on the rack.

b. Connect cables J1 and J2 on the rear of the supply.

c. Switch on the power switch on the front of the UPS supply.

d. Verify proper operation of the UPS battery supply by turning off the AC power switch on the processor supply (supported by the replacement UPS supply) and checking for the proper memory voltages.

NOTE

The UPS module may need to charge the batteries for up to 15 hours to obtain full charge if the spare was not attached to AC power while in storage.

5.2.4 Packaging Defective Units for Reshipping

After the new unit has been installed, pack the defective unit for shipment, using the packing material from the new unit.

a. Each unit should be packed carefully and reshipped in the same packing material in which the replacement unit was received.

b. More than one unit may be shipped in a large container provided that adequate packing is used to keep them separated.

c. The box must be closed securely with tape. For information concerning shipping companies and their particular requirements refer to the Shipping Guide bulletin (available on request from Tandem Shipping Dept., Cupertino.)

d. To avoid confusion, remove or cover all addressing information used in previous shipping. This includes airport codes or destination stamps.

5.2.5 Documentation Used in Reshipping

When returning a power supply unit to the Tandem repair depot, fill out an Incident Report (IR) Form (99751) and a part Return Tag (99056). Attach the Part Return Tag to the defective unit. Leave the IR and defective controller at the nearest Tandem office.

When returning a unit for repair, report the type of error, the error symptoms, and the conditions under which the error occurred.

SECTION 6
PREVENTIVE MAINTENANCE

6.0 PREVENTIVE MAINTENANCE

All DC power supply voltages should be checked and adjusted, if necessary, during scheduled routine preventive maintenance on all NonStop II and NonStop TXP processing systems. Refer to paragraphs 4.2.1 and 4.2.2 for adjustment procedures and voltage limits.

SECTION 7
SPECIAL TOOLS AND TEST EQUIPMENT

7.0 SPECIAL TOOLS AND TEST EQUIPMENT

In addition to the normal complement of service tools, the special tools listed in Table 7.1 are required for servicing the power subsystem.

Table 7.1 Special Tools and Test Equipment

PART NUMBER	DESCRIPTION
99624	Wire wrap/unwrap tool. *
99526	Digital test meter.

* This tool is only required if an upgrade or other wiring change to the system is being performed.

SECTION 8
RECOMMENDED SPARE PARTS LIST

8.0 RECOMMENDED SPARE PARTS LIST

Table 8.1 describes the recommended spare parts for the power subsystem. Refer to Figure 8-1 for parts location diagram.

Table 8.1 Recommended Spare Parts List

REFERENCE NUMBER	TANDEM PART NUMBER	DESCRIPTION
1	42555	Power Distribution Module, 60 Hz CPU (previously 52308)
2	42556	Power Distribution Module, 60 Hz MT (previously 52307)
3	45984	Power Distribution Module, 50 Hz CPU (previously 52713)
4	45988	Power Distribution Module, 50 Hz MT (previously 52712)
5	45989	AC Power Module, Expansion Cabinet, 50 Hz (previously 57519)
6	53270	7900 Processor Power Supply ASM
7	23349	Fuse, 20 Amp, 250 V (F1)
8	23126	Fuse, 10 Amp, 250 V (F2)
9	52730	7301 I/O-Only P/S ASM (115 V)
10	23349	Fuse, 20 Amp, 250 V (F1)
11	52875	7301A I/O-Only P/S ASM (230 V)
12	23892	Fuse, 12 Amp, 250 V (F1)

Table 8.1 Recommended Spare Parts List (Cont'd)

REFERENCE NUMBER	TANDEM PART NUMBER	DESCRIPTION
13	50276	7303 UPS Battery ASM (115 V)
14	52655	UPS ASM w/o Battery (115 V)
15	25813	Fuse, 3 Amp, 250V (F1)
16	50282	7303A UPS Battery ASM (230 V)
17	52659	UPS ASM w/o Battery (230 V)
18	25813	Fuse, 3 Amp, 250V (F1)
19	51550	Battery Pack (single)
20	24021	Fuse, 8 Amp, 250V
21	59790	Plenum Diode Assembly (previously 45041)
22	42554	RFI Filter Assembly (previously 51700)
23	54600	I/O Regulator Assembly
24	46163	PDM/RFI Filter Assembly, 60 Hz CPU
25	46164	PDM/RFI Filter Assembly, 60 Hz MT

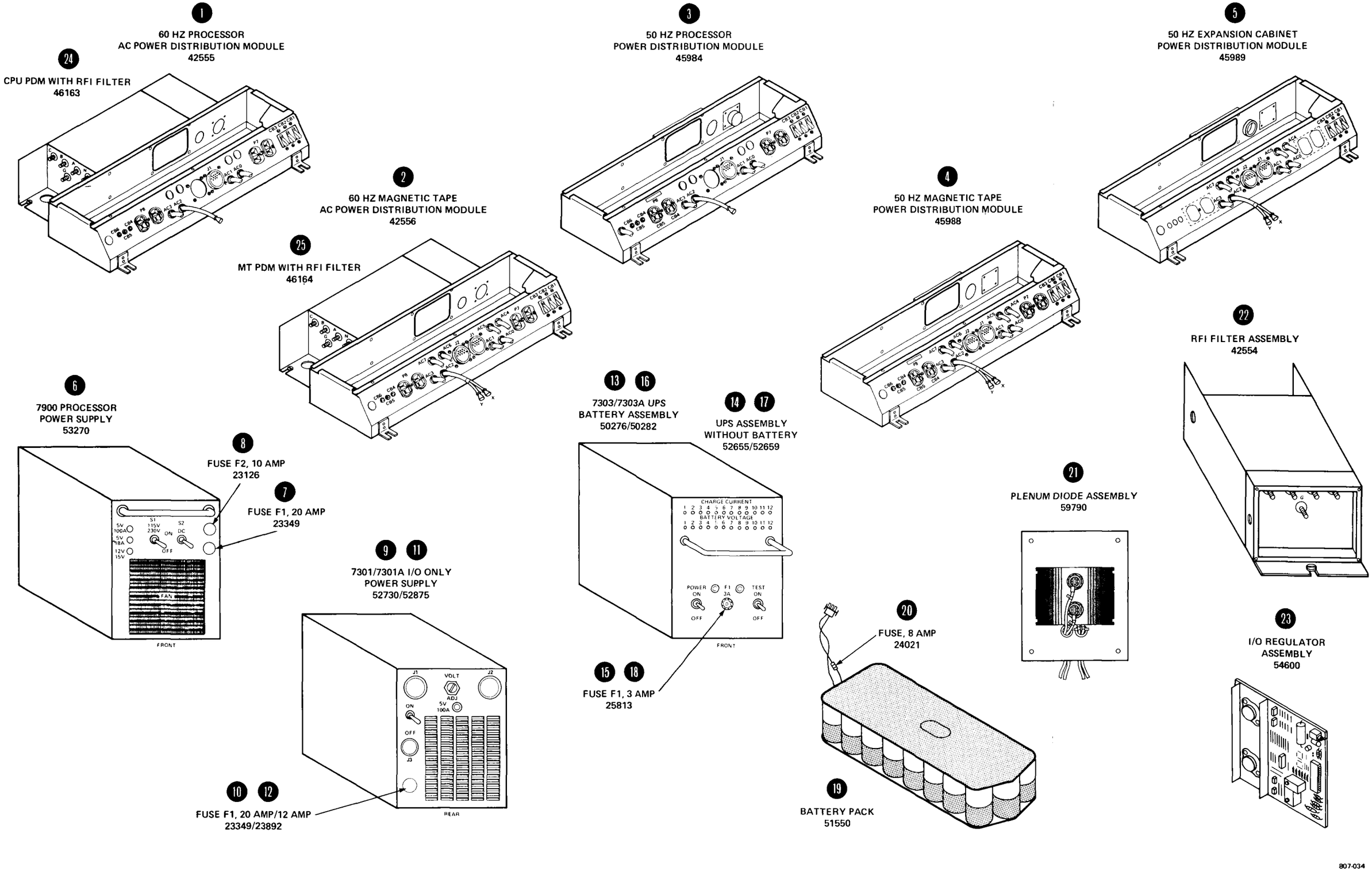
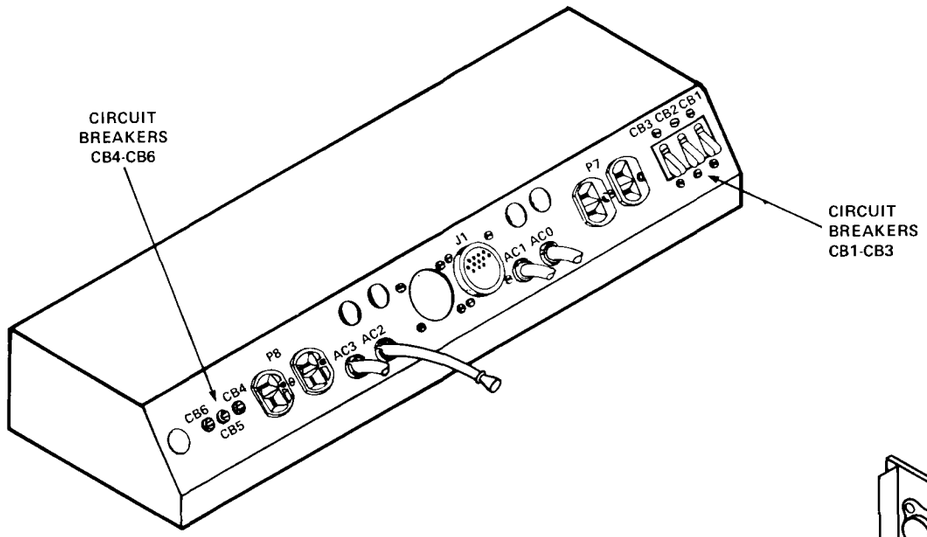


Figure 8-1 Parts Location Diagram

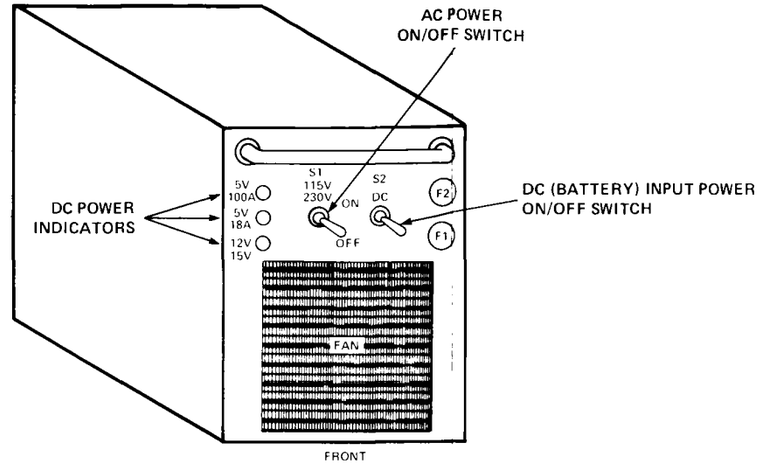
APPENDIX A
FOLDOUTS

A.0 FOLDOUTS

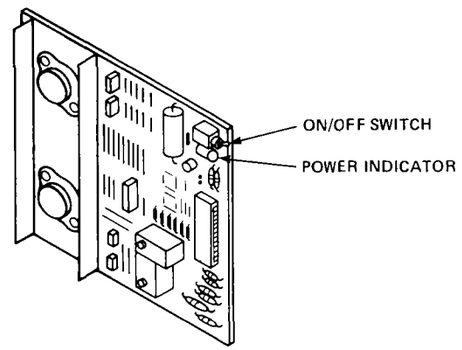
Figure A-1 shows the locations of the switches on the components that make up the power subsystem for NonStop II and NonStop TXP processing systems. Figure A-2 shows the locations of the components of the power subsystem in the cabinets (sample configuration).



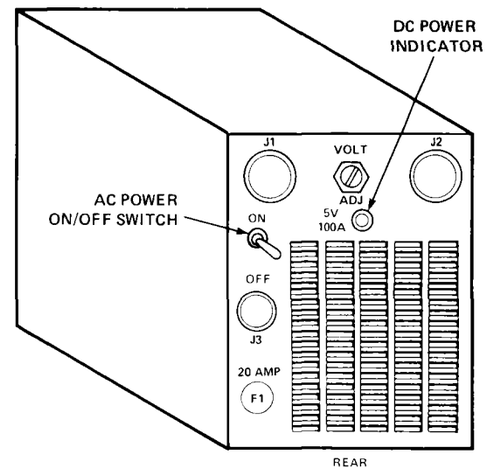
PROCESSOR AC POWER DISTRIBUTION MODULE



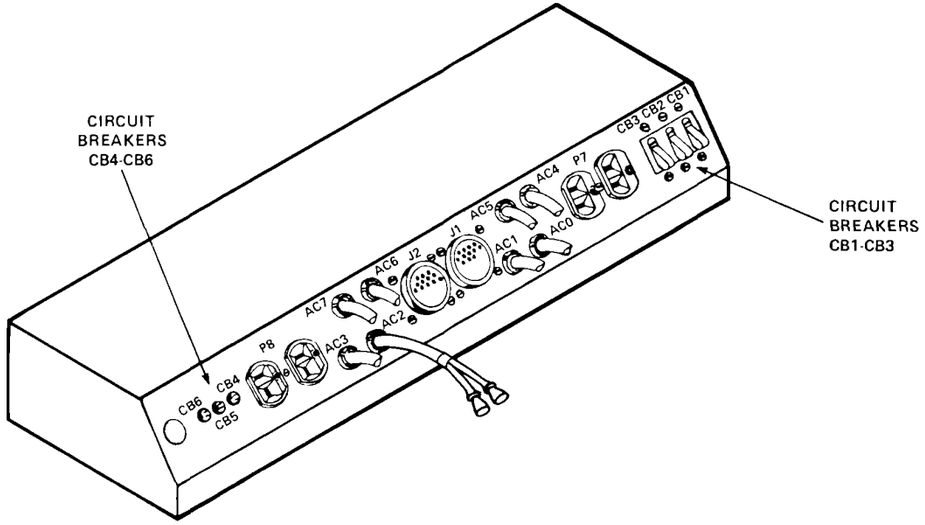
PROCESSOR POWER SUPPLY



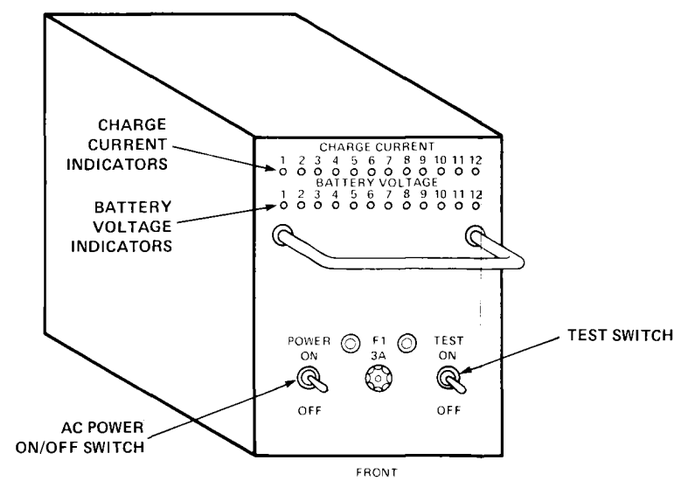
I/O REGULATOR BOARD



I/O-ONLY POWER SUPPLY



MAGNETIC TAPE AC POWER DISTRIBUTION MODULE



UPS BATTERY SUPPLY

807-009

Figure A-1 Switch and Indicator Location Diagram

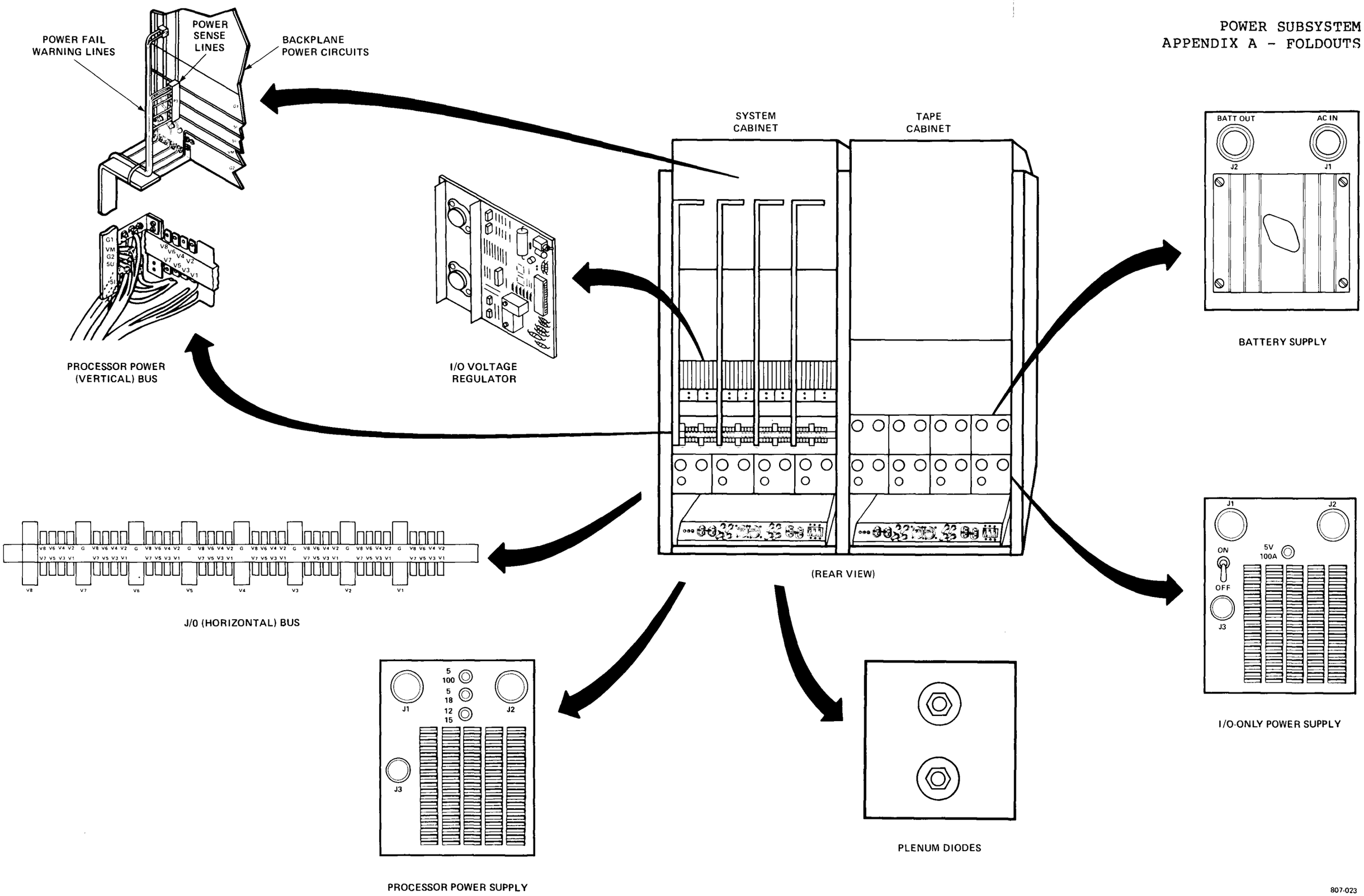


Figure A-2 Power Subsystem Location Diagram

APPENDIX B
FOREIGN REQUIREMENTS

B.0 FOREIGN REQUIREMENTS

Tandem processing systems in many countries outside the United States require special considerations. The following paragraphs describe some of the special requirements for foreign installations.

B.1 ISOLATION TRANSFORMERS

For systems installed in Europe and some other locations outside the United States, isolation transformers are required. Isolation transformers (rated at 5 KVA each) are used for inductive coupling of input to output, providing an effective AC connection without a hard-wired connection. Three isolation transformers (one for each phase) are supplied for systems that require this type of inductive coupling.

A system with isolation transformers does not require an RFI filter. A terminal box for AC power line connections is located in front of the AC power distribution module.

The isolation transformers must be housed in either a magnetic tape cabinet or a 7107 system expansion cabinet. A single set of three isolation transformers can feed AC power modules located in the home cabinet and adjacent cabinets. This may affect power cable requirements.

It is the responsibility of the customer to supply an electrician to connect the AC power cable to the terminal box, but it the responsibility of the Tandem customer engineer to indicate which phases are A, B, and C. Refer to paragraph 4.4 for phase balancing information.

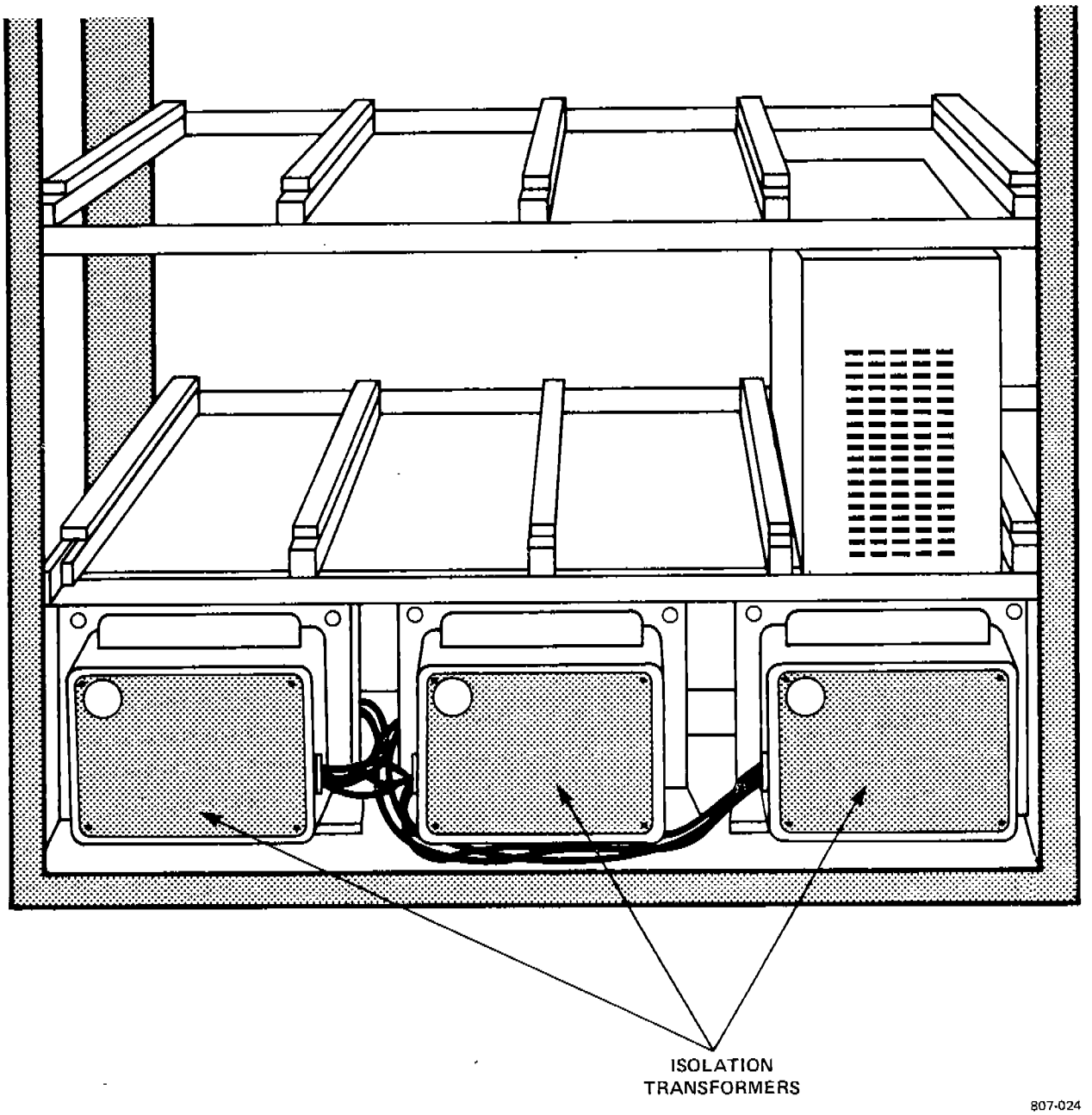


Figure B-1 Isolation Transformers

B.2 COMMERCIAL AC POWER GAZETTEER

Figure B-2 and Table B.1 describe the circuit types and commercial power available in the United States and other countries.

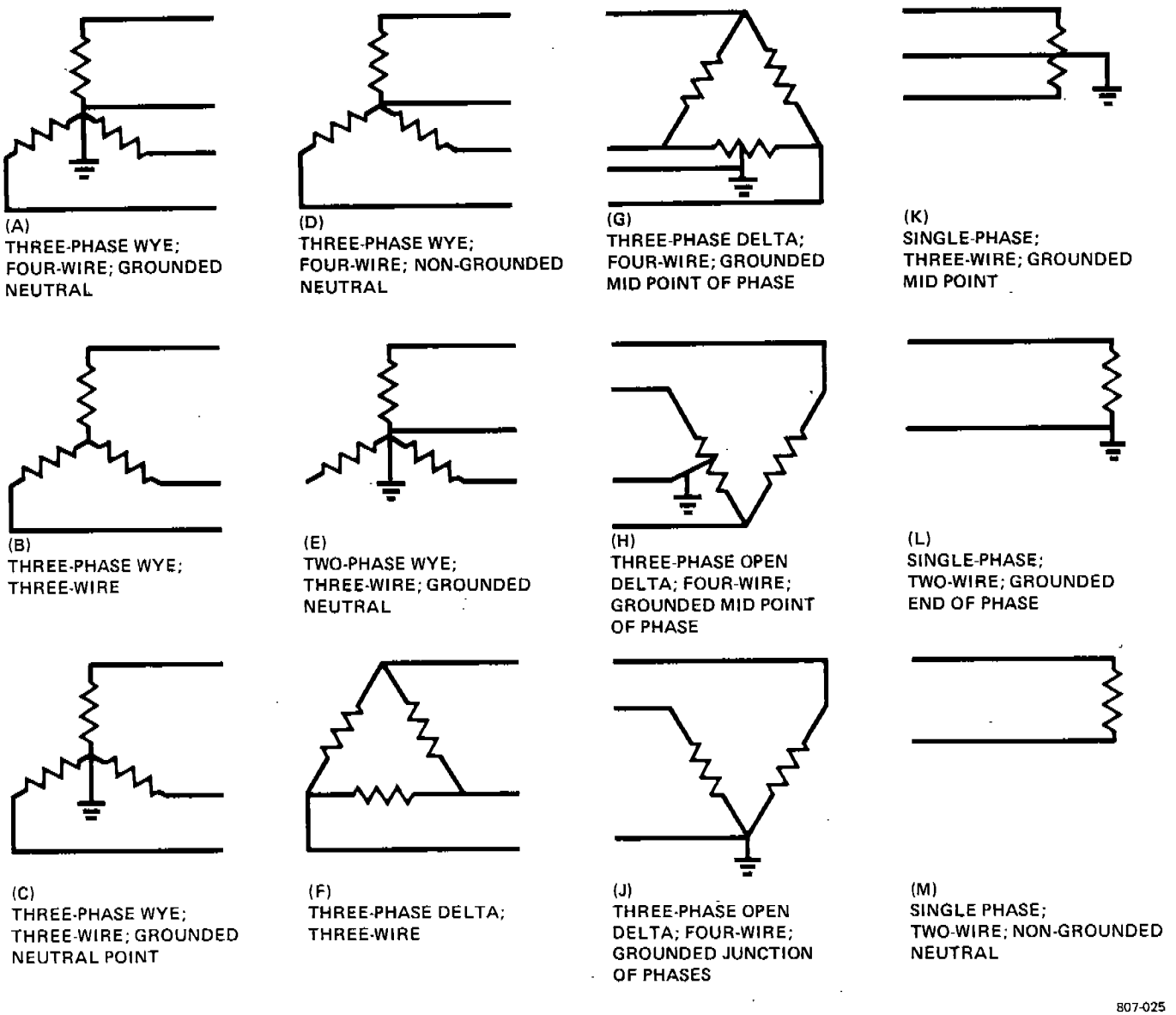


Figure B-2 Circuit Types

Table B.1 Worldwide Commercial Power Table

COUNTRY	COMMERCIAL VOLTAGE	TOLERANCE (±%)	FREQUENCY (Hz)	TOLERANCE (±%)	TYPE
Algeria	380/220 220/127	10%	50	1.5%	A
Argentina	390/225 380/220 220	10%	50	1%	A A L
Australia	415/240 440/250	6%	50	0.1%	A
Austria	380/220 220	5%	50	0.1%	A,B L
Belgium	380/220 220/127 220	5% (day) 10% (night)	50	3%	A A F
Bolivia	230/115	5%	50	1%	H
Brazil	380/220 220/127	?	60	?	A
Bulgaria	380/220 220	5%	50	0.1%	A L
Canada	600/347 480 240 240/120 208/120	+4%, -8.3%	60	0.02%	A F F K A
Chile	380/220	?	50		A
Czechoslovakia	380/220 220	10%	50	0.1%	A L
Denmark	380/220 220	10%	50	0.4%	A L

Table B.1 Worldwide Commercial Power Table (Cont'd)

COUNTRY	COMMERCIAL VOLTAGE	TOLERANCE (±%)	FREQUENCY (Hz)	TOLERANCE (±%)	TYPE
Ecuador	240/120	?	60	?	K
	208/120				A
	220/127				A
	220/110				K
Egypt	380/220	10%	50	1%	A
	220				L
Finland	380/220	10%	50	0.1%	A
France	380/220	10%	50	1%	A
	380/220				D
	380				B
Germany (BR) (West)	380/220	10%	50	0.3%	A
Germany (DDR) (East)	380/220	5%	50	0.3%	A
	220				L
Greece	6.6 kv	5%	50	1%	
	380/220				A
Hong Kong	11 kv	6%	50	2%	
	346/200				A
	200				L
Hungary	380/220	+5%, -10%	50	2%	A
	220				L
Iceland	380/220	?	50	0.1%	A
	220				L
India					
Bombay	440/250	4%	50	1%	A
	230				L
New Delhi	400/230	6%	50	3%	A
	230				L
Indonesia	380/220	5%	50	+1%, -2%	A
	220/127				A
Iran	380/220	15%	50	5%	A

Table B.1 Worldwide Commercial Power Table (Cont'd)

COUNTRY	COMMERCIAL VOLTAGE	TOLERANCE (±%)	FREQUENCY (Hz)	TOLERANCE (±%)	TYPE
Iraq	380/220	?	50	?	A
Ireland					
Northern	400/230	6%	50	0.4%	A
	380/220				A
Republic of	380/220	?	50	?	A
Israel	400/230	6%	50	0.2%	A
	230				L
Italy	380/220	5%	50	0.4%	A
	220/127				E
Japan					
Eastern	200/100	10%	50	0.2%	H,K
Western	210/105	10%	60	0.1%	H,K
	200/100				K
	100				L
Jordan	380/220	?	50	?	A
Korea	200/100	?	60	?	K
Kuwait	415/240	?	50	?	A
Luxembourg	380/220	10%	50	0.5%	A
	220				L
Mexico	220/127	6%	60	0.2%	A
	220				L
	120				M
Monaco	380/220	?	50	?	A
Netherlands	380/220	6%	50	0.4	A
New Zealand	415/240	5%	50	1.5%	A,E
	400/230				A,E
	230				L
	240				L
Nicaragua	240/120	?	60	?	G,K

Table B.1 Worldwide Commercial Power Table (Cont'd)

COUNTRY	COMMERCIAL VOLTAGE	TOLERANCE (±%)	FREQUENCY (Hz)	TOLERANCE (±%)	TYPE
Norway	380/220 230	10%	50	0.2	A B
Pakistan	400/230 230	?	50	?	A L
Panama	480/277 240/120	5%	60	0.17	A K
Paraguay	440/220 380/220	?	50	?	K A
Peru	225	?	60	?	B,M
Philippines	13.8 kv 4.16 kv 2.4 kv 220	5%	60	0.16	 M
Poland	380/220	?	50	?	A
Portugal	15 kv 5 kv 380/220	1%	50	5%	 A
Puerto Rico	480 240/120	10%	60	10%	F K
Romania	380/220	5%	50	1%	A,L
Saudi Arabia	380/220 220/127 127	5%	60	0.5%	A A L
Singapore	6.6 kv 400/230	3%	50	0.5%	 A
Spain	380/220 220/127	7%	50	3%	A A
Sweden	380/220 220	10%	50	0.2%	A L

Table B.1 Worldwide Commercial Power Table (Cont'd)

COUNTRY	COMMERCIAL VOLTAGE	TOLERANCE (±%)	FREQUENCY (Hz)	TOLERANCE (±%)	TYPE
Switzerland	380/220	10%	50	0.5%	A
	220				L
Syria	380/220	?	50	?	A
	220				L
	200/215				A
	115				L
Taiwan	380/220	5%	60	4%	A
	220/110	10%			H
United Kingdom	415	5%	50	1%	A
	240				
Uruguay	220	6%	50	1%	B,L
U.S.A	4.8 kv	5%	60	0.3%	
	480/277				A,C
	480				F
	460/265				A
	240/120				G,H
	240/120				K
	240				F
	230				F
	208/120				A,K
U.S.S.R.	380/220	?	50	?	A
	220				L
Venezuela	240/120	?	60	?	G
	208/120				A
Yugoslavia	380/220	?	50	?	A
	220				L

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TANDEM

NonStop II™ Maintenance Manual

Processor Subsystem (T16/250)

Third Level

Publication No. T16/8809
Part No. 82809

THIRD LEVEL

MAINTENANCE MANUAL

NonStop II (TM)

PROCESSOR SUBSYSTEM (T16/250)

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TANDEM COMPUTERS INCORPORATED
19333 Vallco Parkway
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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits of Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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CHANGE RECORD

This A01 update of Processor Subsystem, T16/250, is issued to correct errors in the original release.

To bring the manual up to the A01 level, make changes in the following sections:

a. Title Page: Remove title page; replace with new title page.

b. Table of Contents: Add pages ii-a and ii-b. Remove page v; replace with new page v.

c. Section 1: Remove pages 1-1 through 1-2; replace with new pages 1-1 through 1-2.

d. Section 2: Remove pages 2-1, 2-3, and 2-34 through 2-37; replace with new pages 2-1, 2-3, and 2-34 through 2-37.

e. Section 4: Remove pages 4-2 through 4-3; replace with new pages 4-2 through 4-3.

f. Section 5: Remove pages 5-6 through 5-10 and page 5-14; replace with new pages 5-6 through 5-10 and page 5-14.

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SECTION 1
INTRODUCTION

1.0 INTRODUCTION

The purpose of this manual is to provide Tandem field engineering personnel with an overview and brief functional description of the Tandem NonStop II TM processor and its associated components.

The scope of this manual is to provide step-by-step removal and installation procedures of malfunctioning boards. Therefore, it is assumed that the Tandem system is already installed and fully operational.

The NonStop II processor provides a greatly enhanced overall functional capability and an increased level of data integrity over previous systems. The data integrity level has been increased with additional self-checking and fault isolation diagnostic routines. Its increased expandability includes expanded mapping, which has increased the number of major code and data areas from 4 to 16. A 23-bit physical address is provided via three additional map register output bits, expanding addressable memory to 16 megabytes. This increased expandability also includes storage for library procedures.

The NonStop II processor consists of a three-board CPU (refer to paragraph 2.0) plus up to a maximum of four memory boards (semiconductor only) per processor (minimum 512 kB).

1.1 REFERENCE DOCUMENTATION

The documents used as reference throughout this manual are as follows:

Functional Description Manual, T16/8800
OSP Users Guide, T16/8801
OSP Maintenance Manual, T16/8846
OSP Diagnostics Manual, T16/8804
IPB Diagnostics Manual, T16/8803
Site Planning Manual, T16/8851
Stress Manual, T16/8852
System Configuration Manual, T16/I8001
Guardian (TM) Operating Manual, T16/8019
Power Subsystem Maintenance Manual (TNS II), T16/8807

SECTION 2
PHYSICAL DESCRIPTION

2.0 PHYSICAL DESCRIPTION

The Tandem NonStop II TM processor includes seven board types: the Instruction Processing Unit (IPU), the Memory Control and Interprocessor Bus board (MCB), the Channel, Control Store, and DDT board (CCD), the Memory board (MEM), Control Panel, Processor Maintenance Interface (PMI), and the Test Panel. For detailed information on the Operations Service Processor (OSP), refer to Maintenance Manual T16/8846.

The following paragraphs describe the type of PC board to be used, the expected complexity of each board, the principal contents of each board, and the expected current drain on the power supplies: Vcc (+5V interruptible), Vuu (+5V uninterruptible), and Vdd (-12V). Figure 2-1 shows the NonStop II processor interconnection.

2.1 POWER REQUIREMENTS

2.1.1 AC Power

AC power is distributed to the T16/7301 Power Modules, the UPS Battery Packs, and the fans by the AC Distribution Unit. Primary AC power can be any one of the following:

120/208 VAC, 3 phase, 60 Hz

2.1.2 DC Power

The following DC voltages are required by the processor; the current listed is for maximum system load.

+ 5VDC IPS @ 100 amps
+ 5VDC UPS @ 18 amps
+12VDC UPS @ 4 amps (MOS memory)

IPS - Interruptible Power Source
UPS - Uninterruptible Power Source

(Refer to the Power Subsystem Maintenance Manual (T16/8807) for further power information.)

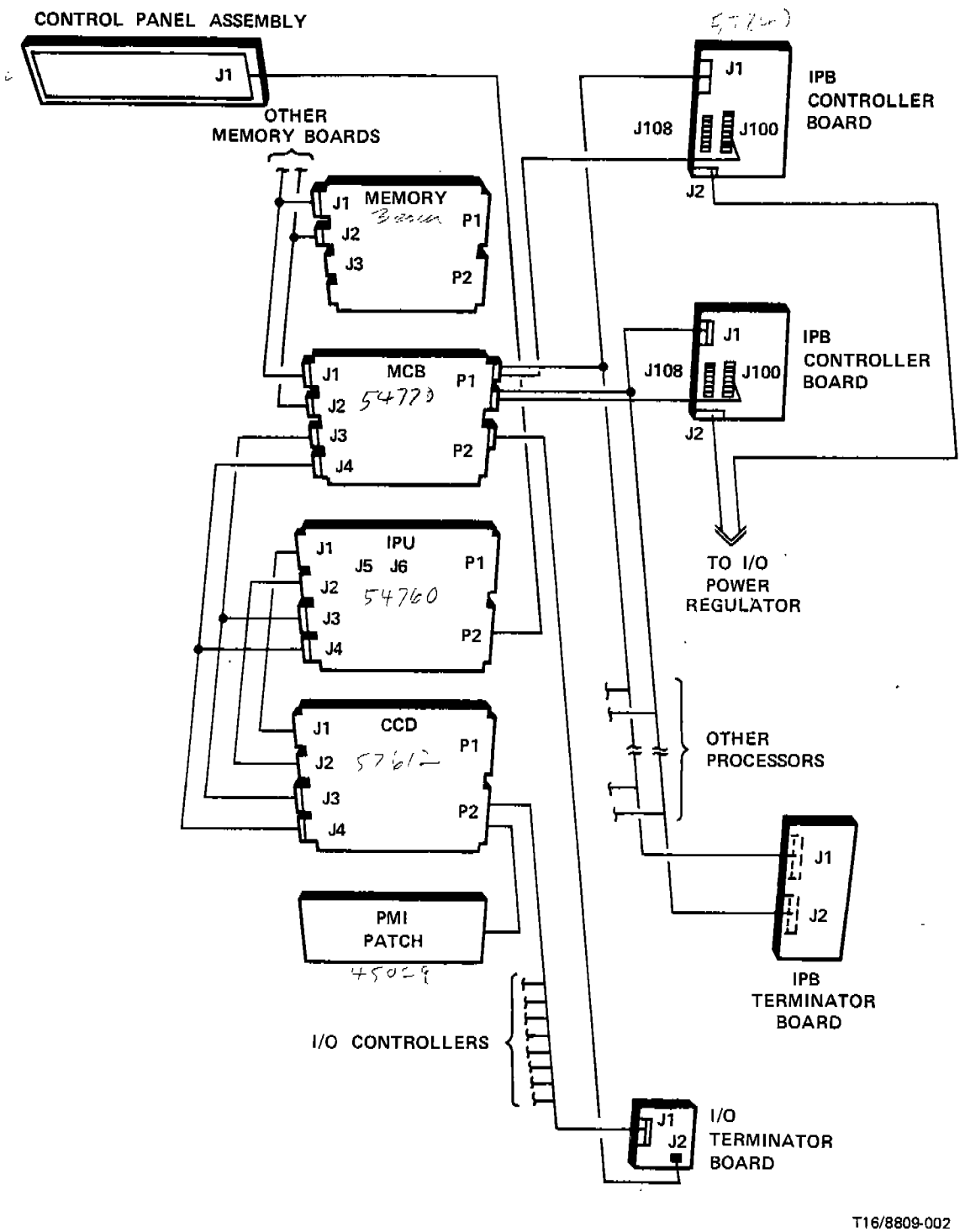


Figure 2-1 NonStop II Processor Interconnection

2.2 OPERATING ENVIRONMENT

The system requires the following operating environment.

Temperature - 60 to 90 degrees F (15-32 degrees C)
Humidity (Rel) - 30 to 80 percent (noncondensing)

2.3 SWITCHES, INDICATORS, AND JUMPERS

2.3.1 Address Switches

The memory module address is set by a six-pole DIP switch (SW-2A) mounted at the front edge of each memory board. The first (uppermost) switch is BOARD ENABLE, which must be closed to enable reading and writing to the board. Address count is binary from zero. An open switch represents binary zero. See Table 2.1 for setting address switches.

Table 2.1 Address Switch Settings

MEMORY BD. NO.	ADDRESS %	SWITCH POSITION 1	2	3	4	5	6
1	00	C	O	O	O	O	O
2	01	C	O	O	O	O	C
3	02	C	O	O	O	C	O
4	03	C	O	O	O	C	C

O = OPEN (Binary 0)
C = CLOSED (" 1)

SEE NOTE

NOTE

Switch 1 is BOARD ENABLE and must be closed to enable reading and writing to the board.

2.3.2 Test/Clear Pushbutton Switch

A SPDT pushbutton switch (SW-1A) is mounted on the front edge of each memory board to test the LEDs on the board, and to clear the error latches. The LEDs are:

a. GREEN (DS-3A) - indicates status of memory voltages (when ON indicates memory voltage is OK).

b. YELLOW (DS-2A) - indicates a CME (when ON indicates that a correctable memory error has occurred).

c. RED (DS-1A) - indicates an UCME (when ON indicates that an uncorrectable memory error has occurred).

2.4 PROCESSOR BOARDS

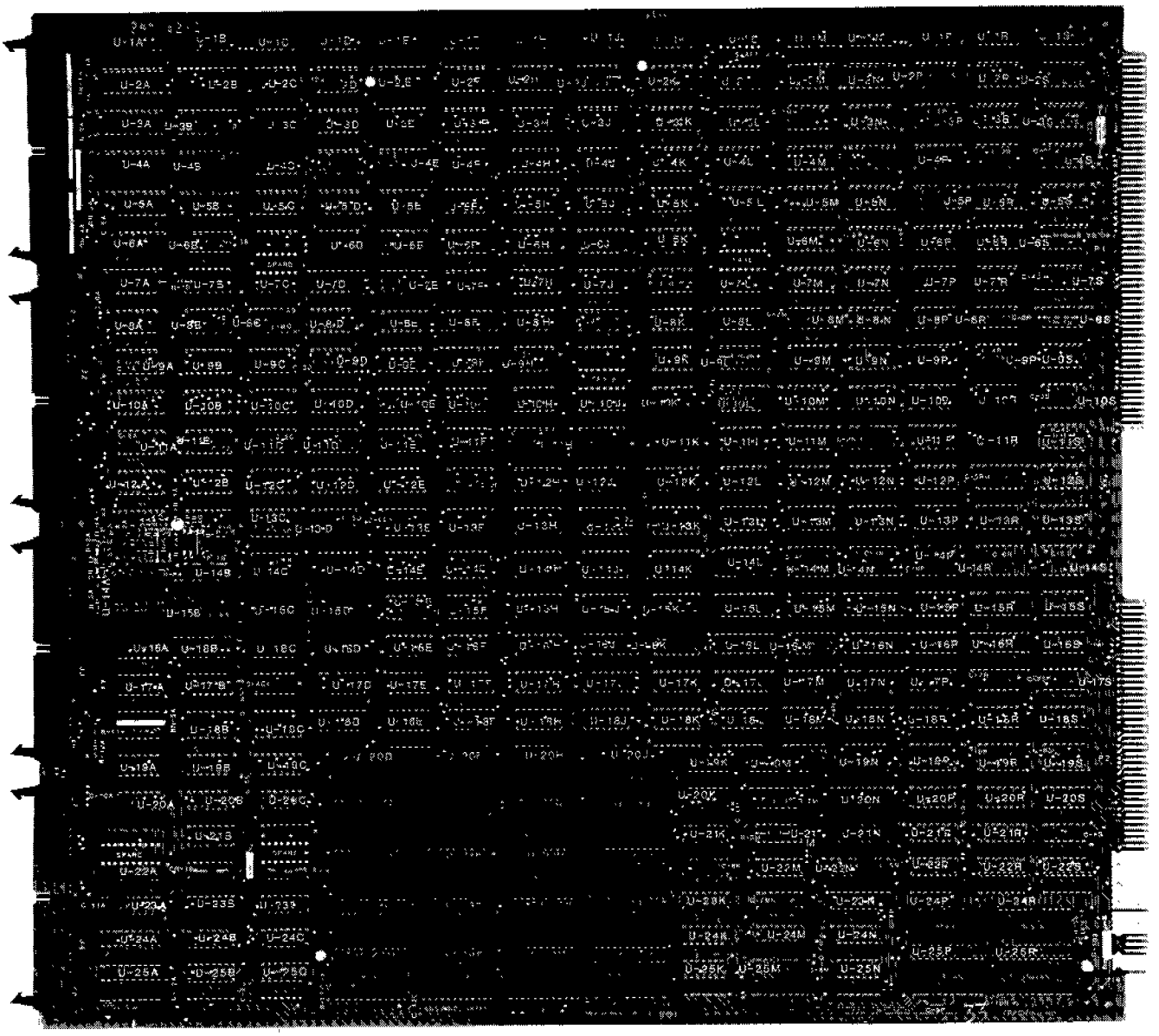
2.4.1 Instruction Processing Unit (IPU) Board

The board layout is shown in Figure 2-2, and connector pin assignments are listed in Table 2.2 (P1), Table 2.3 (P2), Table 2.4 (J1), Table 2.5 (J2), Table 2.6 (J3), and Table 2.7.

a. Board type: NonStop II PC outline, six layer.

b. Power: +5Vdc (IPS) 19A, +5Vdc (UPS) 0A, -12Vdc 0A.

c. Contents: register files, ALU, shifter, microprocessor address register, instruction register, instruction decoding.



T16/8809-003

Figure 2-2 Instruction Processing Unit (IPU) Board

Table 2.2 IPU Board Connector P1

SIGNAL	CONNECTOR PINS		SIGNAL
CCS<00>	01	02	CCS<01>
CCS<02>	03	04	CCS<03>
CCS<04>	05	06	CCS<05>
CCS<06>	07	08	CCS<07>
CCS<08>	09	10	CCS<09>
CCS<10>	11	12	CCS<11>
CCS<12>	13	14	CCS<13>
CCS<14>	15	16	CCS<15>
CCS<16>	17	18	CCS<17>
CCS<18>	19	20	CCS<19>
CCS<20>	21	22	CCS<21>
CCS<22>	23	24	CCS<23>
CCS<P0>	25	26	CCS<P1>
CCS<P2>	27	28	CCS<P3>
CCSA<0>	29	30	CCSA<1>
CCSA<2>	31	32	CCSA<3>
CCSA<4>	33	34	CCSA<5>
CHMC/CMAPA<0>	35	36	CHMC/CMAPA<1>
CCSA<6>	37	38	CCSA<7>
CCSA<8>	39	40	CCSA<9>
CPU#<0>	41	42	CPU#<1>
CPU#<2>	43	44	CPU#<3>
CPU#<4>	45	46	CPU#<5>
CPU#<6>	47	48	CPU#<7>
CBUS<00>	49	50	CBUS<01>
CBUS<02>	51	52	CBUS<03>
CBUS<04>	53	54	CBUS<05>
CBUS<06>	55	56	CBUS<07>
CBUS<08>	57	58	CBUS<09>
CBUS<10>	59	60	CBUS<11>
CBUS<12>	61	62	CBUS<13>
CBUS<14>	63	64	CBUS<15>
CBUS<PL>	65	66	CBUS<PR>
CHMC/CMAPA<2>	67	68	CHMC/CMAPA<3>
CHMC/CMAPA<P>	69	70	CHMC/WRT*
	71	72	

Table 2.2 IPU Board Connector P1 (Cont'd)

SIGNAL	CONNECTOR PINS		SIGNAL
	73	74	
	75	76	
	77	78	
	79	80	
	81	82	
IPCH/RD*	83	84	IPCH/WRT*
CHIP/RD*	85	86	CHIP/WRT*
CHIP/LIO	87	88	CHIP/HIO
CHIP/SPCHRQ*	89	90	IPDT/RD*
IPDT/WRT*	91	92	DTIP/CHARINT*
	93	94	
	95	96	
IPDT/PONRST	97	98	
DTIP/DDTHALT*	99	100	EX/NOPCCS*
IPCS/CSWRT*	101	102	EX/CCSENB
CS/CSAPERR	103	104	IPCS/LCSDIN*
MCCH/ADDBKPT	105	106	MCCH/ABS
OPIP/OPTINT	107	108	IPOP/RD*
OPIP/TESTOP*	109	110	IPOP/WRT*
IPIB/RD*	111	112	IPIB/SELQ*
IBIP/XINQF	113	114	IPIB/WRT*
N.C.	115	116	N.C.
N.C.	117	118	N.C.
GND	119	120	IPUCLK*

SPARES (common to OPT,CCD,IPU) = 17

Table 2.3 IPU Board Connector P2

SIGNALS	CONNECTOR PINS		SIGNALS
GND	01	02	IBIP/OQEMP*
IPIB/CLOQ*	03	04	GND
IBIP/YINQF	05	06	IPMC/LOADMDIAG*
IPMC/LOADADBRH*	07	08	IPMC/LOADADBRL*
IPMC/RDMD*	09	10	IPMC/RDNI*
IPMC/RDLSPAGE*	11	12	IPMC/RDLPAGE*
IPMC/RDMPD*	13	14	MCIP/MDAV*
MCIP/NIAV*	15	16	MCIP/PMDAV*
MCIP/MAPAV*	17	18	MCIP/DABS
----------GND	19	20	-------PBUS<00>-------
PBUS<01>	21	22	GND
PBUS<02>	23	24	PBUS<03>
GND	25	26	PBUS<04>
PBUS<05>	27	28	GND
PBUS<06>	29	30	PBUS<07>
CONTROL GND	31	32	PBUS<08>
PANEL PBUS<09>	33	34	GND
PBUS<10>	35	36	PBUS<11>
GND	37	38	PBUS<12>
PBUS<13>	39	40	GND
PBUS<14>	41	42	PBUS<15>
GND	43	44	GND
IP/RDPNLS*	45	46	IP/WRTPNLD*
GND	47	48	MRESET*
HLTKY*	49	50	GND
PNLKY*	51	52	PWARN*
GND	53	54	IP/END3*
CPIP/SLIC*	55	56	GND
IP/PON	57	58	
N.C.	59	60	CPPWR
CPPWR	61	62	N.C.
CPPWR	63	64	CPPWR
MCIP/NMEM	65	66	MCIP/ADDBRPT
MCIP/IABS	67	68	IPMC/LOADPMD*
	69	70	MCIP/CME
MCIP/UCME	71	72	
MCBCCD/XTALCLK*	73	74	
MCDT/MAPPE	75	76	MCDT/MAPE
MCDT/MAPAPE	77	78	MCDT/WDPE
PWARN*	+-79	80-+	
Power Warn Cable ----GND	|_81	82_|	GND----------

Table 2.3 IPU Board Connector P2 (Cont'd)

SIGNALS			CONNECTOR PINS		SIGNALS	
		GND	81	82	GND	
		GND	83	84	GND	
		GND	85	86	GND	
		GND	87	88	GND	
		GND	89	90	GND	
		GND	91	92	GND	
		GND	93	94	GND	
POWER		GND	95	96	GND	
		GND	97	98	GND	
		GND	99	100	GND	
		Vcc	101	102	Vcc	
		Vcc	103	104	Vcc	
	IPS	Vcc	105	106	Vcc	IPS
		Vcc	107	108	Vcc	
		Vuu	109	110	Vuu	
	UPS	Vuu	111	112	Vuu	UPS
		Vuu	113	114	Vuu	
		Vcc	115	116	Vcc	
	IPS	Vcc	117	118	Vcc	IPS
		Vcc	119	120	Vcc	

SPARES (common to OPT,CCD,IPU,MCB)= 74,80
SPARES (common to IPU,MCB)= 69,72

Table 2.4 IPU/CCD Board Connector J1

SIGNAL	CONNECTOR PINS		SIGNAL
GND	01	02	CSDATA<00>
CSDATA<01>	03	04	GND
CSDATA<02>	05	06	CSDATA<03>
GND	07	08	CSDATA<04>
CSDATA<05>	09	10	GND
CSDATA<06>	11	12	CSDATA<07>
GND	13	14	CSDATA<08>
CSDATA<09>	15	16	GND
CSDATA<10>	17	18	CSDATA<11>
GND	19	20	CSDATA<12>
CSDATA<13>	21	22	GND
CSDATA<14>	23	24	CSDATA<15>
GND	25	26	CSDATA<16>
CSDATA<17>	27	28	GND
CSDATA<18>	29	30	CSDATA<19>
GND	31	32	CSDATA<20>
CSDATA<21>	33	34	GND
CSDATA<22>	35	36	CSDATA<23>
GND	37	38	CSDATA<24>
CSDATA<25>	39	40	GND
CSDATA<26>	41	42	CSDATA<27>
GND	43	44	CSDATA<28>
CSDATA<29>	45	46	GND
CSDATA<30>	47	48	CSDATA<31>
GND	49	50	CSDATA<P0>
CSDATA<P1>	51	52	GND
CSDATA<P2>	53	54	CSDATA<P3>
GND	55	56	ROMA<00>
ROMA<01>	57	58	GND
ROMA<02>	59	60	ROMA<03>

SPARES = 0

Table 2.5 IPU/CCD Board Connector J2

SIGNAL	CONNECTOR PINS		SIGNAL
GND	01	02	ROMA<04>
ROMA<05>	03	04	GND
ROMA<06>	05	06	ROMA<07>
GND	07	08	ROMA<08>
ROMA<09>	09	10	GND
ROMA<10>	11	12	ROMA<11>
GND	13	14	ROMA<12>
ROMA<13>	15	16	GND
ROMA<14>	17	18	ROMA<15>
GND	19	20	IPTP/RDPNLA*
IPTP/WRTPNLA*	21	22	GND
	23	24	EXCS/ENB
GND	25	26	IPTP/NOP1
IPTP/NOP2	27	28	GND
IPTP/TESTMET	29	30	IPTP/INTRP
GND	31	32	IPTP/SUBR
IPTP/FLAGA	33	34	GND
IPTP/FLAGB	35	36	IPTP/FLAGC
GND	37	38	IP/END3*
TPIP/CLKINH*	39	40	GND
HLTKY*	41	42	PNLKY*
GND	43	44	IP/RDPNLS*
IP/WRTPNLD*	45	46	GND
TPIP/DISPBUS*	47	48	IPDT/JPERR
GND	49	50	CCDIPU/PON
IPDT/KPERR	51	52	GND
IPDT/ROMAPERR	53	54	IPDT/CSDPERR
GND	55	56	IPTP/SYNC*
IP/REPFRZ	57	58	GND
IP/CSAPARL	59	60	IP/CSAPARR

SPARES = 1

Table 2.6 IPU/CCD/MCB Board Connector J3

SIGNAL	CONNECTOR PINS		SIGNAL
GND	01	02	MCBTPL/CLK*
IPMC/PCR*	03	04	GND
IPMC/PDR*	05	06	IPMC/PDW*
GND	07	08	IPMC/MR*
IPMC/MW*	09	10	GND
IPMC/OPVALID*	11	12	IP/RDST*
GND	13	14	IPIT/RD*
CHMC/CRDREAD*	15	16	GND
CH/PE	17	18	IP/SFLG*
GND	19	20	IP/RFLG*
IP/PE	21	22	GND
MC/PE	23	24	IP/ERRFRZ
GND	25	26	IP/RESET*
IP/FRZDE	27	28	GND
IP/CLKINH	29	30	MRESET*
GND	31	32	EX/TESTRESET*
MCCH/CRDAV*	33	34	GND
ITIP/INT	35	36	MCDT/CHREQ
GND	37	38	MCDT/MDIAGPE
IPMC/MAPA<0>	39	40	GND
IPMC/MAPA<1>	41	42	IPMC/MAPA<2>
GND	43	44	IPMC/MAPA<3>
	45	46	GND
MCCH/CWDAV*	47	48	CHMC/MREQ*
GND	49	50	CHMC/WDSND*
CHMC/ERRST*	51	52	GND
MCCH/MAPAV*	53	54	MCCH/UCME
GND	55	56	CHMC/RSV*
MCIP/PDRMAPACC	57	58	GND
MCIP/PCRMAPACC	59	60	MCIP/ENDABS

SPARES = 1

Table 2.7 IPU/CCD/MCB Board Connector J4

SIGNAL	CONNECTOR PINS		SIGNAL
GND	01	02	KBUS<00>
KBUS<01>	03	04	GND
KBUS<02>	05	06	KBUS<03>
GND	07	08	KBUS<04>
KBUS<05>	09	10	GND
KBUS<06>	11	12	KBUS<07>
GND	13	14	KBUS<08>
KBUS<09>	15	16	GND
KBUS<10>	17	18	KBUS<11>
GND	19	20	KBUS<12>
KBUS<13>	21	22	GND
KBUS<14>	23	24	KBUS<15>
GND	25	26	KBUS<PL>
KBUS<PR>	27	28	GND
	29	30	MBUS<00>
GND	31	32	MBUS<01>
MBUS<02>	33	34	GND
MBUS<03>	35	36	MBUS<04>
GND	37	38	MBUS<05>
MBUS<06>	39	40	GND
MBUS<07>	41	42	MBUS<08>
GND	43	44	MBUS<09>
MBUS<10>	45	46	GND
MBUS<11>	47	48	MBUS<12>
GND	49	50	MBUS<13>
MBUS<14>	51	52	GND
MBUS<15>	53	54	MBUS<PL>
GND	55	56	MBUS<PR>
MBUS<PV>	57	58	GND
IPU/PON	59	60	MCBIPU/PON

SPARES = 1

2.4.2 Memory Control and Interprocessor Bus Board (MCB)

The board layout is shown in Figure 2-3, and connector pin assignments are listed in Table 2.8 (P1), Table 2.9 (P2). Refer to Table 2.6 for J7, and Table 2.7 for J4 connector pin assignments.

a. Board type: NonStop II PC outline, four layer.

b. Power: +5VDC (IPS) 15A, +5VDC (UPS) 0.5A, -12VDC 0A.

c. Contents: memory request control, address translation map, memory ECC, address trap comparator, refresh timer, processor clock, interprocessor bus control, interval timer.

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Figure 2-3 Memory Control and Interprocessor Bus Board (MCB)

Table 2.8 MCB Board Connector Pin P1

	SIGNALS	CONNECTOR PINS		SIGNALS
	GND	01	02	XBUS<00>*
	XBUS<01>*	03	04	GND
	XBUS<02>*	05	06	XBUS<03>*
	GND	07	08	XBUS<04>*
	XBUS<05>*	09	10	GND
	XBUS<06>*	11	12	XBUS<07>*
	GND	13	14	XBUS<08>*
XBUS	XBUS<09>*	15	16	GND
	XBUS<10>*	17	18	XBUS<11>*
	GND	19	20	XBUS<12>*
	XBUS<13>*	21	22	GND
	XBUS<14>*	23	24	XBUS<15>*
	GND	25	26	
	XBUS<SNDREQ>*	27	28	GND
	XBUS<RCVCMD>*	29	30	XBUS<SNDCMD>*
	GND	31	32	XBUS<RCVACK>*
	XBUS<SNDACK>*	33	34	GND
CHMC/CMAPA<0>		35	36	CHMC/CMAPA<1>
	XBUS<SELECT>*	37	38	GND
XBUS	XBUS<CLK>	39	40	GND
	CPU#<7>*	41	42	CBUS<00>
	CPU#<6>*	43	44	CBUS<01>
	CPU#<5>*	45	46	CBUS<02>
	CPU#<4>*	47	48	CBUS<03>
	CPU#<3>*	49	50	CBUS<04>
	CPU#<2>*	51	52	CBUS<05>
	CPU#<1>*	53	54	CBUS<06>
	CPU#<0>*	55	56	CBUS<07>
	CBUS<08>	57	58	CBUS<09>
	CBUS<10>	59	60	CBUS<11>
	CBUS<12>	61	62	CBUS<13>
	CBUS<14>	63	64	CBUS<15>
	CBUS<PL>	65	66	CBUS<PR>
	CHMC/CMAPA<2>	67	68	CHMC/CMAPA<3>
	CHMC/CMAPA<P>	69	70	CHMC/WRT*

Table 2.8 MCB Board Connector Pin P1 (Cont'd)

SIGNALS	CONNECTOR PINS	SIGNALS
+----------GND	71 72	YBUS<00>*--------+
YBUS<01>*	73 74	GND |
YBUS<02>*	75 76	YBUS<03>* |
GND	77 78	YBUS<04>* |
YBUS<05>*	79 80	GND |
YBUS<06>*	81 82	YBUS<07>* |
GND	83 84	YBUS<08>* |
YBUS YBUS<09>*	85 86	GND |
YBUS<10>*	87 88	YBUS<11>* |
GND	89 90	YBUS<12>* |
YBUS<13>*	91 92	GND |
YBUS<14>*	93 94	YBUS<15>* |
GND	95 96	|
YBUS<SNDREQ>*	97 98	GND |
YBUS<RCVCMD>*	99 100	YBUS<SNDCMD>* |
GND	101 102	YBUS<RCVACK>* |
YBUS<SNDACK>*	103 104	GND |
MCCH/ADDBKPT	105 106	MCCH/ABS
+--YBUS<SELECT>*	107 108	GND----------+
YBUS YBUS<CLK>	109 110	GND |
IPIB/RD*	111 112	IPIB/SELQ*
IBIP/XINQF	113 114	IPIB/WRT*
MCBIPU/CLK*	115 116	MCBCCD/CLK*
MCBOPT/CLK*	117 118	MCBMCB/CLK*
GND	119 120	MCBMCB/CLK*

SPARES = 0

Table 2.9 MCB Board Connector Pin P2

SIGNALS	CONNECTOR PINS		SIGNALS
GND	01	02	IBIP/OQEMP*
IPIB/CLOQ*	03	04	GND
IBIP/YINQF	05	06	IPMC/LOADMDIAG*
IPMC/LOADADBRH*	07	08	IPMC/LOADADBRL*
IPMC/RDMD*	09	10	IPMC/RDNI*
IPMC/RDLSPAGE*	11	12	IPMC/RDLPAGE*
IPMC/RDMPD*	13	14	MCIP/MDAV*
MCIP/NIAV*	15	16	MCIP/PMDAV*
MCIP/MAPAV*	17	18	MCIP/DABS
OSC	19	20	EXTCLK
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
NO	35	36	
CONNECTIONS	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
GND	47	48	EX/TESTRESET*
N.C.	49	50	GND
N.C.	51	52	N.C.
N.C.	53	54	N.C.
CPPWR	55	56	CPPWR
CPPWR	57	58	CPPWR
N.C.	59	60	N.C.
N.C.	61	62	IOTPWR
IOTPWR	63	64	N.C.
MCIP/NMEM	65	66	MCIP/ADDBRPT
MCIP/IABS	67	68	IPMC/LOADPMD*
	69	70	MCIP/CME
MCIP/UCME	71	72	
MCBCCD/XTALCLK*	73	74	
MCDT/MAPPE	75	76	MCDT/MAPE
MCDT/MAPAPE	77	78	MCDT/WDPE
PWARN*	79	80	

Table 2.9 MCB Board Connector Pin P2 (Cont'd)

SIGNALS		CONNECTOR PINS		SIGNALS	
----------GND		81	82	GND----------+	
	GND	83	84	GND	
	GND	85	86	GND	
	GND	87	88	GND	
	GND	89	90	GND	
	GND	91	92	GND	
	GND	93	94	GND	
POWER	GND	95	96	GND	
	GND	97	98	GND	
	GND	99	100	GND	
-------Vcc		101	102	Vcc----	
	Vcc	103	104	Vcc	
IPS	Vcc	105	106	Vcc	IPS
_____Vcc		107	108	Vcc____	
-------Vuu		109	110	Vuu----	
UPS	Vuu	111	112	Vuu	UPS
_____Vuu		113	114	Vuu____	
-------Vcc		115	116	Vcc----	
IPS	Vcc	117	118	Vcc	IPS
_____Vcc		119	120	Vcc_____	

SPARES (common to OPT,CCD,IPU,MCB)= 74,80
SPARES (common to IPU,MCB)= 69,72

Table 2.10 MCB/MEM Board Connector Pin J1

SIGNAL	CONNECTOR PINS		SIGNAL
GND	01	02	MCMM/WD<00>
MCMM/WD<01>	03	04	GND
MCMM/WD<02>	05	06	MCMM/WD<03>
GND	07	08	MCMM/WD<04>
MCMM/WD<05>	09	10	GND
MCMM/WD<06>	11	12	MCMM/WD<07>
GND	13	14	MCMM/WD<08>
MCMM/WD<09>	15	16	GND
MCMM/WD<10>	17	18	MCMM/WD<11>
GND	19	20	MCMM/WD<12>
MCMM/WD<13>	21	22	GND
MCMM/WD<14>	23	24	MCMM/WD<15>
GND	25	26	MCMM/WD<C0>
MCMM/WD<C1>	27	28	GND
MCMM/WD<C2>	29	30	MCMM/WD<C3>
GND	31	32	MCMM/WD<C4>
MCMM/WD<C5>	33	34	GND
MMMC/RD<C0>	35	36	MMMC/RD<C1>
GND	37	38	MMMC/RD<C2>
MMMC/RD<C3>	39	40	GND
MMMC/RD<C4>	41	42	MMMC/RD<C5>
GND	43	44	MMMC/OPCHK
MCMM/START*	45	46	GND
MCMM/READ*	47	48	MCMM/WRITE*
GND	49	50	MCMM/REFRESH*
MCMM/RESET*	51	52	GND
MCMM/CME*	53	54	MCMM/UCME*
GND	55	56	MCMM/TREFDIS*
MCMM/TSPARE*	57	58	GND
MCMM/TMARGIN*	59	60	MCMM/TLTC*

SPARES= 0

Table 2.11 MCB/MEM Board Connector Pin J2

SIGNAL	CONNECTOR PINS		SIGNAL
GND	01	02	MMMC/RD<00>
MMMC/RD<01>	03	04	GND
MMMC/RD<02>	05	06	MMMC/RD<03>
GND	07	08	MMMC/RD<04>
MMMC/RD<05>	09	10	GND
MMMC/RD<06>	11	12	MMMC/RD<07>
GND	13	14	MMMC/RD<08>
MMMC/RD<09>	15	16	GND
MMMC/RD<10>	17	18	MMMC/RD<11>
GND	19	20	MMMC/RD<12>
MMMC/RD<13>	21	22	GND
MMMC/RD<14>	23	24	MMMC/RD<15>
GND	25	26	MCMM/AD<00>
MCMM/AD<01>	27	28	GND
MCMM/AD<02>	29	30	MCMM/AD<03>
GND	31	32	MCMM/AD<04>
MCMM/AD<05>	33	34	GND
MCMM/AD<06>	35	36	MCMM/AD<07>
GND	37	38	MCMM/AD<08>
MCMM/AD<09>	39	40	GND
MCMM/AD<10>	41	42	MCMM/AD<11>
GND	43	44	MCMM/AD<12>
MCMM/AD<13>	45	46	GND
MCMM/AD<14>	47	48	MCMM/AD<15>
GND	49	50	MCMM/AD<16>
MCMM/AD<17>	51	52	GND
MCMM/AD<18>	53	54	MCMM/AD<19>
GND	55	56	MCMM/AD<20>
MCMM/AD<21>	57	58	GND
MCMM/AD<22>	59	60	MMMC/SLOW*

SPARES= 0

2.4.3 Channel, Control Store and DDT Board (CCD)

The board layout is shown in Figure 2-4, and connector pin assignments are listed in Table 2.12 (P1) and Table 2.13 (P2). Refer to Table 2.4 for J1, Table 2.5 for J2, Table 2.6 for J3, and Table 2.7 for J4 connector pin assignments.

a. Board type: NonStop II PC outline, six layer.

b. Power: +5VDC (IPS) 19A, +5VDC (UPS) 0A, -12VDC 0A.

c. Contents: control store array, I/O channel, diagnostic data transceiver.

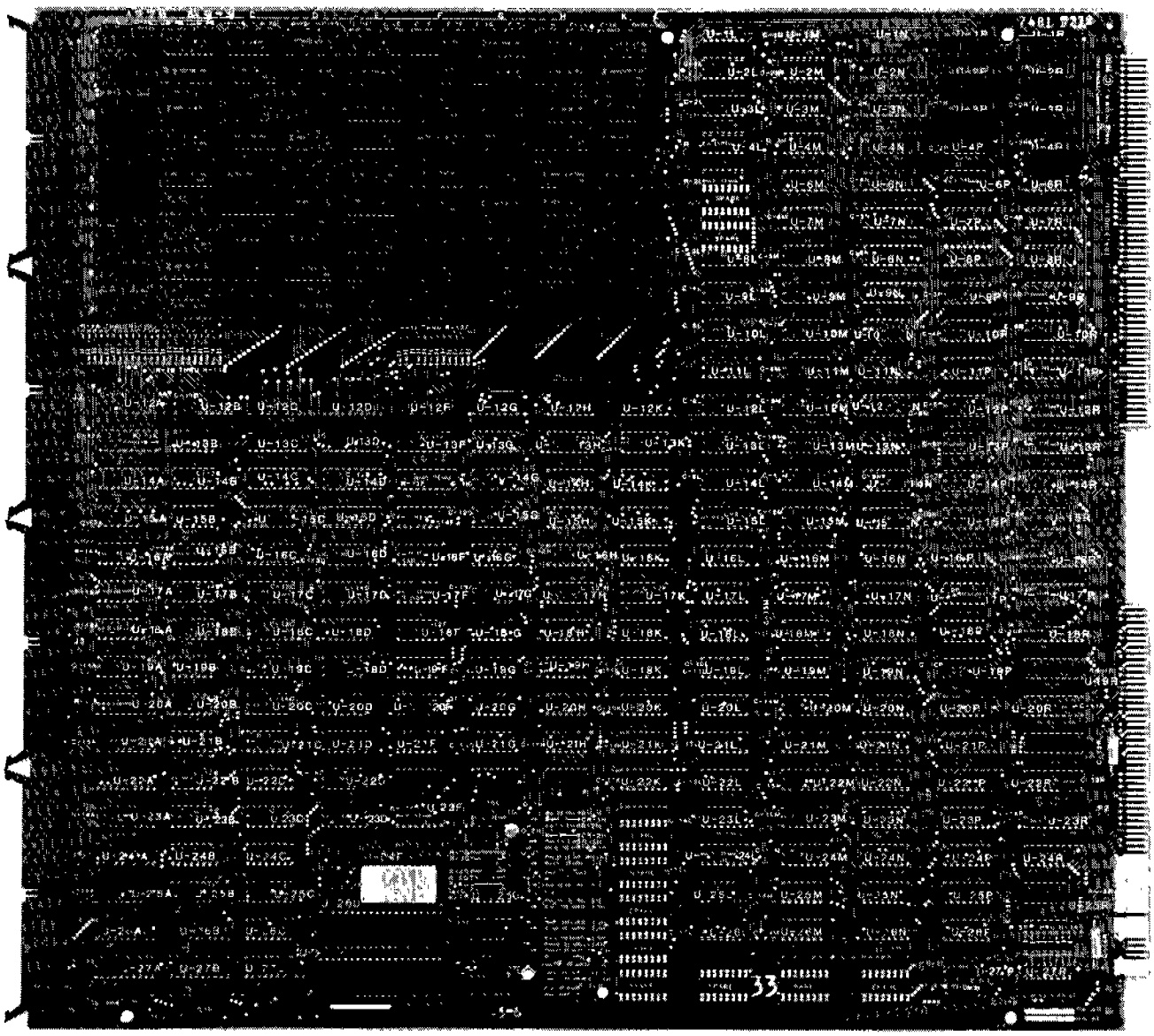

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Figure 2-4 Channel, Control Store and DDT Board (CCD)

Table 2.12 CCD Board Connector P1

SIGNALS	CONNECTOR PINS		SIGNALS
GND	01	02	CCS<00>
CCS<01>	03	04	GND
CCS<02>	05	06	CCS<03>
CCS<04>	07	08	CCS<05>
CCS<06>	09	10	CCS<07>
CCS<08>	11	12	CCS<09>
CCS<10>	13	14	CCS<11>
CCS<12>	15	16	CCS<13>
CCS<14>	17	18	CCS<15>
CCS<16>	19	20	CCS<17>
CCS<18>	21	22	CCS<19>
CCS<20>	23	24	CCS<21>
CCS<22>	25	26	CCS<23>
CCS<P0>	27	28	CCS<P1>
CCS<P2>	29	30	CCS<P3>
GND	31	32	CCSA<0>
CCSA<1>	33	34	GND
CHMC/CMAPA<0>	35	36	CHMC/CMAPA<1>
CCSA<8>	37	38	CCSA<7>
GND	39	40	GND
CPU#<7>*	41	42	CBUS<00>
CPU#<6>*	43	44	CBUS<01>
CPU#<5>*	45	46	CBUS<02>
CPU#<4>*	47	48	CBUS<03>
CPU#<3>*	49	50	CBUS<04>
CPU#<2>*	51	52	CBUS<05>
CPU#<1>*	53	54	CBUS<06>
CPU#<0>*	55	56	CBUS<07>
CBUS<08>	57	58	CBUS<09>
CBUS<10>	59	60	CBUS<11>
CBUS<12>	61	62	CBUS<13>
CBUS<14>	63	64	CBUS<15>
CBUS<PL>	65	66	CBUS<PR>
CHMC/CMAPA<2>	67	68	CHMC/CMAPA<3>
CHMC/CMAPA<P>	69	70	CHMC/WRT*
GND	71	72	OPTIPU/PON
OP/PERR*	73	74	GND
CCSA<4>	75	76	CCSA<5>
CCSA<6>	77	78	CCSA<9>
CCSA<3>	79	80	CCSA<2>

Table 2.12 CCD Board Connector P1 (Cont'd)

SIGNALS	CONNECTOR PINS		SIGNALS
	81	82	
IPCH/RD*	83	84	IPCH/WRT*
CHIP/RD*	85	86	CHIP/WRT*
CHIP/LIO	87	88	CHIP/HIO
CHIP/SPCHRQ*	89	90	IPDT/RD*
IPDT/WRT*	91	92	DTIP/CHARINT*
	93	94	
IPCS/CSWRT*	95	96	
	97	98	IPCS/LCSDIN*
DTIP/DDTHALT*	99	100	EXCH/NOPCCS*
GND	101	102	EXCH/CCSENB
CS/CSAPERR	103	104	GND
MCCH/ADDBKPT	105	106	MCCH/ABS
OPIP/OPTINT	107	108	IPOP/RD*
OPIP/TESTOP*	109	110	IPOP/WRT*
IPIB/RD*	111	112	IPIB/SELQ*
IBIP/XINQF	113	114	IPIB/WRT*
	115	116	
	117	118	
GND	119	120	MCBCCD/CLK*

SPARES (common to OPT,CCD,IPU) = 10

Table 2.13 CCD Board Connector P2

SIGNALS	CONNECTOR PINS		SIGNALS
GND	01	02	IOBUS<00>*
IOBUS<01>*	03	04	GND
IOBUS<02>*	05	06	IOBUS<03>*
GND	07	08	IOBUS<04>*
IOBUS<05>*	09	10	GND
IOBUS<06>*	11	12	IOBUS<07>*
GND	13	14	IOBUS<08>*
IOBUS<09>*	15	16	GND
IOBUS<10>*	17	18	IOBUS<11>*
GND	19	20	IOBUS<12>*
IOBUS<13>*	21	22	GND
IOBUS<14>*	23	24	IOBUS<15>*
GND	25	26	GND
IOBUS<PARITY>*	27	28	IOBUS<T0>*
GND	29	30	IOBUS<T1>*
IOBUS<T2>*	31	32	GND
IOBUS<T3>*	33	34	IOBUS<SVO>*
GND	35	36	IOBUS<SVI>*
IOBUS<STI>*	37	38	GND
IOBUS<HIRQ>*	39	40	IOBUS<LIRQ>*
GND	41	42	IOBUS<PADI>*
IOBUS<PADO>*	43	44	GND
IOBUS<EOT>*	45	46	IOBUS<ODD>*
GND	47	48	IOBUS<IORST>*
IOBUS<RCI>*	49	50	GND
N.C.	51	52	N.C.
N.C.	53	54	N.C.
DTPM/DATA+	55	56	DTPM/DATA-
DTPM/DATARDY+	57	58	DTPM/DATARDY-
DTPM/SHRQ+	59	60	DTPM/SHRQ-
PMI DTPM/SEL+	61	62	DTPM/SEL-
PMDT/RSTEN+	63	64	PMDT/RSTEN-
PMDT/SHLT+	65	66	PMDT/SHLT-
PMDT/DATA+	67	68	PMDT/DATA-
DTPM/SHENB+	69	70	DTPM/SHENB-
PMDT/HIBAUDSEL+	71	72	PMDT/HIBAUDSEL
MCBCCD/XTALCLK*	73	74	
MCDT/MAPPE	75	76	MCDT/MAPE
MCDT/MAPAPE	77	78	MCDT/WDPE
PWARN*	79	80	

Table 2.13 CCD Board Connector P2 (Cont'd)

SIGNALS			CONNECTOR PINS		SIGNALS	
		GND	81	82	GND	
		GND	83	84	GND	
		GND	85	86	GND	
		GND	87	88	GND	
		GND	89	90	GND	
		GND	91	92	GND	
		GND	93	94	GND	
POWER		GND	95	96	GND	
		GND	97	98	GND	
		GND	99	100	GND	
		Vcc	101	102	Vcc	
		Vcc	103	104	Vcc	
	IPS	Vcc	105	106	Vcc	IPS
		Vcc	107	108	Vcc	
		Vuu	109	110	Vuu	
	UPS	Vuu	111	112	Vuu	UPS
		Vuu	113	114	Vuu	
		Vcc	115	116	Vcc	
	IPS	Vcc	117	118	Vcc	IPS
		Vcc	119	120	Vcc	

SPARES (common to OPT,CCD,IPU)= 74,80

2.4.4 Memory Board (MEM)

The board layout is shown in Figure 2-5, and connector pin assignments are listed in Table 2.14 (P1), Table 2.15 (P2). Refer to Table 2.10 for J1, and Table 2.11 for J2 for connector pin assignments.

a. Board type: NonStop II PC outline, modified (indicators and switches replace J3 connector); four layer.

b. Power: +5VDC (IPS) 0.6A, +5VDC (UPS) 1.8A, -12VDC 1.4A, active

c. Contents: 256 x 22 dynamic RAM memory array, drivers, timing, control.

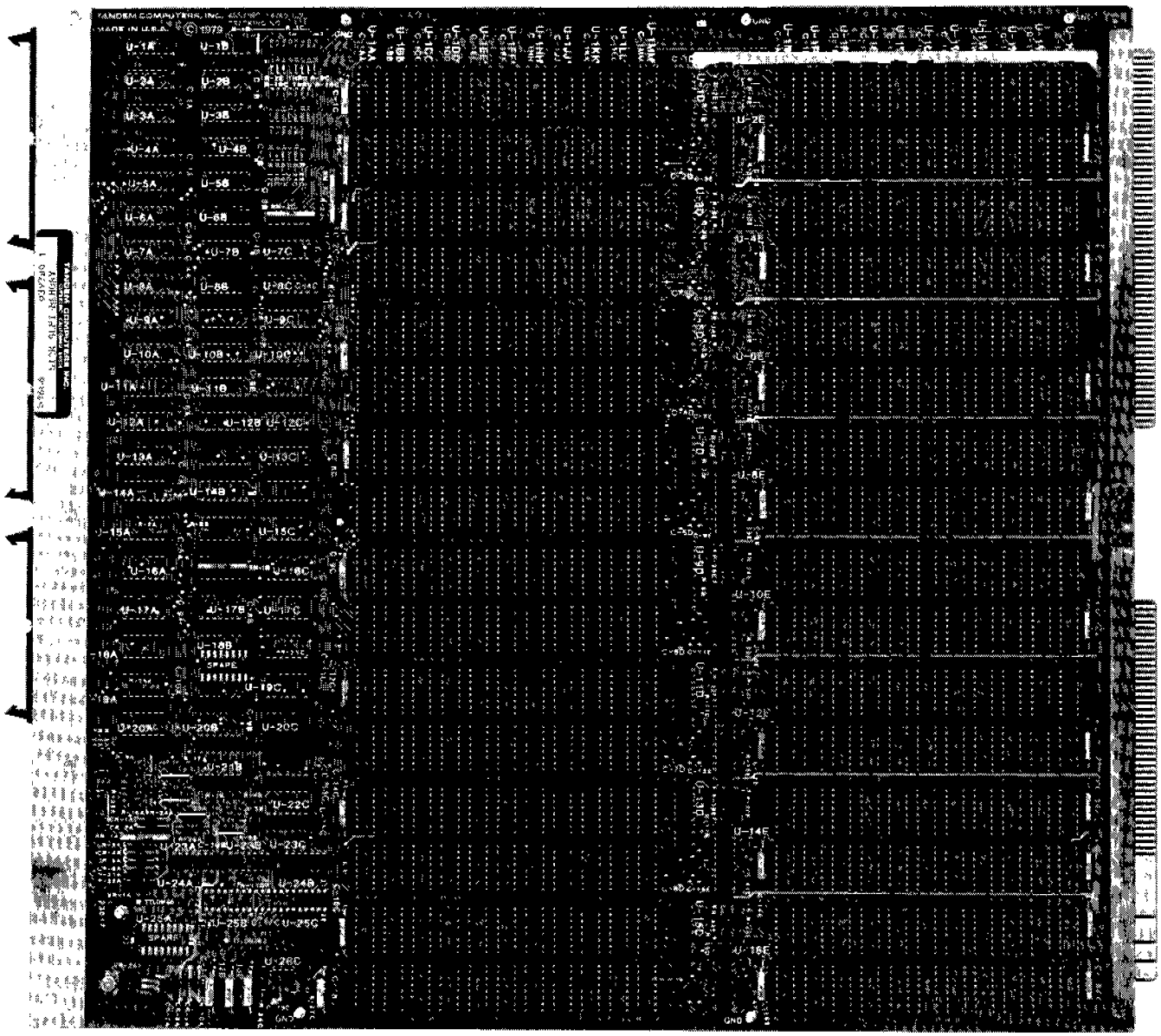

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Figure 2-5 Memory Board (MEM)

Table 2.14 Memory Board Connector P1

SIGNAL	CONN PINS		SIGNAL
GND	01	02	
	03	04	GND
	05	06	
	07	08	
	09	10	
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
GND	31	32	
	33	34	GND
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
NO CONNECT	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
			→

Table 2.14 Memory Board Connector P1 (Cont'd)

SIGNAL	CONN PINS		SIGNAL
GND	71	72	
	73	74	GND
	75	76	
	77	78	
	79	80	
	81	82	
	83	84	
	85	86	
	87	88	
	89	90	
	91	92	
	93	94	
	95	96	
	97	98	
	99	100	
GND	101	102	
	103	104	GND
	105	106	
	107	108	
	109	110	
	111	112	
	113	114	
	115	116	
	117	118	
GND	119	120	

Table 2.15 Memory Board Connector P2

SIGNALS	CONNECTOR PINS	SIGNALS
GND	01 02	
	03 04	GND
	05 06	
	07 08	
	09 10	
NO CONNECTION	11 12	
	13 14	
	15 16	
	17 18	
	19 20	
	21 22	
	23 24	
	25 26	
	27 28	
	29 30	
	31 32	
	33 34	
	35 36	
	37 38	
	39 40	
	41 42	
	43 44	
	45 46	
GND	47 48	
	49 50	GND
	51 52	
	53 54	
	55 56	
	57 58	
	59 60	
	61 62	
	63 64	
	65 66	
	67 68	
	69 70	
	71 72	
	73 74	
	75 76	
	77 78	
	79 80	
		→

Table 2.15 Memory Board Connector P2 (Cont'd)

SIGNALS			CONNECTOR PINS		SIGNALS	
		GND	81	82	GND	
		GND	83	84	GND	
		GND	85	86	GND	
		GND	87	88	GND	
		GND	89	90	GND	
		GND	91	92	GND	
		GND	93	94	GND	
POWER		GND	95	96	GND	
		GND	97	98	GND	
		GND	99	100	GND	
		Vcc	101	102	Vcc	
		Vcc	103	104	Vcc	
	IPS	Vcc	105	106	Vcc	IPS
		Vcc	107	108	Vcc	
		Vuu	109	110	Vuu	
	UPS	Vuu	111	112	Vuu	UPS
		Vuu	113	114	Vuu	
		Vdd	115	116	Vdd	
	UPS	Vdd	117	118	Vdd	UPS
		Vdd	119	120	Vdd	

2.5 CONTROL PANEL

a. Board type: 3 inch x 18 inch (7.62cm x 45.72cm), four layer.

b. Power: +5VDC (IPS) 1A, +5VDC (UPS) 0A, -12VDC 0A.

c. Contents: control panel switch and indicator interfaces, software licensing firmware.

2.6 PMI PATCH PANEL

a. Power: +5VDC (IPS) 2A from IPB regulator.

b. Contents: maintenance interface common logic, system halt logic

2.7 TEST PANEL

a. Board Type: 12 inch x 16 inch (30.48cm x 40.64cm),four layer.

b. Complexity: 80 ICs, 40 switches, 80 indicators.

c. Power: Self-contained 5V supply; operates from 110 VAC

d. Contents: controls and displays for operating microdiagnostics, and examining hardware and firmware operation. This is implemented as a development tool, not as a product needed by customers or by hardware/software support.

2.8 INTERCONNECTIONS

The IPU, MCB, CCD, and one or more MEM boards which make up one processor are interconnected by backpanel wiring and by flat cables, which connect to the front edge connectors of the boards. Connection of the processor to the interprocessor bus, the IOBUS, the control panel, to the power supply, I/O Terminator Board, and to the PMI patch panel is made through flat cables which plug onto the backpanel connector pins. Connection between the processor and the test panel (not present in an installed system) is made through special cabling to the front edge connectors.

2.9 BACKPANEL CONNECTIONS

Each of the P1 and P2 backpanels consists of a 2-layer PC board and eight integral 120-pin edge connectors with wirewrap tails in a 0.100 x 0.100 inch grid pattern.

The P1 (upper) backpanel provides straight-across PC signal interconnections among the MCB, IPU, CCD, and OPT slots and wirewrap posts at the MCB slot for plugging on the X and Y interprocessor buses. Jumpers provide the processor with its identifying processor number within the system. Refer to Figure 2-6.

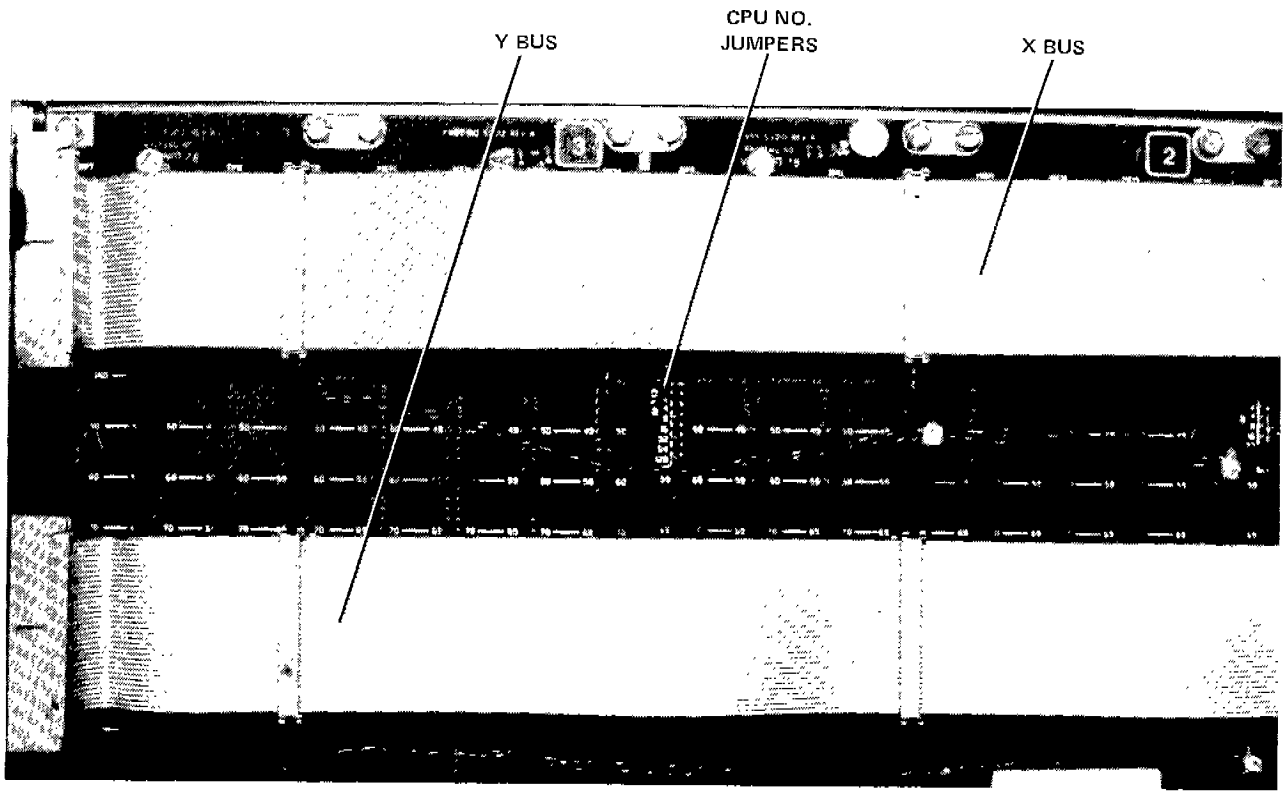


Figure 2-6 P1 Backpanel (Rear View)

The P2 (lower) backpanel (refer to Figure 2-7) provides the following:

a. Vcc (+5V IPS), Vuu (+5V UPS), Vdd (+12V UPS), and Vss (ground) DC power connections to all eight slots

b. Straight-across signal interconnections among the MCB, IPU, CCD, and OPT slots

c. Clock connections (not straight across) from the MCB to itself and to the IPU, CCD, and OPT slots

d. Wrap posts as follows:

   1. At the IPU slot for the control panel cable and the power-failure warning (PWARN) cable

   2. At the MCB for I/O terminator power

   3. At the CCD slot for the I/O bus cable

   4. At the CCD slot for the PMI cable.

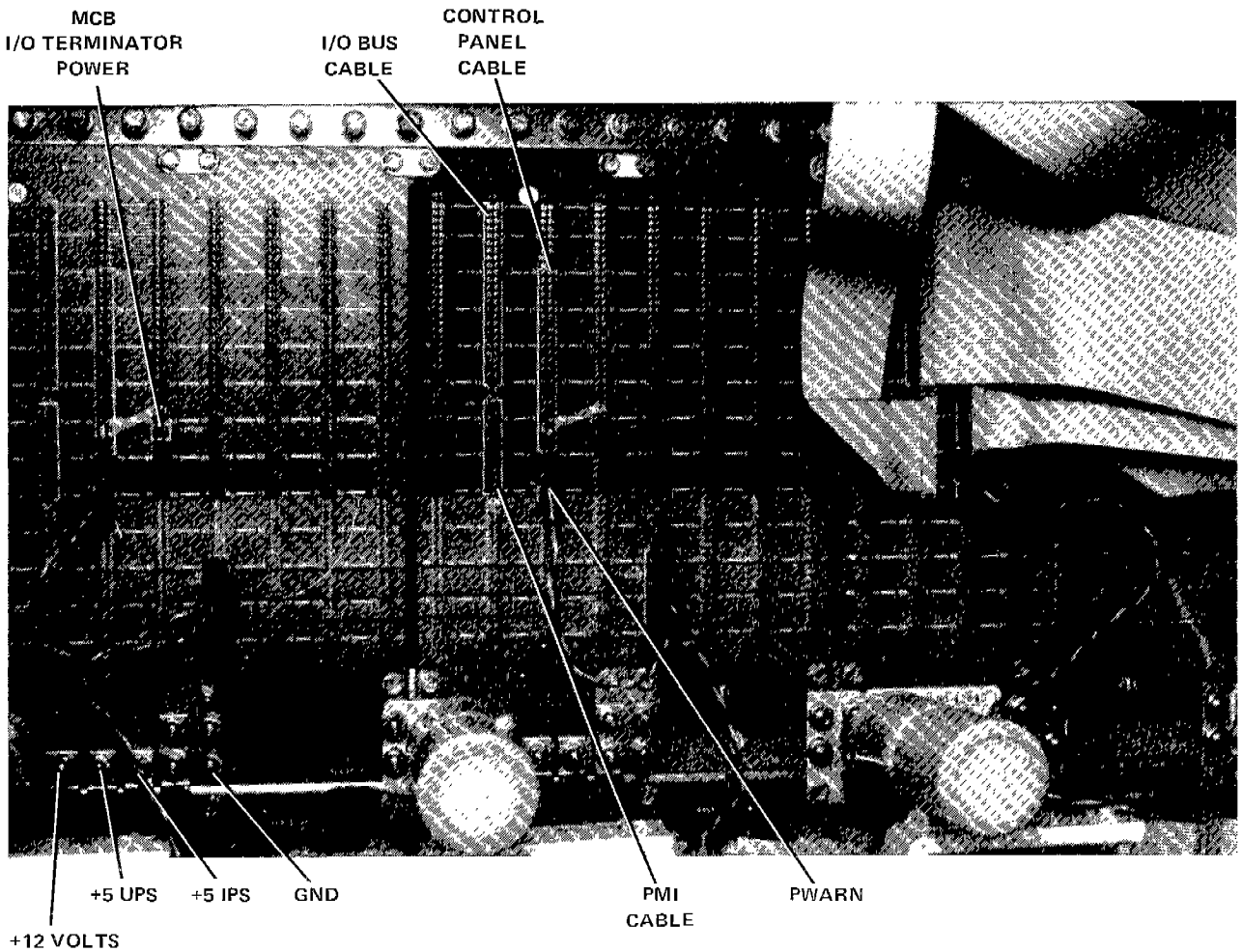


Figure 2-7 P2 Backpanel (Rear View)

A01

2.10 FRONT CABLES

Each of the J1-J4 front cables consists of a 60-conductor flat cable and 60-pin socket connector which mate to right-angle latching headers on the PC boards. Each cable contains 20 ground wires and 40 signal wires for straight-across interconnections.

SECTION 3
FUNCTIONAL DESCRIPTION

3.0 FUNCTIONAL DESCRIPTION

The following functional description addresses only the hardware portion of the processor subsystem. Refer to System Description Manual Part Number 82077 for detailed information on software related functions such as microinstructions format, microcode, and microprogramming sequencing.

The scope of Section 3 is to provide the user with a brief functional overview of the processor subsystem. For example, this section includes a brief, overall functional description of the processor subsystem, the function of each board and component within the subsystem, and finally how these boards and components are interfaced within the subsystem. Refer to Functional Description Manual T16/8800 for detailed functional description of the processor subsystem. Figure 3-9 at the end of this section shows an overall functional block diagram of the processor subsystem.

The Tandem NonStop II TM processor subsystem is organized as follows. The functional description is organized in a similar manner.

a. Instruction Processing Unit (IPU).

   This board includes the hardware for register files, ALU, shifter, microprocessor address register, instruction register, and instruction decoding. (The IPU can be considered as the CPU of the processor subsystem.)

b. Memory Control Board (MCB).

   This board includes the hardware for memory request control, address translation map, memory ECC, address trap comparator, refresh timer, processor clock, interprocessor bus control, and interval timer.

c. Channel, Control Store, DDT (CCD).

   This board includes hardware for the I/O channel, control store array, and diagnostic data transceiver.

d. Memory (Semiconductor).

   This board includes the 256 x 22 (16 rows with 22 16K RAMs in each row) dynamic RAM array, drivers, and timing control.

e. Control Panel.

The control panel contains panel switches, LED interfaces, and software licensing hardware.

NOTE

Subsystems a) through d) are mounted in their respective slots in the processor card cage of the processor cabinet. The control panel is mounted on the front door of the processor cabinet.

3.1 INSTRUCTION PROCESSING UNIT (IPU)

The Instruction Processing Unit (IPU) is the principal control unit for the processor. Under control of a microprogram resident in the control store, the IPU communicates with the I/O channel, the memory control, the diagnostic data transceiver, the test panel (depot level use only), and the interprocessor bus; and it can read or write selected words of the control store under microprogram control. Through the memory control the IPU communicates with software residing in main memory, fetching, interpreting, and executing instructions. Refer to Figure 3-1.

3.1.1 Internal and External Buses

The internal and external buses of the IPU are listed in Table 3.1. Refer to Table 3.2 for a listing of the microprogram sequencer components and their function.

Table 3.1 Internal/External Buses

BUS	FUNCTION
J BUS	JBUS.<0:15,PL,PR,PV> ,within the IPU only
IK BUS	IKBUS.<0:15,PL,PR,PV> ,internal K bus
KBUS	KBUS.<0:15,PL,PR> ,external K bus
L BUS	Alu output BUS.<0:15>,within the IPU only
IM BUS	Internal MBUS.<0:15,PL,PR,PV>,within the IPU only.
M BUS	MBUS.<0:15,PL,PR,PV>, only drives loads external to the IPU.
ROMA BUS	Rom address bus to control store, ROMA.<0:15>
MAPA BUS	Map address bus to memory control unit MAPA.<0:3>
P BUS	Low asserting bidirectional bus between the control panel and IPU, PBUS.<0:15>

Table 3.2 Microprogram Sequencer

REGISTER	FUNCTION
ROMA	Rom address register/counter for microinstructions.
RMD	Rank 1 control store data register where J & K microop fields are decoded and executed.
RME	Rank 2 control store data register where the microinstruction is executed.
RETURN	Microsubroutine return address register/counter.

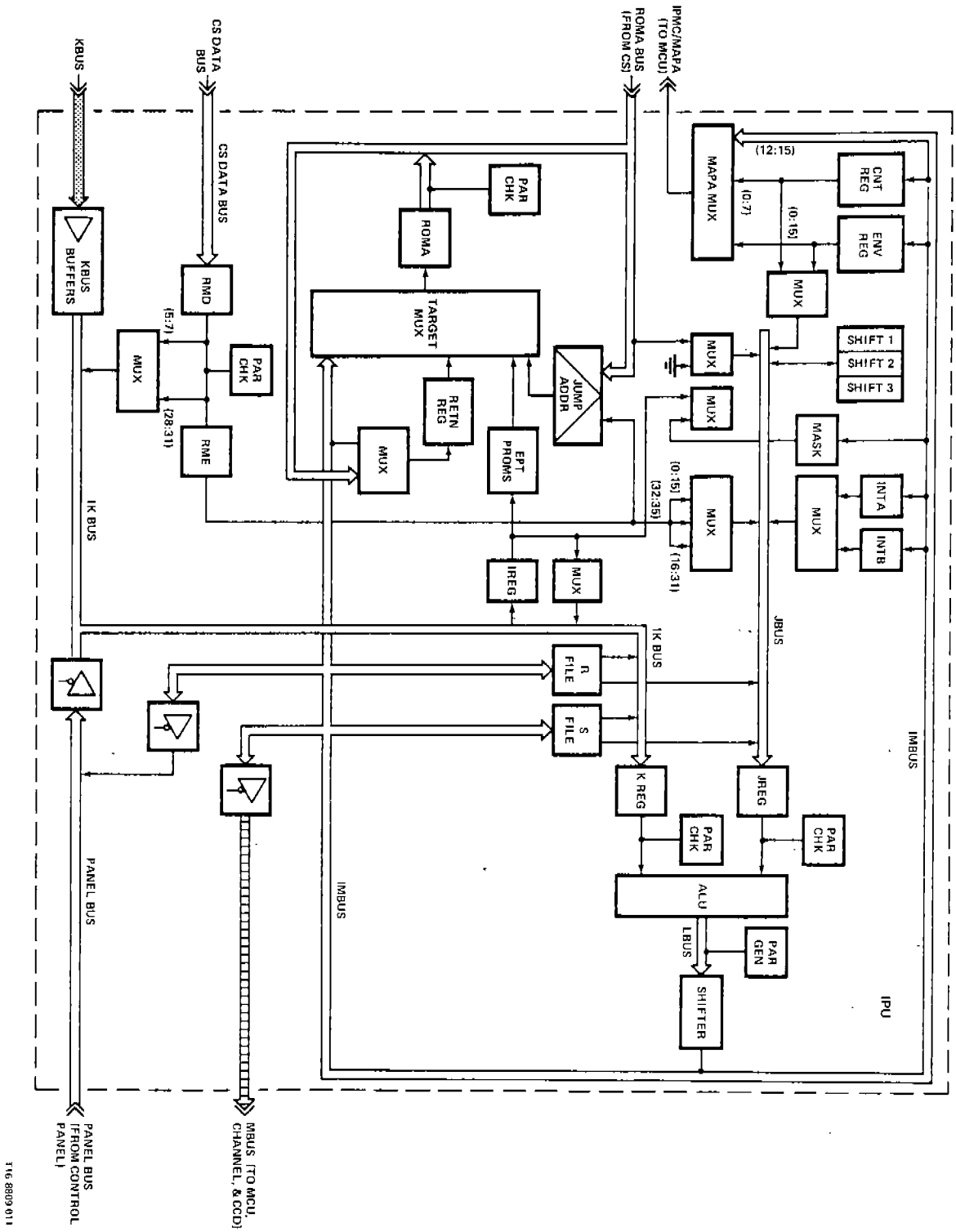


Figure 3-1 IPU Functional Block Diagram

3.2 I/O CHANNEL (CHANNEL)

The channel allows I/O controllers on the IOBUS to communicate with memory and with the IPU. The channel is a microprogrammed processor which functions as IOBUS controller, as a port into the memory control, and as an interface to the IPU. It is able to accept reconnect requests from device controllers on the IOBUS as well as requests for I/O service from the IPU. These requests are accepted under microprogram control only since the channel is not interruptible; the channel, however does have the ability to interrupt the IPU to make special requests for service or to report exceptional conditions. Refer to Figure 3-2 for the channel data paths.

The channel provides status information to the Diagnostic Data Transceiver to assist in diagnosis of gross failures.

3.2.1 Channel Structure

The I/O channel is a bus-organized microprocessing unit. It consists of the control unit and a set of registers.

3.2.1.1 Buses.

The I/O channel communicates internally over the CBUS: with the memory control via the CBUS and the CMAPA bus; with the IPU via the MBUS and KBUS; and with the I/O controllers via the IOBUS.

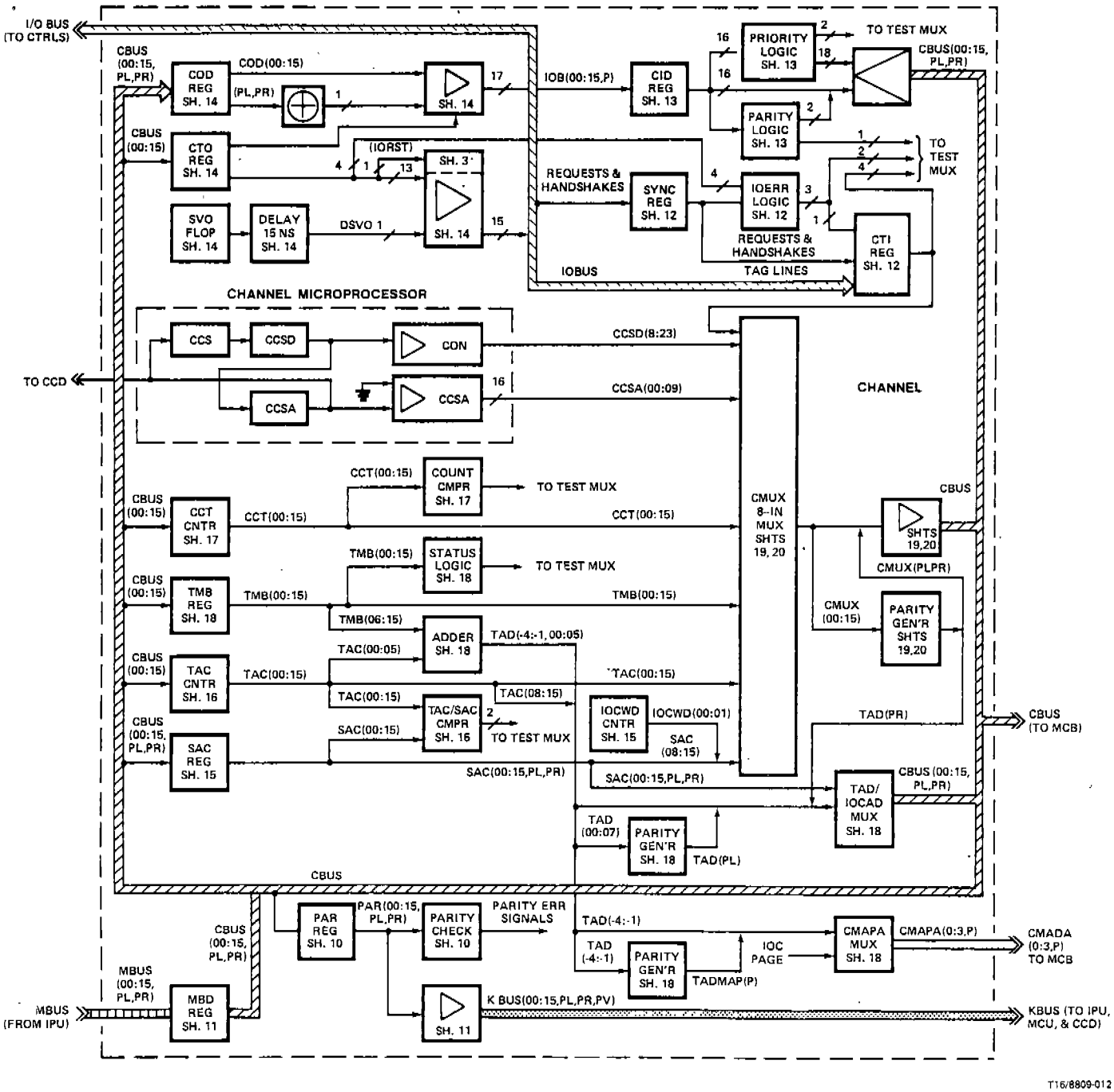


Figure 3-2 Channel Data Paths

3.3 MEMORY CONTROL (MCB)

The memory control provides access to memory for both the channel and the IPU. It arbitrates memory requests; pipelines address, data, control and error information; maps logical addresses into physical addresses; provides error checking and correction on data transfers from memory; and controls the timing of refresh operations on semiconductor memory.

The memory mapping unit maps 20-bit logical addresses into 23-bit physical addresses.

Data (16-bit) are coded by the MC in a 22-bit single-error-correcting, double-error-detecting code for storage in main memory. The MCU checks parity on data and addresses from the channel and from the IPU. Parity errors are reported to the IPU, the channel, and the Diagnostic Data Transceiver.

3.3.1 Map/Memory Control

The Map/Memory Control Unit (MCU), which resides on the MCB board, consists of MAP access hardware and Memory access hardware. The MAP machine arbitrates the Instruction Processing Unit (IPU) MAP requests for MAP READS(MR), MAP WRITES (MW), PROCESSOR CODE READS (PCR), PROCESSOR DATA READS (PDR), and PROCESSOR DATA WRITES (PDW); and Channel MAP requests for CHANNEL READS(CR) and CHANNEL WRITES(CW).

The Memory machine arbitrates between MAP memory requests and REFRESH memory requests (made by a timer internal to the MCU). The memory machine also does single error correction (SEC) and double error detection (DED) on read data, and single error detection (SED) on memory read addresses. Refer to Figure 3-3 for the Memory Control Unit data paths.

3.3.2 Interprocessor Bus (IPB) Control

The IPB control, which also resides on the MCB board, handles the sending and receiving of packets over the two interprocessor buses (X bus and Y bus). The IPB provides separate input and output buffers for each bus and is capable of sending and receiving over the X bus at the same time it is sending and receiving over the Y bus. Refer to Figure 3-4 for the IPB Control data paths.

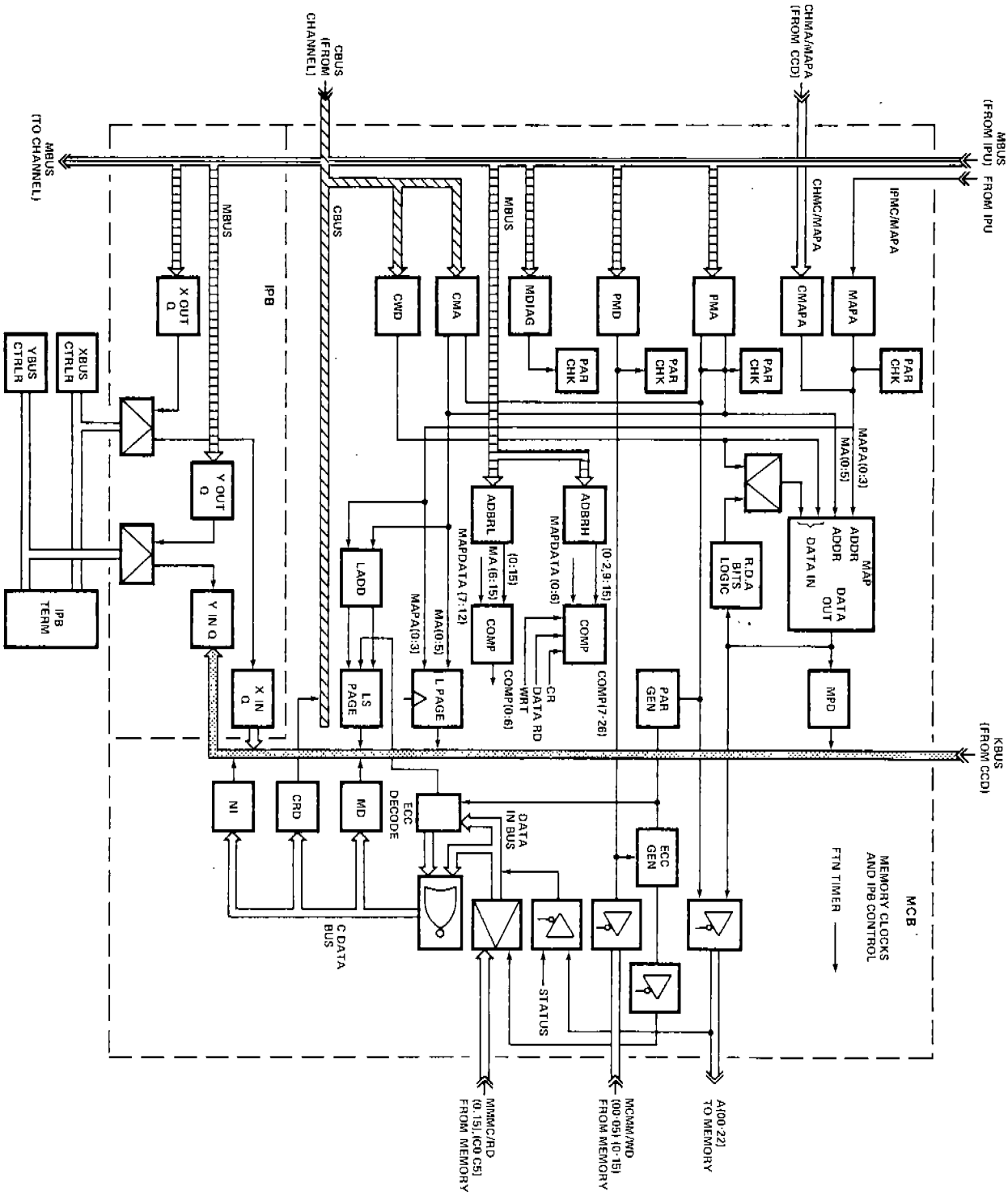


Figure 3-3 Memory Control Unit Data Paths

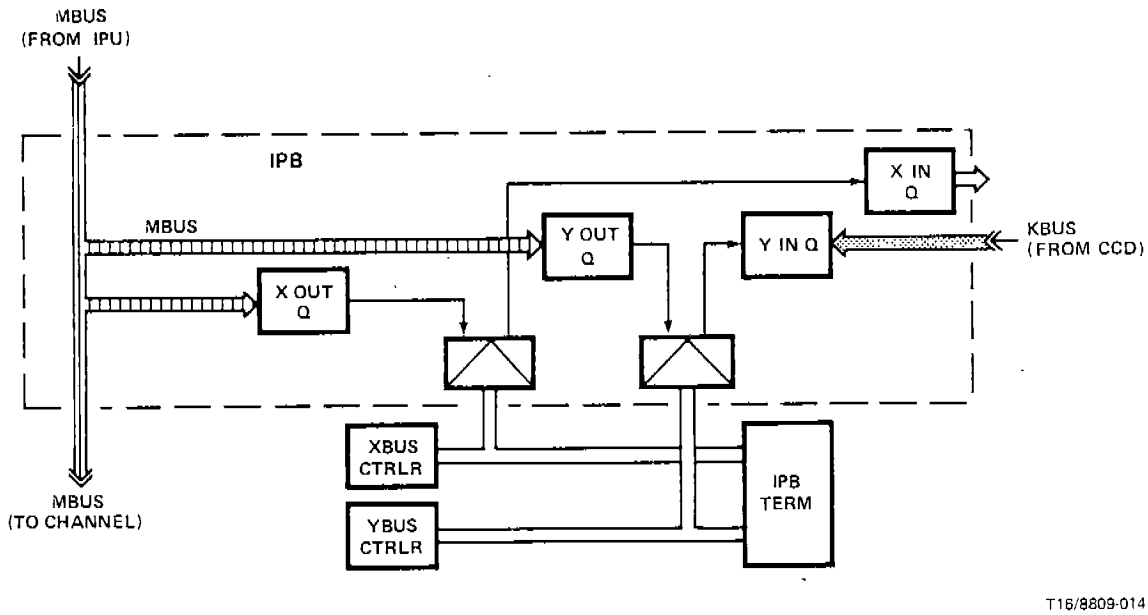
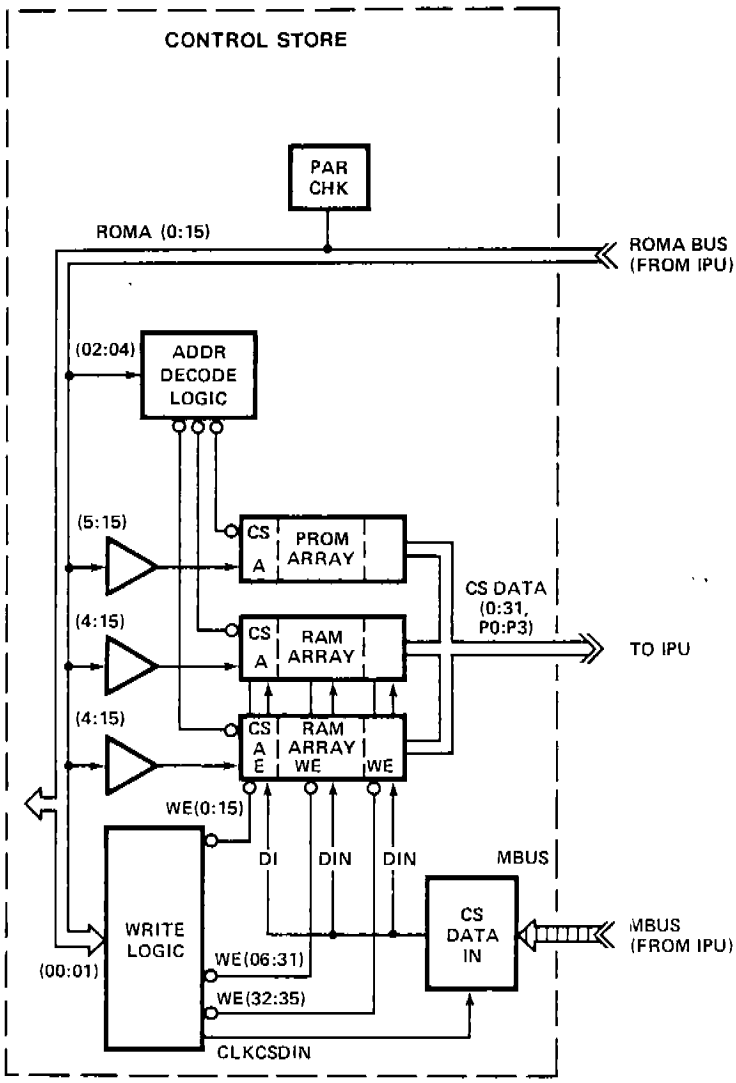


Figure 3-4 IPB Control Data Paths

3.4 CONTROL STORE (CS)

The Control Store (CS) resides on the CCD board and is the storage element for the microprogram executed by the IPU. The majority of the CS is Writable Control Store (WCS). It is 36 bits wide: 32 data bits and 4 data parity bits. The maximum address space is 16K. CS address parity checking is done on ROMA.<0:15>. The data path is shown in Figure 3-5.



T16/8809-015

Figure 3-5 Control Store Data Path

3.5 DIAGNOSTIC DATA TRANSCEIVER (DDT)

The Diagnostic Data Transceiver (DDT) resides on the CCD board and provides communication between the processor and the rest of the system through the PMI patch panel, which in turn provides communication with a local or remote operator through an Operations and Service Processor (OSP). The DDT permits the operator to examine processor status information which will give indication of hardware failures. It also provides two-way communication between the microprogram and the operator for system software debugging. If appropriately enabled, the DDT permits the operator to reset and cold load the processor, and it permits one processor in the system to suspend the operation of other processors (under microprogram and software control). Refer to Figure 3-6 for the DDT data paths.

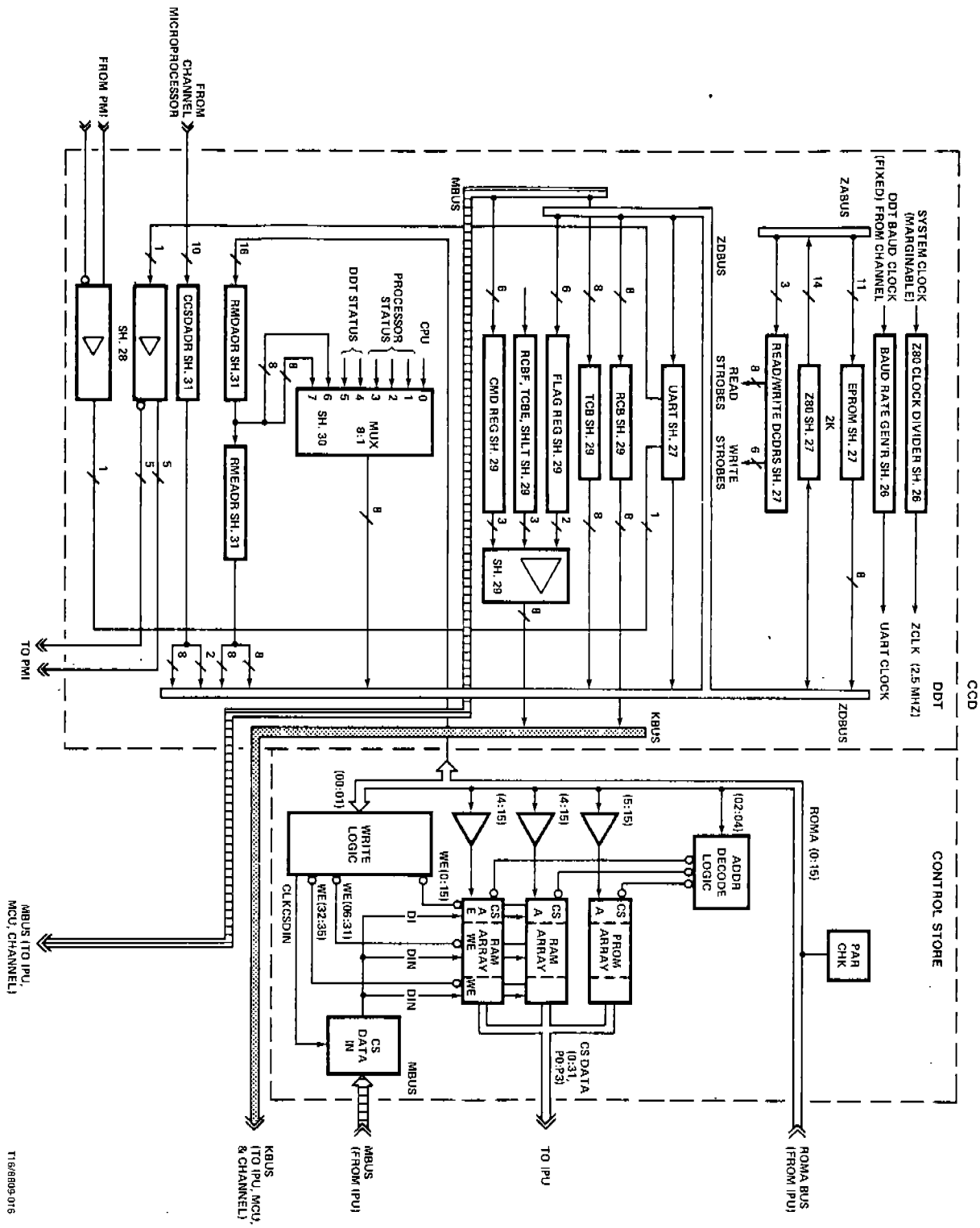
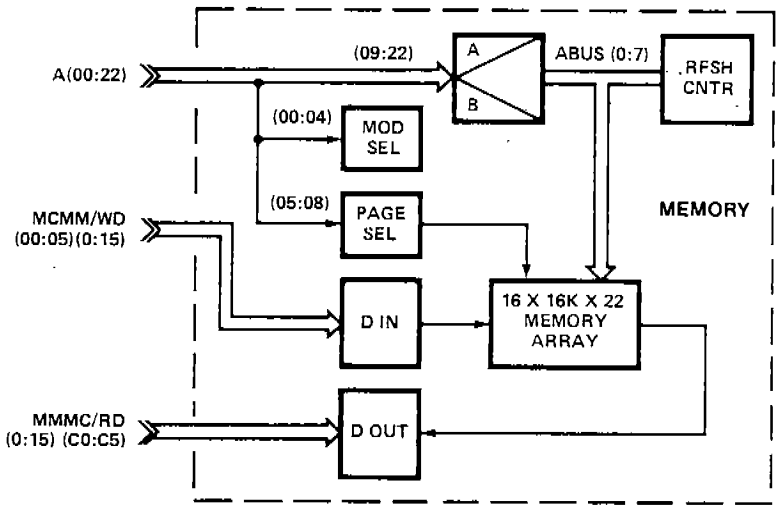


Figure 3-6 DDT Data Paths

3.6 MEMORY (MEM)

Main memory is organized in 256 Kword modules. Up to eight Mword addressability is provided. MOS dynamic RAM technology is used, with an uninterruptible (battery) power supply ensuring memory integrity in the event of power interruptions. (Core memory is not available in a NonStop II processor.) Refer to Figure 3-7 for memory data paths.



T16/8809-017

Figure 3-7 Memory Data Paths

3.7 CONTROL PANEL

The control panel is an interface between an operator and the NonStop II CPU and enables an operator to reset, cold load a processor, and run some processor microdiagnostics. Refer to Figure 3-8 for control panel data paths.

The NonStop II control panel contains the following:

a. A bank of sixteen yellow LEDs for data output.

b. A bank of sixteen toggle switches for data input.

c. A Reset/Load switch (activated by the cabinet door key).

d. A green Power LED.

e. A green Run LED.

f. A Power Warn/Halt switch (inside door).

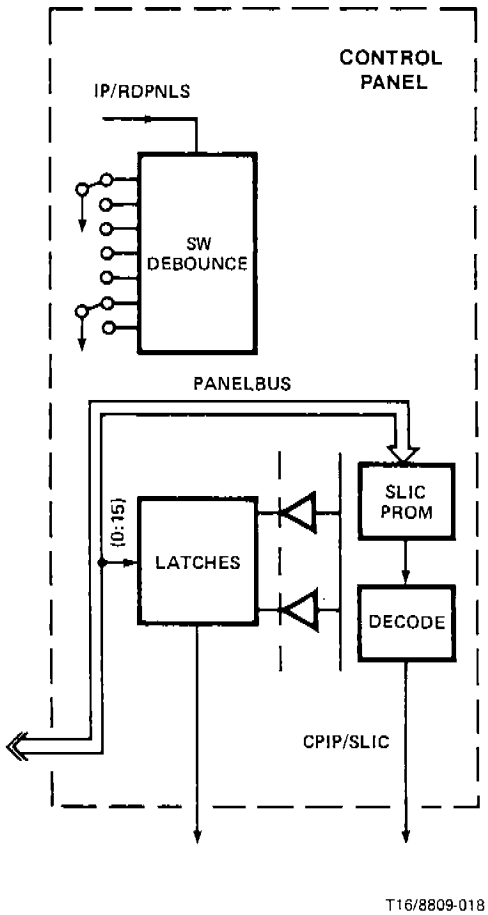


Figure 3-8 Control Panel Data Path

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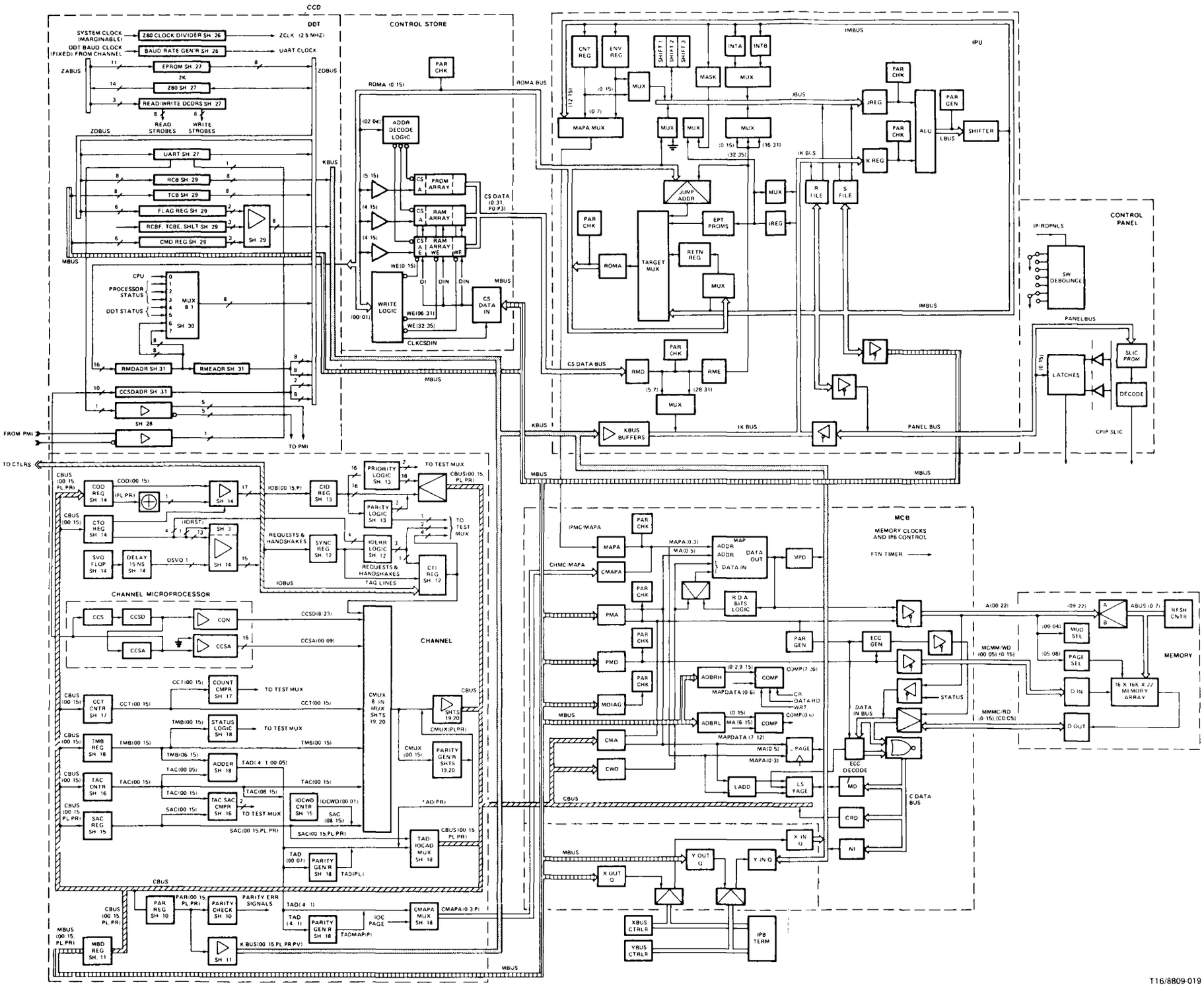


Figure 3-9 Processor Subsystem Functional Block Diagram

SECTION 4
INSTALLATION

4.0 INSTALLATION

The following procedure includes installation of a new board.

4.1 INSTALLING AN MCB, CCD, MEMORY, OR IPU BOARD

To install one of the above named boards perform the following:

NOTE 1

Large boards should NOT be inserted in their slot using the PCB hold-down screw. Over tightening of this screw can break traces or cause seating problems. Use the hold-down screw to start the board into the connectors; then, push the board in from the front until it is seated into the connector. The hold-down screw should only be "finger tight".

NOTE 2

When installing a new Memory board set the address for that memory board in accordance with Table 4.1.

a. Install the new board by carefully sliding it in from the front of the system cabinet. Make sure that rear edge connectors P1 and P2 are lined up properly and slowly tighten the PCB hold down screw in the rear of the cabinet.

b. Connect the jumpers to the appropriate front-edge connectors.

c. Restore DC power to the processor taken off-line.Refer to paragraph 5.2.9.

d. Restore the processor to full operation. Refer to paragraph 5.2.7.

Table 4.1 Address Switch Settings

MEMORY BD. NO.	ADDRESS %	SWITCH POSITION 1	2	3	4	5	6
1	00	C	O	O	O	O	O
2	01	C	O	O	O	O	C
3	02	C	O	O	O	C	O
4	03	C	O	O	O	C	C

O = OPEN (Binary 0)
C = CLOSED (Binary 1)

See NOTE 3

NOTE 3

Switch 1 is BOARD ENABLE and must be closed to enable reading and writing to the board.

4.2 INSTALLING AN I/O TERMINATOR BOARD

To install the I/O terminator board perform the following:

a. Install the I/O bus cable to connector J2 and the DC power cable to connector J1.

b. Secure the I/O terminator to the I/O bus cable with a cable tie.

c. Apply DC power to the appropriate processor module in accordance with paragraph 5.2.6.

d. Verify that the power indicator LED is lit.

e. Reload processor in accordance with paragraph 5.2.7.

4.3 INSTALLING AN IPB TERMINATOR BOARD

To install an IPB Terminator Board perform the following:

a. Take the appropriate bus X or Y bus off-line in accordance with paragraph 5.1.6.

b. Install the replacement IPB Terminator Board to the stand-offs, and secure it with the two slotted screws.

c. Connect the bus cable to connector J2 on the IPB Terminator Board.

d. Place the appropriate X or Y Bus on-line (paragraph 5.2.8). The <from processor> and <to processor> must be specified as -1.

4.4 INSTALLING AN OPERATOR CONTROL PANEL ASSEMBLY

a. Install the new control panel assembly to the front door of the system cabinet and secure in place with the three slotted screws.

b. Connect the flat ribbon cable from backplane to the operator control panel.

c. Apply DC power to the appropriate processor module in accordance with paragraph 5.2.6.

d. Reload the processor in accordance with paragraph 5.2.7.

4.5 PACKING AND SHIPPING OF REPLACEABLE COMPONENTS

Refer to Operational Guide Lines for procedures on how to pack and reship replaceable items for depot or factory repair and on how to fill out an IR.

SECTION 5
CORRECTIVE MAINTENANCE

5.0 CORRECTIVE MAINTENANCE

The corrective maintenance approach used on a processor module is dictated by the type of failure and by the degree of redundancy that exists. In general, processor failures can be categorized as follows:

a. Internal CPU failures

b. I/O Channel failures

c. Memory failures

d. IPB failures

The initial indication of a failure in a processor module is typically in the form of an error message (refer to Users Guide T16/8801 for a listing of error messages). In many cases, the information provided by such a message is adequate for localizing a particular failure to a major hardware component of a processor module. For example, MCB, CCD, IPU, Memory, Interprocessor Bus. Those failures that are not as easily defined may warrant the use of one or more diagnostic programs.

The C.E. should evaluate the effect of a failure on the system as a whole prior to initiating any corrective action. In a system that employs little or no redundancy, a processor failure may have a dramatic effect on system operation. The primary maintenance objective in such cases is to administer the necessary corrective action in an expeditious manner. In systems that employ some degree of hardware or software redundancy in an effort to ensure Non-Stop operation, a processor failure will disable a part, but not all, of the system. In such cases, the maintenance objective is to administer the necessary corrective action without impacting the user operation any more than is absolutely necessary. To this end, the maintenance approach should be as follows:

a. Take any and all steps necessary to ensure that user application programs remain operational during the period of maintenance. In cases where a processor is rendered inoperable:

   1. All I/O controllers owned by the "down" processor will be taken over automatically by other operational processors.

2. NonStop processes will automatically revert to their respective back-up processes in other operational processors.

3. Processes that are not NonStop will have to be restarted in other operational processors.

b. Take off-line only that portion of the system necessary to perform maintenance.

c. Run the diagnostic programs, if necessary, to localize the failure.

d. Once the failure has been successfully localized, perform the appropriate corrective action.

e. Mount any disc volumes that were removed during the maintenance period.

f. Place on-line the portion of the system that was taken off-line for maintenance purposes. If diagnostic programs were used, it will also be necessary to place on-line the tape unit used to load the diagnostic programs.

g. Take the steps necessary to restore the system to its original configuration and level of performance.

1. Have the user restart any applications that may have been rendered inoperable due to the failure.

2. Assist the user in verifying the integrity of any disc volumes that may have been damaged as a result of the failure. This may involve reformatting or restoring entire volumes; refer to "RESTORING THE SYSTEM AFTER A DISC FAILURE" in Section 14 of the Tandem 16 Operating Manual, T16/8002.

5.1 REMOVAL

The following procedures include steps for removing a suspected malfunctioning board after a diagnostic routine has isolated the problem to a specific board.

5 1.1 Removing An MCB, CCD, MEMORY, or IPU Board

To remove an any one of the above named boards perform the following steps:

a. Take the appropriate processor module off-line (paragraph 5.1.7).

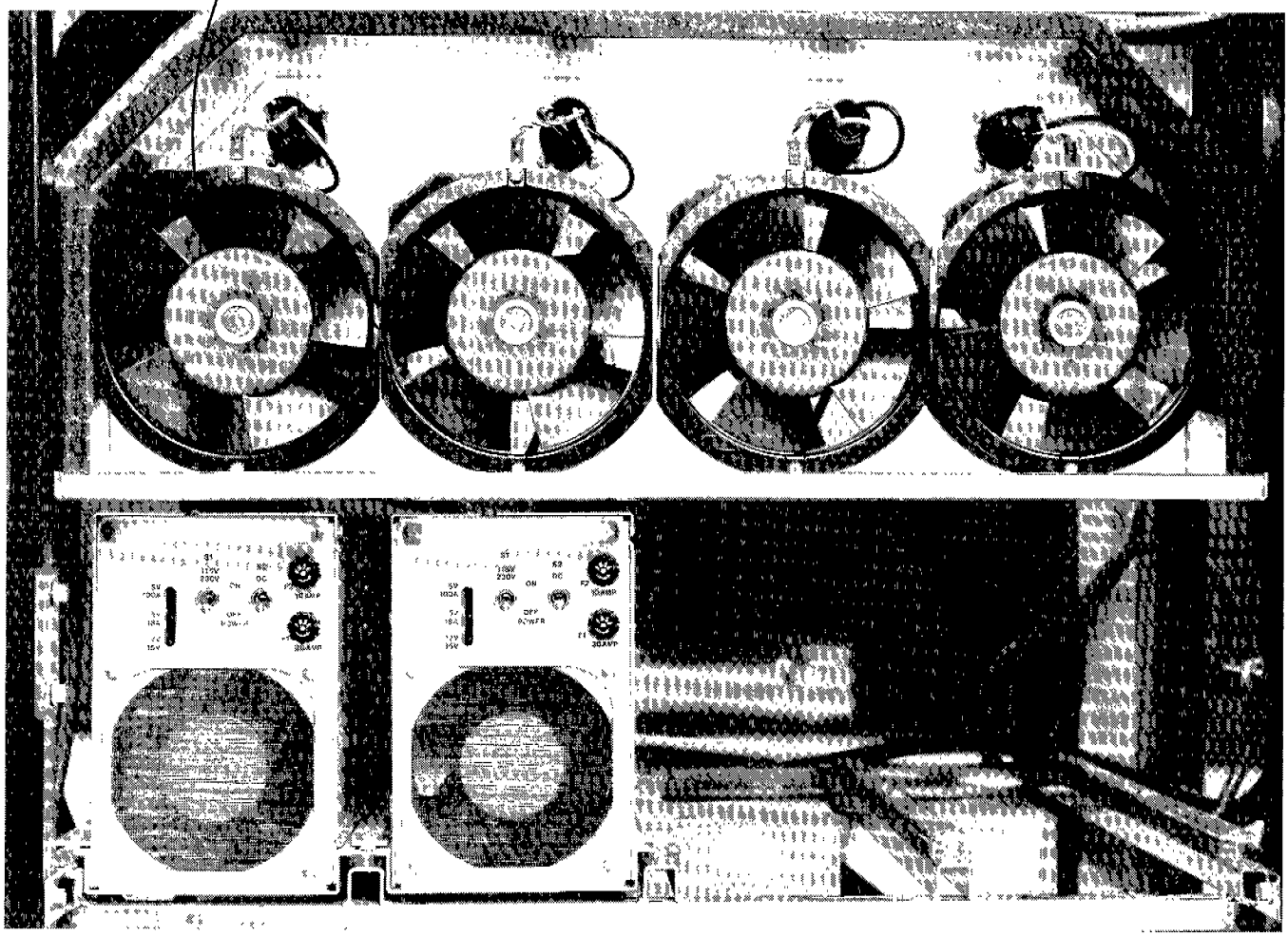
b. Remove DC power from the processor module taken off-line by placing the 115/230VAC Power and the DC Power switches on the associated T16/7301 DC Power Module in the OFF (down) position. Refer to Figure 5-1.

c. Remove the jumpers from the appropriate front-edge connectors. If necessary label jumpers/cables.

d. Loosen the PCB hold-down screw in the rear of the system cabinet and carefully remove the board from the front of the cabinet.

e. Refer to paragraph 5.2.1 for replacement procedure.

IMC Magnetics (Cage 28875)
P/N Model 12
NSN 440-00-136-7174



T16/8809-021

Figure 5-1 T16/7301 DC Power Module

5.1.2 Removing An IPB Controller Board.

To remove an IPB Controller Board perform the following:

a. Take the bus to which the IPB Controller is attached off-line (paragraph 5.1.6). The <from processor> and <to processor> must be specified as -1 ("down" entire bus).

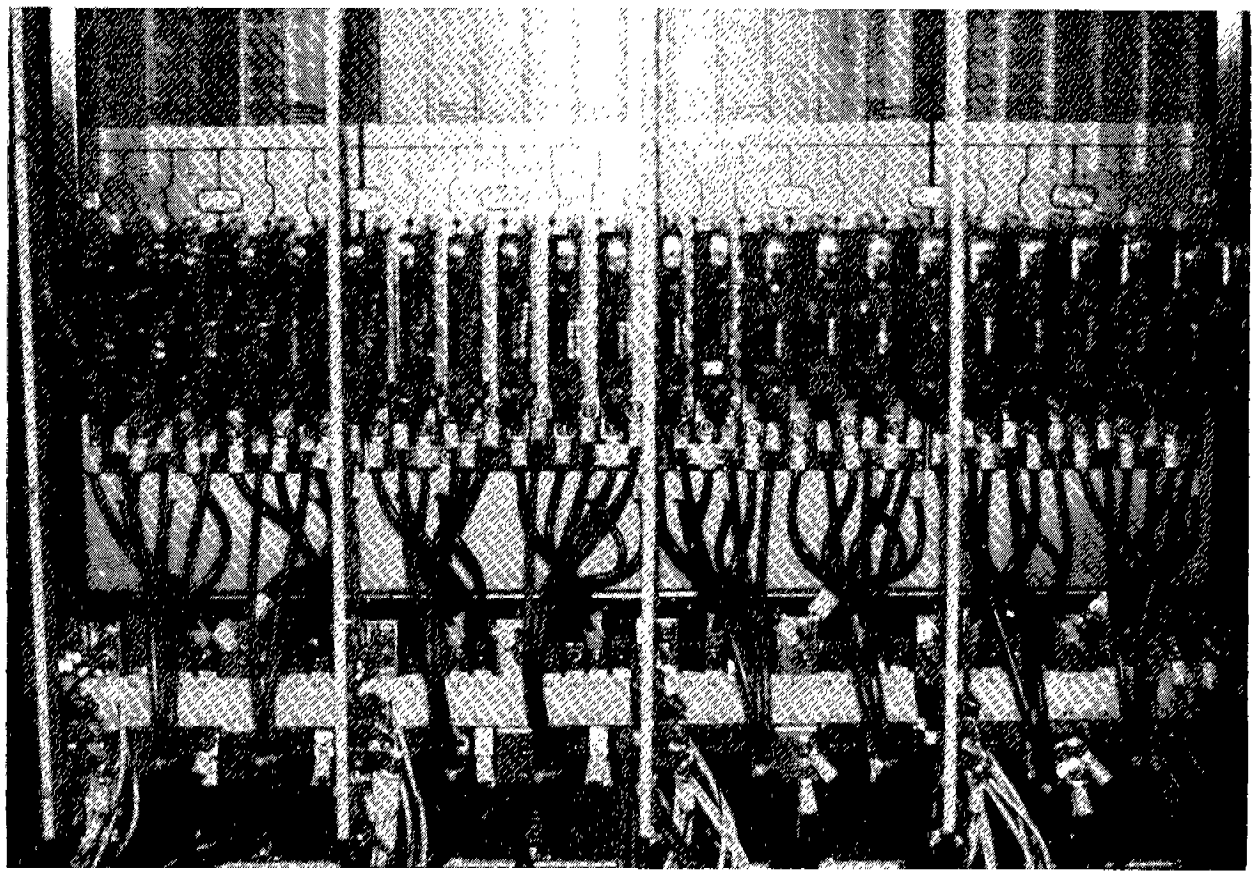
b. Remove DC power by placing the power switch on the power regulator card for this controller in the OFF (down) position. Refer to Figure 5-2.

c. Remove the bus cable from connector J1. Remove the DC power cable from connector J2. Remove the CPU select cables from connectors J100 through J115.

d. Release the plunger latch in the upper right-hand corner of the board.

e. Remove the two slotted screws that secure the board to the stand-offs. Carefully remove the board.

f. Refer to paragraph 5.2.2 for replacement procedure.



T16/8809-020

Figure 5-2 I/O Power Regulator

5.1.3 Removing An I/O Terminator Board.

To remove an I/O Terminator Board perform the following:

a. Take the appropriate processor module off-line (paragraph 5.1.7).

b. Remove DC power from the processor by placing the 115/230VAC Power and DC Power switches on the associated T16/7301 DC Power Module in the OFF (down) position. Refer to Figure 5-1.

c. Remove the I/O bus cable from J1 and the DC power cable from J2 on the I/O Terminator Board.

d. Cut the cable tie that secures the board to the I/O bus cable and remove the board.

e. Refer to paragraph 5.2.3 for replacement procedure.

5.1.4 Removing An IPB Terminator Board.

To remove an IPB Terminator Board perform the following:

a. Take the bus to which the IPB Terminator is attached off-line (paragraph 5.1.6). The <from processor> and <to processor> must be specified as -1.

b. Remove the bus cable from J1 on the IPB Terminator Board and remove the board.

c. Refer to paragraph 5.2.4 for replacement procedure.

5.1.5 Removing An Operator Control Panel Assembly.

To remove an Operator Control Panel Assembly perform the following:

a. Take the appropriate processor module off-line (paragraph 5.1.7).

b. Remove DC power from the processor taken off-line by placing the 115/230VAC Power and DC Power switches on the associated T16/7301 DC Power Module in the OFF (down) position. Refer to Figure 5-1.

c. Remove the flat ribbon cables from the control panel.

d. Remove the three slotted screws that secure the assembly to the front door of the system cabinet.

e. Remove the control panel assembly.

f. Refer to paragraph 5.2.5 for replacement procedure.

5.1.6 Take Interprocessor Bus Off-Line.

To take a Interprocessor Bus off-line perform the following:

a. Select a terminal with an executing Command Interpreter and enter the following command to "down" the desired bus:

```
{X} BUSDOWN <from processor>,<to processor>
{Y}
```

examples:

: X BUSDOWN 1,2

down the X-Bus from processor 1 to processor 2

: Y BUSDOWN -1,0

down the Y-Bus from all processors to processor 0

: X BUSDOWN 0,-1

down the X-Bus from processor 0 to all other processors

: Y BUSDOWN -1,-1

down the Y-Bus from all processors to all processors

b. The following console message is printed for the bus taken off-line:

```
20 {...} X Bus to processor n DOWN (BEL)
21 {...} Y Bus to processor n DOWN (BEL)
```

5.1.7 Take A Processor Module Off-Line.

When taking a Processor Module off line, try to choose a period of low activity and inform the user that you are going to bring the processor down.

Before taking the processor off line, perform the following:

a. Take the necessary steps to ensure that user processes currently running in the processor remain operational when it is taken off line.

   1. Execute the COMINT command PPD to determine which processes, if any, are currently running without backup.

   2. If there are any user processes operating without backup in the processor to be taken off line, notify the system manager, who can authorize their termination or arrange for them to be restarted in another processor.

   3. Execute the PUP command REFRESH to ensure that the File Labels represent the actual status of files on disc.

NOTE

When a processor is taken off line, all NonStop (TM) processes currently active in that processor automatically revert to the backup processor assigned to them.

b. Transfer to another processor the path preference of all controllers whose preferred path is currently assigned to the processor to be taken off line. The procedure is as follows:

   1. Execute the PUP command LISTDEV to determine which controllers currently have preferred paths assigned in the processor to be taken off line.

   2. For all affected controllers, execute the PUP command PRIMARY to reassign the preferred path to the backup processor.

   3. Exercise all affected devices to verify that the newly assigned path is operational.

   4. Reexecute the PUP command LISTDEV to verify that the switch takes place.

NOTE

The PUP commands LISTDEV and PRIMARY are described in Section 7 of the Tandem 16 GUARDIAN Operating Manual, T16/8019

This page is intentionally left blank.

c. Go to the operator panel of the processor to be taken off line. Insert the processor key in the RESET/LOAD key switch and turn the key to the RESET position.

NOTE

The control panel lights to out, and a message is logged at the system console acknowledging that the processor is off line.

5.2 REPLACEMENT

The following procedures include steps on replacing a new board or one that has been repaired.

5.2.1 Replacing An MCB, CCD, MEMORY, or IPU Board

To replace one of the above named boards perform the following steps:

NOTE 1

Large boards should NOT be inserted in their slot using the PCB hold-down screw. Over tightening of this screw can break traces or cause seating problems. Use the hold-down screw to start the board into the connectors, then push the board in from the front until it is seated into the connector. The hold-down screw should only be "finger tight."

NOTE 2

When replacing a Memory board set the address for that memory board in accordance with Table 5.1.

a. Install the replacement board by carefully sliding it in from the front of the system cabinet. Make sure that rear edge connectors P1 and P2 are lined up properly and slowly tighten the PCB hold-down screw in the rear of the cabinet.

b. Install the jumpers removed in paragraph 5.1.1, step c.

c. Restore DC power to the processor taken off-line. Refer to paragraph 5.2.9.

a. Install the replacement board by carefully sliding it in from the front of the system cabinet. Make sure that rear edge connectors P1 and P2 are lined up properly and slowly tighten the PCB hold-down screw in the rear of the cabinet.

b. Install the jumpers removed in paragraph 5.1.1, step c.

c. Restore DC power to the processor taken off-line. Refer to paragraph 5.2.9.

d. Restore the processor to full operation (refer to paragraph 5.2.7).

Table 5.1 Address Switch Settings

MEMORY BD. NO.	ADDRESS %	SWITCH POSITION 1	2	3	4	5	6
1	00	C	O	O	O	O	O
2	01	C	O	O	O	O	C
3	02	C	O	O	O	C	O
4	03	C	O	O	O	C	C

O = OPEN (Binary 0)
C = CLOSED (Binary 1)

See NOTE 3

NOTE 3

Switch 1 is BOARD ENABLE and must be closed to enable reading and writing to the board.

5.2.2 Replacing An IPB Controller Board

To replace an IPB Controller Board perform the following:

a. Install the replacement board by securing it to the stand-offs with two slotted screws. Engage the plunger latch.

b. Install the bus cable to connector J1 and the DC power cable to connector J2. Install the CPU select cables to connectors J100 through J115.

c. Apply DC power by placing the power switch on the power regulator card for this controller in the ON (up) position. Refer to Figure 5-2.

d. Place the bus, to which the IPB Controller is attached on-line. Refer to paragraph 5.2.8. The <from processor> and the <to processor> must be specified as -1 (up the entire bus).

5.2.3 Replacing An I/O Terminator Board

To install the I/O terminator board perform the following:

a. Install the I/O bus cable to connector J2 and the DC power cable to connector J1.

b. Secure the I/O terminator to the I/O bus cable with a cable tie.

c. Apply DC power to the appropriate processor module in accordance with paragraph 5.2.6.

d. Verify that the power indicator LED is lit.

e. Reload the processor in accordance with paragraph 5.2.7.

5.2.4 Replacing An IPB Terminator Board

To replace an IPB Terminator Board perform the following:

a. Take the appropriate bus off-line (X or Y Bus) in accordance with paragraph 5.1.6.

b. Install the replacement IPB Terminator Board to the stand-offs, and secure it with the two slotted screws.

c. Install the bus cable to connector J2 on the IPB Terminator Board.

d. Place the appropriate bus on-line (X or Y Bus) (paragraph 5.2.8). The <from processor> and <to processor> must be specified as -1.

5.2.5 Replacing An Operator Control Panel Assembly

Refer to paragraph 5.1.5 and install the control panel in the reverse order of steps c) and d).

a. Apply dc power to the appropriate processor module in accordance with paragraph 5.2.6.

b. Reload the processor in accordance with paragraph 5.2.7.

5.2.6 Powering Up A Processor Module

Power up a processor as follows:

a. Apply dc power to the processor module by placing the 115/230VAC power and DC power switches on the associated T16/7301 DC Power Module in the ON (up) position.

b. Proceed to paragraph 5.2.7 to reload the processor.

5.2.7 Reloading A Processor Module

This procedure is used to bring a processor module back into operation in an otherwise operational system. The procedure, using a Command Interpreter, is as follows:

a. On the Control panel for the processor module to be reloaded, set switch register .<0> to the UP position. (This indicates a bus cold load to the hardware.)

b. On the same Control panel, turn the key in the RESET/LOAD switch first to the RESET position and then to the LOAD position.

c. Using a Command Interpreter, enter the following command:

:RELOAD <cpu> [, $<volume name> , {0:1}]

<volume name> is the name of a volume containing <cpu's> operating system image.

If the reload is successful the switch register display LEDs will show

%177777

5.2.8 Placing An Interprocessor Bus On-Line

Place the appropriate bus on-line as follows:

a. Enter via the command interpreter:

{X|Y}BUSUP <from cpu number>, <to cpu number>

b. The following console message will be printed for the bus placed on-line.

22 {...} X BUS TO PROCESSOR n UP (BEL)
23 {...} Y BUS TO PROCESSOR n UP (BEL)

5.2.9 Cold Loading The System From Disc

If the system is to be cold-loaded using OSP, follow instructions provided in paragraph 3.6 of the Operations and Service Processor User Guide, T16/8801 (B00). If the system is to be cold-loaded without using OSP, follow instructions provided in Section 3 of the Guardian Operating System Operations Manual, P/N 8205 (AOO), "Cold-Loading with a Processor Operator Panel."

5.3 SYSTEM DIAGNOSTIC

Refer to the following Diagnostic Manuals.

IPB Diagnostic Manual T16/8803
OCS Diagnostic Manual T16/8804
OSP Users Guide T16/8801 (B00)

SECTION 6
PREVENTIVE MAINTENANCE

6.0 PREVENTIVE MAINTENANCE

Refer to Preventive Maintenance Manual T16/8851 for detailed preventive maintenance information.

SECTION 7
SPECIAL TOOLS AND TEST EQUIPMENT

7.0 SPECIAL TOOLS AND TEST EQUIPMENT

* (SPECIAL TOOLS OR TEST EQUIPMENT ARE NOT REQUIRED FOR THE TANDEM NonStop II PROCESSOR)

SECTION 8
RECOMMENDED SPARE PARTS

8.0 RECOMMENDED SPARE PARTS

Refer to Table 8.1 for the recommended spares. The Tandem NonStop II Processor Kit component spares include the items listed in Table 8.2.

Table 8.1 NonStop II Processor Spares Field Kit

NAME	PART NUMBER
IPU board	54760
CCD board	54840
MCB board	54770
Memory Array (512Kbytes)	54740
OCS Maint Proc PWA	55700
Universal Proc Cbl.	55664

NOTE

This processor kit also contains an extra 60-wire flat cable assembly (PN 55664) that attaches to the front connector of the processor and array boards. Cable assembly Part Number 55664 can be cut down on site to replace processor cable assemblies 55642, 55643 and 55660 through 55664

Table 8.2 NonStop II Processor Kit Component Spares

QTY.	NAME	PART NUMBER
1	IPU Board	54760
1	CCD Board	54840
1	MCB Board	54770
1	Memory Array (512Kb)	23912
1	SMP Board	55700
1	Universal Processor Cable	55664
Box	Kit Component Spares	99643
2	UART (CCD Board)	23525
2	UART (SMP Board)	24151
2	WCS RAM	24112
2	Array RAM (16K x 1 Mostek)*	23912
2	Array RAM (16K x 1 Fujitsu)*	23914
2	Array RAM (16K x 1 TI)*	23968
2	Array RAM (16K x 1 National Semi)*	24321
2	Map RAM (1K x 1; 93425A)	24111
1	Kit Carrying Case	92557

* Choice of any

8.1 FIELD REPLACEABLE PARTS

Refer to Table 8.3 for a listing of field replaceable parts.

Table 8.3 NonStop II Processor Field Replaceable Parts

NAME	PART NUMBER
IPU Board	54760
CCD Board	54840
MCB Board	54770
UART	23525
UART	24151
RAM (16K x 1 Mostek)	23912
RAM (16K x 1; TI)	23968
RAM (16K x 1; Fujitsu)	23914
RAM (16K x 1; National Semi)	24321
RAM Map (1K x 1)	24111
RAM (4K x 1)	24112
Memory Array (512Kb)	54740
IPB Controller (New for TNS II)	56270
IPB Bus Terminator	51430
IPB Power Board	54600
IPB Cable Assy	55680
IPB Cable Assy	55691
Processor Power Supply	50050
Processor Power Supply	53270
I/O Power Supply	52730
I/O Power Supply	52875
I/O Regulator	54600
I/O Bus Cable	56114
I/O Bus Cable	56118
I/O Bus Terminator	51440
PMI Assembly	45029
PMI Patch Panel	42025
PMI Power Board	54600
PMI Board	55330
PMI/Processor Cable Assy	55521
PMI/Processor Cable Assy	55522
PMI/PMI (ext) Cable Assy	55524
PMI/PWR Cable Assy	51142
Control Panel Board	55060
OSP Maint. Processor PWA	55700

Table 8.3 NonStop II Processor Field Replaceable Parts (Cont'd)

NAME	PART NUMBER
OSP Power Supply (5V)	24163
OSP Power Supply (12V)	24162
Floppy Disc (5.5 Inch)	01732
Modem	01722
Floppy Cable Assy	55808
Modem Cable Assy	55520
SMT/PMI Cable Assy	55523
Terminal Cable Assy	55809
Fan, OSP Logic Drawer	23747
CPU Upper Backplane	55010
CPU Lower Backplane	55020
I/O Upper Backplane (1 x 6)	55080
I/O Lower Backplane (1 x 6)	54640
6520 Repair Kit	82788
Universal Processor Cable Assy	55664

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TANDEM

NonStop™ Systems

Shadow Diagnostic Language

Diagnostic Manual

Part No. 82848

DIAGNOSTIC OPERATING PROCEDURES

NonStop SYSTEMS

SHADOW DIAGNOSTIC LANGUAGE

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TANDEM COMPUTERS INCORPORATED
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SECTION 1
INTRODUCTION

1.0 INTRODUCTION

SHADOW is a high-level language designed for writing diagnostic programs to test I/O subsystems in an offline environment. The SHADOW program module requires that both the processor into which it is loaded and the I/O subsystem under test be off line.

Interaction between the user and SHADOW occurs at a designated test terminal. In the NonStop system this terminal must be configured to the Diagnostic Link Subsystem. In the NonStop II and NonStop TXP systems, the OSP terminal serves as the test terminal. All user directives and replies to SHADOW (with the exception of certain processor switch register settings) are entered at the test terminal keyboard, and all outputs generated by SHADOW, including error messages, are displayed on the test terminal screen.

A SHADOW diagnostic program consists of any series of valid SHADOW program statements existing as a Tandem EDIT-type file on tape or disc. The EDIT file serves as a source-code file for the program; it is automatically compiled at run time. Tandem provides a library of programs in this format for the range of supported peripheral devices. This library is available on the SHADOW diagnostic cold load tapes produced by Tandem; it is also sometimes present on the system, usually in $SYSTEM.ZZDIAG.

A typical use of SHADOW in the field involves loading one of the standard program files and running it from the test terminal. To use SHADOW effectively at this level you need only know a few basic commands in the SHADOW command set. As an alternative to running one of the prewritten programs, any series of valid SHADOW statements can be generated, either in an EDIT file or interactively at the test terminal, and then executed. However, to use SHADOW effectively at this level, a thorough understanding of the structure and syntax of the language is required.

For convenience and uniformity, the symbolic notation employed in this manual for describing the syntax of both the SHADOW command set and the SHADOW language itself is an adaptation of the widely used Backus-Naur/Normal Form (BNF).

1.1 METALANGUAGE CONVENTIONS

A metalanguage is a set of symbols and associated conventions for defining exhaustively the syntax of another language. Since BNF notation is a metalanguage devised and commonly in use for the description of programming languages, it is used here to describe the syntax of SHADOW.

Metalanguage production rules consist of a nonterminal symbol followed by "::=" (representing the phrase "is written as"), followed by the definitions of the symbol. A nonterminal symbol is a string of lower-case letters and underline characters (_). Each definition is a sequence of terminal or nonterminal symbols in the required order. Alternate definitions are separated by the 'or' character (|).

Upper-case letters and special characters (except those used as punctuation of the metalanguage) are reserved as explicit characters of the SHADOW language for composing the terminal symbols. In a few obvious cases a definition is provided by an English language explanation rather than by a list of symbols, but these should not create any confusion. Other metalanguage conventions are as follows:

a ...	one or more appearances of 'a'
{a|b|c}	required choice among alternatives listed
[a]	optional appearance of 'a'
[a] ...	none or more appearances of 'a'
[a|b|c]	optional choice among alternatives listed
[a|b|c] ...	none or more independent choices of alternatives

NOTE

A symbol having the suffix '_list' implicitly represents one or more occurrences of the symbol thus qualified, separated by commas (e.g., item_list ::= item [, item] ...).

These conventions can be nested to indicate options within options, choices within choices, and so on.

SECTION 2
SHADOW PROGRAM ENVIRONMENT AND EXECUTION

2.0 SETTING UP THE PROGRAM ENVIRONMENT

In order to run an existing SHADOW program or to write a new one, the SHADOW program module must first be loaded into an offline processor. The three methods for loading the SHADOW program module are as follows:

a. I/O load direct from tape

b. Bus load from tape through an offline processor

c. Bus load from tape or disc through an online processor.

The implementation of these methods is different in each type of system (NonStop and NonStop II/TXP).

2.1 LOADING SHADOW ON THE NonStop SYSTEM

Refer to NonStop Diagnostic Operating Procedures, Part Number 82802, Volume 1, Chapter 2, Part 1.

2.2 LOADING SHADOW ON THE NonStop II SYSTEM

Refer to NonStop II Diagnostic Operating Procedures, Part Number 82803, Volume 1, Chapter 2, Part 1.

2.3 CPU SWITCH REGISTER SETTINGS FOR USING SHADOW

The switch register settings for running SHADOW are summarized in Table 2.1.

Table 2.1 Standard SHADOW Switch Register Settings *

SWITCH	FUNCTION
<0>	If toggled on and off, generates a user break request and returns the SHADOW interpreter to conversational mode, where it waits for further instruction.
<3>	If placed in the ON position, suppresses error printout and enables setting of the special numerics ERROR and COMPERR . The special numerics COMPERR and ERROR are described in paragraphs 5.1 and 5.2, respectively.
<4>	If placed in the ON position, suppresses error printout, disables setting of the special numerics ERROR and COMPERR , and disables ERROR limit decrement.
<5>	If placed in the ON position, causes a program halt on I/O error.

* Switches <1>, <2>, <6>, and <7> may be specially defined by the individual diagnostics; switches <8> through <15> reflect the I/O address.

2.4 EXECUTING SHADOW PROGRAMS

Once loaded, SHADOW is always in one of three modes: conversational, execution, or halt. Whenever SHADOW has no request to process, it enters conversational mode, issues a prompt character (>) at the test terminal, and waits for user instruction. When a valid request is received from the user, SHADOW enters execution mode and processes the request. When execution completes, normally or abnormally, SHADOW returns to conversational mode. An unexpected I/O interrupt received during program execution causes SHADOW to suspend current activity, issue an error message, and either return to execution mode or enter halt mode, according to the setting of bit 5 of the processor switch register. If bit 5 is set to the OFF position, SHADOW resumes current mode of operation automatically after reporting an error. However, if bit 5 is set to the ON position, SHADOW enters halt mode after reporting the error.

In conversational mode, the system will execute either a SHADOW language program statement or a SHADOW command. These terms have their customary significance. Statements are the discrete executable units of which SHADOW programs are composed. As in many languages, statements are preceded or identified by an integer as a line or statement number in the first nonblank column. Commands are functions provided for the manipulation, modification, and execution of groups of program statements. Commands begin with some character other than an integer.

Any entered line that does not begin with an integer (leading blanks ignored) is interpreted as a command. Lower-case letters are interpreted as their upper-case equivalents; all other characters (except the special interactive characters carriage return, control-H, control-X, and escape) represent themselves in the command text. The format of a command is simply the command name (the first character sufficing for some commands) followed by any parameters. Multiple parameters are separated by commas, and the first parameter is separated from the command by one or more blanks. If the command is valid, it is executed immediately. SHADOW rejects a command if the command or parameters are not recognized or if they are syntactically incorrect. SHADOW always returns to conversational mode when a command is rejected.

Any entered line that begins with an integer is interpreted as a program statement. The integer serves as a line number for the statement, indicating a position relative to all other statements in the program. The value of the line number must fall in the range [1,9999]. Each program statement is checked for correctness of syntax when entered, and either accepted or rejected at that time. However, acceptance implies only that the statement is syntactically correct. It is possible to enter a statement that is syntactically correct yet logically incorrect in the context of a given program. Final validity checks are made only when a RUN command is entered, causing SHADOW to attempt program execution.

The first step in executing a SHADOW program is to specify it as the current program. This may be accomplished in one of two ways, with a GET command or with a RUN command. In general, the most recently executed GET command defines the current program. The other commands of the SHADOW command set are in turn defined as operating on the currently specified program. Once a current program is specified, any of the other SHADOW commands (including the RUN command) may be executed on that program. In the common case, where a program file is simply to be invoked and run without preceding modification, a RUN command can be substituted for the formal GET command. In this case, SHADOW precedes actual run processing with an implicit GET command.

Execution of a program begins with the statement having the lowest line number (excluding the ranges of all DEF statements). When execution of a statement is complete, control passes to the next sequential statement unless the one just executed specifies otherwise. When control reaches the last statement in a program, unless that statement transfers control to some other statement, program execution is complete, and SHADOW returns to conversational mode.

The user may stop program execution at any point before normal program completion in one of two ways. Bit <0> of the Switch Register may be toggled on and off, or either the ESCAPE or BREAK key may be depressed at the test terminal. Use the ESCAPE key with NonStop systems and the BREAK key with NonStop II and NonStop TXP systems.

2.5 GET COMMAND

The SHADOW GET command replaces the current program, if any, with the statements contained in the specified SHADOW text file, read either from a library tape or from the interprocessor bus. Syntactically incorrect lines are reported and deleted. The form of the GET command is as follows:

```
get_command  ::= GET file_name

file_name  ::=  any string of not more than eight alphanumeric
                characters, the first of which must be a letter
```

The GET command is aborted with an appropriate error message in the following instances:

a. If the storage space for program text is exhausted.

b. If a nonrecoverable tape read error occurs.

c. If a nonrecoverable interprocessor bus read error occurs.

d. If a text file with the specified name is not found.

Example:

```
>GET TAPE3206          ! accesses the SHADOW source-code file TAPE3206
                       ! and defines it as the current program
```

2.6 RUN COMMAND

The SHADOW RUN command initiates the execution of a program. If a file name is specified in the command line, SHADOW precedes run processing with an implicit GET command, establishing the specified file as the current program. This provides a convenient method for executing a complete program read either from a library tape or from the interprocessor bus. If no file name is specified in the command line, the current program is run. The form of the SHADOW RUN command is as follows:

```
run_command  ::=  { RUN [file_name] | R [file_name] }
```

Preliminary processing checks the program for completeness and structural integrity, compiles it, and allocates the data spaces for all variables, arrays, and special numerics defined in the program.

This phase is omitted if the program is unmodified from a previous execution. In either case, the system initializes the special numerics, sets all arrays to defined sizes, initializes the device table to show no devices, and transfers control to the first statement in the program. If control reaches the last statement in the program, unless that statement transfers control to some other statement, active execution is considered complete, and the SHADOW system returns to conversational mode. SHADOW continues to process I/O interrupts as if the program were active until all expected interrupts have occurred or the program is modified. Program errors (but not device errors) or a user break request aborts execution completely and causes SHADOW to return to conversational mode. In all cases, the data spaces remain available for inspection until the program is modified.

Examples:

```
>GET DEX4110          ! accesses the SHADOW source-code file DEX4110
                      ! and defines it as the current program
>RUN                  ! runs DEX4110

>RUN DISC4105         ! gets and runs the SHADOW source-code file
                      ! named DISC4105
```

2.7 USER BREAK REQUEST

When a user break request is detected by an executing SHADOW program, the following message is displayed at the test terminal and SHADOW enters conversational mode:

** BREAK **

2.8 ERROR MESSAGES GENERATED DURING PROGRAM EXECUTION

SHADOW reports three classes of errors during program execution:

a. Program errors

b. I/O or device-type errors

c. Non-I/O unexpected interrupt errors.

The messages that can be generated in each of these classes are described in paragraphs 2.8.1 through 2.8.3. In general, the interpretation and full understanding of the significance of these error messages requires some familiarity with the syntax of SHADOW and with the internal structure of SHADOW programs.

2.8.1 Program Error Messages

Program errors range from the simple case, where a command is rejected because of illegal operator input, to more complicated cases, where some internal inconsistency either in syntax or in control flow logic is detected. In general, program errors cause processing to abort, an error message to be displayed, and SHADOW to return to conversational mode.

Program error messages are displayed in the following format:

** ERROR <number> ** <message>.

The possible error numbers and corresponding messages are listed with probable causes in Table 2.2.

Table 2.2 Program Error Messages

ERROR NUMBER	MESSAGE	PROBABLE CAUSE
1	ILLEGAL SYNTAX	Sequence of symbols in the line does not form a legal statement or command.
2	ILLEGAL CHARACTER	Next symbol cannot begin with the character supplied.
3	ILLEGAL CONSTANT	Constant is too large in magnitude or contains an illegal digit.
4	ILLEGAL STRING	String constant is not terminated with quotation mark or contains no characters.
5	ILLEGAL OPERATOR	Specified operator not recognized.
6	ILLEGAL NAME	Identifier exceeds 15 characters, special numeric name misspelled, or OPTION parameter misspelled.
11	SYSTEM OVERFLOW	Physical memory is exhausted or program text is too long.
12	REGISTER OVERFLOW	An expression is too complex to compile.

Table 2.2 Program Error Messages (Cont'd)

ERROR NUMBER	MESSAGE	PROBABLE CAUSE
13	ADDRESS OVERFLOW	Out of data addressing range or PEP entries due to: too many variables or defined commands, or argument list in command statement is too long and complex.
14	CODE SPACE OVERFLOW	Program's code space requirements are too large.
15	DATA SPACE OVERFLOW	Program's data space requirements are too large.
16	STACK OVERFLOW	Working space requirements for program are too large; data spaces are lost in this case and cannot be examined with DUMP or DEV command.
17	TABLE OVERFLOW	An internal compiler table has overflowed; program is too large.
19	ILLEGAL WAIT VALUE	Value assigned to WAIT is not in the range [0,3], or an illegal subscript has caused program data spaces to be overwritten (see paragraph 5.10).
20	LITERAL VS. NUMERIC	Variable name or expression used in a context that requires a literal name or literal value, or vice versa.
21	NOT SIMPLE	Array or string constant appears where a single value or simple variable is expected.
22	NOT ARRAY	Simple variable or single value appears where an array is expected.
23	ALREADY ARRAY	Array name appears in more than one DIM statement (see paragraph 4.1.1).
24	STRING VS. NUMERIC	Type mismatch in an assignment statement, a COMP statement (see paragraph 4.5.2), or a command invocation argument list.

Table 2.2 Program Error Messages (Cont'd)

ERROR NUMBER	MESSAGE	PROBABLE CAUSE
25	ILLEGAL RELATION	IF statement compares two mask constants (see paragraph 4.5.1).
26	DUPLICATE NAME	A command name appears in more than one DEF statement; command name duplicates a SHADOW keyword; two parameters in a DEF statement have the same name (see paragraph 4.10.1).
27	TOO MANY	A statement has too many parameters or the trace table is full.
28	TOO FEW	A command invocation has too few arguments.
30	ILLEGAL RANGE	First is greater than last in line number, input value, or bit range; first or last falls outside specified maximum range.
31	ILLEGAL LINE NUMBER	Line number (after adjustment, if an ADD is active) is not in the range [0,9999].
34	MISSING 'DEFEND'	A DEF statement (see paragraph 4.10.1) does not have a closing DEFEND before the end of program text occurs, or a DEF appears within the range of another DEF.
35	UNMATCHED 'DEFEND'	DEFEND statement occurs without a preceding DEF statement (see paragraph 4.10.1).
36	MISSING 'NEXT'	FOR statement (see paragraph 4.4.3) is not matched by a NEXT statement before the range is terminated by end of program text, by end of command definition, or by another FOR with the same control variable.

Table 2.2 Program Error Messages (Cont'd)

ERROR NUMBER	MESSAGE	PROBABLE CAUSE
37	UNMATCHED 'NEXT'	NEXT statement occurs where the preceding FOR, if any, has a different control variable.
38	ILLEGAL BRANCH	GOTO (see paragraph 4.4.1), GOSUB (see paragraph 4.4.2), or IF destination does not exist; a transfer of control was attempted into the range of a DEF or FOR from outside the range; a transfer of control was attempted from within the range of a DEF to a statement outside its range (excluding command invocations).
39	MISSING COMMAND	Named command is not defined in a DEF statement (see paragraph 4.10.1).
40	UNMATCHED 'RETURN'	RETURN statement does not have a corresponding GOSUB (see paragraph 4.4.2).
41	OVERFLOW	Numeric overflow or divide by zero occurred.
42	ILLEGAL VALUE	Value is found to be outside a prescribed range; e.g., value received by an INPUT statement was not within the range [low value, high value].
43	ILLEGAL ARRAY SIZE	Dimensioned length in a DIM statement (see paragraph 4.1.1) is not in the range [1,32767] or new length in a SIZE statement (see paragraph 4.1.2) is not in the range [1, dimensioned length].
49	ILLEGAL COUNT	The byte count in a SETIOC statement (see paragraph 4.9.2) is not in the range [0,4095].
50	ILLEGAL LOGICAL UNIT	Logical unit number is not in the range [0,255].

Table 2.2 Program Error Messages (Cont'd)

ERROR NUMBER	MESSAGE	PROBABLE CAUSE
51	MISSING LOGICAL UNIT	Referenced logical unit does not exist.
52	ILLEGAL PHYSICAL UNIT	Physical unit number is not in the range [0,255].
53	MISSING PHYSICAL UNIT	SETDEV statement (see paragraph 4.8.1 create a new UNIT | device table entry does not supply a physical unit number.
54	PHYSICAL UNITS MATCH	Physical unit number appears more than once in the device table.
57	NOT FOUND	Referenced variable is not defined within the range of the reference (e.g., in the range of a DEF), or data space has not yet been allocated for the referenced variable.
58	TOO MANY STEPS	Program cannot be renumbered; specified increment is too large or default increment would be 1.
59	MISSING FILE	Requested program text file is not found in tape library.
60	KILL FAILURE	System failed in an attempt to put a controller offline whose devices are producing an inordinate number of unexpected interrupts.
61	EIO FAILURE	CCG or CCL is received in response to an EIO issued to the library tape unit (EIO status precedes this message).
62	IIO FAILURE	CCG or CCL is received in response to an IIO or HIIO issued to the library tape unit (first interrupt status word precedes this message).
63	TAPE NOT READY	Library tape unit is not ready.

Table 2.2 Program Error Messages (Cont'd)

ERROR NUMBER	MESSAGE	PROBABLE CAUSE
64	MISSING WRITE RING	Write ring is not installed on library tape.
65	READ FAILURE	Library tape has a nonrecoverable read error (second interrupt status word precedes this message).
66	WRITE FAILURE	Library tape has a nonrecoverable write error; second interrupt status word precedes this message).
67	TAPE OVERFLOW	End-of-tape is sensed while a program text file is being written on the library tape; the file is not saved.
68	TAPE FAILURE	CCE is received in response to an EIO issued to library tape unit, but EIO status is unacceptable (EIO status precedes this message).
69	MISSING TAPE	Processor switch register did not contain the physical unit number of the library tape; reload SHADOW if a library tape is to be used.

2.8.2 I/O Error Messages

SHADOW detects and reports six basic types of I/O error conditions. These error conditions, identified as E0 through E5, are summarized in Table 2.3.

Table 2.3 I/O Error Types

I/O ERROR TYPE	DESCRIPTION
E0	During execution of a COMP statement, an element in one array does not compare with its counterpart in the other array.
E1	The EIO status word returned as the result of an EIO statement does not compare with the supplied EIO mask.
E2	The interrupt status word or the interrupt cause word returned from an expected I/O interrupt does not compare with the supplied (or default) status mask or cause mask.
E3	A device creates an unexpected I/O interrupt.
E4	The number of I/O errors generated exceeds the buffer space available for holding them before printing.
E5	Special channel error interrupt. I/O channel detects error that requires software servicing. Found only on NonStop II and NonStop TXP processors.

2.8.2.1 Error Message E0

SHADOW error message E0 is generated when the elements of two arrays are being compared and an element in one array does not compare with its counterpart in the other array. Error message E0 takes two slightly different forms, depending on whether the array being compared when the error occurs is a numeric-type array or a string-type array. (Refer to paragraph 4.1.1 for a description of numeric- and string-type arrays.)

For NonStop systems, if the error occurs during comparison of a numeric-type array, the format of error message E0 is as follows:

```
*E0 DEVICE cc:u FAILED FROM <jjjj>
    IN <command name> AT <kkkk>. LUN IS <logical unit num>
WORD nnnnn IS a aaa aaa aaa aaa aaa FROM <array id>
    SHOULD BE b bbb bbb bbb bbb bbb
```

If the error occurs during comparison of a string-type array, the format of error message E0 is as follows:

```
*E0 DEVICE cc:u FAILED FROM <jjjj>
    IN <command name> AT <kkkk>. LUN IS <logical unit num>
BYTE nnnnn IS aa aaa aaa FROM <array id>
    SHOULD BE bb bbb bbb
```

Typical examples of a type E0 error message for NonStop systems are shown below:

```
1.  *E0 DEVICE 14:1 FAILED FROM 110
    WORD    12 IS 1 111 111 111 111 101 FROM BUFFER1
        SHOULD BE 1 111 111 111 111 111

2.  *E0 DEVICE 14:1 FAILED FROM 25 IN RDREC AT 10. LUN IS 20
    BYTE    45 IS 00 001 011 FROM INBUF
        SHOULD BE 01 001 011
```

Error message E0 appears for each unequal compare until either: a) the error limit set by the COMP statement is exhausted, or b) the error count set by the SETDEV statement for the specified logical device is exhausted.

The format for E0 type errors on NonStop II and NonStop TXP systems is shown below:

```
*E0 DEVICE  {cc:u}  [,LUN <logical unit num> ] FAILED
            {NULL}

ON LINE jjjj [IN D...D AT kkkk]

 {BYTE}  nnnnn  IS  {aa aaa aaa                }   FROM <array id>
 {WORD}             {a aaa aaa aaa aaa aaa     }

SHOULD BE  {bb bbb bbb                }
           {b bbb bbb bbb bbb bbb     }
```

NOTE: In this and subsequent sections describing these notations, the shorter strings of a's and b's represent BYTEs; the longer strings represent WORDs.

Some typical examples of this type of error are given below:

```
1.  *E0 DEVICE NULL FAILED
    ON LINE 8224 IN LOADCODE AT 1796
    BYTE     0 IS 01 001 101 FROM FILENAME$
        SHOULD BE 01 000 010

2.  *E0 DEVICE NULL FAILED
    ON LINE 8224 IN LOADCODE AT 1796
    BYTE     0 IS 01 001 101 FROM FILENAME$
        SHOULD BE 01 010 011

3.  *E0 DEVICE 01:3, LUN   3 FAILED
    ON LINE 9048
    BYTE     0 IS 11 011 011 FROM READ$
        SHOULD BE 01 011 011
```

Table 2.4 Active Fields in Error Message E0

FIELD	DESCRIPTION
cc:u	The controller and unit number of the device (in octal), or NULL if the logical unit number of the device was not supplied in the COMP statement.
jjjj	The line number of the COMP statement in the main program, or the line number of the command invocation statement if the COMP statement is in the range of a DEF statement (see kkkk below).
<command name>	The name of the command definition if the COMP statement is in the range of a DEF statement; otherwise blank.
kkkk	The line number of the COMP statement if it is in the range of a DEF statement; otherwise blank.
<logical unit num>	The logical unit number of the device if supplied in the COMP statement; otherwise blank.
nnnnn	The index of the faulty word or byte in the array being compared (the left-hand array in the COMP statement).
a...a	The binary value of the faulty word or byte.
b...b	The binary value of the word or byte in the other participating array (the right-hand array in the COMP statement).
<array id>	The name of the array being compared (the left-hand array in the COMP statement).
D...D	The name of the DEF in which the error occurred.

2.8.2.2 Error Message E1

SHADOW error message E1 is generated when a faulty status word is returned by an EIO statement. The format of error message E1 for NonStop systems is follows:

```
*E1 DEVICE cc:u FAILED FROM <jjjj>
    IN <command name> AT <kkkk> LUN IS <logical unit num>
EIO STATUS IS a aaa aaa aaa aaa aaa (ccx)
    SHOULD BE b bbb bbb bbb bbb bbb
```

Typical examples of the E1 error message for NonStop systems are shown below:

```
1.  *E1 DEVICE 08:4 FAILED FROM 240. LUN IS 5
    EIO STATUS IS 0 000 000 011 000 000 (CCE)
        SHOULD BE 0 000 000 001 DDD 000

2.  *E1 DEVICE 14:1 FAILED FROM 25 IN RDREC AT 10. LUN IS 20
    EIO STATUS IS 0 000 000 001 110 000 (CCE)
        SHOULD BE 0 000 000 00D D00 DDD
```

The format for type E1 errors on NonStop II and NonStop TXP systems is shown below:

```
*E1  DEVICE cc:u  [,LUN <logical unit num>]  FAILED [WITH WAIT#=w]
ON LINE jjjj  [IN D...D AT kkkk] (If failed from DEF)

EIO STATUS IS  a aaa aaa aaa aaa aaa (CCx)
    SHOULD BE  b bbb bbb bbb bbb bbb

[CTI STATUS IS c ccc ccc ccc ccc ccc] (If not CCE)
```

NOTE 1: The logical unit number is given in the message only if it is known.

NOTE 2: In the condition code notation, CCx, the x is E (equal), L (less than), or G (greater than).

Some typical examples of E1 type errors for NonStop II and NonStop TXP systems are shown below:

```
1.  *E1 DEVICE 11:0, LUN     1 FAILED
    ON LINE 6840 IN CONTROL4110 AT 696
    EIO STATUS IS 0 000 100 000 000 000   (CCE)
        SHOULD BE 0 000 000 000 000 000


2.  *E1 DEVICE 01:6,  LUN    7 FAILED WITH WAIT  = 3
    ON LINE 8948 IN SETCYLINDER4109 AT 2212
    EIO STATUS IS 0 010 000 000 000 000   (CCG)
        SHOULD BE 0 000 000 000 000 000
    CTI STATUS IS 0 000 000 001 000 000


3.  *E1 DEVICE 11:0,  LUN    1 FAILED
    ON LINE 5368
    EIO STATUS IS 0 010 000 000 000 000   (CCG)
        SHOULD BE 0 000 000 000 000 000
    CTI STATUS IS 0 000 000 001 000 000
```

The contents of the active fields in error message E1 are described in Table 2.5.

Table 2.5 Active Fields in Error Message E1

FIELD	DESCRIPTION
cc:u	The controller and unit number of the device (in octal).
jjjj	The line number of the EIO or EXPECT statement in the main program, or the line number that called the DEF that caused the error.
<command name>	The name of the command definition if the EIO statement is in the range of a DEF statement; otherwise blank.
kkkk	The line number of the EIO or EXPECT statement if it is in the range of a DEF statement; otherwise optioned.
<logical unit num>	The logical unit number of the device.
a...a	The binary value of the returned EIO status word.
b...b	The binary value of the EIO mask supplied in the EIO statement (or the default value).
w	The value of WAIT , if other than zero.
c...c	Channel status field, or channel termination interrupt (see Table 2.8).
CCx	The condition code (CCE, CCL, or CCG).

2.8.2.3 Error Message E2

SHADOW error message E2 is generated when a faulty interrupt status or interrupt cause word is returned from an expected I/O interrupt. The format of the error message for NonStop systems is as follows:

```
*E2 DEVICE cc:u FAILED FROM <jjjj> WITH WAIT  = w
    IN <command name> AT <kkkk> LUN IS <logical unit num>
    SHOULD BE x xxx xxx xxx xxx xxx AND y yyy yyy y
```

If the interrupt status and cause words are unavailable because timeout occurs first, the following message replaces the field that ordinarily displays the interrupt status:

```
INT STATUS IS UNAVAILABLE (TIME OUT)
```

Some typical examples of type *E2 error messages for NonStop systems are shown below:

```
1.  *E2 DEVICE 07:4 FAILED FROM 240. LUN IS 5
    INT STATUS IS 0 100 000 000 001 000 AND 0 000 000 0
        SHOULD BE 0 000 000 000 D00 000 AND 0 000 000 0

2.  *E2 DEVICE 14:1 FAILED FROM 25 IN RDREC AT 10. LUN IS 20
    INT STATUS IS UNAVAILABLE (TIME OUT)
        SHOULD BE 0 000 000 00D D00 DDD AND 0 000 000 0

3.  *E2 DEVICE 10:0 FAILED WITH WAIT  = 2. LUN IS 8
    INT STATUS IS 0 000 000 000 000 000 AND 0 001 000 0
        SHOULD BE 0 000 000 000 D00 000 AND 0 000 DDD D
```

The format for E2 type errors on NonStop II and NonStop TXP systems is shown below:

```
*E2 DEVICE cc:u  [,LUN <logical unit num>] FAILED [WITH WAIT  = w]
ON LINE jjjj [IN D...D AT kkkk]
 {INT STATUS IS UNAVAILABLE (TIME OUT)                                 }
 {INT STATUS IS a aaa aaa aaa aaa aaa AND b bbb bbb bbb bbb bbb (CCx)}
      SHOULD BE x xxx xxx xxx xxx xxx AND y yyy yyy yyy yyy yyy
[CTI STATUS IS c ccc ccc ccc ccc ccc] (only if not CCE)
```

Some typical examples of this type of error are shown below:

```
1.  *E2 DEVICE 30:0, LUN   10 FAILED
    ON LINE 8568 IN READTAPE AT 2752
    INT STATUS IS 0 000 110 000 101 000 AND 0 000 000 011 000 000
                                                                (CCE)
        SHOULD BE 0 DD0 1D0 000 000 000 AND 0 000 000 0DD DDD DDD

2.  *E2 DEVICE 30:0, LUN   10 FAILED
    ON LINE 8568 IN REWINDTAPE AT 2916
    INT STATUS IS UNAVAILABLE (TIME OUT)
        SHOULD BE 0 100 1D0 000 000 000 AND 0 000 000 0DD DDD DDD

3.  *E2 DEVICE 01:0, LUN   1 FAILED

    ON LINE 5344 IN READDATA4110 AT 1888
    INT STATUS IS 0 000 000 000 111 111 AND 0 010 000 000 001 000
                                                                (CCG)
        SHOULD BE 0 000 000 000 000 011 AND 0 000 000 0DD DDD DDD
    CTI STATUS IS 0 000 000 001 000 000
```

The contents of the active fields in error message E2 are listed in Table 2.6.

Table 2.6 Active Fields in Error Message E2

FIELD	DESCRIPTION
cc:u	The controller and unit number of the device (in octal).
jjjj	The line number of the EIO or EXPECT statement in the main program, or the line number that called the DEF that caused the error.
w	The value of WAIT , if other than zero.
<command name>	The name of the DEF statement if the EIO or EXPECT statement is in the range of a DEF statement; otherwise blank.
kkkk	The line number of the EIO or EXPECT statement if it is in the range of a DEF statement; otherwise optional.
<logical unit num>	The logical unit number of the device.
a...a	The binary value of the returned interrupt cause word.
b...b	The binary value of the returned interrupt status word.
c...c	channel status field or channel termination interrupt (see Table 2.8).
x...x	The binary value of the cause mask supplied in the EIO or EXPECT statement (or the default value).
y...y	The binary value of the status mask supplied in the EIO or EXPECT statement (or the default value).
CCx	Condition code; the value of x can be E (equals), G (greater than), or L (less than).

2.8.2.4 Error Message E3

SHADOW error message E3 is generated when a device creates an unexpected I/O interrupt. The format of the error message for NonStop systems is follows:

```
*E3 DEVICE cc:u INTERRUPTED. LUN IS <logical unit num>
INT STATUS IS a aaa aaa aaa aaa aaa AND b bbb bbb b
IOC ENTRY HAS x xxx xxx xxx xxx xxx AND y yyy yyy yyy yyy yyy
```

Some typical examples of the *E3 type of error message for NonStop systems are shown below:

```
1.  *E3 DEVICE 08:4 INTERRUPTED
    INT STATUS IS 0 001 000 000 000 000 AND 0 000 000 0
    IOC TABLE HAS 0 000 000 000 000 000 AND 0 000 000 000 000 000

2.  *E3 DEVICE 14:1 INTERRUPTED. LUN IS 20
    INT STATUS IS 0 010 000 010 000 000 AND 0 000 000 0
    IOC TABLE HAS 0 100 100 000 000 000 AND 0 000 000 000 010 000
```

The format for E3 type errors on NonStop II and NonStop TXP systems is shown below:

```
*E3 DEVICE cc:u [, LUN <logical unit num>] INTERRUPTED
ON LINE jjjj [IN D...D AT kkkk]  (If failed in DEF)
  {INT STATUS IS UNAVAILABLE (TIMEOUT)                                  }
  {INT STATUS IS a aaa aaa aaa aaa aaa AND b bbb bbb bbb bbb bbb (CCx)}

[CTI STATUS IS c ccc ccc ccc ccc ccc]  (This line is reported only if
                                        CCx is CCL or CCG.)
IOC ENTRY HAS x xxx xxx xxx xxx xxx AND y yyy yyy yyy yyy yyy, CER: ss
                                                                   sss
```

Some typical examples of this type of error are shown below:

```
1.  *E3 DEVICE 00:0 INTERRUPTED
    ON LINE 6252
    INT STATUS IS 0 000 000 000 000 000 AND 0 000 000 000 000 000
                                                              (CCL)
    CTI STATUS IS 1 000 000 100 001 001
    IOC ENTRY HAS 0 000 000 000 000 000 AND 0 000 000 000 000 000,
                                                      CER: 00 001


2.  *E3 DEVICE 01:4, LUN    5 INTERRUPTED
    ON LINE 8512 IN CONTROL AT 472
    INT STATUS IS 0 000 000 100 000 010 AND 0 000 000 000 001 100
                                                              (CCE)
    IOC ENTRY HAS 0 000 000 000 000 000 AND 0 000 000 000 000 000,
                                                      CER: 00 000


3.  *E3 DEVICE 01:4, LUN    5 INTERRUPTED
    ON LINE 8512 IN CONTROL AT 472
    INT STATUS IS UNAVAILABLE (TIMEOUT)
    IOC ENTRY HAS 0 000 000 000 000 000 AND 0 000 000 000 000 000,
                                                      CER: 00 000
```

The contents of the active fields in error message E3 are listed and described in Table 2.7.

Table 2.7 Active Fields in Error Message E3

FIELD	DESCRIPTION
cc:u	The controller and unit number of the device (in octal).
<logical unit num>	The logical unit number of the device.
a...a	The binary value of the returned interrupt cause word.
b...b	The binary value of the returned interrupt status word.
jjjj	The line number at which the error occurred or the line number that called the DEF that caused the error.
kkkk	The line number within the DEF at which the error occurred.
D...D	The name of the DEF in which the error occurred.
c...c	channel status field, or channel termination interrupt (see Table 2.8).
CCx	Condition code; the value of x can be E (equals), G (greater than), or L (less than).
s...s	The status returned in the IOC (see Table 2.9).
x...x	The binary value of the buffer address word from the IOC table entry for the specified device.
y...y	The binary value of the byte count word from the IOC table entry for the specified device.

The Channel Status Field, represented by c...c in the error message tables, defines a possible channel error. The values of c...c in the tables and the significance of the codes are described in Table 2.8.

Table 2.8 Channel Status Field Codes (c...c Values)

CODE NUMBER	DESCRIPTION
%000000	No error detected by the channel.
%000100	Device Status <0:3> is nonzero.
%000200	Channel detected a parity error on RIC (Read Interrupt Command).
%000400	Channel detected a parity error on RIST (Read Interrupt Status) or RDST (Read Status).
%177777	Instruction timed out waiting for the I/O channel to become available.
%1-----	Channel Status = IOBUS Control Field.

The IOC Status Field, represented by s...s in the error message tables for a type E3 error, defines a possible system error. The values of s...s in the tables and the significance of the codes are described in Table 2.9.

Table 2.9 IOC Status Field Codes (s...s Values)

CODE NUMBER	DESCRIPTION
%00	I/O incomplete -- operation in progress.
%01	End; either byte count reached zero or device stopped transfer with handshaking problem.
%02	Zero byte count on WRITE.
%03	Zero byte count on READ.
%06	Controller command not read or write.
%07	Unexpected reconnect.
%10	Channel/device handshaking problem.
%11	UCME on IOC1.
%12	UCME on IOC2.
%13	Parity error on data to channel.
%14	Protect bit, IOC0.<0>, on for READ.
%15	Channel/device handshaking problem.
%16	Device handshaking problem.
%17	UCME on data word during transfer.
%20	Memory address breakpoint hit on IOC0
%21	Memory address breakpoint hit on IOC1
%22	Memory address breakpoint hit on IOC2
%23	Memory address breakpoint hit while reading data.
%24	Memory address breakpoint hit while writing data.
%25	Timeout during data transfer.

Table 2.9 IOC Status Field Codes (s...s Values) (Cont'd)

CODE NUMBER	DESCRIPTION
%26	Device handshaking problem.
%27	Device handshaking problem on a write.
%30	Page absent during data transfer.
%31	Page absent on IOC1, IOC2, or IOC3.

2.8.2.5 Error Message E4

SHADOW error message E4 is generated when the number of I/O errors exceeds the available buffer space. The format of the error message is as follows:

```
*E4 nnnnn I/O ERRORS LOST
```

The active field, nnnnn, contains the number of lost error messages (in decimal).

Example:

```
*E4     5 I/O ERRORS LOST
```

2.8.2.6 Error Message E5

SHADOW error message E5 is generated by a special channel error interrupt when the I/O channel detects types of errors that require software servicing. The format of the error message is as follows:

```
*E5 I/O CHANNEL xx:u [, LUN <logical unit number>] INTERRUPTED
ON LINE jjjj [IN D...D AT kkkk]
INT PARAM1 IS a aaa aaa aaa aaa aaa, INT PARAM2 IS b bbb bbb bbb bbb
                                                                 bbb
```

The first two lines have optional parameters as indicated by the square brackets. The logical unit number of the interrupting device appears only when the SHADOW program can determine it. In the second line the bracketed quantities are generated within a SHADOW DEF. D...D is the DEF, and kkkk is the line number within the DEF where the error occurred. jjjj is the line number that called the DEF.

A typical example of the E5 type of error is given below:

```
*E5 I/O CHANNEL  01:7, LUN   7 INTERRUPTED
ON LINE 6532 IN TESTCHAN AT 2115
INT PARAM1 IS 1 110 110 000 010 100, INT PARAM2 IS 0 000 110 000
                                                    001 111
```

Table 2.10 Active Fields in Error Message E5

FIELD	DESCRIPTION
cc:u	The controller and unit number of the device (in octal).
<logical unit num>	The logical unit number of the device.
jjjj	The line number at which the error occurred or the line number that called the DEF that caused the error.
DDDD	The name of the DEF in which the error occurred.
kkkk	The line number within the DEF at which the error occurred.
a...a	The binary value of the error that caused the interrupt. See Table 2.11
b...b	The subchannel address and command pertinent to the error.

The error code displayed by the system for E5 type errors is as follows: %166xxx. Table 2.11 shows the significance of the "xxx" portion of this code. All of these errors represent a serious hardware problem.

Table 2.11 Error Code Significance, Type E5 Errors

CODE NUMBER	DESCRIPTION
%00	The channel is frozen at an unknown location.
%01	Reconnect was asserted but no device, Rank 0 or Rank 1, has responded to the reconnect poll. If this error occurs repeatedly, the channel should be taken down. The second word is not useful.
16	UCME found in IOC0. The second word is the subchannel address and command.
17	The map for the current IOC page is marked absent. The second word is the subchannel address and command.
20	A device illegally sent a handshake during reconnect poll of Rank 0. The second word is not useful.
21	A device illegally sent a handshake during reconnect poll of Rank 1. The second word is not useful.
22	A device did not handshake correctly during a select TBUS function. The second word shows all devices that responded to the previous poll.
23	A device did not handshake correctly or a parity error occurred on the data while the address and command were being read. The second word contains the suspect data.
24	The same device has had a continuous reconnect pending at least twice. The first time the device was aborted, but the IPU was not interrupted. When the device continues to try to reconnect, the IPU is interrupted. The second word is subchannel address and command.
25	The same device has had a continuous reconnect pending at least twice, and the command was not recognizable.
70	The channel is frozen with an unknown command.

2.8.3 Non-I/O Unexpected Interrupt Messages

The following non-I/O unexpected interrupt conditions cause SHADOW to generate error messages:

a. When a Power Fail interrupt is generated, SHADOW suspends any current activity and saves its state. When power is restored, SHADOW resumes in conversational mode and the following message is displayed at the test terminal:

```
*** POWER FAILED
```

b. When a Correctable Memory Error interrupt is generated, SHADOW resumes the interrupted activity and displays the following message at the test terminal:

```
*** MEMORY ERROR nnnnnn
```

The active field, nnnnnn, contains the interrupt parameter (in octal).

c. When a Bus Receive Completion interrupt is generated, SHADOW resumes the interrupted activity and displays one of the following two error messages, depending on whether the X-bus or the Y-bus was interrupted:

```
*** X-BUS INTERRUPT nn

*** Y-BUS INTERRUPT nn
```

The active field, nn, contains the number of the sending processor.

d. When an Uncorrectable Memory Error interrupt is generated, causing the system to halt with 1 displayed in the switch register of the test processor, SHADOW displays the following message when the RUN switch on the operator control panel is depressed, and then the system halts completely:

MEMORY DEATH nnnnnn

The active field, nnnnnn, contains the interrupt parameter (in octal).

e. When a Map Parity Error interrupt is generated, causing the system to halt with 2 displayed in the switch register of the test processor, SHADOW displays the following message when the RUN switch on the operator control panel is depressed, and the system halts completely:

MAP PARITY nnnnnn

The active field, nnnnnn, contains the interrupt parameter (in octal).

f. When an Unimplemented Instruction or a Privileged Violation interrupt is generated, causing the system to halt with 4 displayed in the switch register of the test processor, SHADOW displays the following message when the RUN switch on the operator control panel is depressed, and then the system halts completely:

INSTRUCTION nnnnnn

The active field, nnnnnn, contains the address of the offending instruction.

g. When a PAGE FAULT interrupt is generated from the code area, causing the system to halt with 6 displayed in the switch register of the test processor, SHADOW displays the following message when the RUN switch on the operator control panel is depressed, and then the system halts completely:

PAGE FAULT nnnnnn

The active field, nnnnnn, contains the interrupt parameter (in octal).

If a Page Fault occurs in the data area, SHADOW attempts to assign a new physical page. If this attempt is successful, activity resumes with no further action; otherwise the following message is displayed at the test terminal:

** ERROR 11 ** SYSTEM OVERFLOW

h. When an Arithmetic Overflow interrupt is generated from the system code area, causing the system to halt with 7 displayed in the switch register of the test processor, SHADOW returns the following message before the system halts completely:

Shadow ERROR nnnnnn

The active field, nnnnnn, contains the address of the offending instruction. An Arithmetic Overflow interrupt generated from the user code area is treated as a program error.

2.9 ALTERING RUN-TIME PARAMETERS

SHADOW provides a number of options that may be selected by the user before the current program is run. If one or more of these options is desired for a given run of a diagnostic program, the user first issues a GET command for the desired program, then an OPTION command specifying the desired options, and then a RUN command.

The options that can be specified in the OPTION command are as follows:

a. STRIP/NOSTRIP: STRIP option strips comments from all text subsequently entered; default is NOSTRIP.

b. TRACE/NOTRACE: TRACE option enables the SHADOW trace facility, which compares the line number of each statement with those in the trace table during program execution; default is NOTRACE.

c. SYNC/NOSYNC: SYNC option provides a delay to all for carriage movement on a hard-copy terminal; default is NOSYNC. NOSYNC implies the use of a CRT terminal (no delay) and provides true backspacing.

d. IDENT/NOIDENT: IDENT option assigns an integer identifier to be printed with SHADOW prompts and error messages. Legal range is [0,99]; default is NOIDENT.

e. TAPE: enables tape-load mode and disables interprocessor-bus-load mode; the supplied physical unit number is assigned as the number of the system tape. Subsequent ADD, GET and RUN commands read text files from the system tape.

f. XBUS/YBUS: enables interprocessor-bus-load mode and disables tape-load mode. Subsequent ADD, GET and RUN commands read text files from the specified processor over either the X-bus or the Y-bus.

g. Line length: an integer constant that defines the test terminal line length. Legal range is [72,132]; default is 80.

h. DEBUG: used for SHADOW system maintenance only.

The form of the SHADOW OPTION command is as follows:

```
option_command  ::=  OPTION { [STRIP | NOSTRIP] | [TRACE | NOTRACE] |
                              [SYNC | NOSYNC] |
                              [IDENT,num | NOIDENT] | TAPE,pu |
                              [XBUS,cpu | YBUS,cpu | line_length |
                              DEBUG }

  num  ::=  integer_constant
  pu  ::=  integer_constant
  cpu  ::=  integer_constant
  line_length  ::=  integer_constant
```

Examples:

```
  OPTION TRACE          ! enables the SHADOW trace facility
  OPTION 72             ! sets the number of characters per line on
                        ! the test terminal at 72

  OPTION TAPE,%31       ! sets tape-load mode through physical
                        ! device %31

  OPTION XBUS,14        ! set interprocessor-bus-load mode through
                        ! processor 14
```

SECTION 3
LEXICAL ELEMENTS OF SHADOW

3.0 LANGUAGE OVERVIEW

The SHADOW language supports three forms of data and two data structures. The data forms are 16-bit two's-complement integer, 16-bit binary pattern, and 8-bit ASCII-encoded character. The data structures are simple variable (a single value) and array (a one-dimensional collection of values).

Each of the three data forms can be structured as either simple variable or array. Individual array elements can be used as simple variables or the array may be manipulated as one entity.

SHADOW implements two data types, numeric and string. Both integers and bit patterns are treated as numeric data. ASCII characters are treated as string data.

Numeric variables can be manipulated both by integer operators (addition, subtraction, multiplication, division, modulus, and right and left arithmetic shift) and by pattern operators (bit-wise complement, AND, OR, EXCLUSIVE OR, right and left logical shift, bit extraction, and bit deposition). Reference, assignment, input, display, and comparison operators are available for both numeric and string data types. In addition, a special comparison form tests a numeric value (viewed as a pattern) against a mask that allows some bits to be accepted as either 1's or 0's (don't care). This capability is especially valuable for checking several noncontiguous fields of status words simultaneously.

The SHADOW statements provide methods of filling arrays with random or repetitive test data; of manipulating the data in arrays; of comparing two arrays for equality; of adjusting the size of an array within initially declared limits; of executing conditional and unconditional transfers, loops, and subroutines; of extending the language through user-defined parametric procedures; of defining devices and device attributes; of assigning and querying the contents of IOC table entries; of issuing I/O commands and instructions for handling expected interrupts; and of storing and displaying status information.

3.1 LEXICAL ELEMENTS OF SHADOW

The alphabet used for SHADOW is the ASCII character set. Outside the context of a string constant or a comment (defined in paragraphs 3.2 and 3.6.1, respectively), a lowercase letter is interpreted in a program text as the corresponding uppercase letter. Because the quotation mark (") is used to introduce and terminate string constants, it cannot be used to represent itself directly. To represent a quotation mark as part of a string constant, a double quotation mark ("") must be entered.

Several nonprinting ASCII characters are reserved for interactive control and cannot be directly entered as part of a program. These interactive control characters are listed in Table 3.1. All other characters are accepted in the program text as they appear.

Table 3.1 Interactive Control Characters in SHADOW

CHARACTER	FUNCTION
Carriage Return	Signals the end of the current input line.
Control/H	Deletes the last character entered (backspace).
Control/X	Cancels the current line (SHADOW responds with `@`, carriage return, and line feed).
Escape	User break request (operative only during SHADOW outputs to the test terminal).

The metalinguistic definition of the alphabet of SHADOW is as follows:

```
character  ::=  " | text_character
  text_character  ::= letter | digit | open_bracket | close_bracket |
                      any other ASCII character except " and those
                      reserved for special interactive conventions
                      (carriage-return, control-H, control-X, escape)
  letter  ::=  A | B | C | D | E | F | G | H | I | J | K | L | M |
               N | O | P | Q | R | S | T | U | V | W | X | Y | Z
  digit  ::=  octal_digit | 8 | 9
  octal_digit  ::=  binary_digit | 2 | 3 | 4 | 5 | 6 | 7
  binary_digit  ::=  0 | 1
  open_bracket  ::=  [
  close_bracket  ::=  ]
  empty  ::=  none or more blanks
```

The bracket characters, "[" and "]", when they appear as part of a SHADOW construct, are metalinguistically described as "open_bracket" and "close_bracket", respectively, in order to avoid confusion with the use of brackets in BNF notation to enclose optional portions of SHADOW constructs.

The basic syntactical elements generated from this alphabet (and of which SHADOW statements are in turn composed) are as follows:

a. Constants

b. Identifiers

c. Variables (simple, array, and special numeric)

d. Expressions.

3.2 CONSTANTS

The metalinguistic representation of a constant is as follows:

```
constant  ::=  { integer_constant | string_constant }

  integer_constant  ::=  { decimal_constant | octal_constant |
                           binary_constant | mask_constant }
  decimal_constant  ::=  digit ...
  octal_constant  ::=  % octal_digit ...
  binary_constant  ::=  %B binary_digit ...
  mask_constant  ::=  %B binary_digit ... D [binary_digit | D] ...
  string_constant  ::=  "character_constant ..."
  character_constant  ::=  { text_character | quote_rep }
  quote_rep  ::=  ""
```

Numeric values can be represented in three different ways. A decimal constant represents an integer value in the range [0,32767]. An octal constant represents a 16-bit pattern in the range [0,177777 octal]. A binary constant represents a 16-bit pattern in the range [0,1111111111111111 binary]. Leading zeroes are ignored when determining the value of an integer constant. A mask constant is a special form of binary constant intended for use in equal or not-equal tests against values interpreted as bit patterns. The letter D is used to indicate a "don't care" condition for a given bit position. It matches either a 0 or a 1 in the same bit position of the value being tested.

A string constant is represented as a sequence of character constants within delimiting quotation marks (\"). Blanks and nonprinting characters are significant, and a quotation mark itself is represented by a pair of quotation marks (\"\") within the character sequence. In some contexts, an integer constant in the range 0:%377 is accepted as the equivalent of a single-character string constant. This permits the representation of characters, such as carriage return, which cannot be directly entered.

3.3 IDENTIFIERS

The metalinguistic representation of an identifier is as follows:

identifier ::= letter [letter | digit] ...

An identifier is the name of an entity and is used to reference it. The entity identified can be a simple variable, an array, or a program-defined command. Two entities of the same class (e.g., two arrays) must have different names. In some cases, two entities in different classes can have the same name, where the context serves to distinguish them. This practice, however, should be avoided since it can cause confusion. An identifier can have from 1 to 15 alphanumeric characters; the first character must be alphabetic.

Certain identifiers are reserved as the names of the SHADOW program statements and of the SHADOW commands.

3.4 VARIABLES

SHADOW recognizes three types of variable, simple, array, and special numeric. Both simple variables and array variables may be either numeric or string. In addition, SHADOW declares certain predefined special numeric variables that are accessible to the user. Each is identified by a unique name the last character of which is a pound sign (#).

The metalinguistic respresentation of a variable is as follows:

```
variable  ::=  { simple_numeric | simple_string | array_numeric |
                 array_string | special_numeric }

  simple_numeric  ::=  identifier
  simple_string  ::=  identifier $
  array_numeric  ::=  identifier [range_index]
  range_index  ::=  open_bracket first_index  [: last_index]
                      close_bracket
  first_index  ::=  expression
  last_index  ::=  expression
  array_string  ::=  identifier $ [range_index]
  special_numeric  ::=  { COMPERR# | ERROR# | ERRORMASK# | IDENT# |
                          INTERRUPT# | INSTAT# | LITES# | NONE# |
                          RAND# | SWITCHES# | TIMER# | WAIT# | G0# |
                          G1# | G2# | G3# | G4# | G5# | G6# | G7# |
                          G8# | G9# }
```

3.4.1 Simple Variables

Simple variables are identifiers that refer to data spaces containing single values. Declaration of a simple variable is accomplished by using the identifier in a context that implies access to a single value.

Numeric-type data is represented by a simple variable the final character of whose identifier is not a dollar sign ($). The data space contains one word (16 bits). The value of a simple numeric variable is viewed as either a two's complement integer in the range -32768:32767 or a 16-bit binary pattern.

String-type data is represented by a simple variable the final character of whose identifier is a dollar sign ($). The data space contains one byte (8 bits). The value of a simple string variable is viewed as an 8-bit pattern corresponding to one of the ASCII characters.

3.4.2 Array Variables

Array variables are identifiers that refer to groups of 'n' contiguous data spaces, each of which is called an element, implicitly numbered from 0 to n-1. Declaration of an array variable requires that the array identifier appear in a DIM statement defining the initial number of elements (i.e., dimension).

Numeric-type data is represented by an array variable the final character of whose identifier is not a dollar sign ($). Each of its elements has the attributes of a simple numeric variable.

String-type data is represented by an array variable the final character of whose identifier is a dollar sign ($). Each of its elements has the attributes of a simple string variable.

An array identifier that appears alone is a reference to the entire data space it represents. An array identifier can also be used, together with a bracketed expression called a subscript or range index, to access either a single one of the elements or a range of elements. The value of the bracketed expression is used as an index to select the particular array element or elements. If a range of elements is designated, the first index and the last index must evaluate to integers in the range [0, n-1]. The last index must be greater than or equal to the first index. When an array identifier qualified by an index range is used as a source of values, only those elements with indexes in the specified range are accessed to supply the sequence of values. A subscripted array variable designating a single value can be used as the equivalent of a simple variable. Examples of array variables are given in Table 3.2.

Table 3.2 Examples of Array Variables

EXAMPLE	DESCRIPTION
BUFFER[12]	Designates element 12 in the numeric array BUFFER
BUFFER[0:20]	Designates elements 0 through 20 in the numeric array BUFFER
INBUFFER$[28]	Designates element 28 in the string array INBUFFER
INBUFFER$[10:49]	Designates elements 10 through 49 in the string array INBUFFER$
PATTERN$[I+J]	Designates the element identified by the value of the expression I+J in the string array PATTERN$
PATTERN$[0:I+K]	Designates element 0 through the element identified by the value of the expression I+K in the string array PATTERN$

3.5 EXPRESSIONS

The metalinguistic representation of an expression is as follows:

```
expression  ::=  [signop] term [addop term] ...

  signop  ::=  { + | - }
  term  ::=  factor [mulop factor] ...
  factor  ::=  ['-'] shift
  shift  ::=  primary [bit_range] [shiftop shift_count] ...
  primary  ::=  { integer_constant | simple_numeric | array_numeric |
                  special_numeric }
  bit_range  ::=  .< first_bit [: last_bit] >
  first_bit ::=  integer_constant
  last_bit  ::=  integer_constant
  shiftop  ::=  { << | >> | '<<' | '>>' }
  shift_count  ::=  integer_constant
  mulop  ::=  { * | / | MOD }
  addop  ::=  { signop | LAND | LOR | XOR }
```

An expression represents a sequence of operations performed with numeric values and resulting in a single numeric value (in the range -32768:32767). The simplest forms of an expression are a single integer constant, a single numeric variable, or a special numeric variable. More complex expressions consist of one or more terms separated from each other by arithmetic or logical operators.

These complex expressions are evaluated from left to right. As each term is encountered, the factors are evaluated from left to right before the next term is examined. Evaluation of a factor proceeds as follows: a) evaluate primary; b) apply bit-range qualifier, if present; c) apply shift operator, if present; and d) apply one's complement operator ('-'), if present.

Evaluation of a primary can invoke evaluation of a lower-level expression if the primary is a parenthesized expression or a subscripted variable. If a bit-range qualifier is applied, it supplies only the specified bits of its primary, right justified in a 16-bit numeric field with leading zeroes inserted. All primaries of each term are evaluated before any primaries of succeeding terms. However, any desired order of evaluation can be specified by properly ordering the components of the expression and by using parentheses to convert groups into primaries. The actions indicated by the various integer and pattern operators are listed in Table 3.3.

Table 3.3 Integer and Pattern Operators in SHADOW Expressions

OPERATOR	ACTION INDICATED
bit range	Extract contiguous bit field and right justify as a 16-bit pattern with implied leading zeros.
<<	Arithmetic shift left by indicated shift count.
>>	Arithmetic shift right by indicated shift count.
'<<'	Logical shift left by indicated shift count.
'>>'	Logical shift right by indicated shift count.
'-'	One's complement on 16 bits of operand.
*	Two's complement integer multiply.
/	Two's complement integer divide (retain quotient, discard remainder).
MOD	Logical integer divide (retain remainder, discard quotient). This operator is only useful if the left operand is a nonnegative integer and the right operand is positive.
+	Two's complement integer add (or no action if used as a unary operator).
-	Two's complement integer subtract (or negation if used as a unary operator).
LAND	Bitwise 'and' on all 16 bits of operands.
LOR	Bitwise 'inclusive or' on all 16 bits of operands.
XOR	Bitwise 'exclusive or' on all 16 bits of operands.

For example, the expression:

```
A+B/C-D*3
```

is evaluated as follows:

a. B is divided by C,

b. D is multiplied by 3,

c. A is added to the value obtained in step a,

d. The value obtained in step b is subtracted from the value obtained in step c.

Whereas, the expression:

```
(A+B)/((C-D)*3)
```

is evaluated as follows:

a. A is added to B,

b. D is subtracted from C,

c. The value obtained in step b is multiplied by 3,

d. The value obtained in step a is divided by the value obtained in step c.

Examples:

```
A<<8 - B
```

designates the value of simple numeric variable B subtracted from the value of simple numeric variable A arithmetically shifted left by 8

```
(A+B).<10:15>
```

designates bits 10 through 15 of the value represented by the sum of the values of simple numeric variables A and B

```
L1 XOR L2
```

designates a bitwise 'exclusive or' operation on all 16 bits of simple numeric variables L1 and L2

3.6 OTHER SYNTACTICAL CONVENTIONS

Two other syntactical conventions of SHADOW deserve mention: the use of comments and the use of blank spaces.

3.6.1 Comments

In SHADOW syntax, characters introduced by an exclamation mark (!) are interpreted as a comment. The metalinguistic representation of a SHADOW comment is as follows:

```
comment  ::=  ! [character] ...
```

The comment consists of the exclamation mark and all following characters, including blanks, up to the carriage return that terminates the line. The exclamation point should be preceded by at least one blank. Comments cannot begin within a string constant because the exclamation point is accepted therein as a text character. Comments provide a means of including explanatory remarks in a program. They may appear anywhere in a SHADOW program without affecting program execution.

Examples:

```
!This is a comment
!And so is this
```

3.6.2 Use of Blanks

Within a string constant or a comment, a blank represents one character of a symbol. In all other cases, a blank signifies the termination of a basic syntactical element. Blanks cannot appear between two letters, two digits, or a letter and a digit that belong to the same symbol. However, one or more blanks may precede or follow any nonalphanumeric character, even when that character is part of some multicharacter symbol. One or more blanks must appear after a letter or digit that terminates one symbol if the next symbol also begins with a letter or digit. As a simple rule, all basic syntactical elements (constants, variables, operators, expressions) should be entered without embedded blanks and separated from predecessors and successors by one or more blanks.

Examples:

(legal spacing):	% 35	% B101	ARRAY [55]	AB $
(illegal spacing):	%3 5	%B 101	AR RAY[5 5]	A B$
(optimum spacing):	%35	%B101	ARRAY[55]	AB$

SECTION 4
SHADOW STATEMENTS

4.0 SHADOW STATEMENTS

Ten classes of SHADOW statements are discussed in this section.

4.1 ARRAY DESCRIPTION STATEMENTS

SHADOW provides two statements for defining the number of elements in an array. The DIM statement is used to define which variables shall be interpreted as array variables in any given program and the initial number of elements in each. The SIZE statement is used to alter the initially established number of elements for any given array or arrays.

4.1.1 DIM Statement

The metalinguistic representation of the SHADOW DIM statement is as follows:

```
dim_statement  ::=  line_number DIM array_specification_list

  array_specification_list  ::=  { array_numeric open_bracket length
                                   close_bracket |
                                   array_string open_bracket length
                                   close_bracket }
  length  ::=  integer_constant
```

A DIM statement declares one or more identifiers to be array variables, rather than simple variables, and specifies the maximum number of elements each is to contain. If the last character of the identifier is a dollar sign ($), it identifies a string array; otherwise it identifies a numeric array.

Since the first index of an array is always 0, the range of legal indexes is [0,length-1]. The DIM statement containing the specification for a particular array must have a lower line number than any other statement referencing that array. If control passes to a DIM statement during execution, it is immediately passed on to the following statement with no other effect.

Examples:

```
10      DIM BUFFER[128]
20      DIM ARRAY1$[12],ARRAY2$[24],OUTBUFFER[256]
```

4.1.2 SIZE Statement

The metalinguistic representation of the SHADOW SIZE statement is as follows:

```
size_statement  ::=  line_number SIZE { array_numeric | array_string }
                     open_bracket new_length close_bracket

  new_length  ::=  expression
```

The SIZE statement is used to reset the range of legal indices for an array during execution of the program. The value of the new length must equal at least 1 and cannot exceed the initial length established for the array in the DIM statement (refer to paragraph 4.1.1). Following execution of a SIZE statement the array contains elements with indices in the range [0,new length-1]. No data is moved or altered. If the size is decreased, the values of elements whose indices are deleted from the range become inaccessible; if the size is increased, the values whose indices are restored to the range should be assumed unknown. Elements present both before and after execution of the SIZE statement retain the values originally assigned.

Examples::

```
105    SIZE BUFFER[64]
210    SIZE INBUF$[HEADER+RECORD]
```

4.2 ASSIGNMENT STATEMENT

The SHADOW assignment statement is provided as a means of assigning values both to simple and to array variables. The metalinguistic definition of the assignment statement is as follows:

```
assignment_statement  ::=  line_number { simple_assignment |
                           array_assignment | rotate_assignment }

  simple_assignment  ::=  { simple_destination = source |
                            special numeric = source }
  simple_destination  ::= { simple_numeric [bit_range] |
                            simple_string [bit_range] }
  source  ::=  { expression | character_constant |
                 simple_string [bit_range] }

  array_assignment  ::=  { array_destination = array_source |
                           array_destination = [rep_factor]
                                               (array_source) }
  array_destination  ::=  { array_numeric [bit_range] |
                            array_string [bit_range] }
  array_source  ::=  { source | array_numeric [bit_range] |
                       array_string [bit_range] }

  rotate_assignment  ::=  { array_id = -> | array_id = <- }
  array_id  ::=  { array_numeric | array_string }
```

A simple assignment statement assigns a single value from the source, on the right of the assignment operator (=), to the destination, on the left of the operator. If a simple destination is qualified by a bit range, only the specified field is affected by the assignment; the bits of the destination not within the bit range retain their previous value. If an expression is assigned to a string variable, only the 8 least significant bits (<8:15>) of the expression are used for the assignment. If a string constant or a string variable is assigned to a numeric variable, the 8-bit value is treated as a 16-bit value with eight leading zero bits. A special numeric used as a simple destination cannot be qualified by a bit range.

An array assignment assigns a group of values to either all or part of an array. If the destination is simply an array with no range index specified, the entire array is filled by repeating as many times as necessary the sequence of values obtained from the source. If the destination is an array qualified by a single-element range index, the assignment begins with that element and continues until either the last element of the array is filled or the sequence of values from the source is exhausted (no repetition of the source values occurs). Thus, an array can be filled either from the first element to the last or from any intermediate element to the last.

If the source is a single value, it provides a sequence consisting of the one value. If the source is a string constant containing more than one character, the destination must be a string array. If the source is an array, its elements provide the sequence of values. In this case, a range index can be applied to restrict the source to some portion of the array.

If the source is the special numeric RAND#, successive values are obtained from a pseudo-random source. All other expressions, including those in which RAND# appears as a primary, are evaluated once and the result applied as the source value.

In instances when the destination is an array qualified by a single-element range index, a repetition factor (greater than 0) can be applied to the source to provide a sequence consisting of the source value repeated as specified. A repetition factor need not be supplied when the destination is an array without range-index qualifier because repetition is implict in that case.

The rotate assignment is a special form of the assignment statement that permits a circular shift of the elements of an array to the left (<-) or to the right (->). The effect is to save the value of either the first (the leftmost) or the last (the rightmost) element, assign the value of each of the remaining elements to the appropriate neighbor, and assign the saved value to the element that is left vacant.

Examples of simple and array assignment are given in Table 4.1.

Table 4.1 Examples of Simple and Array Assignment

EXAMPLE	DESCRIPTION
XVAR = YVAR+1	The simple numeric variable XVAR is assigned the value of decimal 1 added to the value of the simple numeric variable YVAR
G2# = 3	The special numeric G2# is assigned the value of decimal 3
Z = Z$	The simple numeric variable Z is assigned the 8-bit value of the simple string variable Z$ with eight leading zero bits supplied
Z$ = RAND#	The simple string variable Z$ is assigned the value of the eight least significant bits (<8.15>) of the special numeric RAND#
CMDWD.<0:5> = CMD	Bits 0 through 5 of the simple numeric variable CMDWD are assigned the value of the simple numeric variable CMD
ARRAY = BARRAY	The numeric array ARRAY is filled by repeating as many times as necessary the values of the elements in numeric array BARRAY
CARRAY = RAND#	The numeric array CARRAY is filled with a pseudo-random sequence of numbers obtained from special numeric RAND#
X$ = A$[I]	The string array X$ is filled by repeating as many times as necessary the value of the element of string array A$ represented by the expression I
DARRAY[20] = EARRAY	The values of the elements of numeric array EARRAY are used as far as they go to fill numeric array DARRAY starting at element 20
RARRAY$ = "ABC"	The string array RARRAY$ is filled by repeating as many times as necessary the string constant "ABC"

Table 4.1 Examples of Simple and Array Assignment (Cont'd)

EXAMPLE	DESCRIPTION
SARRAY$[5] = 6(%53)	The octal value %53 is assigned to six elements of the string array SARRAY$ starting at element 5
ARRAY <-	The value of element ARRAY[0] is assigned a temporary data space, the value of ARRAY[1] is assigned to ARRAY[0], the value of ARRAY[2] is assigned to ARRAY[1], and so on until the value of the last element of ARRAY has been assigned to the element immediately preceding it; the value stored in the temporary data space is then assigned to the last element

Examples:

```
10    X = (Y+1)/(Z-12)*W
20    G2# = HOLD-25
30    ARRAY$ = " "
40    BUFFER$[0] = 5(TESTPAT$)
45    TESTPAT$ = ->
50    CMDWD.<0:7> = CMD
55    CMDWD.<8:15> = CTLR '<<' 3 + DEVICE
60    ARRAY1$[10] = ARRAY2$[10:40]
```

4.3 LITERAL STATEMENT

The SHADOW literal statement associates an identifier with the integer value found by evaluating the expression on the right-hand side of an assignment operator (=). Whenever the literal name appears in a context where an integer constant is legal, it is treated as a pseudonym for the constant. The metalinguistic representation of the SHADOW literal statement (LIT) is as follows:

```
literal_statement  ::=  line_number LIT literal_name =
                        literal_expression

  literal_name  ::=  identifier
  literal_expression  ::=  an expression all of whose primaries are
                           integer_constants, literal_names, or
                           parenthesized literal_expressions
```

A LIT statement must have a line number smaller in value than that of any other statement that makes reference to the literal name. A LIT statement appearing within the range of a DEF statement has no influence outside of that range. A LIT statement appearing outside of the ranges of all DEF statements has no influence inside any of their ranges.

A literal expression can appear anywhere that an integer constant can (or must) appear, except as a line number, a shift count, or within a bit range. In particular, a literal name or literal expression can be used as the dimension of an array, as a repetition factor in an assignment statement, as an operand in the defining expression of another literal name, etc. The value of a literal name can even be reassigned by a succeeding LIT statement during compilation. If control is passed to a LIT statement during program execution, control immediately passes to the following statement with no other effect.

Examples:

```
10      LIT FIVE=5
20      LIT PARM=10
30      LIT YARN=PARM+%37
40      LIT FERN=PARM+YARN
50      LIT GERM=FERN/(YARN+1)
```

4.4 SIMPLE AND LOOP CONTROL STATEMENTS

SHADOW provides several statements for controlling the flow of program execution. The GOTO statement is a means for altering the normal linear flow of execution. The GOSUB and RETURN statements together provide a simple subroutine capability.

4.4.1 GOTO Statement

The metalinguistic representation of the SHADOW GOTO statement is as follows:

```
goto_statement  ::=  line_number GOTO line_number_2

  line_number_2  ::=  line_number
```

A GOTO statement alters the normal sequential flow of control. The next statement to be executed is not the one immediately following the GOTO statement, but the one referenced by the line number specified in the GOTO statement.

GOTO statements cannot reference a statement within the range of a FOR statement (see paragraph 4.3.3) or a DEF statement (see paragraph 4.1.0) unless they are also in that range. A GOTO statement can transfer control from within the range of a FOR statement to a statement outside of the range, but not from within the range of a DEF statement to a statement outside of its range.

Examples:

```
30   GOTO 120
260  GOTO 550
```

4.4.2 GOSUB and RETURN Statements

The metalinguistic representation of the SHADOW GOSUB and RETURN statements is as follows:

```
gosub_statement  ::=  line_number GOSUB line_number_2

  line_number_2  ::=  line_number

return_statment  ::=  line_number RETURN
```

The GOSUB and RETURN statements together provide a simple subroutine capability. Execution of a GOSUB statement saves the line number of the statement immediately following and then transfers control to the statement whose line number is specified in the GOSUB statement. Execution of a RETURN statement returns control to the statement whose line number was saved by the most recently executed GOSUB statement.

There is no practical limit to the number of GOSUB statements that can be "active" at any one time, thereby permitting the execution of subroutines within subroutines. The association of RETURN statements with GOSUB statements is completely interactive.

A GOSUB statement cannot make reference to a statement within the range of a FOR statement or a DEF statement unless it is also in that range. A GOSUB statement within the range of a FOR statement can transfer control to a statement outside the range. However, a GOSUB statement within the range of a DEF statement cannot transfer control to a statement outside the range.

Examples:

```
30   GOSUB 120
       :
       :
140  RETURN          !return to statement following
                     !GOSUB 120
```

4.4.3 Loop Control Statements

The SHADOW FOR and NEXT statements used together provide a simple iterative looping capability. The metalinguistic representation of the FOR and NEXT statements is as follows:

```
for_statement  ::=  line_number FOR control_variable = initial,limit
                    [,line_size]

  control_variable  ::=  simple_numeric
  initial  ::=  expression
  limit  ::=  expression
  line_size  ::=  integer_constant

next_statement  ::=  NEXT control_variable
```

The range of a FOR statement begins with the first statement following the FOR statement and extends up to and includes the first NEXT statement containing the same control variable.

Execution of a FOR statement evaluates the initial and limit expressions, assigns the initial value to the control variable, and performs a loop test. The loop test compares the value of the control variable with the value of the assigned limit. If the limit is not exceeded, control continues with the following statement. When the NEXT statement that terminates the range is executed, the control variable is incremented by the value of the line size, and the loop test is repeated. The default value of the line size is 1; the legal range of values is [1,255]. Looping continues until the value of the control variable exceeds the assigned limit. When the loop test fails, control passes to the first statement following the NEXT statement.

One FOR statement can appear inside the range of another if the associated NEXT statement (and hence the associated range) also appears within the range of the other. This is referred to as "nesting" FOR loops and can be done to any desired depth of nested ranges, as long as the range of an inner loop does not extend beyond the range of an outer loop.

No FOR statement can use a control variable that matches the control variable of an enclosing range. No statement outside the range of a FOR statement can explicitly transfer control to a statement within it. However, a statement within the range can transfer control to a statement outside of it. If then, such a transfer is made by a GOSUB statement, the associated RETURN statement is permitted to restore control to the statement within the range at the line number following that from which the transfer took place.

Example:

```
100     FOR L1=N,M,4
         :
120     FOR L2=L1,M
         :
135     NEXT L2
         :
155     NEXT L1
```

4.5 COMPARISON STATEMENTS

SHADOW provides statements that allow for the comparison of program-generated values. The IF statement provides a means for conditional transfer of control. The COMP statement provides a convenient means of testing for equality between two arrays of the same type.

4.5.1 IF Statement

The metalinguistic representation of the SHADOW IF statement is as follows:

```
if_statement  ::=  line_number IF relation, line_number_2

  relation  ::=  { relation_primary relational_op relation_primary |
                   expression }

  relation_primary  ::=  { expression | character_constant |
                           simple_string | array_string |
                           mask_constant }

  relational_op  ::=  { < | <= | = |  >= | > | <> }
```

The IF statement provides a means for conditional transfer of control. If the relation is true, then control is transferred to the statement referred to by the line number specified in the IF statement. If the relation is false, then control passes to the statement immediately following the IF statement. The permitted forms for a relation are comparison of numeric values, comparison of string values, comparison of a numeric or a string value with a mask constant, and testing of an expression for a nonzero value. Comparisons can be for the following conditions:

a. Less than (<)

b. Less than or equal (<=)

c. Equal (=)

d. Greater than or equal (>=)

e. Greater than (>)

f. Not equal (<>)

A mask constant is intended for use only in equal or not-equal tests where a D ("don't care") is used to match either a 0 or a 1 in the same bit position of a numeric value. Therefore, a mask constant cannot be compared with another mask constant.

Since only single values can be compared, an array string variable used as a relation primary must be qualified by a single-element range index. A string value is compared to a numeric value or a mask constant by considering the bit pattern to have eight implied leading zero bits.

Although an expression can appear as a relational primary, it can also appear alone as a complete <relation>. In the latter case, the relation is 'false' if the value of the expression is zero or 'true' if the value is nonzero. COMPERR# can be tested in this way, for example, if program logic depends upon the correct execution of a COMP statement.

An IF statement cannot refer to a statement within the range of a FOR statement or a DEF statement unless it is also in that range. It can transfer control out of the range of a FOR statement but not out of the range of a DEF statement.

Examples:

```
115    IF A>B+3,135
120    IF STATUS=%B11000DDD000,450
135    IF COMPERR#,325
140    IF ARRAY$[5]=" ",265
```

4.5.2 COMP Statement

The metalinguistic representation of the SHADOW COMP statement is as follows:

```
compare_statement  ::=  line_number COMP comparison [,error_limit
                        [,logical_unit_specifier] ]

  comparison  ::=  { numeric_comparand,numeric_comparand |
                     string_comparand,string_comparand }
  numeric_comparand  ::=  array_numeric [bit_range]
  string_numeric  ::=  array_string [bit_range]
  error_limit  ::=  { expression | empty }
  logical_unit_specifier  ::=  expression
```

The compare statement provides a convenient means of testing for equality between two arrays of the same type. Each array supplies a range of elements, the shorter of which determines the length of the comparison. An array identifier alone supplies all of its elements (beginning with element 0). An array id qualified by a range index supplies all elements within the range. The range for an array id subscripted with a single element begins with the indicated element and continues through the last element.

A comparison is made between the two sequences of elements, which may or may not have corresponding indexes within respective arrays. Pairs of elements are tested until one of the following conditions occurs: a) one sequence of elements is exhausted, b) the number of unequal pairs reaches the optional error limit, or c) the number of errors charged against the optional logical unit specifier exhausts the cumulative error count established for that device. Each unequal pair of elements tested is reported as a separate error. If the entire comparison is successful, the special numeric COMPERR# is set to 'false' (0). If an unequal comparison occurs, COMPERR# is set to 'true' by assigning it %100000 plus the index value of the left-hand array element from the unequal pair. Thus, the value of COMPERR# reflects the last reported error, if any, from the most recently executed COMP statement. If a logical unit number is specified, the comparison is delayed until completion of any I/O activity on the associated device (see paragraph 5.10, describing the special numeric WAIT#, for exceptions).

Examples:

```
65   COMP ARRAY1$,ARRAY2$
75   COMP BUFFER1,BUFFER2,1,DISC
120  COMP ARRAY[10],BUFFER[20:29],,TAPEUNIT
```

4.6 INTERACTIVE STATEMENTS

SHADOW provides several statements to enable user interaction with an executing program. The PRINT statement causes information, including error messages and instructions, to be displayed at the test terminal. The INPUT statement allows the user to enter values for specified program variables. The PAUSE statement allows the user to decide whether to continue from a point of program suspension.

4.6.1 PRINT Statement

The metalinguistic representation of the SHADOW PRINT statement is as follows:

```
print_statement  ::=  line_number PRINT [print_item_list]

  print_item  ::=  { string_constant | simple_string | array_string |
                     expression [:format] }
  format  ::=  { % | %B }
```

The PRINT statement outputs print items in left-to-right order and then issues a carriage return and line feed. A simple string variable or an element in a string array is printed by reproducing the single character that is the current value. A string constant is printed by reproducing the sequence of characters that are its value. The value of an expression can be printed in any of three ways. If the format is not specified, the default is a signed decimal integer right-justified in a seven-character field. The sign immediately precedes the leftmost digit (leading zeros are not printed) and is either a hyphen (explicit minus sign) or a blank (implicit plus sign). If the expression is qualified by a format, the value of the expression is then printed as a bit pattern. An isolated percent sign (%) formats the value as an octal integer, right-justified in a seven-character field. Leading zeros are not printed. A percent sign qualified by the letter B (%B) formats the value as a binary integer, right-justified in a 22-character field. All sixteen digits are always printed in this format. The bits are printed in groups of three (except for bit 0 which forms a separate group) with each group preceded by a blank.

In all formats, any unspecified leading characters of the field are printed as blanks. At least one blank always separates the representation of a numeric value from that of the preceding print item. Whenever the field width of the next print item exceeds the number of character positions remaining in the current line, a carriage return and line feed are issued before printing the value.

If no print items are specified, a carriage return and line feed are sent to the test terminal.

Examples:

```
45      PRINT "Enter loop count"
60      PRINT ! carriage-return and line-feed only !
95      PRINT DECNUM,OCTNUM:%,BINUM:%B,SAVE+5
100     PRINT "Test number",TESTNUM,"No. of errors",ERRCNT
110     PRINT "Nominal values are",44,-5:%,%1777:%B
```

4.6.2 INPUT Statement

The metalinguistic representation of a the SHADOW INPUT statement is as follows:

```
input_statement  ::=  line_number INPUT destination

  destination ::=  { simple_numeric [,value_range] |
                     array_numeric [,value_range] |
                     simple_string | array_string | special_numeric }
  value_range  ::=  low_range,high_range
  low_range  ::=  integer_constant
  high_range  ::=  integer_constant
```

The INPUT statement allows the program to assign a user-specified value to a variable during program execution. Interpretation of the user response depends on the specified destination.

If the destination is a simple numeric variable or an array numeric variable, the input must be in the form of an integer constant, optionally preceded by a minus sign (-). Preceding and following blanks are ignored. If an optional value range is specified, the value (viewed as a two's complement integer) must lie in the range [low value,high value]. The high value cannot be less than low value. If the destination is an array numeric variable with no range index specified, the input value is assigned to each element of the array. If the array numeric variable is qualified by a single-element range index, the input value is assigned to that element with no repetition. If the numeric destination contains a bit-range qualifier, only the specified bit range is affected by the input; the previous value of bits outside the range are retained.

If the destination is a simple string variable or an array string variable, the characters of the input line are assigned to it without editing (blanks are considered part of the data). If the destination is a simple string variable, only the first character of the input line is assigned. If the destination is an array string variable with no range index specified, the string constant represented by the input line is repeated, if necessary, to provide values for all elements of the array. If the array string variable is qualified by a single-element range index, assignment begins with the specified element with no repetition.

The special numeric NONE# is set by each execution of an INPUT statement. When a numeric value is expected, either an empty line or an all-blank line sets NONE# to 'true'; otherwise NONE# is set to 'false'. When a character string is expected, only an empty line sets NONE# to 'true'. Thus, NONE# can be tested in an IF statement to check for a null response to the last INPUT statement.

Execution of an INPUT statement causes a question-mark "?" to be sent to the test terminal as a user prompt. An invalid response produces an error message followed by another prompt.

Examples:

```
45      PRINT "Enter loop count"
50      INPUT LOOPCOUNT,1,255
55      IF NONE#,45
          :
100     PRINT "Enter test pattern as: cccc"
110     INPUT TESTPAT$
```

4.6.3 PAUSE Statement

The metalinguistic representation of the SHADOW PAUSE statement is as follows:

```
pause_statement  ::=  line_number PAUSE
```

The execution of a PAUSE statement causes program execution to be suspended until the user responds with a carriage return at the test terminal. However, no indication is given to the user that the program is in the paused state. It is left to the individual program to precede the PAUSE statement with an appropriate message.

Example:

```
100   PRINT "PRESS RETURN TO CONTINUE"
110   PAUSE
```

4.7 I/O CONTROL STATEMENTS

SHADOW provides two statements dealing with I/O control, the EIO and EXPECT statements.

4.7.1 EIO Statement

The metalinguistic representation of the SHADOW EIO statement is as follows:

```
eio_statement  ::=  line_number EIO logical_unit_specifier
                    ,io_command:protection
                    ,[eio_parameter]
                    ,[eio_mask]
                    ,interrupt_part

  io_command  ::=  expression
  protection  ::=  integer_constant
  eio_parameter  ::=  expression
  eio_mask  ::=  { expression | mask_constant }
  interrupt part  ::=  number_of_interrupts
                       [,timeout [, [status_mask:] cause_mask] ... ]
  number_of_interrupts  ::=  integer_constant
  timeout  ::=  { expression | empty }
  status_mask  ::=  { expression | mask_constant }
  cause_mask  ::=  { expression | mask_constant | empty }
```

NOTE: Masks are right justified.

An EIO statement constructs and issues an EIO instruction to the device associated with the logical unit referred to. The 8-bit hardware command field is taken from bits <8:15> of the io-command parameter. Bits <13:15> of the protection parameter set the states of three protection toggles; the default values depend on whether or not interrupts are expected (refer to paragraph 5.10, describing the special numeric WAIT#, for further information). The value of the EIO parameter is used as the device-dependent parameter word (default value is 0). The status returned is stored in the EIO status field of the device table entry for the specified logical unit. The number of interrupts expected in response to the EIO instruction (0 to 3 inclusive) must be supplied. The timeout parameter gives the interval within which all interrupts are expected to occur (in milliseconds*10); default is 100, implying 1 second. Any commas that would follow the last nonempty parameter in an EIO statement can be omitted.

A condition code of CCL always produces an error message and completes execution of the statement. Otherwise the status of the EIO instruction is tested against the EIO mask (whose default value is 0). A failure to compare equal (except for "don't care" bit positions) produces an error message. The special numeric ERROR# is set to 'true' if an error is reported, otherwise to 'false'. Interrupt status and cause words are tested against the corresponding status mask and cause mask (whose default values are 0). An error message is generated if bits 0 through 7 of the interrupt status word do not match bits 8 through 15 of the status mask, or if the interrupt cause word does not match the cause mask (except for "don't care" bit positions). If more than one interrupt is expected, a separate status mask and cause mask may be supplied for each interrupt; otherwise the default values are used. The special numeric ERROR# is also set to 'true' if the special numeric WAIT# has the value 0 when an error is reported for an interrupt.

If the condition code is CCE, execution of the EIO statement continues until all interrupts are processed. Any interrupts not received within this interval are assumed to be permanently missing. The processing of each expected interrupt stores the two words of status in the interrupt status fields of the device table entry of the specified logical unit.

Failures associated with condition code CCG imply rejection of the EIO instruction. In these cases (any combination of the O-bit, I-bit, A-bit, or P-bit set), statement execution completes without further action.

Refer to paragraph 5.10, describing the special numeric WAIT#, for further information regarding I/O activity and the degree of concurrency permitted among I/O operations.

Examples:

```
100     EIO LUN,READ,PARM,EIOMASK,1,10,INTMASK:
120     EIO PTR,WRT,PARWORD,%B1100DD,1,,CAUSEMSK
225     EIO LUN,2,PARA,%B10DDD,1,50,%BD00000:0
300     EIO DISC,LDHDSECT,HEAD'<<'8+SECT.<8:15>,,1
395     EIO TAPE,RWD:6,,,1,10000
415     EIO LUN,WRCMD,CTLCHAR,EIOMSK,1,,INTMSK1:INTMSK2
```

4.7.2 EXPECT Statement

The metalinguistic representation of the SHADOW EXPECT statement is as follows:

```
expect_statement  ::=  line_number EXPECT logical_unit_specifier,
                       interrupt_part
```

The EXPECT statement instructs the system to expect from one to three interrupts from the specified logical device. The interpretation of the parameters is identical as that for the corresponding parameters of the EIO statement, except that no EIO instruction is issued and that no EIO status processing occurs. The special numeric ERROR# is also set to 'true' if the special numeric WAIT# has the value 0 when an error is reported for an interrupt. The EXPECT statement allows a program to anticipate and process attention interrupts. Any commas that would follow the last nonempty parameter may be omitted.

Refer to paragraph 5.10, describing the special numeric WAIT#, for further information regarding I/O activity.

Examples:

```
155     EXPECT TAPE,2,,STMASK:,CAUSEMSK
225     EXPECT DISC+I,1
300     EXPECT LUN,2,10000,%B100DD:,%B110DD:%B1DDD
```

4.8 DEVICE TABLE STATEMENTS

SHADOW provides two statements that access the device table. (The device table is a special data space maintained by every executing SHADOW program.) The SETDEV statement causes an entry to be made in the device table identifying each device under test and defining certain attributes of each device. The GETDEV statement is used to retrieve the current contents of the device table for a given device under test.

4.8.1 SETDEV Statement

The metalinguistic representation of the SHADOW SETDEV statement is as follows:

```
set_device_table_statement  ::=  line_number SETDEV
                                 logical_unit_specifier
                                 [,error_count
                                 [,characteristic
                                 [,physical_unit_number] ] ]

  error_count ::=  { expression | empty }
  characteristic  ::=  { expression | empty }
  physical_unit_number  ::=  integer_constant
```

The SETDEV statement creates a device table entry for the specified logical unit, or, if an entry already exists for that logical unit, alters or deletes it.

The error count parameter sets a limit on the cumulative number of errors allowable for the logical unit. A negative value given for the error count is treated as equivalent to the positive value found by adding 65536 to it. Each error charged against the unit reduces the value in the device table by 1. If the error count reaches 0, the SHADOW system automatically stops issuing operations to the logical unit and stops executing COMP statements that refer to it. The characteristic supplies a device-dependent numeric value that can be associated with the logical unit; SHADOW makes no implicit use of it. The physical unit number evaluates to an integer in the range [0:255], which identifies the physical location of the device; i.e., the controller number and unit number. Each logical unit must be associated with a unique physical unit number.

If an entry is created for a new device, any empty parameters have the following default values: a) error count = 32767; b) characteristic = 0; and c) physical unit number - no default exists (an attempt to perform an operation with the associated logical unit will result in a program error). If an entry already exists for the indicated logical unit, the nonempty parameters supply new values to be assigned to the corresponding fields of the device table entry. As a special case, a physical unit number that evaluates to a negative number is interpreted as a request to deallocate the device; the device table entry associated with the referenced logical unit is then deleted.

Examples:

```
5       SETDEV 5,,64 '<<' 8 + 132,32
10      SETDEV LUN+I,256,DEVCHAR+I,CTLR '<<' 3 + UNIT
15      SETDEV DISC,,,CTLR '<<' 3 + UNIT
20      SETDEV DISC1,,,-1
```

4.8.2 GETDEV Statement

The metalinguistic representation of the SHADOW GETDEV statement is as follows:

```
get_device_table_statement  ::=  line_number GETDEV
                                 logical_unit_specifier
                                 [,interrupt_status
                                 [,interrupt_cause
                                 [,eio_status
                                 [,error_count
                                 [,characteristic
                                 [,physical_unit_number] ] ] ] ] ]

  interrupt_status  ::=  { simple_numeric | array_numeric | empty }
  interrupt_cause   ::=  { simple_numeric | array_numeric | empty }
  eio_status  ::=  { simple_numeric | array_numeric | empty }
  error_count  ::=  { simple_numeric | array_numeric | empty }
  characteristic  ::=  { simple_numeric | array_numeric | empty }
```

The GETDEV statement unpacks the device table entry associated with the specified logical unit. Each nonempty parameter is assigned a value from the table, as follows:

a. Interrupt status contains the status word returned by the last expected interrupt from the device.

b. Interrupt cause contains the interrupt cause word returned by the last expected interrupt from the device.

c. EIO status contains the status returned by the last EIO instruction issued to the device.

d. Error count contains the remaining error count allowed for the device.

e. Characteristic contains the device-dependent numeric value for the device.

f. Physical unit number contains the controller and unit number of the device.

Examples:

```
1055  GETDEV 2,ISTAT,ICAUS,EIOSTAT,ERRCNT,CHAR,PHYSUNIT
1100  GETDEV DISC,,,,STAT
1200  GETDEV I,INT1[I],INT2[I],EIO[I],ERR[I],CHAR[I],ADR[I]
1235  GETDEV LP+I,,,EIOST,ERRORS
```

4.9 DATA TRANSFER STATEMENTS

SHADOW provides two statements that access the IOC table. (The IOC table is a special hardware-defined data space available to every executing SHADOW program.) The SETIOC statement causes the device table entry associated with the specified logical unit to be filled. The GETIOC statement is used to retrieve the current contents of the IOC table entry associated with the specified logical unit.

4.9.1 SETIOC Statement

The metalinguistic representation of the SHADOW SETIOC statement is as follows:

```
set_ioc_table_statement  ::=  line_number SETIOC
                              logical_unit_specifier,buffer,count [,P]

  buffer  ::=  { array_numeric | array_string }
  count   ::=  expression
```

The SETIOC statement fills the device table entry associated with the specified logical unit. An array identifier (optionally qualified by a single-element range index) identifies the location to be used as the starting buffer address for the next data transfer operation. The count is an expression that yields the byte count to be used for the next data transfer operation. If P is present, it sets the P-bit to invoke read protection.

Examples:

```
60      SETIOC 5,INBUFFER,80
85      SETIOC LUN+I,LINE$,LENGTH,P
150     SETIOC DISC,RECORDS$[I*255],256
```

4.9.2 GETIOC Statement

The metalinguistic representation of the SHADOW GETIOC statement is as follows:

```
get_ioc_table_statement  ::=  line_number GETIOC
                              logical_unit_specifier
                              [,buffer_address
                              [,residual_count
                              [,chan_error] ] ]

  buffer_address  ::=  { simple_numeric | array_numeric | empty }
  residual_count  ::=  { simple_numeric | array_numeric | empty }
  chan_error  ::=  {simple_numeric | array_numeric | empty }
```

The GETIOC statement unpacks the IOC table entry associated with the the specified logical unit. The nonempty parameters are assigned values from the accessed IOC table entry as follows:

a. Buffer address contains the current buffer address.

b. Residual count contains the current byte count.

c. Channel error contains the current channel error bits right-justified in a 16-bit field.

Examples:

```
60      GETIOC 5,ADDRESS,REMCNT,CHERR
85      GETIOC LUN+I,,,CHANERR
150     GETIOC DISC,,COUNT
```

4.10 COMMAND DEFINITION AND INVOCATION STATEMENTS

SHADOW provides two statements, DEF and DEFEND, that can be used to define special user-devised SHADOW statements. The DEF statement designates an identifier that can be invoked and executed throughout the current program as a program statement. Together, the DEF and DEFEND statements delimit a range of standard SHADOW statements that are automatically executed whenever the designated identifier is invoked.

4.10.1 DEF AND DEFEND Statements

The metalinguistic representation of the SHADOW command definition statements is as follows:

```
command_definition_statement ::=  line_number DEF command
                                  [parameter_list]

  command   ::=  identifier
  parameter  ::=  { simple_numeric | simple_string |
                    array_numeric open_bracket close_bracket |
                    array_string open_bracket close_bracket }

end_definition_statement  ::=  line_number DEFEND
```

The purpose of the command definition statements is to permit the user to extend the SHADOW language by introducing new statements which are, in effect, aggregates of the basic SHADOW statements. Command definitions are self-contained entities consisting of a heading and a range. The heading specifies the name assigned to the user statement and lists any parameters. The range specifies the sequence of basic SHADOW statements to be executed by any invocation of the user statement.

Once defined, user statements are invoked in a program by a command invocation statement (refer to paragraph 4.10.2). The command invocation statement specifies the command name assigned in the command definition statement, and furnishes values for any command parameters.

A DEF statement declares the range to be a subpart of the program accessible only through invocation of the command name it specifies. The range of a DEF statement begins with the statement following DEF and continues up to and includes the closing DEFEND statement. Command definition statements cannot be nested, and every DEF statement must have a matching DEFEND statement with a higher line number. A GOSUB statement, a GOTO statement, or an IF statement cannot transfer control into or out of a command range; however, a statement within the command range can invoke another command definition, if desired. Command definitions can appear anywhere and in any order within a program.

If control is passed directly to a DEF statement during execution, it is passed on to the statement following the DEFEND statement with no other effect. Once control is passed into the range, it remains there (except for any nested invocations of other commands) until execution of the DEFEND statement. Control then returns to the statement following the command invocation statement. Except for special numerics, parameters, and any command statements that invoke another user command, all identifiers appearing within a command range are local to it and cannot be referenced from outside the command range. If a local identifier duplicates an identifier used outside of the command range, the reference is directed to the local data space. Thus, the only external data spaces that can be referenced from within a command range are those associated with a parameter by the invoker, which are indirectly accessible. The identifier used for a command name can also be used as an identifier for a data space, since the context in which they are used serves to distinguish them. The same identifier cannot be used to identify a user command in two different DEF statements of a program. The identifiers reserved for the SHADOW commands and statements cannot be defined as command names.

Examples:

```
15    DEF SEEK SLUN,CYL,HEAD,SECTOR
20      EIO SLUN,CYLCMD,CYL,0,0
25      EIO SLUN,HEADSEC,HEAD'<<'8+SECTOR.<8:15>,0,0
30      EIO SLUN,SEEKCMD,0,0,1,10
35    DEFEND

50    DEF READ RDLUN,RCYL,RHEAD,RSECT,BUFFER$[],BYTECOUNT
55      SEEK RDLUN,RCYL,RHEAD,RSECT
60      SETIOC RDLUN,BUFFER$,BYTECOUNT
70      EIO RDLUN,RDCMD,0,0,1,1
75    DEFEND
```

4.10.2 Command Invocation Statement

The metalinguistic representation of the SHADOW command invocation statement is as follows:

```
command_invocation_statement  ::=  line_number command [argument_list]

  command  ::=  identifier
  argument_list  ::=  { expression | simple_string | array_string |
                        string_constant }
```

Execution of a command invocation statement invokes the range of the command definition statement that created the command name. (Refer to paragraph 4.10.1 for a description of the command definition statements.) The arguments in the command invocation statement must correspond to the parameters in the command definition statement in number, order, type, and structure (simple or array). The allowable arguments to parameter associations are as follows:

a. Expression to simple numeric variable

b. Simple string variable or string constant to simple string variable

c. Array numeric variable to array numeric variable

d. Array string variable to array string variable.

A string constant used as an argument can contain only one character. The arguments are substituted for the parameters by reference; that is, the addresses of the arguments are made available to the statements in the command range. Thus the assignment made to a parameter associated with a simple variable or an array accesses the data space of the argument. Expressions and character constants are associated with parameters by creating a copy of the value in a local data space. A special numeric used as an argument is treated as an expression; a local copy of the current value is associated with the parameter. The identifiers used for local variables and parameters within the range of a command definition can be used as arguments for other user commands invoked from within the same range.

Examples:

```
150   SEEK DISC[I],100,5,0
200   SEEK RDLUN,RCYL,RHEAD,RSECT
235   READ DISC2,2,1,12,INBUFFER$,255
```

SECTION 5
SPECIAL NUMERIC VARIABLES

5.0 SPECIAL NUMERIC VARIABLES

SHADOW declares certain predefined special numeric variables that are accessible to the user. Each is identified by a unique name the last character of which is a pound sign (#). The SHADOW special numeric variables are COMPERR#, ERROR#, ERRORMASK#, IDENT#, LITES#, NONE#, RAND#, SWITCHES#, TIMER#, WAIT#, INTERRUPT#, INTSTAT#, and G0# through G9#.

Several of the special numeric variables are assigned values dynamically by SHADOW during program execution so that at any given time they indicate the disposition of the latest occurrence of some class of events. These can be used in relations and as primaries in expressions. Since it may be useful in the logic of a program to simulate the occurrence of a particular event, it is also permissible for the program to explicitly assign values to these variables. However, they should not be used to hold temporary results for more general purposes. The numeric variables G0# through G9#, which are not used by SHADOW, are provided as temporary storage spaces. In addition, they can be used to pass information between command definitions and the main program. The special numeric variable WAIT# is interrogated by SHADOW throughout program execution and is expected to have a value assigned by the program. The values of all special numeric variables are initialized to 0 whenever a program begins execution.

5.1 SPECIAL NUMERIC COMPERR#

COMPERR# contains the status of the most recently executed COMP statement (unless bit 4 of the switch register is set to one). Each execution of a COMP statement sets COMPERR# either to 'true' (by assigning it %100000 plus the index of the left hand array element of the last unequal pair of elements reported) or to 'false' (zero) if no errors occur. COMPERR# can be tested if program logic depends upon the result of a comparison. For example, a program can efficiently analyze the relationship between two arrays by using a loop containing a COMP statement with an error limit of 1. After each error terminates the comparison, the offset of the offending pair of values can be computed and then used to resume testing beyond that point in the arrays. A COMP statement is not executed if it is assigned an error limit of 0, or if it references a deactivated logical unit (e.g., one with an error count of 0). Instead, COMPERR# is simply set to 'false'.

5.2 SPECIAL NUMERIC ERROR#

ERROR# contains the status of the most recently executed I/O control statement (unless bit 4 of the switch register is set to one). Each execution of either an EIO statement or an EXPECT statement sets ERROR# to 'false' (zero) except in the following cases:

a. ERROR# is always set to 'true' (nonzero) if an error is reported in response to an EIO instruction.

b. ERROR# is set to 'true' (nonzero) if WAIT# has a value of 0 and an error is reported during processing of any interrupts associated with the I/O control statement.

In addition, ERROR#.<0> is set to 'true' (one) if an EIO instruction fails with a condition code of CCL.

An EIO statement or EXPECT statement referencing a deactivated logical unit is not executed. Instead, ERROR# is simply set to 'false' (zero).

5.3 SPECIAL NUMERIC ERRORMASK#

ERRORMASK# is a bit mask that may be set by a program to enable or disable various SHADOW error messages. When set to 'true' (one), the bits have the following meanings:

<15> disable reporting of type 0 errors (compare errors)

<14> disable reporting of type 1 errors (EIO errors)

<13> disable reporting of type 2 errors (interrupt errors)

<12> disable reporting of type 3 errors (unexpected interrupts)

<10> disable setting of COMPERR#

<9> disable setting of ERROR#

5.4 SPECIAL NUMERIC IDENT#

The righthand byte of IDENT# contains the message identifier supplied in the most recent OPTION IDENT,<num> command. The lefthand byte of IDENT# contains the processor type -- 3: TNS/II, 1: TNS I. If the IDENT option is not in effect, IDENT# is assigned a value of -1.

5.5 SPECIAL NUMERIC LITES#

LITES# allows a program to display a value in the control panel lights of the processor being used by SHADOW. When used as the left member in an assignment statement, the assigned value is displayed in the control panel lights. When used as the right member in an assignment statement, the previously assigned value is returned.

5.6 SPECIAL NUMERIC NONE#

NONE# contains the completion status of the most recently executed INPUT statement. NONE# can be tested by a program after the execution of an INPUT statement for the following conditions:

a. If NONE# is 'true' (nonzero), no data was received.

b. If NONE# is 'false' (zero), data was received.

5.7 SPECIAL NUMERIC RAND#

RAND# supplies a psuedo-random 16-bit pattern each time it is referenced during execution. It provides a convenient means of creating random test data or of introducing an element of variability into the control flow of a program. It is possible to restart the sequence of values at a known point. For example, a program can save the value of RAND# in a temporary data space, perform some computations using RAND# as a source of values, and then reassign the saved value to RAND#. This allows repetitive generation of the same sequence of random patterns.

5.8 SPECIAL NUMERIC SWITCHES#

SWITCHES# returns the value currently in the panel switch register.

5.9 SPECIAL NUMERIC TIMER#

The value of TIMER# is incremented by 1 each time the interval clock interrupts, unless the current value is 32767. TIMER# is provided so that programs can compute elapsed time between various points in processing; it is not used directly by SHADOW.

In a typical instance, TIMER# is assigned an initial value of 0 and then its value sampled at a later time to determine how much time is elapsed. Since 'ticks' of the interval clock occur every 10 milliseconds, intervals up to 327.67 seconds can be measured with TIMER# set initially to zero. If 327.67 seconds is too short for some purpose, TIMER# can be set to -32768 or some other negative value, permitting measurement of intervals up to 655.35 seconds with a slightly more complicated computation.

5.10 SPECIAL NUMERIC WAIT#

The value of WAIT# controls the degree of concurrency permitted among I/O operations. SHADOW can operate in any of four modes: a) I/O with wait, b) I/O without wait but with protection, c) I/O without either wait or protection, or d) I/O without wait, protection, or automatic interrupt processing. Special logical considerations exist for the different modes; programs (or parts of programs) designed for execution in one mode may not behave in the expected way in other modes. Programs can assert the desired mode of operation by assigning the appropriate value to WAIT#. If one part of a program requires a particular mode, it can save the current value of WAIT# and then restore it afterwards to avoid interfering with the proper operation of other parts of the program.

5.10.1 I/O With Wait

The normal mode, I/O with wait, prevails when WAIT# = 0. SHADOW always assigns 0 to WAIT# before initiating execution of a program. In this mode, program control is not advanced beyond an I/O control statement until either all expected interrupts have been processed, or the timeout value is exhausted. No additional protection checks are required since no ongoing I/O activity exists during program execution. Program execution is, in effect, suspended until the current I/O operation is completed.

5.10.2 Concurrent I/O With Protection

The second mode, concurrent I/O with protection, is in effect when WAIT# = 1. In this mode, when an EIO statement is encountered, the EIO status is analyzed and control is then passed immediately to the next program statement. Similarly, when an EXPECT statement is encountered, control is passed to the next program statement as soon as the specified EXPECT parameters are noted. The resulting I/O interrupts are processed asynchronously as they occur or until the timeout value is exhausted. I/O activity can, therefore, overlap the execution of subsequent program statements, including other I/O control statements. However, a program statement that specifies the logical unit number of a busy device causes program execution to be suspended until all pending interrupts are processed and the device becomes free. Thus, a GETDEV, SETDEV, GETIOC, SETIOC, COMP, EIO, or EXPECT statement does not affect, or is not affected by, a device that is busy at the time the statement is executed.

Multiple devices on one controller can introduce other dependencies not covered by the previous scheme. The controller for a given device is determined by dividing the physical unit number of the device by 8. Thus, physical devices 30 and 31 share a controller, but devices 31 and 32 do not. Although, for programming flexibility, devices are referenced by logical unit numbers in SHADOW, it is the associated physical unit numbers that determine which ones share controllers. To maximize potential I/O concurrency without sacrificing protection, three toggles are defined for use when WAIT# = 1. They are set by bits 13, 14, and 15 of the protection parameter furnished in each EIO statement. The setting of each toggle asserts an attribute for the resulting EIO instruction as follows:

<15> set to 1: EIO instruction busies the device controller
set to 0: EIO instruction does not busy the controller

<14> set to 1: EIO instruction busies the device
set to 0: EIO instruction does not busy the device

<13> set to 1: EIO instruction can be issued to a busy controller
set to 0: EIO instruction cannot be issued to a busy controller

If no protection is specified, default settings are chosen to minimize the probability of unnecessary execution suspension without creating potential error situations for most devices. Bit 15 is set to 0 if the number of interrupts specified in the EIO parameter is 0; otherwise bit 15 is set to 1. Bit 14 is set to 0 if the number of interrupts specified in the EIO parameter is 0; otherwise bit 14 is set to 1. Bit 13 is always 1 by default. In summary, the default assumption is that every EIO instruction busies both the device and its controller if and only if it expects interrupts, and every EIO instruction can be issued to a busy controller but never to a busy device. An EIO statement whose corresponding EIO instruction cannot be issued to a busy controller should specify bit 13 as 0 to protect itself. An EIO statement whose corresponding EIO instruction expects interrupts but does not busy either the controller, the device, or both should specify as 0 either bit 15, bit 14, or both, respectively, to avoid unnecessary suspensions of subsequent statements. SHADOW cannot provide protection for EIO instructions that expect no interrupts but cause either the device, the controller, or both to be busy, since it has no means other than interrupt processing to determine when a device/controller is no longer busy. If an EIO statement does include a protection qualifier to override any default, it must specify the settings for all three toggles. Since the protection toggles are only interrogated when WAIT# = 1, most programs need not be concerned with these settings.

An EXPECT statement is delayed if the device is busy but not if the controller is busy. It always busies the device but does not busy the device controller.

5.10.3 Concurrent I/O Without Protection

The third mode, concurrent I/O without any protection checking, is in effect when WAIT# = 2. In this mode, control is passed to the next statement following an EIO statement as soon as the EIO status is analyzed. Similarly, control is passed to the next statement following an EXPECT statement as soon as the EXPECT parameters are noted. Execution is never suspended for a subsequent statement even when a device or controller is busy. This mode should be used with extreme caution. It is only needed when a program wishes to force execution of a statement that references a busy device.

5.10.4 Concurrent I/O Without Automatic Interrupt

A fourth mode, WAIT# = 3, is identical to WAIT# = 2 except that device interrupts are not processed automatically. Instead, when SHADOW detects a standard I/O or high-priority I/O interrupt request, it sets INTERRUPT# to 'true' (nonzero) and then returns control to the current program statement. A program that operates in this mode must be designed to accept and process any other device interrupts that may occur prior to the particular one for which it is waiting. Processing of non-I/O interrupts is not affected.

5.11 SPECIAL NUMERICS INTERRUPT# and INTSTAT#

INTERRUPT# and INTSTAT# are intended for use when a program disables automatic I/O interrupt processing by setting WAIT# = 3. A standard I/O or high-priority I/O interrupt request made while WAIT# = 3 is not immediately processed. Instead, SHADOW sets INTERRUPT# to 'true' (nonzero) and returns control to the program. The program may then instruct SHADOW to service the interrupt by setting INTERRUPT# = 0. Along with normal interrupt processing, SHADOW stores the first interrupt status word (which contains the physical unit number of the device) in INTSTAT#. After processing the current interrupt, if other devices are also requesting interrupts, SHADOW again sets INTERRUPT# to 'true' (nonzero) and returns control to the program. Since several devices can contend for service simultaneously, and SHADOW has no control over the order in which the hardware presents them, the program must interrogate INTSTAT# if it is necessary to know which device was serviced last.

5.12 SPECIAL NUMERICS G0# THROUGH G9#

G0# through G9# provide data spaces that are common to all command definitions and the main program. They are not directly used by SHADOW and can be used for the temporary storage of program data. They are also useful when a few key values are used by many commands that would otherwise have to share them through lengthy parameter lists. Any program that uses them for this purpose and is likely to be generally distributed should provide adequate documentation.

SECTION 6
PROGRAM FILE MANIPULATION

6.0 PROGRAM FILE MANIPULATION

As aids to program development and modification, SHADOW provides a number of commands designed to (a) operate on statements or groups of statements in the current program, (b) display the current values of program data spaces, and (c) provide a method for suspending execution at a certain point in a given program. These commands are as follows:

a. ADD command, which causes an entire program file to be appended to the current program.

b. Implicit ADD command, which causes a specified statement to be added to the current program.

c. LIST command, which causes a specified range of statements from the current program to be listed at the test terminal.

d. SAVE command, which causes a specified range of statements in the current program to be placed in a newly specified program file.

e. DELETE command, which causes a specified range of statements to be removed from the current program.

f. RENUMBER command, which causes all the statements in the current program to be renumbered sequentially.

g. FIX command, which causes a specified statement of the current program to be displayed at the test terminal for modification.

h. BREAK command, which enters line numbers into the trace table that indicate the point at which suspension of processing is desired.

i. TRACE command, which is functionally the same as the BREAK command except that program execution is not stopped when a trace line number is reached.

j. CLEAR command, which removes entries from the trace table.

k. DUMP command, which displays portions of the data space of a current program while in conversational mode.

l. DEVice command, which displays device table entries while in conversational mode.

The scope of the LIST, SAVE, and DELETE commands is by default the entire current program file. However, a range parameter can be specified with these commands to limit the scope to any desired portion of the program. The range parameter may be entered in one of four ways:

a. Two line numbers, the first smaller than the second, separated by a comma specify a range that includes all statements from the first line number through the last line number.

b. A single line number followed by a comma specifies a range that includes all statements from the indicated line number through the last statement in the program.

c. A comma followed by a single line number specifies a range that includes all statements from the first statement in the program through the indicated line number.

d. A single line number without punctuation specifies a range that consists solely of the statement identified by the line number.

6.1 ADD COMMAND

The form of the SHADOW ADD command is as follows:

```
add_command  ::=  { ADD file_name | A file_name }

  file_name  ::=  identifier
```

The ADD command appends to the current program the statements contained in the specified text file either read from a library tape or read from the interprocessor bus. File names are used to identify SHADOW text files. A file name can be from 1 to 8 alphanumeric characters in length; the first character must be alphabetic.

The appended statements are renumbered and edited by adding the value of the current last line number to all line numbers in the appended text, thereby preserving all references from one statement to another in the appended statements. Any references to nonexistent line numbers are reported, but the line numbers referenced remain unchanged. Such lines should be corrected before an attempt is made to run the combined program. Any syntactically incorrect lines are also reported and then deleted.

The command is aborted with an appropriate error message if:

a. An adjusted line number exceeds 9999.

b. The storage space for program text is exhausted.

c. A nonrecoverable tape read error occurs.

d. A nonrecoverable interprocessor bus read error occurs.

e. No text file with the specified name is found.

Example:

```
ADD MYDEFS          ! add the text files MYDEFS to the current
                    ! program
```

6.2 IMPLICIT ADD COMMAND

The form of the SHADOW implicit ADD command is as follows:

```
implicit_add_command  ::=  line_number [expression]
```

Any entry at the SHADOW prompt that begins with an integer is interpreted as a program statement with the specified line number. If a statement with the specified line number already exists in the current program, the newly entered statement is interpreted as a replacement for it. SHADOW displays the line to be replaced, deletes it, and inserts the new one. If the specified line number does not exist in the file, the new statement and line number are simply added to the file. If a GET command has not previously been executed, establishing a current program file, a temporary file is created.

Example:

```
100  Y = X[10]*5
```

6.3 LIST COMMAND

The form of the SHADOW LIST command is as follows:

```
list_command  ::=  LIST [range]
```

THE LIST command displays all or a part of the current program text. A range can be used to restrict the listing to any desired portion of the program. The default lists the entire program in order of line numbers.

A program is listed in standard format, not necessarily as entered. Superfluous blanks are deleted; in a few cases blanks are inserted to improve legibility. The ranges of FOR statements and DEF statements are indented to set them off. A user break request made during execution of a LIST command is honored when the current line completes printing.

Examples:

```
LIST 35          ! lists statement 35
LIST 20,30       ! lists statements 20 through 30
LIST ,55         ! lists first statement through statement 55
LIST 25,         ! lists statement 25 through last statement
```

6.4 SAVE COMMAND

The form of the SHADOW SAVE command is as follows:

```
save_command  ::=  SAVE file_name [,range]
```

The SAVE command causes all or part of the current program to be written as a new text file on the library tape. The file name specified is the name to be assigned to the new text file. If the file name duplicates that of a file already present on the tape, the preexisting file is blanked out and the new file is written as the last file on tape. The command does not complete successfully if a nonrecoverable write error occurs or end-of-tape is sensed.

Examples:

```
SAVE MYPROG            ! saves all of current program in a text
                       ! file named MYPROG
SAVE MYPROG, 55,205    ! saves statements 55 through 205 of current
                       ! program in a text file named MYPROG
SAVE MYPROG, ,80       ! saves first statement through statement 80
                       ! of current program in a text file named
                       ! MYPROG
SAVE MYPROG, 80        ! saves statement 80 of current program in a
                       ! file named MYPROG
```

6.5 DELETE COMMAND

The form of the SHADOW DELETE command is as follows:

```
range ::=  { line_number,line_number | line_number, | ,line_number |
```

The DELETE command erases all statements in the current program that have line numbers within the specified range. If no range is specified, the entire program is erased.

Examples:

```
DEL 35                 ! deletes statement 35
DEL 20,30              ! deletes statements 20 through 30
DEL ,55                ! deletes first statement through statement 55
DEL 25,                ! deletes statement 25 through last statement
```

6.6 RENUMBER COMMAND

The form of the SHADOW RENUMBER command is as follows:

```
renumber_command  ::=  REN [increment]

  increment  ::=  integer_constant
```

The RENUMBER command replaces all existing line numbers in the current program with new ones. In the absence of an increment, the new set of line numbers begins with 10 and continues with increments of 10. However, if this would require generation of line numbers greater than 9999, a smaller initial value and increment are used instead. This form of the command is rejected if the only possible increment is 1.

The command can optionally specify the desired initial line number and increment in the range [1,10]. This form is rejected only if it would require generation of line numbers greater than 9999. Note that line numbers are replaced consistently throughout the program so that all references from one statement to another are preserved. If a line number reference in a GOTO statement, a GOSUB statement, or an IF statement does not correspond to an existing line, the reference is not altered.

Example:

```
REN 5                    ! renumbers all statements starting with 5
                         ! and incrementing by 5
```

6.7 FIX COMMAND

The form of the SHADOW FIX command is as follows:

```
fix_command  ::=  FIX [line_number]
```

The FIX command allows the user to edit a statement within the current program. If the line number is omitted, the command defaults to the current statement (the statement last listed, added, or fixed). If during run processing a statement is found to be in error, SHADOW lists the statement. The user may then enter a FIX command (omitting the line number) to edit the statement in error.

Statements are interactively edited by the user. First SHADOW outputs the statement, placing the cursor beneath the first character in the statement and waiting for the user to enter one or more FIX subcommands. FIX subcommands are entered by the user beneath the statement just listed. When the user enters carriage return, SHADOW executes the FIX subcommands and lists the statement in its new form, allowing the user to enter further subcommands. When a carriage return is entered without previous subcommands, SHADOW terminates the FIX command.

The form of the FIX subcommands is as follows:

```
delete_character_subcommand  ::=  { D | d }
replace_character_subcommand  ::= [ R | r ]
insert_character_subcommand  ::=  { I | i }
terminate_subcommand  ::=  //
```

To delete any character, the user enters the letter "D" (or "d") beneath the character. The D subcommand can be followed directly by either of the other subcommands. To replace any character, one for one, with another character, the user enters the letter "R" (or "r") beneath the first character in the statement to be replaced, followed by the replacement character string. The R subcommand need not be entered; if neither D nor I is specified, R is implied. An R subcommand must be terminated with the special termination characters if other FIX subcommands are to be entered for the same line before a carriage return. To insert one or more characters in a line, the user enters the letter "I" (or "i") beneath the character that the insertion is to precede, followed by the insertion character string. An I subcommand must be terminated with the special termination characters if other FIX subcommands are to be entered for the same line before a carriage return.

6.8 USING BREAK POINTS

SHADOW includes several commands for setting and clearing break points in the current program. Used in conjunction with the trace option, these commands provide a convenient method for suspending execution at any number of predetermined points in the program. To set break points in a given program, the user first issues a GET command for the desired program, then an OPTION TRACE, then a BREAK command listing the line number or numbers at which suspension of execution is desired, and then a RUN command. When a break point is reached, SHADOW issues a break message and suspends processing. At this time the program may be modified or the current values of designated program data spaces may be displayed. Entry of the PAUSE command causes programming to resume at the point where it suspended (unless the program was modified during the break). If the RUN command is reentered, the program will start again at the beginning.

The TRACE command may be substituted for the BREAK command; they are functionally the same except that SHADOW does not suspend processing at a trace point but merely displays the break message. The CLEAR command may be issued to delete any or all current entries in the trace table.

6.8.1 BREAK Command

The SHADOW BREAK command enters line numbers into the trace table used by the optional SHADOW trace facility. The form of the BREAK command is as follows:

```
break_command  ::=  { BREAK line_number_list | B line_number_list }

  line_number_list  ::=  line_number [ ,line_number . . . ]
```

Line numbers already present in the table are ignored. Additional line numbers are rejected if the table is full. If the trace option is enabled (refer to paragraph 2.9 for a description of the OPTION Command), SHADOW searches the trace table prior to execution of each program statement while in execution mode. If the line number matches an entry in the table, a break message is displayed, execution is suspended, and SHADOW enters conversational mode. Execution resumes upon entry of a PAUSE command. The full interactive capability of conversational mode is available during a trace break. However, the ability to display data spaces or resume execution is lost if the program is modified. While execution is suspended, data space dumps, device table dumps, or program listings can be aborted with a user 'break' request without losing the ability to resume execution, provided that bit 0 of the switch register is reset to 0 before entering the RUN command. A DIM statement, a DEF statement, a LIT statement, or a statement consisting solely of a comment is not executed and therefore cannot be traced. The form of the break message is as follows:

```
** TRACE **  <line number>
```

The BREAK command, together with the DUMP, DEV, and LIST commands, provides the SHADOW user with a high-level monitoring and debugging facility.

Example:

```
BREAK 10,100,150      !  sets line numbers 10, 100, and 150 in the
                      !  trace table as program break points
```

6.8.2 TRACE Command

Like the BREAK command, the SHADOW TRACE command enters line numbers into the trace table used by the optional SHADOW trace facility. The form of the TRACE command is as follows:

```
trace_command  ::=  TRACE line_number_list
```

Line numbers that are already present in the table are ignored. Additional line numbers are rejected if the table is full. The TRACE command is functionally the same as the BREAK command with the exception that program execution is not stopped when a traced line number is reached; SHADOW simply displays the trace point message and continues processing.

Example:

```
TRACE 5,25,45,50,70
```

6.8.3 CLEAR Command

The SHADOW CLEAR command removes entries from the trace table. If a parameter list is supplied, only the specified line numbers are removed. If no line numbers are given, the entire trace table is cleared. The form of the CLEAR command is as follows:

```
clear_command  ::=  { CLEAR [line_number_list] |
                      C [line_number_list] }
```

Examples:

```
CLEAR 100,150          ! removes line numbers 100 and 150 from the
                       ! trace table
CLEAR                  ! removes all entries from the trace table
```

6.8.4 PAUSE Command

The SHADOW PAUSE command causes a SHADOW program that has been suspend by the BREAK command to resume execution from the point at which the break occurred. The form of the PAUSE command is as follows:

```
pause command ::= { PAUSE | P }
```

Example:

```
PAUSE
?
```

6.9 DISPLAYING PROGRAM DATA SPACES

SHADOW provides two commands, DUMP and DEV, for use in displaying the current values of program data spaces. Typically, they are used in conjunction with the trace option for high-level monitoring and debugging.

6.9.1 DUMP Command

The SHADOW DUMP command displays portions of the data space of the current program while SHADOW is in conversational mode, either after a program has ceased execution or during a trace break. The form of the DUMP command is as follows:

```
dump_command  ::=  DUMP  [/scope/] value_space [:format]

  scope  ::=  command_definition_name
  value_space  ::= { expression | simple_numeric | simple_string |
                     array_numeric | array_string | special_numeric }
  format  ::=  { % | %B }
```

The values of expressions and elements of numeric arrays are displayed in decimal unless either octal (%) or binary (%B) is specified as the format. The values of string variables and elements of string arrays are displayed as ASCII characters by default. If an octal or binary format is specified, each character value is displayed separately as an integer value. Either all of an array or a range of elements can be displayed. A user break request can be used to abort the dump. The ability to dump data spaces is lost if the program is modified.

If the command definition name is not supplied, the data space to be displayed is local only to the main program and excludes all command definitions. Data spaces that are local to a command definition can be displayed by suspending execution within the range of the command definition and by supplying the command name as the scope.

Examples:

```
DUMP /SEEK/ CYL :%      ! dumps CYL in octal (local to SEEK command
                        ! definition)
DUMP WAIT#              ! dumps special numeric WAIT#
DUMP STARRAY$[5:25]     ! dumps elements 5 thru 25 of STARRAY$
DUMP ERROR :%B          ! dumps ERROR in binary
DUMP NUMBERS+7 :%       ! dumps NUMBERS+7 in octal
```

6.9.2 DEVICE Command

The SHADOW DEVICE command displays either one or all device table entries while in conversational mode either after a program has ceased execution or during a trace break. The form of the DEVICE command is as follows:

```
device_command  ::=  DEV [logical_unit_specifier]
```

Default displays all entries in the device table. If a logical unit number is supplied, only the entry for that device is displayed. A user break request is honored only after display of the current table entry is completed. The ability to display the device table is lost if the program is modified.

Examples:

```
DEV 4                   ! displays the device table entry for logical
                        ! unit number 4
DEV                     ! displays entire device table
```

For each device reported, the printed result is as follows:

```
LUN lll IS DEVICE cc:u
ERROR COUNT IS eeeee. CHARACTERISTIC IS cccccc
EIO STATUS IS x xxx xxx xxx xxx xxx
INT STATUS IS s sss sss sss sss sss AND c ccc ccc c
IOC ENTRY HAS i iii iii iii iii iii AND i iii iii iii iii iii
```

The logical unit number (lll) and remaining error count (eeeee) are listed in decimal. The physical unit number (cc:u) and the characteristic (cccccc) are listed in octal. The most recent EIO Status word (x...x), the Interrupt Status word (s...s), and the Interrupt Cause word (c...c) are listed in binary. Only bits <8:15> of the Interrupt Cause Word are listed. The current contents of the IOC table entry (i...i) for the device are listed in binary.

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NonStop EXP™

Cabinet Subsystems

Maintenance Manual

Part No. 82896

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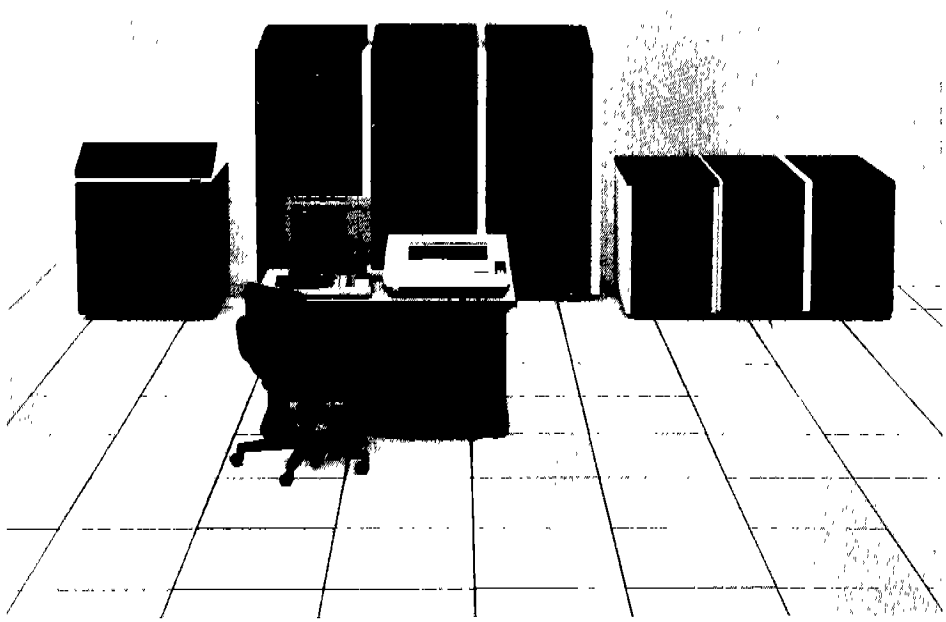
MAINTENANCE MANUAL

NonStop II (TM) and NonStop TXP (TM)

CABINET SUBSYSTEMS



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SECTION 1
INTRODUCTION

1.0 INTRODUCTION

The purpose of this manual is to give installation and maintenance information regarding the cabinet subsystems manufactured to comply with Federal Communications Commission (FCC) standards for electromagnetic interference (EMI).

From the field perspective, the changes may be summarized as follows:

a. All doors are new assemblies with a new latch assembly, EMI gasketing, and a redesigned hinge.

b. Ground straps for the doors and PMI panels have been replaced by straps that have a faston terminal on the frame end to facilitate installation.

c. Cabinet frames have been treated with electrically conductive paint.

d. Cabinet dividers and side covers have been replaced with new assemblies that have EMI gaskets.

e. The two-piece hinge that mounts the plexiglass door to the processor and tape drive cabinets has been replaced.

f. The card cage in processor cabinets is no longer isolated from frame ground.

g. The power distribution units and line filters for both the processor and magnetic tape drive cabinets have been redesigned.

h. The PMI/OSP cable, Tridensity Tape Drive I/O cable, and the Line Printer I/O cable have been separated into an internal and an external cable connected via a universal patch panel fitted with adapters for each connection.

i. IPB Clock and Select cables have been replaced with shielded cables.

j. The PMI Panel assembly has been replaced by an assembly with a redesigned PWA and panel.

k. All disc drive I/O cables have been replaced by shielded versions. Cables that plug into the controller have a ground strap that must be connected to the lower card guide of the card cage. Cables that attach to the patch panel have ground straps that must be terminated to patch panel hardware.

1.1 REFERENCED DOCUMENTS

The following manuals contain supplementary information not covered in this manual:

a. NonStop II AND NonStop TXP SITE PLANNING MANUAL (Part Number 82853). Provides information regarding environmental considerations, electrical requirements, system configuration, cabling, and equipment specifications for products currently supported on the NonStop II and NonStop TXP systems.

b. NonStop II AND NonStop TXP INSTALLATION GUIDE (Part Number 82855). Outlines procedures for installing the NonStop II and NonStop TXP systems.

c. NonStop II AND NonStop TXP POWER SUBSYSTEM (Part Number 82807). Provides information regarding installation and field maintenance of power supplies and battery packs.

SECTION 2
PHYSICAL DESCRIPTION

2.0 PHYSICAL DESCRIPTION

This section describes the cabinets that comprise the system cabinet array.

2.1 SYSTEM CABINETS

The Tandem system normally comprises two or more system cabinets, which are bolted together, side-by-side, to form a single assembly. All system cabinets are supplied with keylocks and two keys. All locks and keys are normally interchangeable.

2.1.1 7123 Processor Cabinet

Processor cabinets come with the following fixed contents regardless of the system configuration (refer to Figure 2-1):

a. A double card cage. The top card cage, which is 32 slots wide, accommodates the processor and memory boards; the lower card cage, which is 24 slots wide, accommodates the I/O controller boards.

b. Four cabinet cooling fans located in a plenum just above the space provided for DC power supplies. The air intake is through a grill and mesh filter at the lower front of the cabinet. The plenum directs the air flow upward through the circuit board cage and out through a grill at the upper rear of the cabinet. Four diodes used in the DC power circuits are mounted on large heat sinks in the fan plenum.

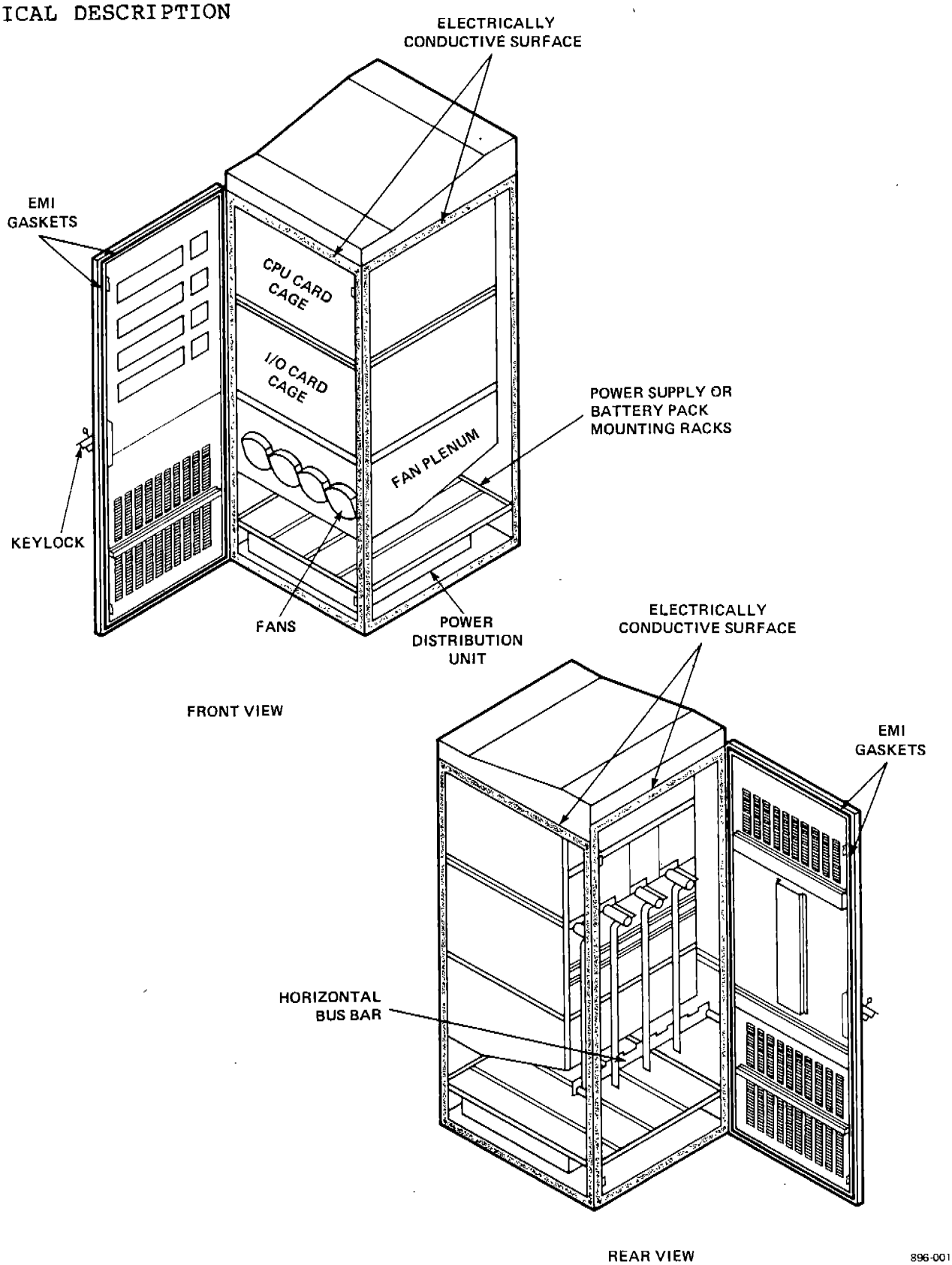

Figure 2-1 Processor Cabinet

c. AC power module located at the bottom of the cabinet (refer to Figure 2-2). This unit receives AC power from the computer power panel via a power cable and distributes it to up to four DC power supplies mounted on rails located just above it. This module also provides AC power outlets for two magnetic tape drives.

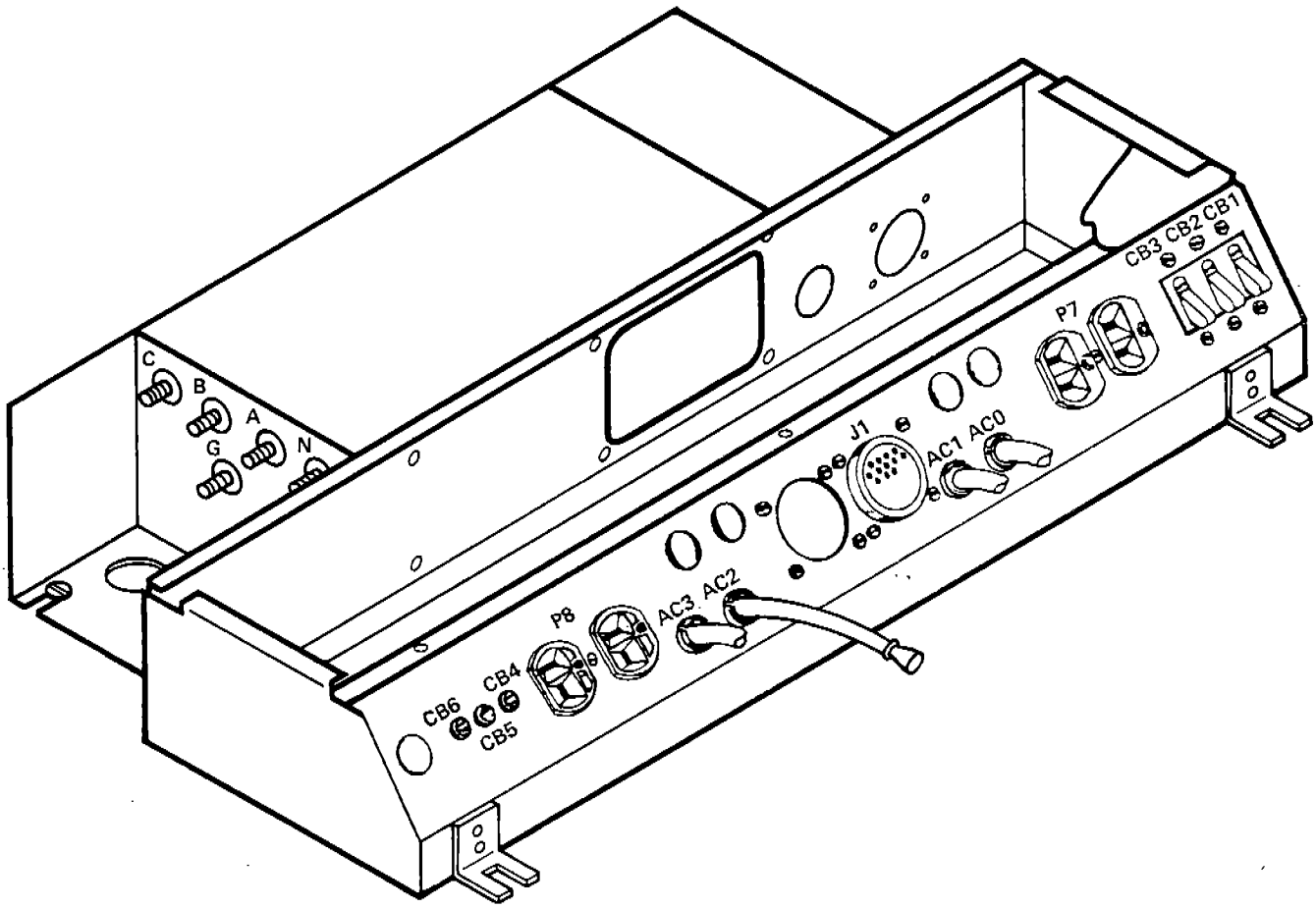

Figure 2-2 AC Power Distribution Module (Processor Cabinet)

d. Laminated horizontal power bus assembly, which distributes DC power to the I/O controllers.

e. Hinged front and rear access doors with keylocks and latches (refer to Figure 2-3). The front door assembly has a metal inner door on which the processor control panels are mounted and a semitransparent acrylic outer door that covers the control panel area. Mountings are provided for four control panels; blanks are installed in unused mountings. Both doors have gaskets, which are designed to fit flush against the conductive surface on the cabinet frame.

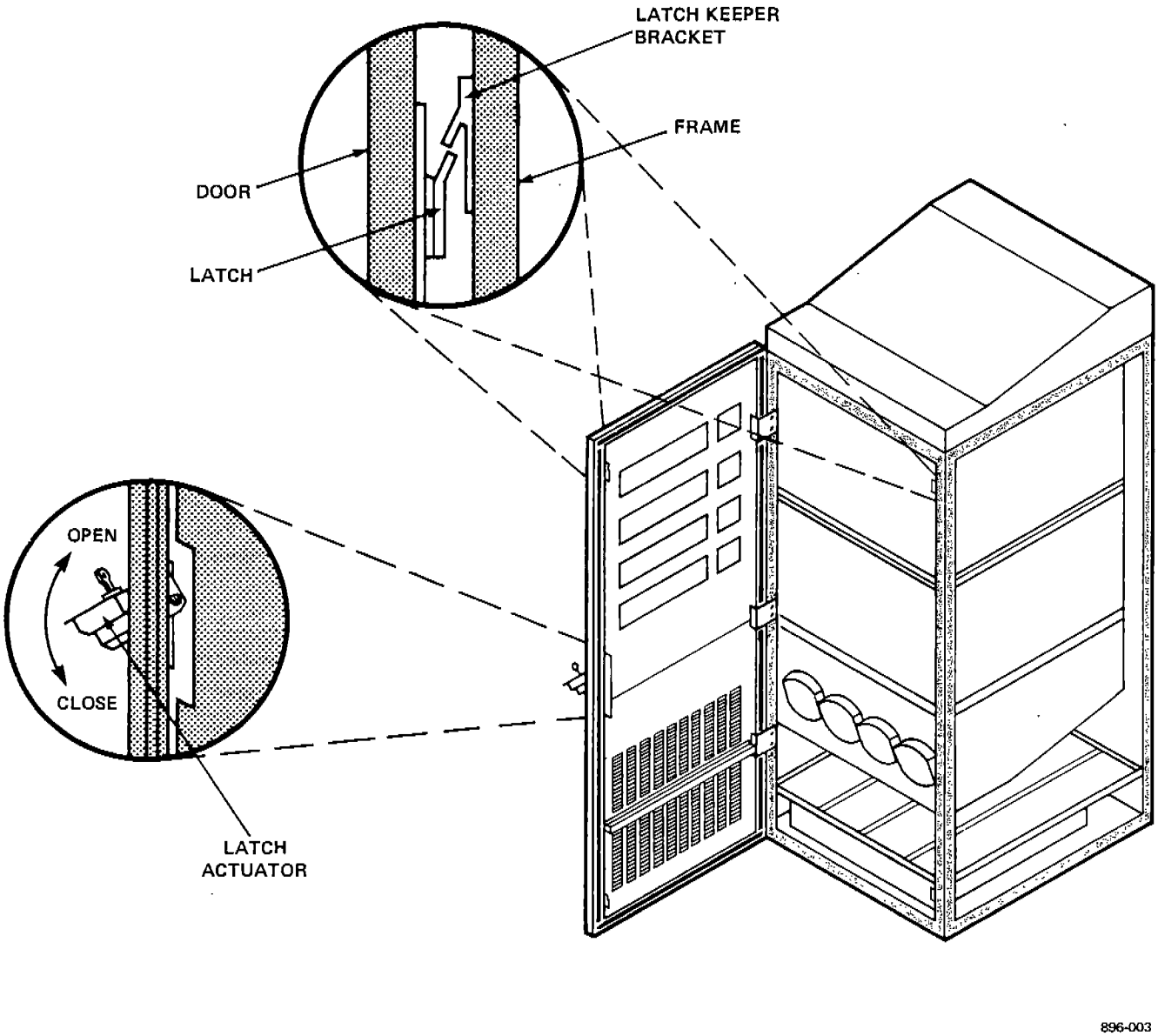

Figure 2-3 Cabinet Door Keylock and Latch Assemblies

f. Cabinet dividers fitted with gaskets on both sides, which are designed to fit flush against the conductive surface on the cabinet frame. Refer to Figure 2-4.

g. End panels fitted with gaskets, which are designed to fit flush against the conductive surface on the cabinet frame. Refer to Figure 2-4. These are interchangeable among system cabinets and, because cabinets are normally fastened together with cabinet dividers, only two end panels are included with each system.

h. Heavy duty casters to facilitate moving the cabinet and extendable feet to support and level the cabinet once it is in place.

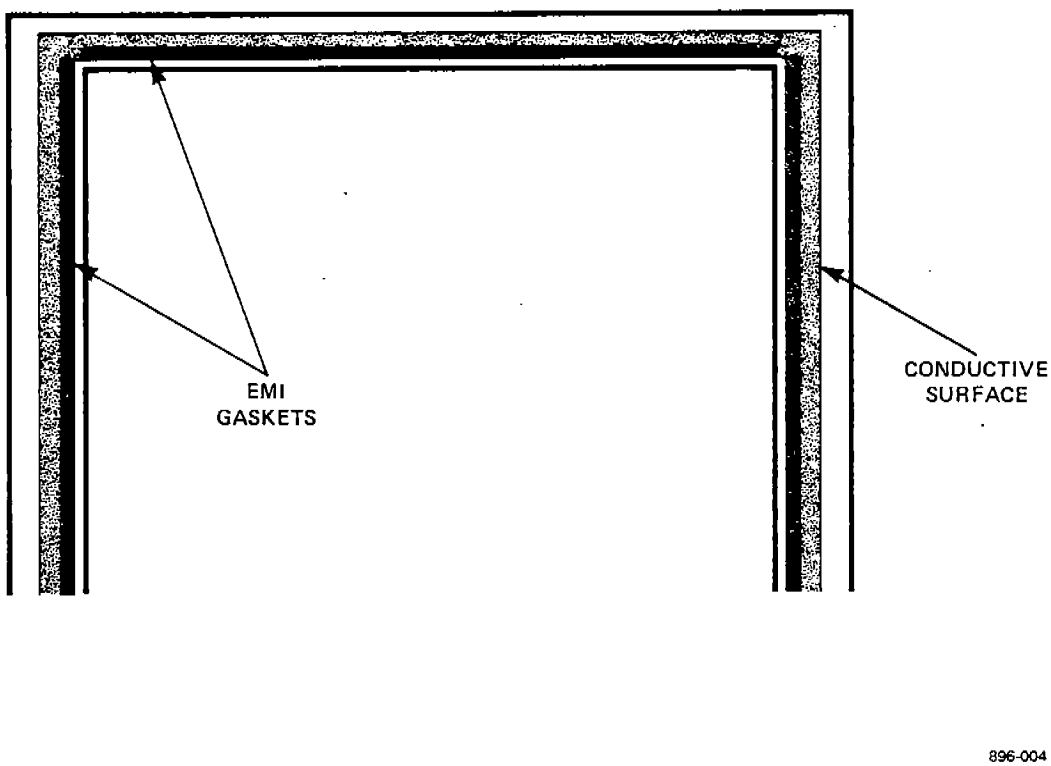

Figure 2-4 Cabinet Divider and End Panel EMI Gaskets

2.1.2 Magnetic Tape Drive Cabinet

The magnetic tape drive cabinet, which has no model number because it is included with the magnetic tape drive, can be used to provide mounting space for various system components besides the magnetic tape drive (refer to Figure 2-5). When used in this capacity, it must be adjacent to the processor cabinet to which it serves as an extension.

The following magnetic tape drives, which may be part of the system cabinet array, are currently supported:

a. 5103 Magnetic Tape Drive, 800/1600 BPI, 45 IPS

b. 5104 Magnetic Tape Drive, 800/1600 BPI, 125 IPS.

NOTE

The 5106/5107 Tridensity Magnetic Tape Drive, which is considered a standalone unit, is not part of the system cabinet array.

The magnetic tape drive cabinet includes the following fixed contents:

a. Tape drive accessible through the front door panel.

b. Front and rear door assemblies with keylocks and gaskets that fit flush against conductive surface of the cabinet frame.

c. Semitransparent acrylic outer door to protect tape drive from dust.

d. Heavy duty casters to facilitate moving the cabinet and extendable feet to support and level the cabinet once it is in place.

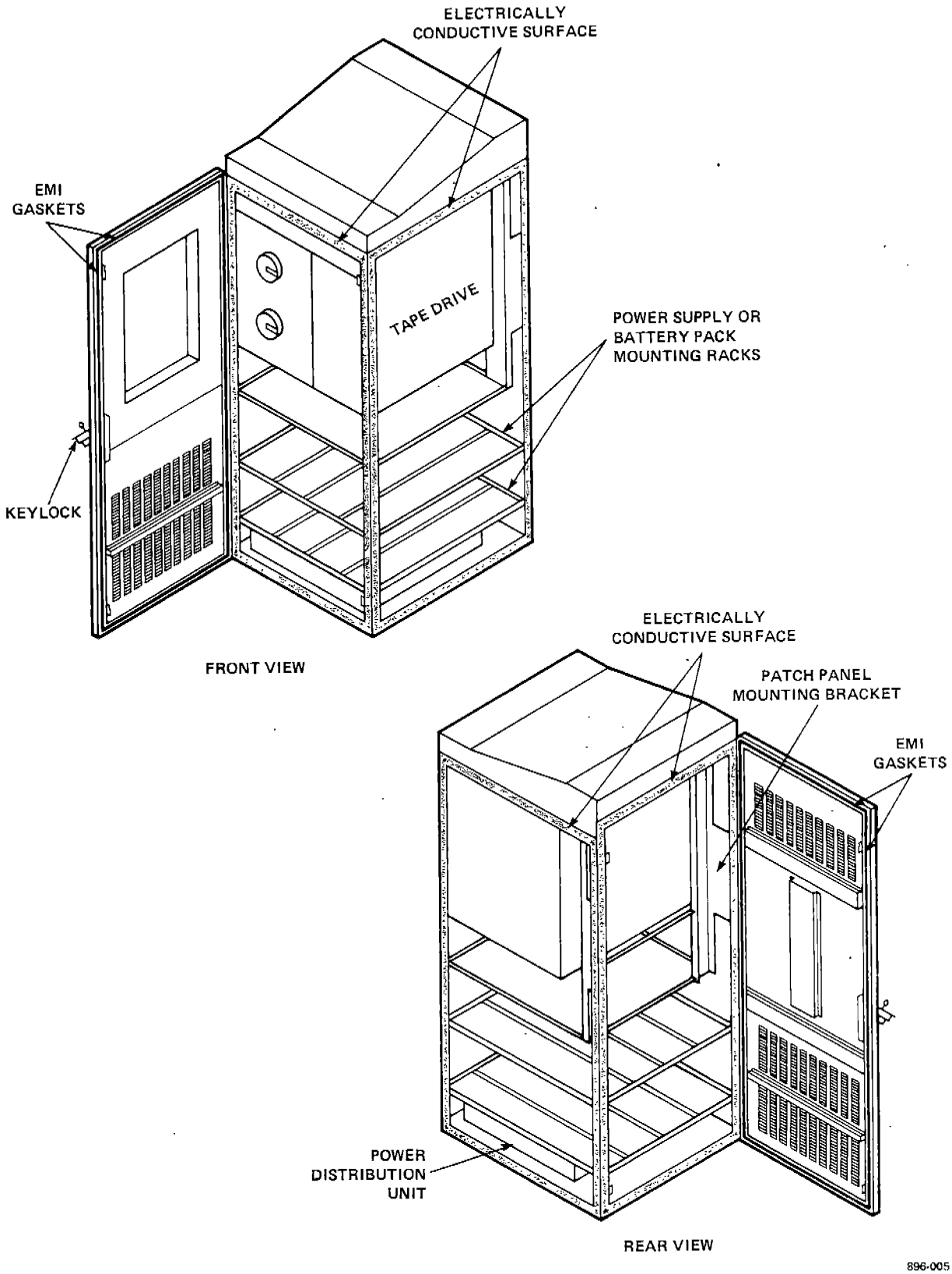

Figure 2-5 Magnetic Tape Drive Cabinet

In addition to the fixed contents, the following components may be included:

a. Battery packs to supply uninterrupted power to memory boards in an adjacent processor cabinet in the event of a power interruption. Up to eight battery packs can be accommodated if none of the mounting racks is used for other power supplies.

b. Supplementary DC power supplies for I/O controllers in an adjacent processor cabinet. Due to AC power current limitation, a maximum of six power supplies can be connected.

c. AC power distribution module to provide power if I/O-only power supplies or battery packs are mounted in the cabinet (refer to Figure 2-6).

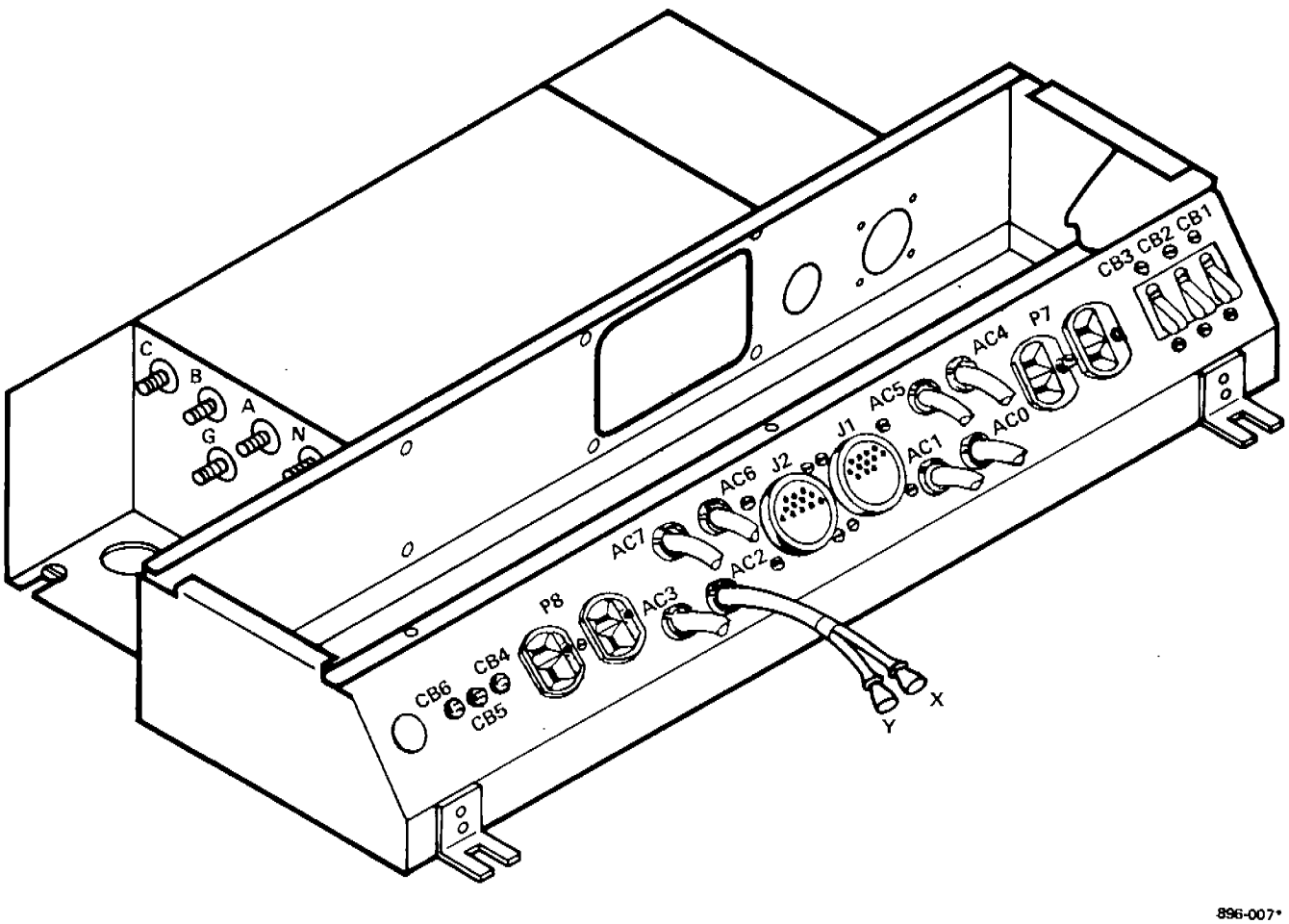

Figure 2-6 AC Power Distribution Module (Magnetic Tape Drive Cabinet)

d. Patch panels. Vertical mounting rails at the rear of the cabinet provide for up to six patch panels of any type.

NOTE

The 5106/5107 Tridensity Magnetic Tape Drive cabinet does not support patch panels, I/O power supplies, or battery packs.

e. End panels. These are interchangeable among system cabinets and, because cabinets are normally fastened together with cabinet dividers, only two end panels are included with each system.

2.1.3 7121 I/O-Only Cabinet

Having the same general appearance as other system cabinets, the 7121 I/O-only cabinet includes an I/O card cage complete with four I/O backplanes to support up to 24 controller boards. It also contains an AC power distribution module like the one in the processor cabinet and one set of power supply rails to support up to three I/O power supplies.

2.1.4 7107 Expansion Cabinet

Having the same general appearance as other system cabinets, the 7107 system expansion cabinet is required for systems that contain three or more processor cabinets. It provides four front mounting spaces and bus extensions in back for any mix of patch panels for the 3106 disc controller, 6303/6304 asynchronous communications controllers, or 6202/6203 synchronous controllers. It also contains an AC power distribution module like the one in the magnetic tape drive cabinet and rails to support up to three I/O power supplies and four battery packs. No more than six I/O power supplies may be installed due to limitations of the AC power distribution module.

2.1.5 7105 Patch Panel Cabinet

Having the same general appearance as other system cabinets, the 7105 patch panel cabinet provides mounting space for I/O device patch panels when the available space in the magnetic tape drive cabinets is inadequate. Normally, no provision is made for AC or DC power distribution within the cabinet, but a power distribution module can be specifically ordered.

SECTION 3
CABLING

3.0 CABLING

To meet FCC regulations regarding EMI, certain changes have been made in the cabling within the system cabinet array and connections to peripheral devices.

3.1 PATCH PANELS

To keep EMI radiation from leaking from the cabinets, three devices that previously were connected directly are now routed through patch panels:

a. OSP/PMI

b. 5513/5514 Line Printer

c. 5506/5507 Tridensity Tape Drives.

More detailed information regarding the cabling of these devices is given in the rest of this section.

Patch panels have ground straps that must be connected to the frame ground when they are installed to ensure FCC compliance.

To ensure that there will be room for the additional patch panels that will be required, the top position in both magnetic tape drive panels and patch panel cabinets is reserved for communication patch panels:

a. 7501 terminal patch panel

b. 7502 synchronous patch panel.

3.2 SYSTEM CABLING

In order to comply with FCC regulations, certain system cable routings are prescribed.

3.2.1 IPB Clock and Select Cables

The IPB Clock and Select cables have been replaced by new shielded cables, which are listed in Table 3.1.

The IPB Select cables are coiled and attached to tie blocks under the cabinet cover directly above the processor to which it is connected. The Select cables for the X Bus IPB controller are positioned toward the middle of the cabinet and routed along the upper cable support brackets to the IPB controller. The cables for the Y Bus IPB controller are positioned toward the rear of the cabinet and routed along the lower cable support brackets to the IPB controller. The prescribed cable routing scheme is depicted in Figure 3-1.

Table 3.1 IPB Clock and Select Cable Part Numbers

DESCRIPTION	PART NO.
IPB Clock Cable:	
TAB DRAWING	42443
6.5 ft (1 or 2 cabinet system)	42444
14 ft (3 to 5 cabinet system)	42445
IPB Select Cable:	
TAB DRAWING	42440
6.5 ft (1 or 2 cabinet system)	42441
14 ft (3 to 5 cabinet system)	42442

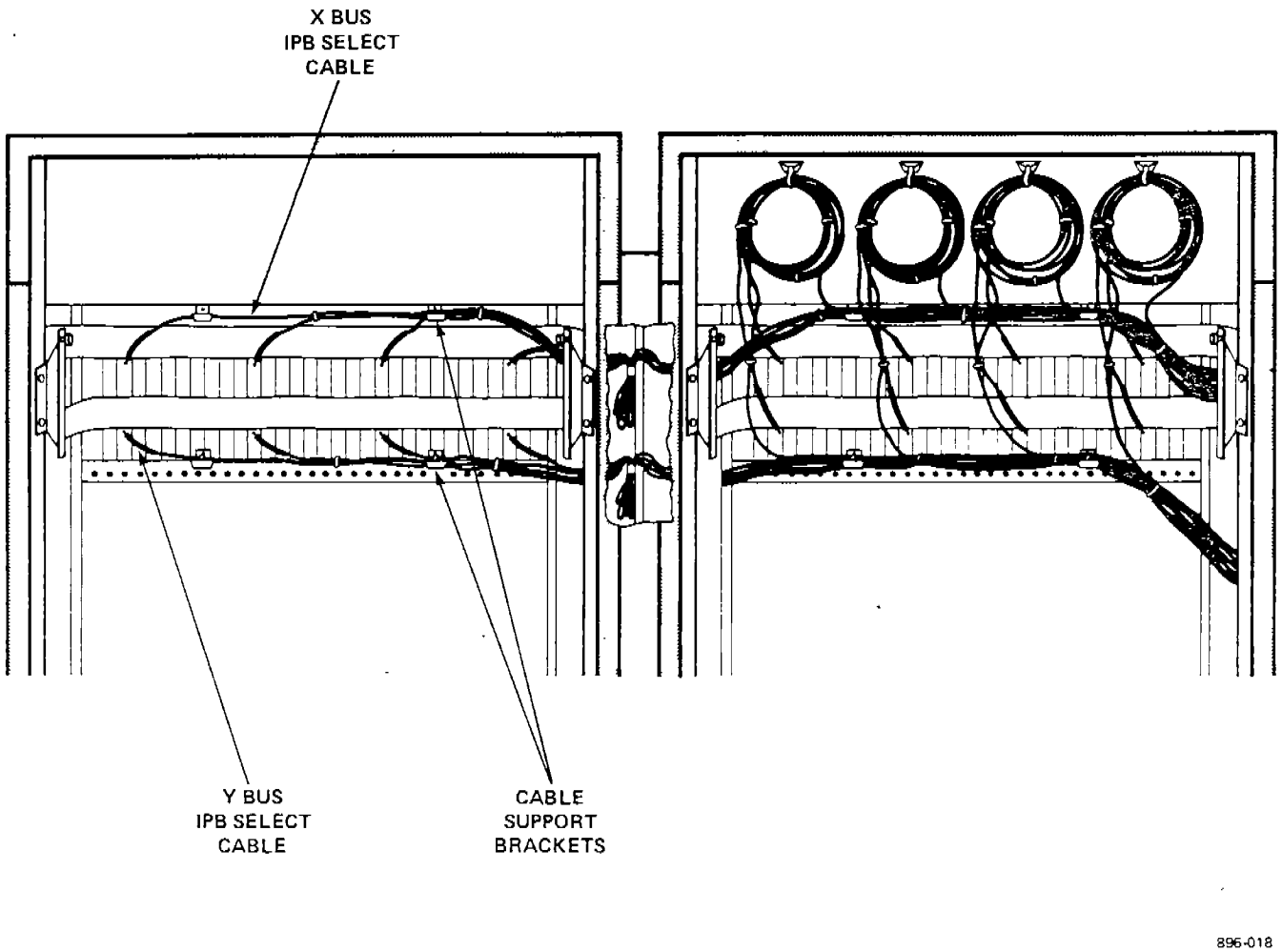

Figure 3-1 IPB Select Cable Routing

3.2.2 Operations and Service Processor

The Operations and Service Processor (OSP) connects to the Processor Maintenance Interface (PMI) through a universal patch panel (Part Number 45535) fitted with an adapter plate. As shown in Figure 3-2, an internal cable connects J8 on the PMI panel of the first CPU cabinet to the patch panel; a second cable runs from the patch panel to J1 of the OSP System Maintenance Processor. Part numbers for the OSP-to-PMI connections are listed in Table 3.2.

Table 3.2 OSP/PMI Part Numbers List

DESCRIPTION	PART NO.
PMI Panel Assembly	42517
PMI Patch Panel	42516
PMI PWA	42470
PMI PWB	42472
Patch Panel to PMI Cable (20 ft)	42583
OSP to Patch Panel Cable (25 ft)	42582
OSP/PMI Patch Panel Adapter Plate	42514

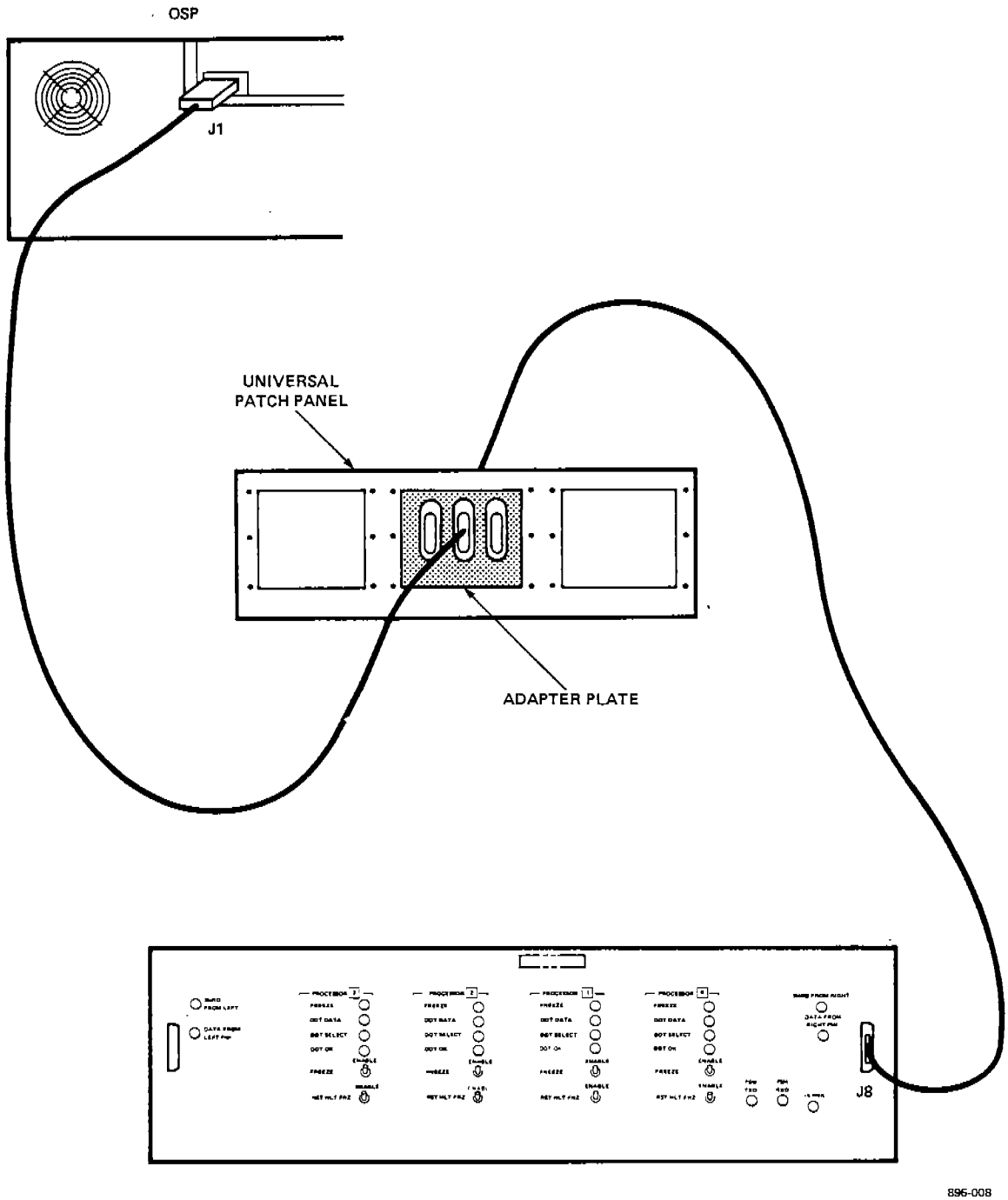

Figure 3-2 OSP-to-PMI Cabling

3.3 PERIPHERAL CABLING

To reduce EMI, many cables to peripheral devices now have braided wire that is attached to ground. In some cases, connections are made through patch panels, rather than directly to the device.

NOTE

> Peripherals that do not comply with FCC regulations cannot be connected to a system that does comply. To determine whether a device meets FCC specifications, look for the FCC compliance label, which must be affixed to the device.

3.3.1 5106/5107 Tridensity Magnetic Tape Drive

The 3206 Magnetic Tape Drive Controller connects to the Tridensity Magnetic Tape Drive via a univeral patch panel (Part Number 45535) fitted with an adapter plate. Refer to Figure 3-3 for cable connections. Part numbers for cables and the adapter plate are listed in Table 3.3.

Table 3.3 Tridensity Magnetic Tape Drive Cabling Part Numbers List

DESCRIPTION	PART NO.
Controller to Patch Panel Cable (8 ft)	49053
Controller to Patch Panel Cable (20 ft)	42557
Patch Panel to Bulkhead Cable (15 ft)	58939
Patch Panel to Bulkhead Cable (25 ft)	58938
Patch Panel to Bulkhead Cable (35 ft)	58581
Adapter Plate	42512

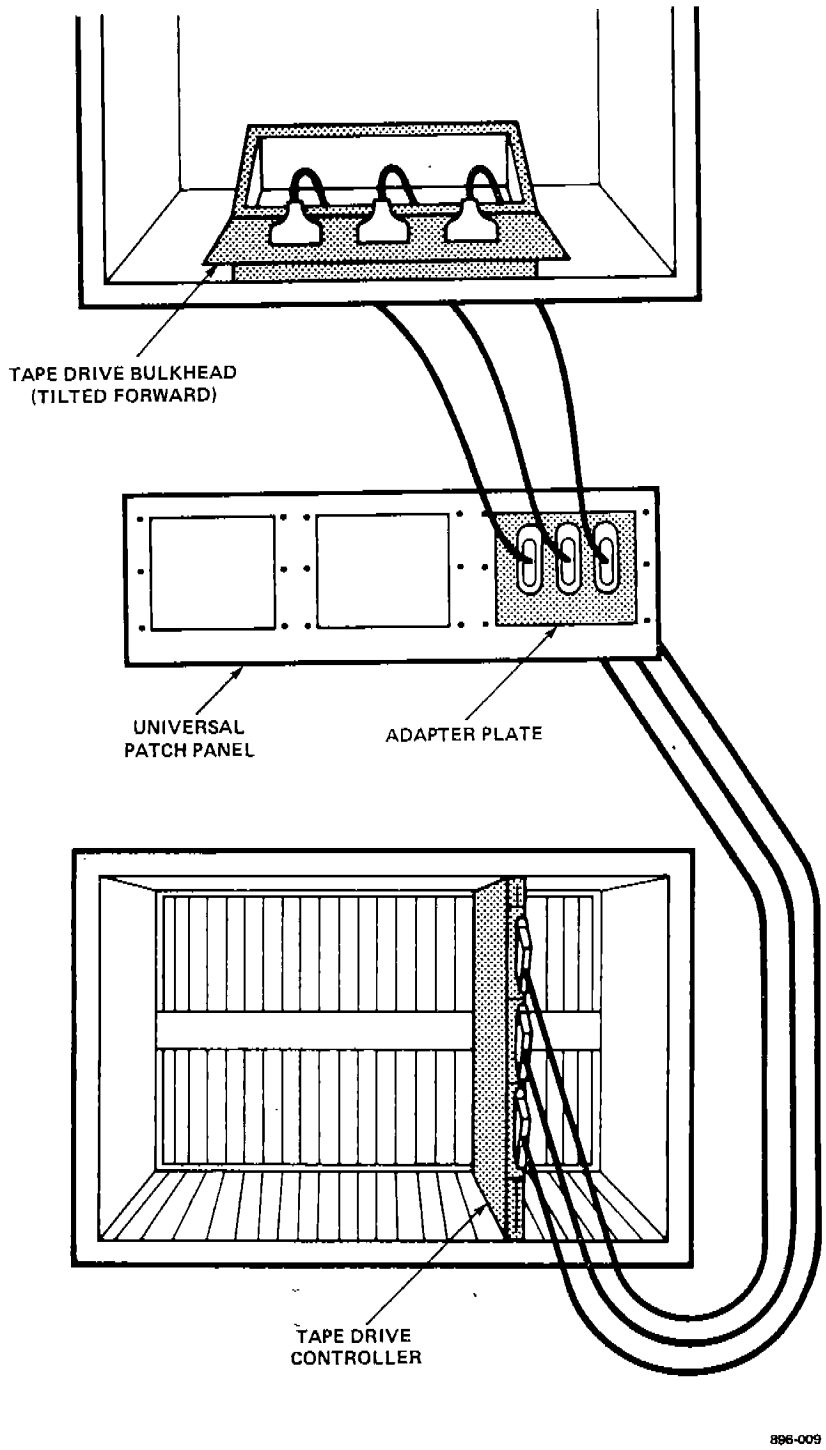

Figure 3-3 5106/5107 Magnetic Tape Drive Cabling

3.3.2 Disc Drives

Cables from the disc drive controller to the patch panel have braided wires that are attached to the I/O card cage ground at the controller end and to patch panel hardware at the patch panel end. A clamp is installed at the cable entry in the disc drive to ground cabling to the disc drive cabinet. Refer to Figures 3-4 through 3-7 for cable routing and connections for all disc drive models that comply with FCC regulations. Table 3.4 lists the disc drive cable part numbers.

Table 3.4 Disc Drive Cable Part Numbers List

DESCRIPTION	PART NO.
Control Cable - Controller to Patch Panel:	
TAB DRAWING	42588
8 ft	42589
16 ft	42590
20 ft	42591
Control Cable - Patch Panel to First Drive:	
TAB DRAWING	42592
25 ft	42597
35 ft	42598
50 ft	42596
Control Cable - Daisy Chain:	
TAB DRAWING	42599
6 ft	42601
10 ft	42602
25 ft	42604
Control Cable - Internal Jumper (2 ft)	55291

Table 3.4 Disc Drive Cable Part Numbers (Cont'd)

DESCRIPTION	PART NO.
Data Cable - Controller to Patch Panel:	
TAB DRAWING	42611
8 ft	42612
16 ft	42613
20 ft	42614
Data Cable - Patch Panel to Drive:	
TAB DRAWING	42606
25 ft	42607
35 ft	42608
50 ft	42609
70 ft	42610

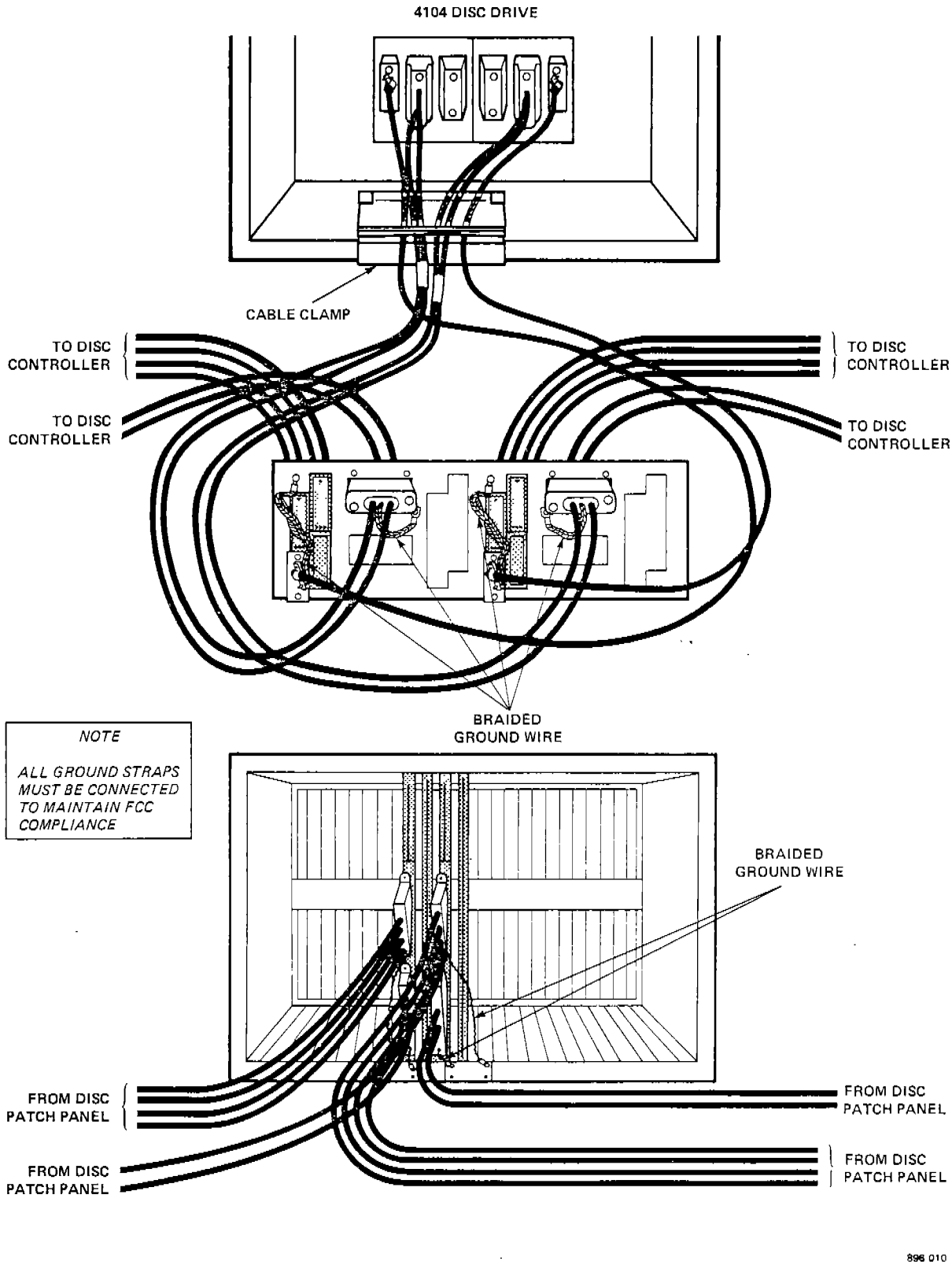

Figure 3-4 4104 Disc Drive Cabling

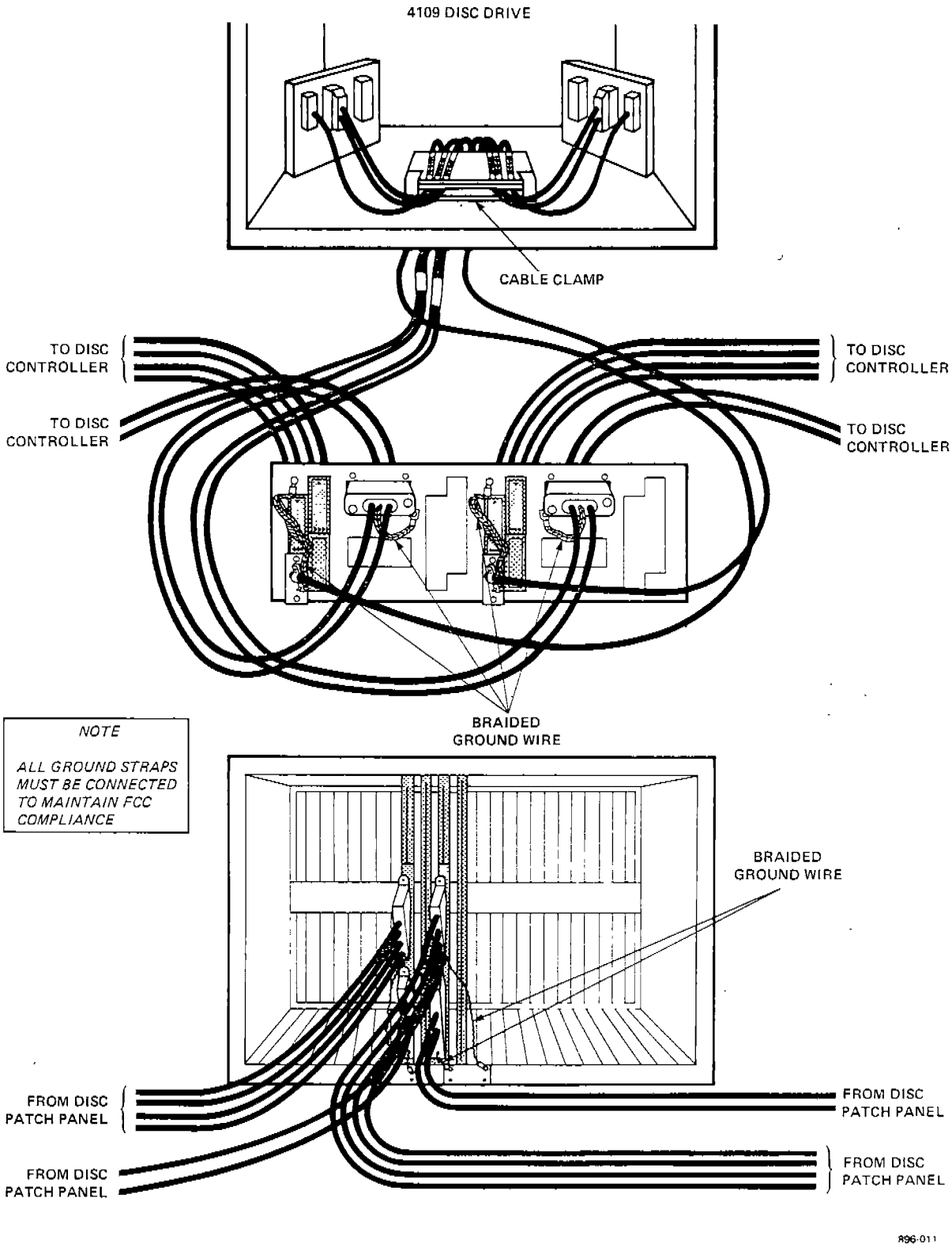

Figure 3-5 4109 Disc Drive Cabling

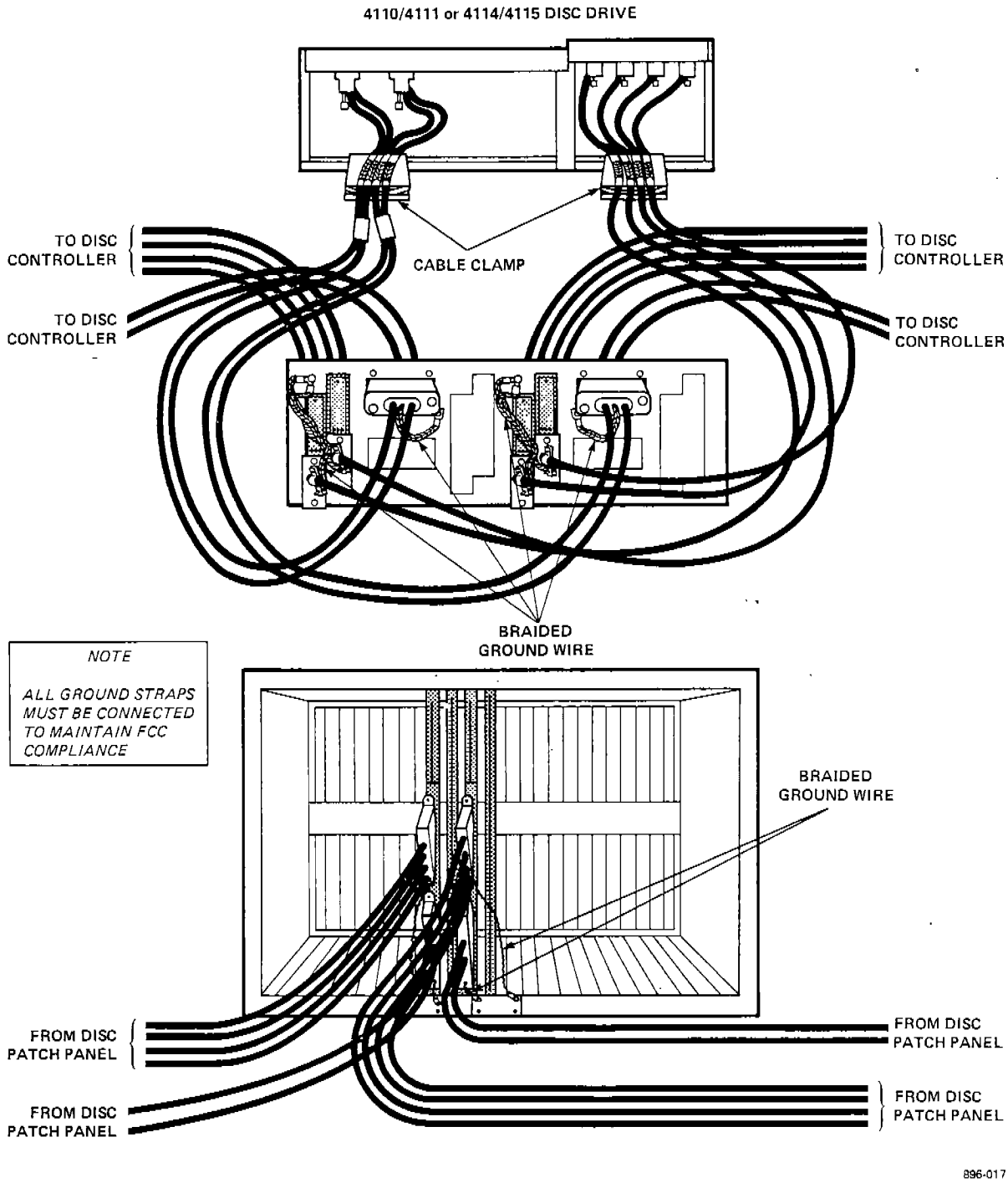

Figure 3-6 4110/4111 and 4114/4115 Disc Drive Cabling

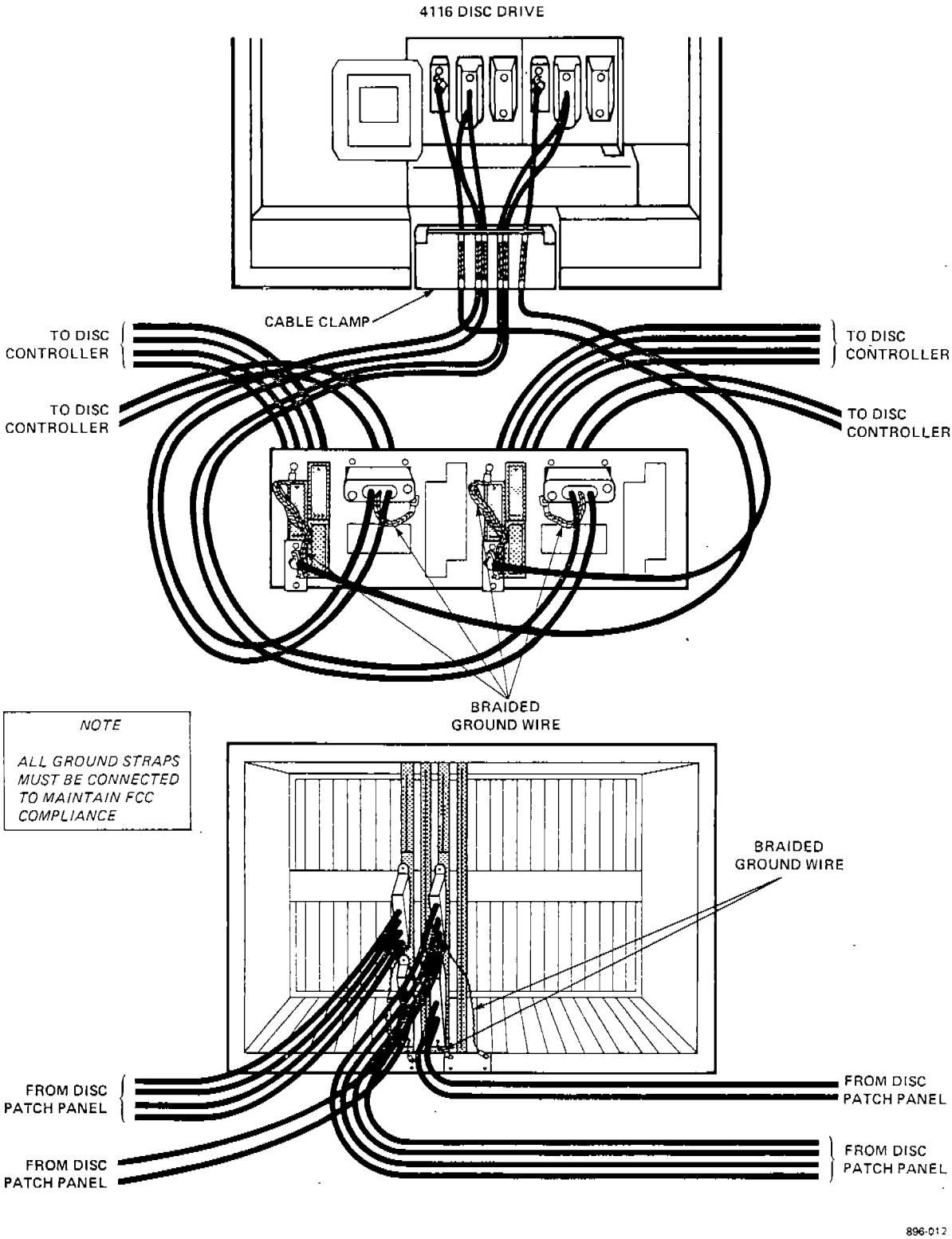

Figure 3-7 4116 Disc Drive Cabling

3.3.3 5513/5514 Band Line Printers

The line printers are connected to the controller via a univeral patch panel (Part Number 45535) fitted with one of two adapter plates:

a. Part Number 42514 - supports one OSP/PMI cable connection and two line printer cable connections.

b. Part Number 42512 - supports three line printer cable connections or three Tridensity Tape Drive cable connections.

Refer to Figure 3-8 for I/O cable connection to the 5513/5514 printers. Table 3.5 lists the part numbers for internal and external cables.

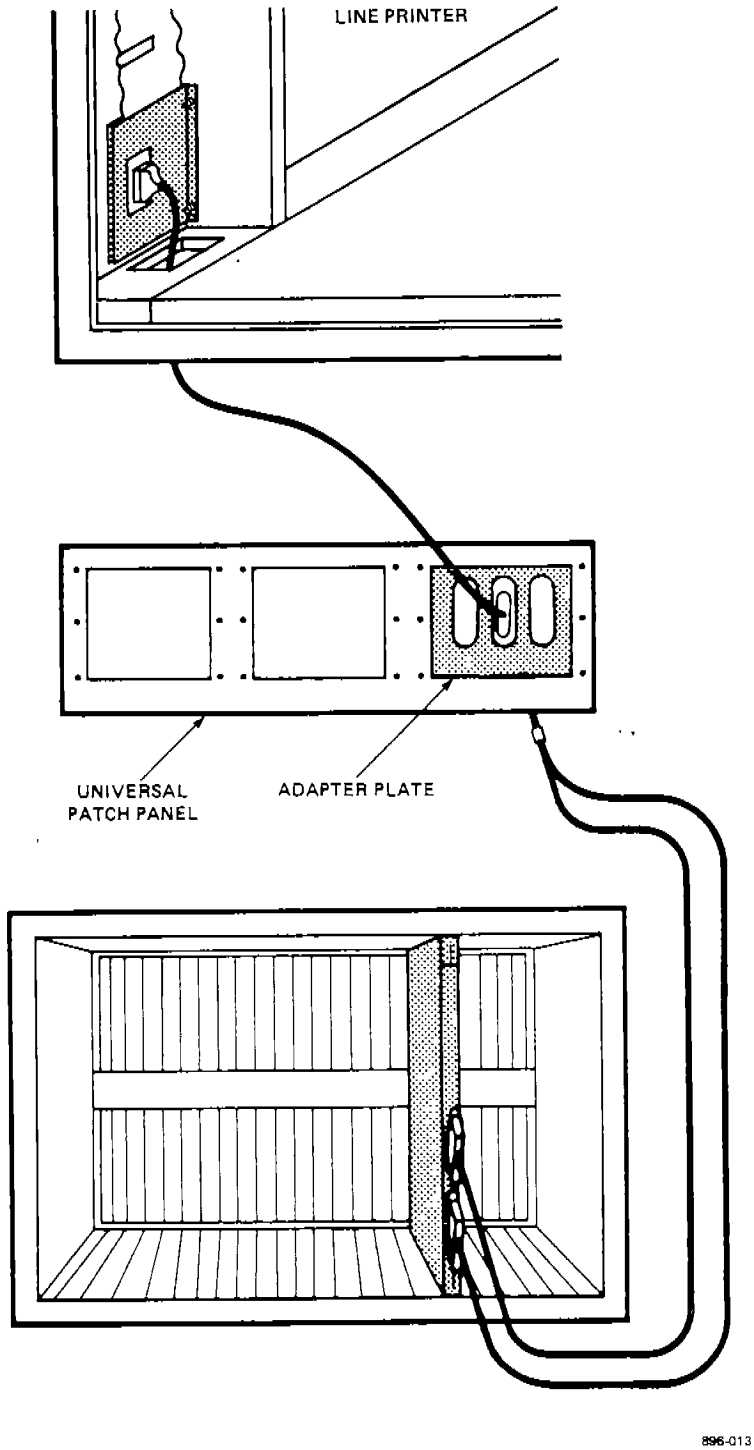

Figure 3-8 5513/5514 Band Line Printer Cabling

Table 3.5 5513/5514 Line Printer Cable Part Numbers

DESCRIPTION	PART NO.
Controller to Patch Panel Cables:	
TAB DRAWING	59598
8 ft	42245
16 ft	42246
20 ft	42247
Patch Panel to Printer Cables:	
TAB DRAWING	58519
15 ft	58939
25 ft	58938
35 ft	58581
50 ft	42558
75 ft	42559
100 ft	42560
150 ft	42561
200 ft	42562
250 ft	42563
300 ft	42564
400 ft	42565
500 ft	42566

3.3.4 Terminals

The customer is responsible for supplying cabling from the terminal patch panel to the terminals. In order to comply with FCC regulations regarding EMI, only shielded cables should be used.

SECTION 4
INSTALLATION

4.0 INSTALLATION

Installing a Tandem system in cabinets designed to meet FCC requirements for EMI differs in only a few particulars from previous installation procedures. Special attention must be paid to insuring the integrity of the EMI gaskets, proper cabinet alignment, and grounding cables, as explained in Section 3.

NOTE

Peripherals that do not comply with FCC regulations cannot be connected to a system that does comply. To determine whether a device meets FCC specifications, look for the FCC compliance label, which must be affixed to the device.

4.1 GASKET INSPECTION

Since EMI radiation is contained within the system cabinet array by the gaskets that fit flush against the conductive surface of the cabinet frame, the gaskets on the doors, cabinet dividers, and side panels should be inspected to ensure that they are not bent or otherwise damaged during shipping. If any are damaged, order replacement parts of the correct size. Refer to Section 8 for a list of EMI gasket part numbers.

4.2 SYSTEM CABINET ALIGNMENT

To establish good electrical bond, the EMI gaskets on the cabinet dividers must be compressed against the conductive surface of the cabinet frame, and the system cabinets must be squarely aligned when the cabinets are bolted together. Refer to Figure 4-1.

The system cabinet array should be visually inspected after cabinets are bolted together to see that they are arranged in a straight line.

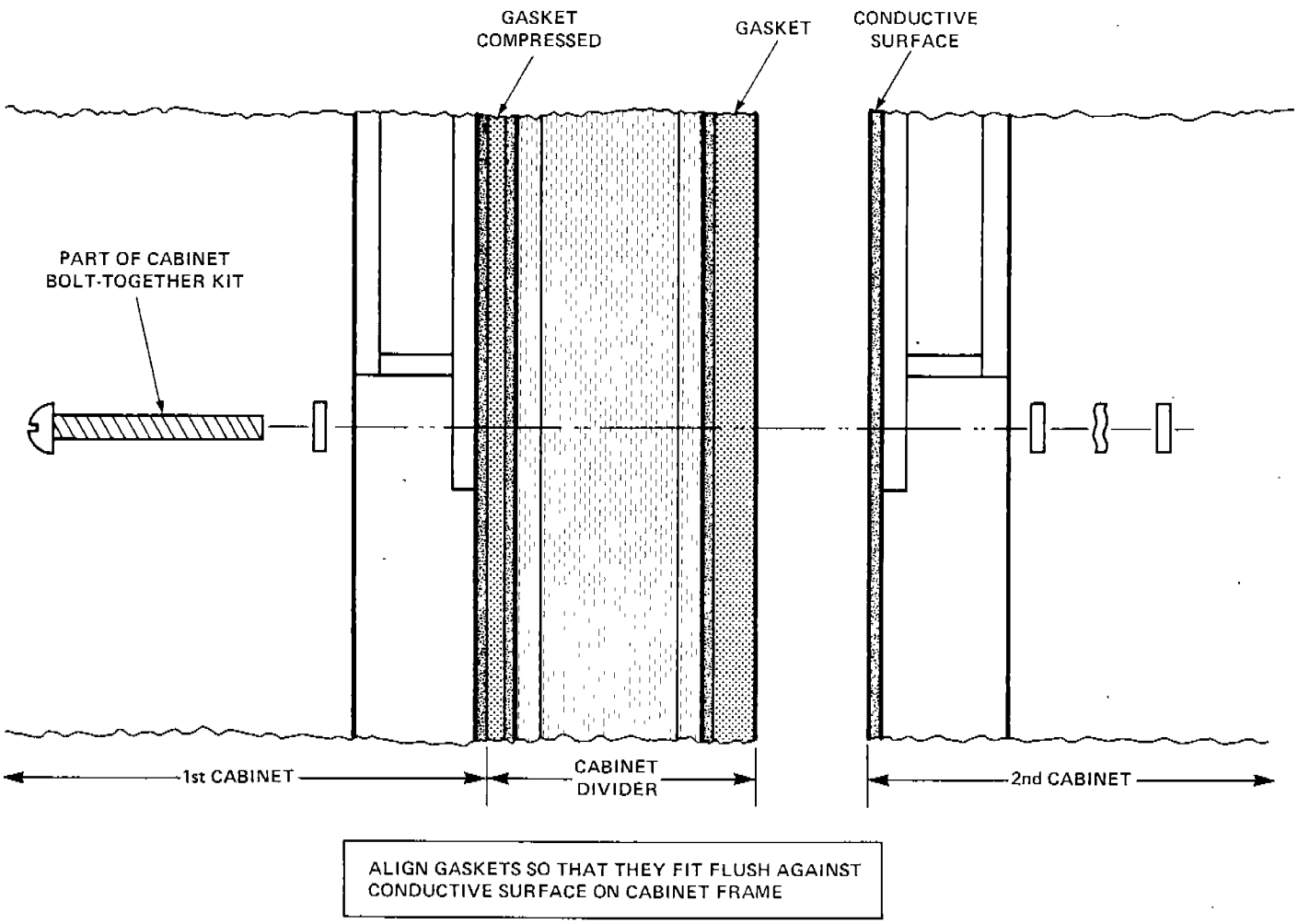

Figure 4-1 Cabinet Divider EMI Gasket Alignment

4.3 DOOR ADJUSTMENT

To maintain a good electrical bond between the door gaskets and the conductive surface of the cabinet frame, there should be a gap of approximately 7/32 inch (± 1/32 inch) between the door and the cabinet frame. A 7/32-inch screw can serve as a measuring tool to determine if doors need to be adjusted.

The screws on the latch keeper bracket at the top and bottom of the door frame fit into slotted holes so that the latch keeper bracket can be adjusted fore and aft. Refer to Figure 4-2.

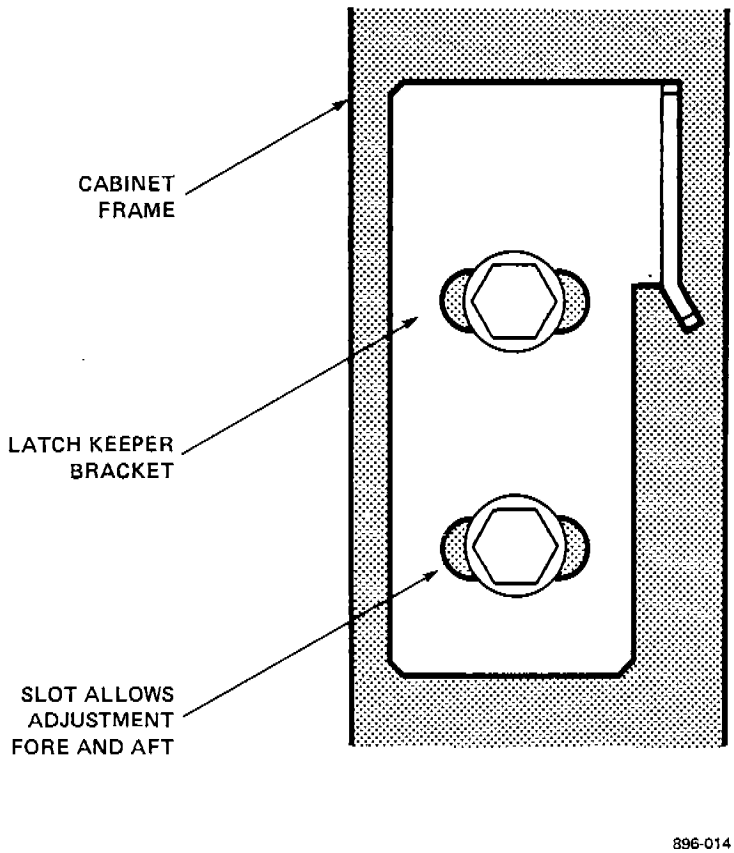

Figure 4-2 Latch Keeper Bracket Adjustment

4.4 LATCH ADJUSTMENT

The lock plate on the latch assembly can be adjusted so that it fits within the cutout of the door. Two studs on the back of the lock plate fit into slotted holes so that the lock plate can be adjusted vertically and horizontally. There should be a 1/16 inch gap on two sides and bottom of the block plate and a 3/32 inch gap at top.

The lock plate can also be adjusted so that it fits flush with the door. The hole where the latch actuator attaches to the vertical stiffener is slotted so that the latch assembly can be adjusted fore and aft. Refer to Figure 4-3.

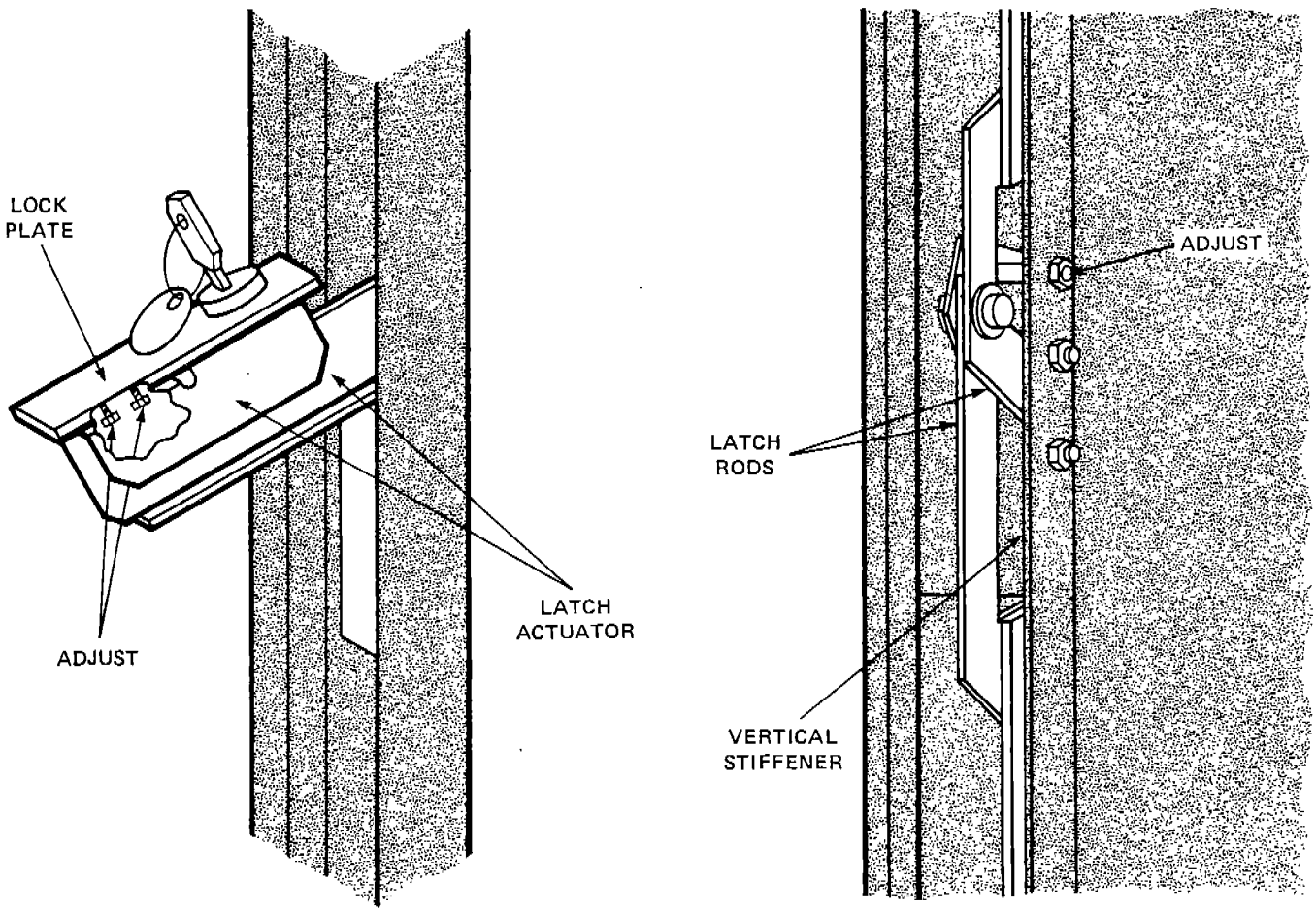

Figure 4-3 Latch Adjustment

4.5 IPB SELECT CABLES INSTALLATION

The IPB Select cables are normally shipped inside the processor cabinets. The cables for all but the last processor cabinet are coiled and attached to tie blocks under the cabinet cover directly above the processor to which they are connected. The Select cables that are routed to the X Bus IPB controller are positioned toward the middle of the cabinet; the cables that are routed to the Y Bus IPB controller are positioned toward the rear of the cabinet. Refer to Figure 4-4.

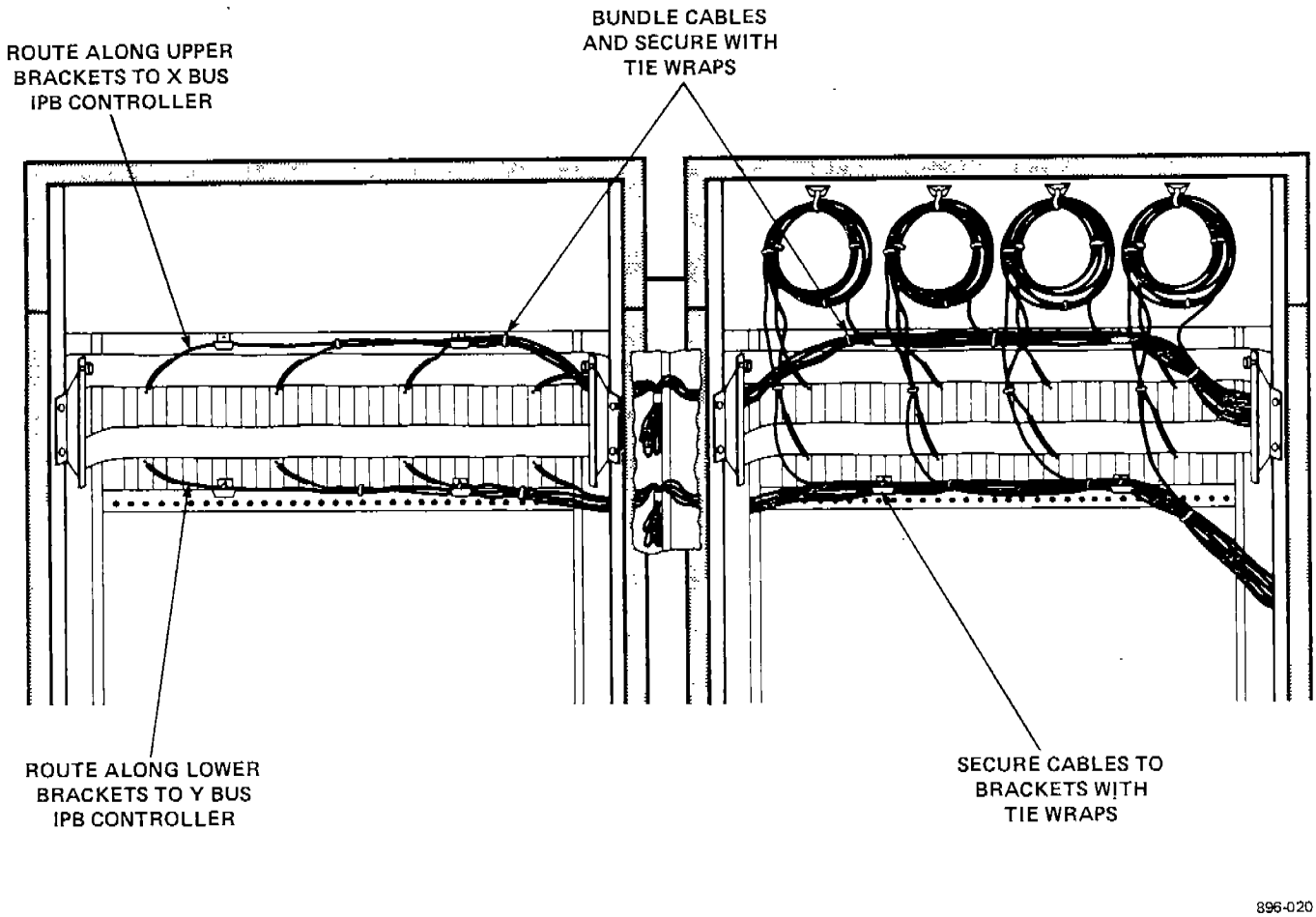

Figure 4-4 IPB Select Cables Installation

To install the IPB Select cables, perform the following (refer to Figure 4-4):

a. Install the IPB Select cable to the X Bus IPB controller, working from the leftmost processor to CPU 0, as follows:

   1. Connect cable to the MCB board at the processor backplane.

   2. Route cable through all cabinet frames along the upper support brackets to the X bus IPB controller.

   3. Connect cable to IPB controller with the brown wire in the lower right position. See Figure 4-5.

   4. Coil excess cable, allowing for a service loop, bundle cables together with tie wraps, and secure cables to the brackets with tie wraps.

      a) In a two or four cabinet system, excess cable from the last cabinet is pulled to the right and secured to the card cage of the previous cabinet with a cable clamp. The cable fits within the cabinet divider. See Figure 4-4.

      b) Excess cable for other cabinets is coiled and secured to the cable clamp in the cabinet cover.

b. Install the IPB Select cable to the Y Bus IPB controller, working from the leftmost processor to CPU 0, as follows:

   1. Connect cable to the MCB board at the processor backplane.

   2. Route cable through all cabinet frames along the lower support brackets to the Y Bus IPB controller.

   3. Connect cable to IPB controller with the brown wire in the lower right position. See Figure 4-5

   4. Coil excess cable, allowing for a service loop, bundle cables together with tie wraps, and secure cables to the brackets with tie wraps.

      a) In a two or four cabinet system, excess cable from the last cabinet is pulled to the right and secured to the card cage of the previous cabinet with a cable clamp. The cable should fit within the cabinet divider. See Figure 4-4.

      b) Excess cable for other cabinets is coiled and secured to the cable clamp in the cabinet cover.

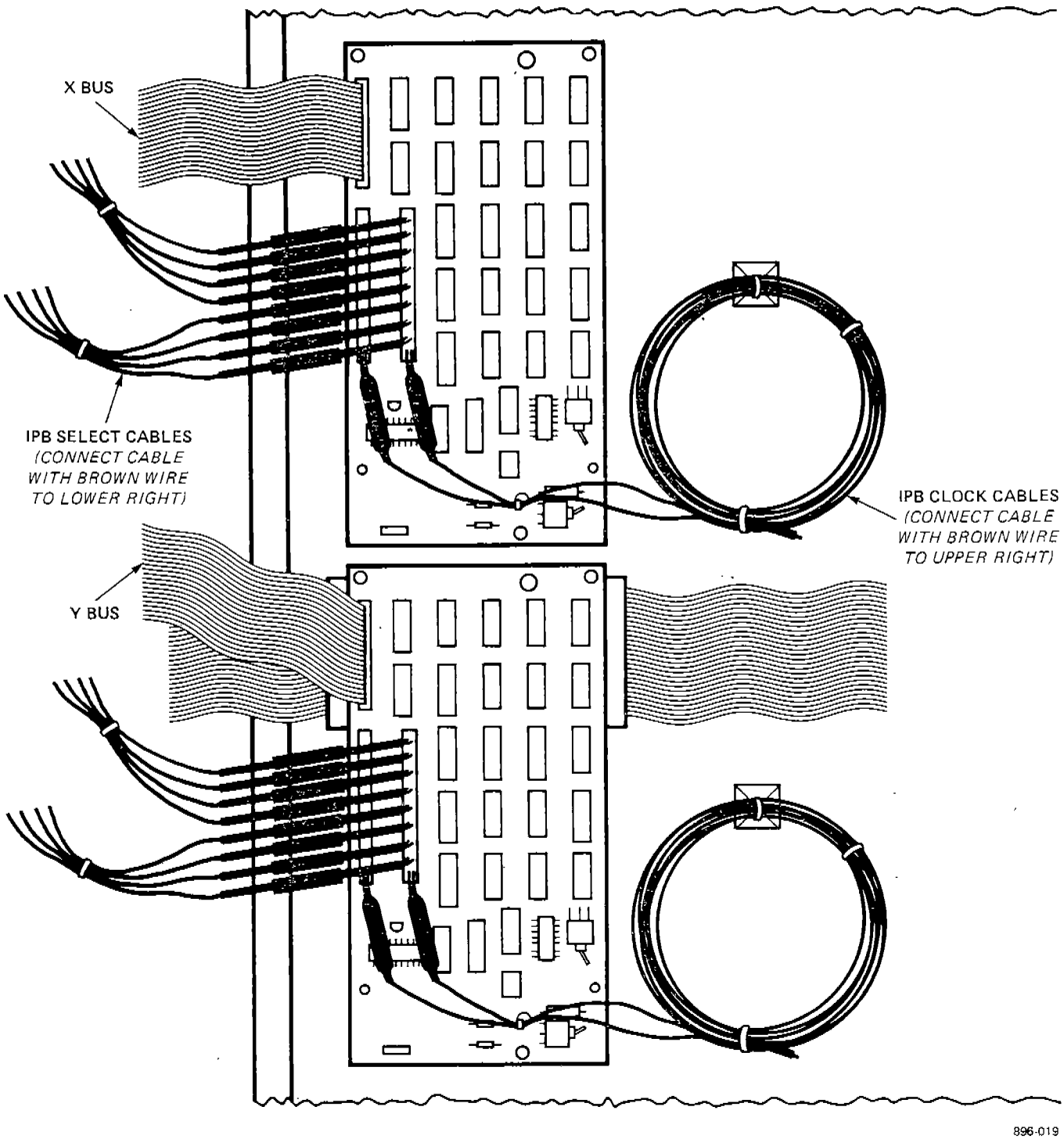

Figure 4-5 IPB Clock and Select Cable Connections

4.6 DISC DRIVE CABLE INSTALLATION

Disc drive cables are routed through a clamp at the cable entry to the disc drive cabinet. To install cables, perform the following (refer to Figure 4-6):

a. Remove screw from clamp cover.

b. Route cables to the appropriate disc drive connectors. Ensure that exposed braid portion of the cable is located on the raised section of the cable clamp.

c. Replace clamp cover and fasten with screw.

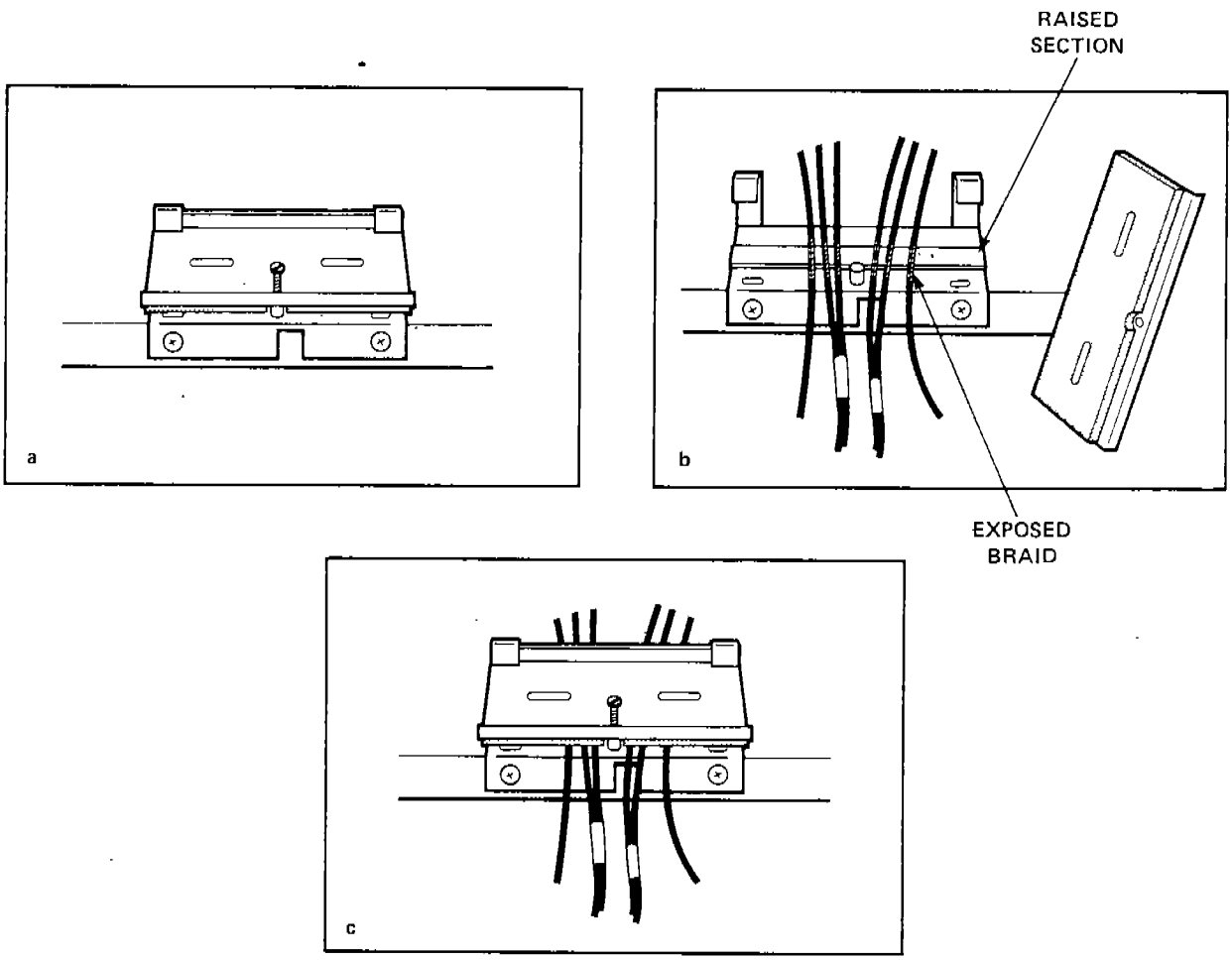

Figure 4-6 Disc Drive Cable Installation

SECTION 5
CORRECTIVE MAINTENANCE

5.0 CORRECTIVE MAINTENANCE

Corrective maintenance consists of replacing Field Replaceable Units (FRUs). A complete list of FRUs is given in Section 8.

5.1 REMOVAL AND REPLACEMENT

Removal and replacement procedures for FRUs are given in the following paragraphs.

5.1.1 EMI Gaskets

EMI gaskets come in nine lengths from 7 inches to 67.12 inches. Before replacing gaskets, make sure that the replacement gaskets are the correct length. Part numbers and available lengths are listed in Table 8.1.

EMI gaskets are attached to flanges on the front and rear doors of the cabinets. No special tools are required, but a screwdriver and a hammer are helpful.

To remove the gasket, use a small screwdriver to pry one end of the gasket from the flange, then pull it from the flange by hand toward the other end.

To replace the gasket, attach the gasket to the flange by hand, working from one end toward the other, then tap the gasket with a hammer to ensure that it is fully seated.

5.1.2 Latch Actuator and Cam Key Lock Offset

The Latch Actuator and Cam Key Lock Offset FRUs are components of the keylock assembly. Refer to Figure 5-1.

To remove and replace the FRUs, perform the following:

a. Remove the bolt that connects the Latch Actuator to the Latch Rods on the inside of the cabinet door. The assembly can then be removed from the cutout in the door.

b. Remove the two screws that hold the keylock assembly together.

c. Replace the FRU as shown in item c of Figure 5-1.

d. Reassemble the keylock assembly.

e. Insert in cutout in cabinet door.

f. Attach bolt that connects the Latch Actuator to the Latch Rods. Adjust the keylock assembly within the cutout if necessary, as explained in paragraph 4.4.

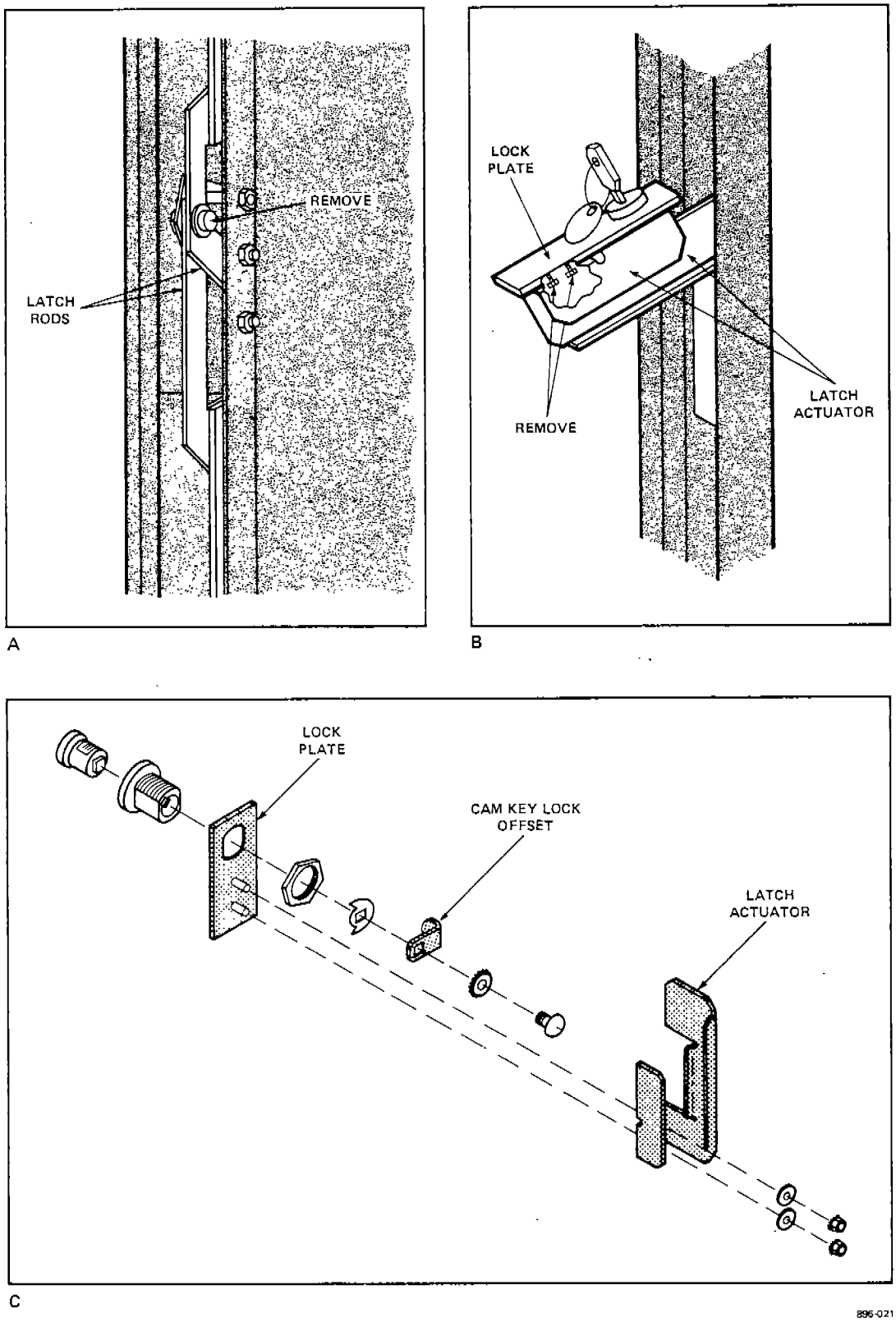

Figure 5-1 Latch Actuator and Cam Key Lock Offset Removal and Replacement

SECTION 6
PREVENTIVE MAINTENANCE

6.0 PREVENTIVE MAINTENANCE

During routine preventive maintenance for the system, the gaskets and the conductive surface on the cabinet frame should be checked for dirt and cleaned if necessary. Only isopropyl alcohol should be used.

SECTION 7
SPECIAL TOOLS AND TEST EQUIPMENT

7.0 SPECIAL TOOLS AND TEST EQUIPMENT

No special tools or test equipment are required for installing or maintaining the cabinets.

SECTION 8
FIELD REPLACEABLE UNITS

8.0 FIELD REPLACEABLE UNITS

Table 8.1 lists field replaceable units.

Table 8.1 Field Replaceable Units

DESCRIPTION	PART NO.
Cabinetry:	
Latch Actuator, Front	42530
Latch Actuator, Rear	42534
Cam Key Lock Offset	42538
EMI Gasket, 62.62 inches	10672
EMI Gasket, 25.00 inches	10673
EMI Gasket, 18.25 inches	10674
EMI Gasket, 9.38 inches	10675
EMI Gasket, 7.00 inches	10676
EMI Gasket, 67.12 inches	10677
EMI Gasket, 11.50 inches	10678
EMI Gasket, 62.00 inches	10679
EMI Gasket, 26.75 inches	10680
EMI Filter	42554

Table 8.1 Field Replaceable Units (Cont'd)

DESCRIPTION	PART NO.
Patch Panels:	
Disc Patch Panel	50548
Terminal & Async Controller Patch Panel	50191
Bit Sync Controller Patch Panel	50445
Feature Patch Panel Module	59648
CPU Power System:	
PWA, Rect Snubber	42554
Cover, Filter Replacements	45987
Power Supply, CPU	53270
Disc Drive Cabling:	
Control Cable - Controller to Patch Panel:	
8 ft	42589
16 ft	42590
20 ft	42591
Control Cable - Patch Panel to First Drive:	
25 ft	42597
35 ft	42598
50 ft	42596
Control Cable - Daisy Chain:	
6 ft	42601
10 ft	42602
25 ft	42604

Table 8.1 Field Replaceable Units (Cont'd)

DESCRIPTION	PART NO.
Control Cable - Internal Jumper (2 ft)	55291
Data Cable - Controller to Patch Panel:	
8 ft	42612
16 ft	42613
20 ft	42614
Data Cable - Patch Panel to Drive:	
25 ft	42607
35 ft	42608
50 ft	42609
70 ft	42610
IPB Clock and Select Cabling:	
IPB Clock Cable:	
6.5 ft (1 or 2 cabinet system)	42444
14 ft (3 to 5 cabinet system)	42445
IPB Select Cable:	
6.5 ft (1 or 2 cabinet system)	42441
14 ft (3 to 5 cabinet system)	42442
Tridensity Tape Drive Cabling:	
Controller to Patch Panel Cable (8 ft)	49053
Controller to Patch Panel Cable (20 ft)	42557
Patch Panel to Bulkhead Cable (15 ft)	58939
Patch Panel to Bulkhead Cable (25 ft)	58938
Patch Panel to Bulkhead Cable (35 ft)	58581

Table 8.1 Field Replaceable Units (Cont'd)

DESCRIPTION	PART NO.
5513, 5514 Printer Cabling:	
Controller to Patch Panel Cables:	
8 ft	42245
16 ft	42246
20 ft	42247
Patch Panel to Printer Cables:	
15 ft	58939
25 ft	58938
35 ft	58581
50 ft	42558
75 ft	42559
100 ft	42560
150 ft	42561
200 ft	42562
250 ft	42563
300 ft	42564
400 ft	42565
500 ft	42566
SMP to PMI Cabling:	
Patch Panel to PMI Cable (20 ft)	42583
OSP to Patch Panel Cable (25 ft)	42582
OSP/PMI Patch Panel Adapter Plate	42514

Table 8.1 Field Replaceable Units (Cont'd)

DESCRIPTION	PART NO.
200 ft	42055
250 ft	42056
300 ft	42057
400 ft	42058
500 ft	42059
SMP to PMI Cabling:	
Patch Panel to PMI Cable (20 ft)	42583
OSP to Patch Panel Cable (25 ft)	42582
OSP/PMI Patch Panel Adapter Plate	42514

APPENDIX A
OLD AND NEW PART NUMBERS CONVERSION TABLE

A.0 OLD AND NEW PART NUMBERS CONVERSION TABLE

Table A.1 lists old and new part numbers for FCC-compliant parts. Only the new part numbers can be used with systems installed after October 1, 1983.

Table A.1 Old and New Part Numbers Conversion Table

DESCRIPTION	OLD PART NO.	NEW PART NO.
Front Door (CPU Cabinet)	50397	42510
Front Door (Tape Cabinet)	50692	42511
Removable Front Door	45880	42511
Rear Door (CPU Cabinet)	50400	42506
Rear Door with Single Louver	45881	42570
Frame (CPU Cabinet)	50395	59685
Frame (Tape Cabinet)	50393	42507
Top Cover	50401	42508
Side Cover	45288	42505
Divider	50611	42509
Hinge, Plexiglass Door	45576	42539
Latch Bracket, Door Lock	50430	OBS
Card Guide, I/O	50876	RR
Insulator, Card Cage	50956	OBS

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
Latch Actuator, Front	-----	42530
Latch Actuator, Rear	-----	42534
Latch Rod, Front Upper	-----	42531
Latch Rod, Front Lower	-----	42532
Latch Rod, Rear Upper	-----	42535
Latch Rod, Rear Lower	-----	42536
Bracket Latch Keeper, Front	-----	42533
Bracket Latch Keeper, Rear	-----	42537
Cam Key Lock Offset	-----	42538
Shoulder Screw	-----	10667
Curved Washer	-----	10665
Lock Washer #6	-----	10666
Lock Plate	-----	42581
FCC Compliance Label, Computer Systems	-----	46044
FCC Compliance Label, Peripherals	-----	46047
4-inch Ground Jumper	-----	42619
TAB DRAWING	-----	42620
GASKET MATERIAL TAB DRAWING	-----	29336
EMI Gasket, 62.62 inches	-----	10672
EMI Gasket, 25.00 inches	-----	10673
EMI Gasket, 18.25 inches	-----	10674

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
EMI Gasket, 9.38 inches	-----	10675
EMI Gasket, 7.00 inches	-----	10676
EMI Gasket, 67.12 inches	-----	10677
EMI Gasket, 11.50 inches	-----	10678
EMI Gasket, 62.00 inches	-----	10679
EMI Gasket, 26.75 inches	-----	10680
MOD Cabinet 80 MB MMD	45173	RR
ASM Cabinet 80 MB MMD	45056	RR
Disc Patch Panel	50548	RR
Terminal & Async Controller Patch Panel	50191	RR
Bit Sync Controller Patch Panel	50445	RR
Mounting Bracket, I/O I/C Panel	45535	RR
Mounting Bracket, I/O Panel, R.H.	50437	RR
Mounting Bracket, I/O Panel, L.H.	50438	RR
PMI Panel Assembly	45029	42517
PMI Patch Panel	45025	42516
PMI PWA	55330	42470
PMI PWB	55332	42472
PWA Control	57550	49080
PWA Data ASM	57560	49070
Housing, Bulkhead	45442	42580
Cover, Bulkhead Data	45480	42575

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
Cover, Bulkhead Control	-----	42577
Plate, Control Board	45481	42578
Cover Plate	45483	42576
Hinge, Bulkhead Cover (Data)	45485	42572
Hinge, Bulkhead Cover (Control)	45486	42571
Bulkhead End Cover	45490	OBS
Clamp, Cable Bulkhead	-----	42573
Retainer, Cable	-----	42574
Gasket, Cable Retainer Bulkhead	-----	42579
Cover, Bulkhead (Control)	-----	42577
ASM: Bulkhead/PDM T/D	58190	42616
B/M ASM: Bulkhead PDM (60 Hz)	57648	42617
B/M ASM: Bulkhead PDM (50 Hz)	57649	42618
Cabinet Assembly Single Drive T/D:		
Basic Machine	45559	RR
ASM: Zipper Tubing	-----	42615
SSA Cover Bulkhead (Data)	45519	45993
SSF Cover Bulkhead (Data)	45519	45994
SSA Cover Bulkhead (Control)	45520	45995
SSF Cover Bulkhead (Control)	45520	45996
Cover PDU	50501	42519

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
EMI Filter	51700	42554
AC Power Module, Magnetic Tape (60 Hz)	52307	42556
AC Power Module, CPU (60 Hz)	52308	42555
Chassis, AC	50498	42553
PWA, Rect Snubber	-----	42490
PWB, Rect Snubber	-----	42492
Power Supply, CPU	53270	RR
Cable Harness, CPU Power Module	52304	45985
Cable Harness, Magnetic Tape Power Module	52305	45992
Angle, Mounting	-----	45986
Cover, Filter Replacements	-----	45987
Cables, Data, Controller to Patch Panel (Octopus):		
TAB DRAWING	52421	42611
8 ft	55237	42612
16 ft	55238	42613
20 ft	55239	42614
Cables, Patch Panel to Drive:		
TAB DRAWING	52988	42592
50 ft	55294	42596
25 ft	55297	42597
35 ft	55298	42598

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
TAB DRAWING		49068
Cable, Control, Internal Jumper (2 ft)	55291	RR
Cables, Control, Drive to Drive T/D		
TAB DRAWING	-----	42599
6 ft	55292	42601
10 ft	55293	42602
25 ft	-----	42604
Cables, Controller to Patch Panel:		
TAB DRAWING	52987	42588
8 ft	55246	42589
16 ft	55247	42590
20 ft	55248	42591
Cables, Data Bus, Patch Panel to Drive:		
TAB DRAWING	56233	42606
25 ft	56234	42607
35 ft	56235	42608
50 ft	56236	42609
70 ft	56238	42610

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
IPB Clock Cable:		
TAB DRAWING	53880	42443
6.5 ft.	53881	42444
	53882	42444
14 ft	53884	42445
	53885	42445
	53886	42445
	53887	42445
	53888	42445
	53889	42445
IPB Select Cable:		
TAB DRAWING	53870	42440
6.5 ft.	53871	42441
	53872	42441
14 ft	53873	42442
	53874	42442
	53875	42442
	53876	42442
	53877	42442
	53878	42442
	53829	42442

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
Ground Plate	45955	OBS
Spring Clips	45956	OBS
Tape Controller to Patch Panel Cable:		
8 ft	-----	49053
20 ft	-----	42557
Cables, Patch Panel to Bulkhead:		
TAB DRAWING	58519	RR
15 ft (Tape Drive to UI)	58939	RR
25 ft (Tape Drive to UI)	58938	RR
35 ft (Tape Drive to UI)	58581	RR
Adapter Plate	-----	42512
Controller to Patch Panel Cables		
TAB DRAWING	-----	59598
8 ft	-----	42245
16 ft	-----	42246
20 ft	-----	42247

Table A.1 Old and New Part Numbers Conversion Table (Cont'd)

DESCRIPTION	OLD PART NO.	NEW PART NO.
Controller to Line Printer Cables		
TAB DRAWING	54630	
25 ft	55210	58938
50 ft	55211	42558
75 ft	55212	42559
100 ft	55213	42560
150 ft	55214	42561
200 ft	55215	42562
250 ft	55216	42563
300 ft	55217	42564
400 ft	55218	42565
500 ft	55219	42566
OSP to PMI Cables:		
Patch Panel to PMI (internal) 20 ft	-----	42583
OSP to Patch Panel (external) 25 ft	-----	42582
OSP/PMI Patch Panel Adapter Plate	-----	42514

CABINET SUBSYSTEMS
OLD AND NEW PART NUMBERS CONVERSION TABLE

READER'S COMMENTS

Cabinet Subsystems
PN 82896-A01

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