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TI 6490.36

INSTRUCTION BOOK
(SYSTEM)

MODEL 1 FULL CAPACITY FLIGHT SERVICE AUTOMATION SYSTEM

WITH

TYPE FA-10017 FLIGHT SERVICE DATA PROCESSING SYSTEM (FSDPS)
TYPE FA-10018 AUTOMATED FLIGHT SERVICE STATION (AFSS)
TYPE FA-10020 AVIATION WEATHER PROCESSOR (AWP)

CONTRACT DTFA01-81-C 10039

CONTRACTOR

E-SYSTEMS, INC.
GARLAND DIVISION
P.O. BOX 660023
DALLAS, TEXAS 75266-0023

CONTROLLED DOCUMENT

416-32142

MADE FOR

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION

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Notice to System Operator

There are two erroneous error messages that may be reported at random intervals by the Tandem system. These error messages are as follows:

1) USART error, and
2) console message 61 from 6203's at power on.

Tandem Computers have acknowledged that under certain circumstances, the Operations and Service Processor's (OSP) Offline Self-Test Software will display at random intervals the USART error detection lines when attempting to identify the type of printer attached to the O.S.P. The failure of this section of the Offline Self-Test is not indicative of a USART failure and does not effect the outcome of the other Offline Printer Diagnostics.

Tandem will at some future date either remove the Offline Printer Recognition Test or make appropriate changes to facilitate the correct functioning of the test.

The console message 61 from the 6203s at power on is due to the power on cycle of the 6203s. It is possible for the power on cycle to momentarily raise the RCI, Reconnect In, line to the channel which is the cause of the console message. By the time the channel in the processor tries to find out who had issued the reconnect request the 6203 has completed its power on cycle and the RCI line is no longer true.

This message at power on time from the 6203s would in no way affect normal operations. The power on interrupt is detected by the channel at power on time, which is normal, and the RCI request that the channel may see at this time could in no way affect any application or driver processes. The message has no imbedded address as to the source of the interrupt since no controller responded to the poll following the reconnect request. This means that the event is simply logged and no process, except the message handling system within Guardian, ever knows it happened. In other words, it is transparent to all application processes and no action is taken except to record the event to the systems log.

Tandem does not perceive this to be a problem since it does not in any way compromise the functionality of the 6203 itself nor the system. Therefore, no further action is planned.

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SAFETY NOTICE

The attention of operating and maintenance personnel is directed to FAA Instruction 6000.15 "Maintenance of Airway Facilities" for instructions on the subject of safety precautions to be observed, and to FAA Order 3900.0 "Accident Prevention Handbook for Airway Facility Personnel." Personnel must observe the safety regulations at all times. Maintenance personnel shall become familiar with the technique for resuscitation.

LIVE CIRCUITS

The Flight Service Automation System is designed to allow maintenance personnel to remove and replace failed units with power applied. However, strict adherence to the removal and replacement procedures given for each line replaceable unit is required.

RESUSCITATION

Maintenance personnel should familiarize themselves with the technique for resuscitation found in the manual of first aid instructions.

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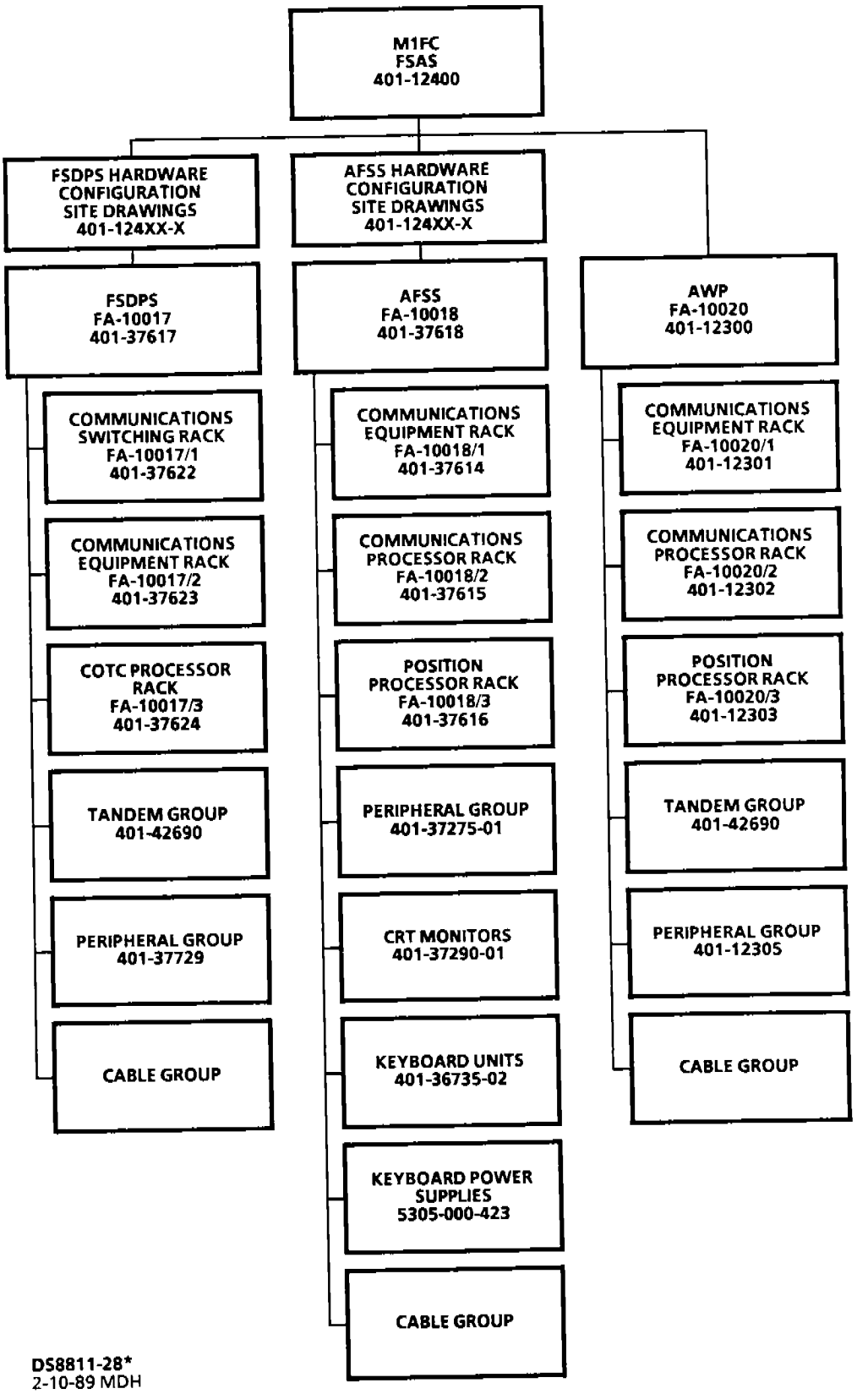

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M1FC FSAS FUNCTIONAL FAMILY TREE CHART

SECTION 1

INTRODUCTION

The following description is an overall view of the Model 1 Full Capacity (M1FC) Flight Service Automation System (FSAS).

NOTE

> The FAA type numbers that appear on equipment nameplates are not item identifying in all cases. One FAA type number may represent more than one configuration of an equipment or subsystem. Therefore, the FAA type numbers should not be used to identify a specific configuration. For complete identification of specific configurations, use the part number that appears on the E-Systems nameplate and refer to the parts list in this manual.

1.1 PURPOSE.- This instruction book is for use by all levels of Federal Aviation Administration personnel who are required to operate and maintain the M1FC FSAS System.

1.2 SCOPE.- The M1FC FSAS System Instruction Book contains an introduction to the system; a description providing general and detailed theory of operation for the system; operating procedures for the system; periodic and system maintenance procedures; a system parts list; and installation, integration, and checkout procedures for the system. For detailed theory of operation, parts lists, and schematics for individual equipment refer to the Model 1 Full Capacity Flight Service Automation System Equipment Instruction Book, TI 6490.37, or see table 1-1 for the list of related equipment manuals.

1.3 DESCRIPTION.- The M1FC FSAS consists of 26 Flight Service Data Processing Subsystems (FSDPSs), one to eight Automated Flight Service Stations (AFSSs) per FSDPS, and two Aviation Weather Processors (AWPs). The M1FC FSAS is composed of data processing equipment and alphanumeric display terminal equipment. The M1FC FSAS is primarily concerned with information movement which facilitates aircraft movement and flight safety. Information related to flight safety and flight movement that flows between the Federal Aviation Administration (FAA), the National Weather Service (NWS), and military and international facilities is collected and stored by the FSDPS system. On request, the information can be displayed at an AFSS where the request originated. Information movement between FSDPS, AFSS, and AWP facilities and their internal and external interfaces is shown in figure 1-1.

Table 1-1. Related Equipment Instruction Books

LSI-11/23 Processor, MRV11-C Memory, MSV11-LF User Guide and Maintenance Print Sets for KDF11-AA, MRV11-C, MSV11-LF	TI 6490.4
KPV11-B Power-Fail/ Line-Time Clock/Terminator	TI 6490.5
LA34 Terminal Instruction Book	TI 6490.6
RL01/RL02 User Guide, RL01/RL02 Disk Drive and Illustrated Parts Breakdown	TI 6490.7 Rev. A
DMA-QB, DMA Controller and HEX-IPB	TI 6490.8
8S Eight Channel Serial Interface	TI 6490.9
Model 9000 Tape Drive	TI 6490.11
DM9300TD Disk Drive	TI 6490.12
P300 Line Printer	TI 6490.13
Analog and Digital Patch Panels	TI 6490.14
TTL-150 Display Monitor	TI 6490.15
Keyboard Unit, P/N 401-36735	TI 6490.16
Model 60-DC Coded Time Source	TI 6490.17
MM43 Regulated Power Supply	TI 6490.18
TANDEM Library	TI 6490.19
M200 Matrix Printer	TI 6490.20
Model 1 Full Capacity FSAS Equipment Instruction Book	TI 6490.37
RM-8E Multiple Modem System	TI 6490.38
LA100 Terminal Instruction Book	TI 6490.39
Modem Sharing Device	TI 6490.40
Maintenance and Diagnostic Test Set Instruction Book	TI 6490.41

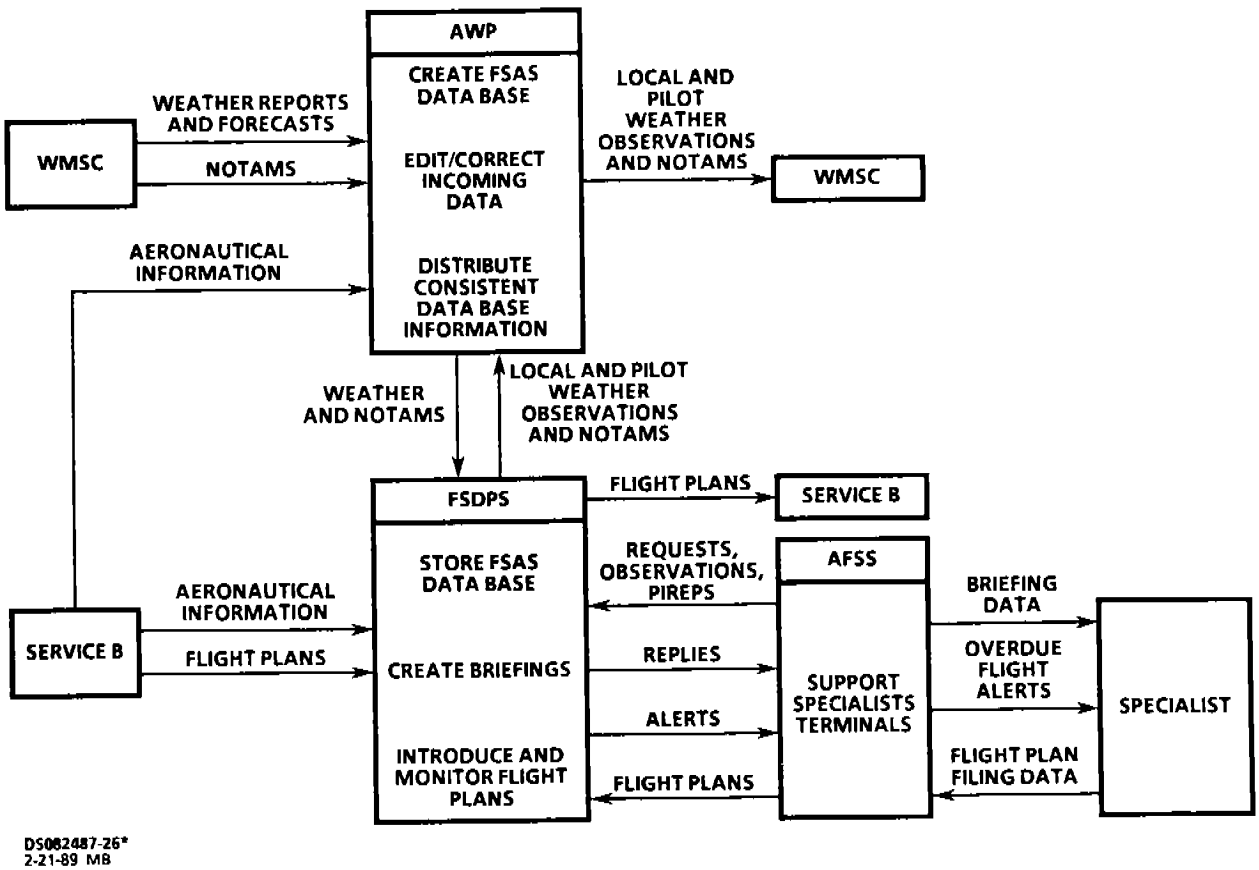

Figure 1-1. M1FC FSAS Data Flow

1.3.1 FSDPS Description.- The data processing equipment is located at designated Air Route Traffic Control Centers (ARTCCs) and is referred to as the Flight Service Data Processing System (FSDPS) equipment. A typical FSDPS equipment configuration is shown in figure 1-2. Each FSDPS consists of four computer subsystems, each with its own pair of disk drive/controllers. Each FSDPS computer subsystem has access to communications line controllers, a coded time source (CTS), system maintenance monitor console (SMMC), magnetic tape drives, line printers, and the backup path to the disks of another computer subsystem in the FSDPS.

The FSDPS provides the dissemination of information related to flight safety to the AFSSs. The FSDPS maintains external interfaces to the Service B circuit and internal interfaces to the Automated Flight Service Station (AFSS) where the alphanumeric display terminal equipment is located, as well as the AWPs.

Flight plans are also processed by the FSDPS. The system automatically formats and transmits outgoing flight plans, receives incoming flight plans and acknowledges receipt. This information is automatically stored and made available for retrieval by the specialists.

The FSDPS aids the AFSS facilities with their daily administrative requirements by automatically collecting and summarizing station and position activities for reports. Events are recorded to provide automatic historical reconstruction for safety-related incidences. Internal FAA administrative and procedural information may be transmitted or received.

Specialists, providing direct pilot support, interface with FSDPS through terminals. The specialist translates pilot requests into instructions for the FSDPS, enters them into a terminal, and interprets the response for the pilot.

1.3.2 AFSS Description.- The AFSS consists of processing and communication equipment which supports the flight service station specialist's interaction with the FSDPS. The AFSSs maintain/control the specialists' terminals and provide for the transfer of information between the AFSSs and their controlling FSDPS. The AFSSs receive information from the specialists via keyboard, send this information to the FSDPS, receive responses from the FSDPS and display this information to the specialist via CRT or printer. A typical AFSS equipment configuration is shown in figure 1-3.

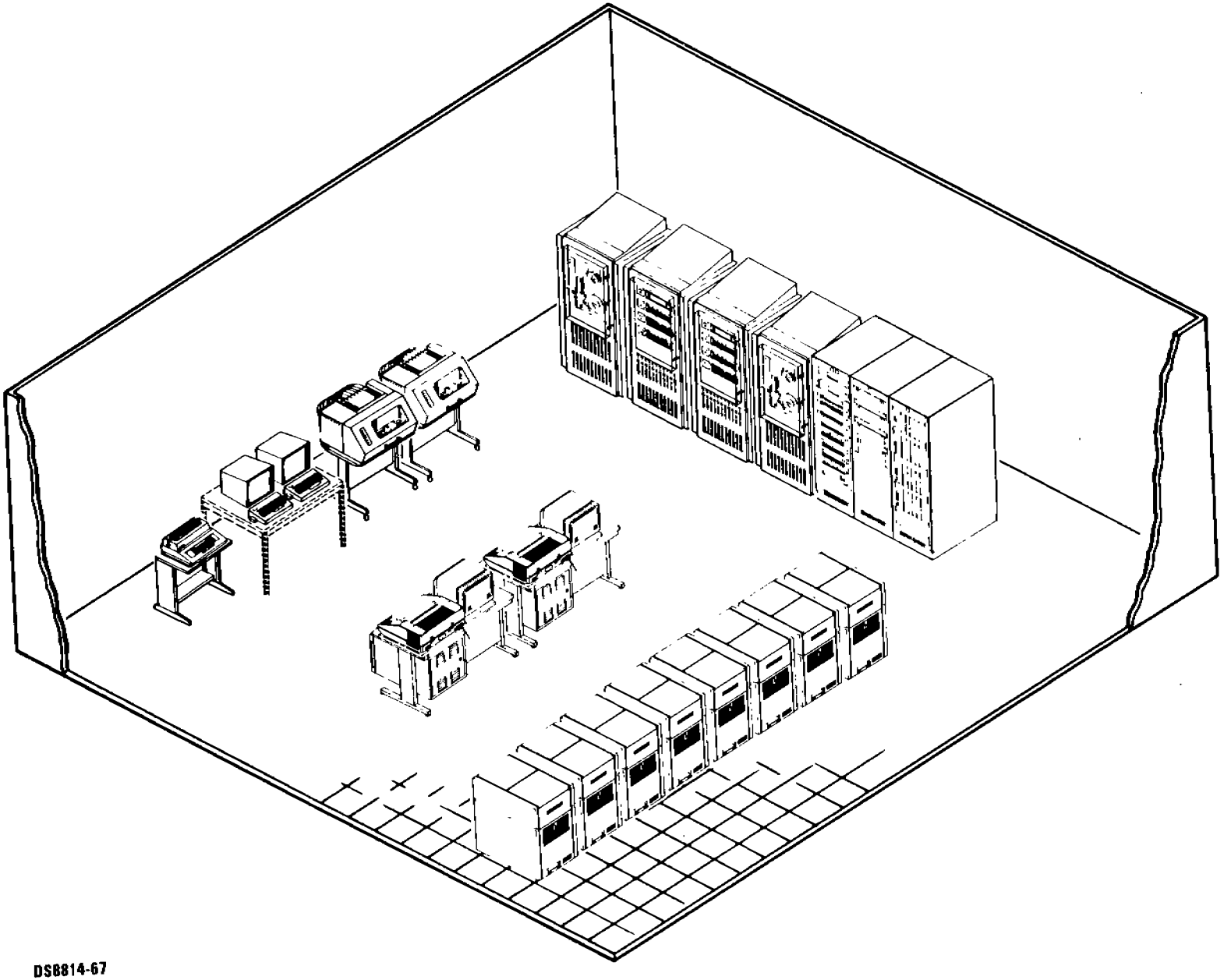

Figure 1-2. Typical M1FC FSDPS Equipment Configuration

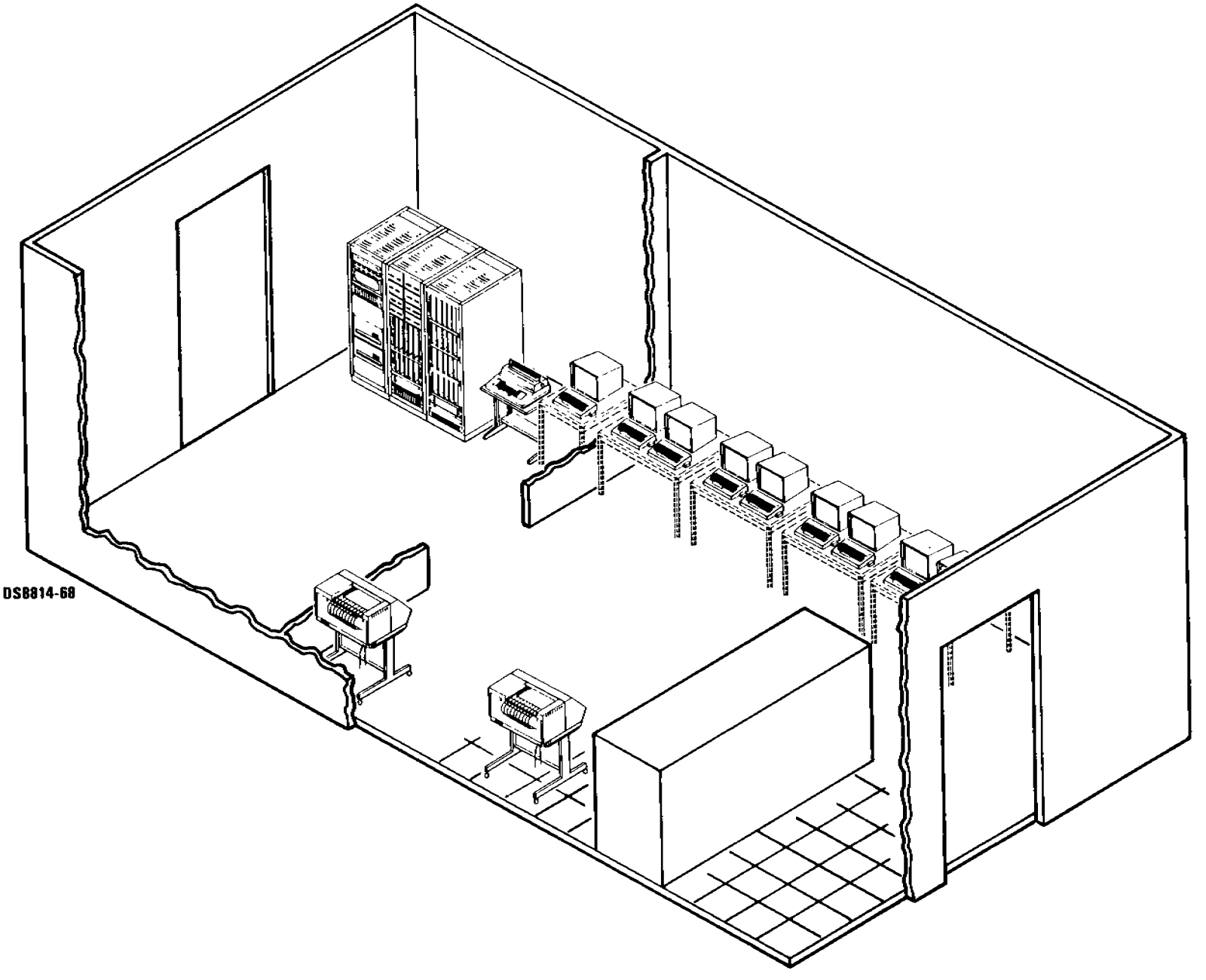

Figure 1-3. Typical M1FC AFSS Equipment Configuration

1.3.3 AWP Description.- The AWP consists of four computer subsystems, each with its own pair of disk drive/controllers. This computer subsystem has access to communications line controllers, CTS, SMMC, magnetic tape drives, line printers, and the backup path to the disks of another computer subsystem in the AWP. The AWP provides for the collection and maintenance of all weather and global flight safety information in the M1FC FSAS. The AWP maintains external interfaces to WMSC and the Service B circuit, and internal interfaces to terminal equipment at the AWP, all FSDPSs, and the other AWP.

The M1FC AWP subsystem connects to WMSC over a medium speed communications line. This interface allows the AWP to receive all domestic, Canadian, and Mexican weather information as well as selected international information. This interface also allows WMSC to collect weather observations from the AWP.

The M1FC AWP subsystem will collect and store this information and forward it to the M1FC FSDPS for storage. On request, the information will be presented to the specialist. Weather and NOTAM (Notice to Airmen Message) information is available at the FSDPS for heavily used areas as well as for uniquely specified routes or areas. A typical AWP equipment configuration is shown in figure 1-4.

1.4 RELATIONSHIP OF UNITS.- Functionally, the M1FC FSAS is divided into three main subsystems: the Flight Service Data Processing Subsystem (FSDPS), Automated Flight Service Station (AFSS), and Aviation Weather Processor (AWP). Figures 1-5 thru 1-7 show the equipment relationship of each subsystem , respectively, while Figure 1-8 shows the equipment relationship of the Maintenance and Diagnostic Test Set (MADTS) which is collocated with Sector FSDPS maintenance equipment for hardware testing.

1.4.1 Relationship of FSDPS Equipment.- Each FSDPS consists of a Tandem Non Stop II Computer Processor System containing four processors, each with its own pair of disk drives/controllers and access to communications line controllers, magnetic tape drives, line printers, and backup paths to the other computer's disks. The processing subsystem is functionally divided into five major areas:

(1) processor,
(2) I/O controllers,
(3) peripherals,
(4) communications channels, and
(5) DC power distribution.

All the processing subsystem's segments, except the communications channels, stand alone and require no external interfacing other than AC power.

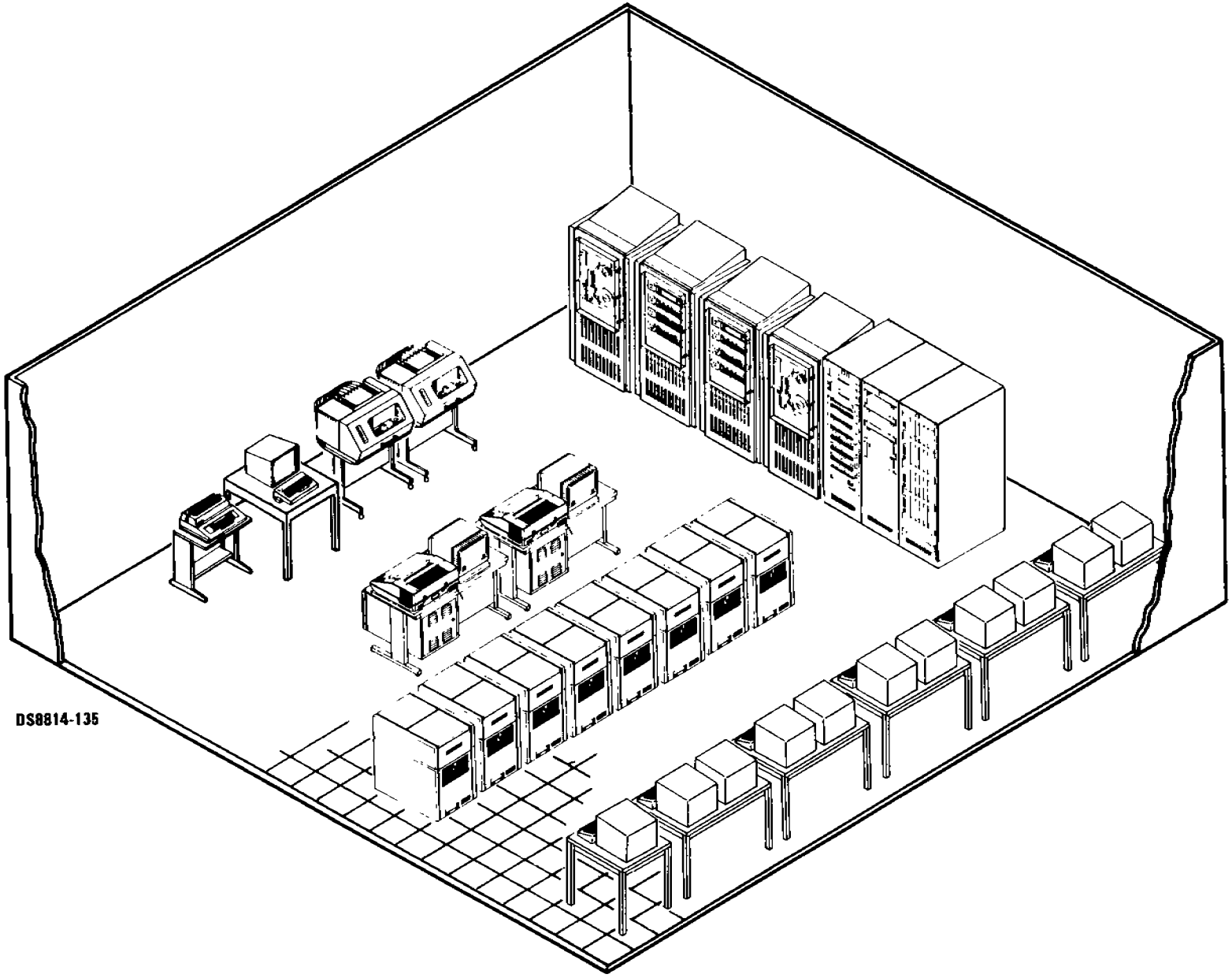

Figure 1-4. Typical M1FC AWP Equipment Configuration

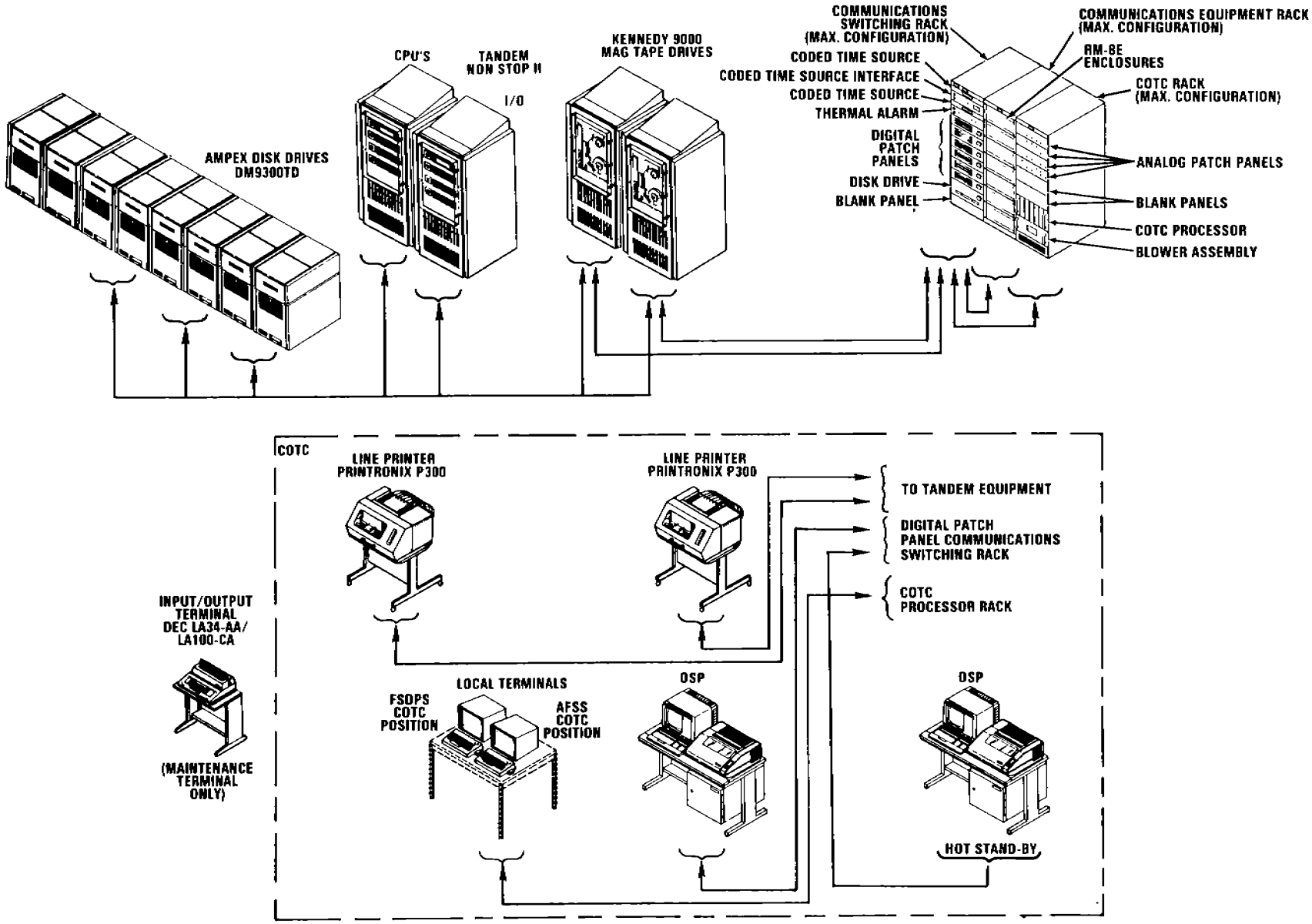

Figure 1-5. M1FC FSDPS Relationship of Units

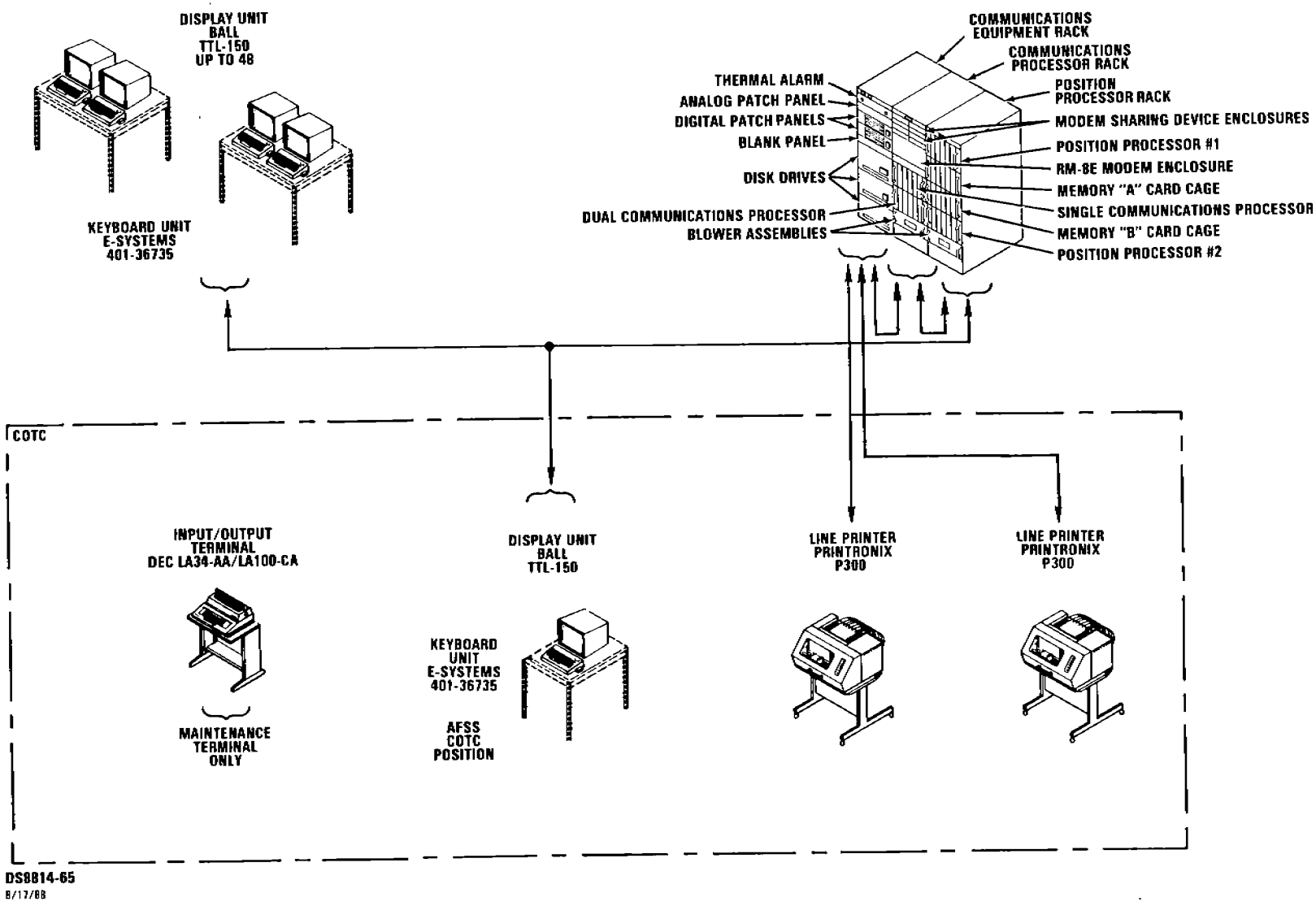

Figure 1-6. M1FC AFSS Relationship of Units

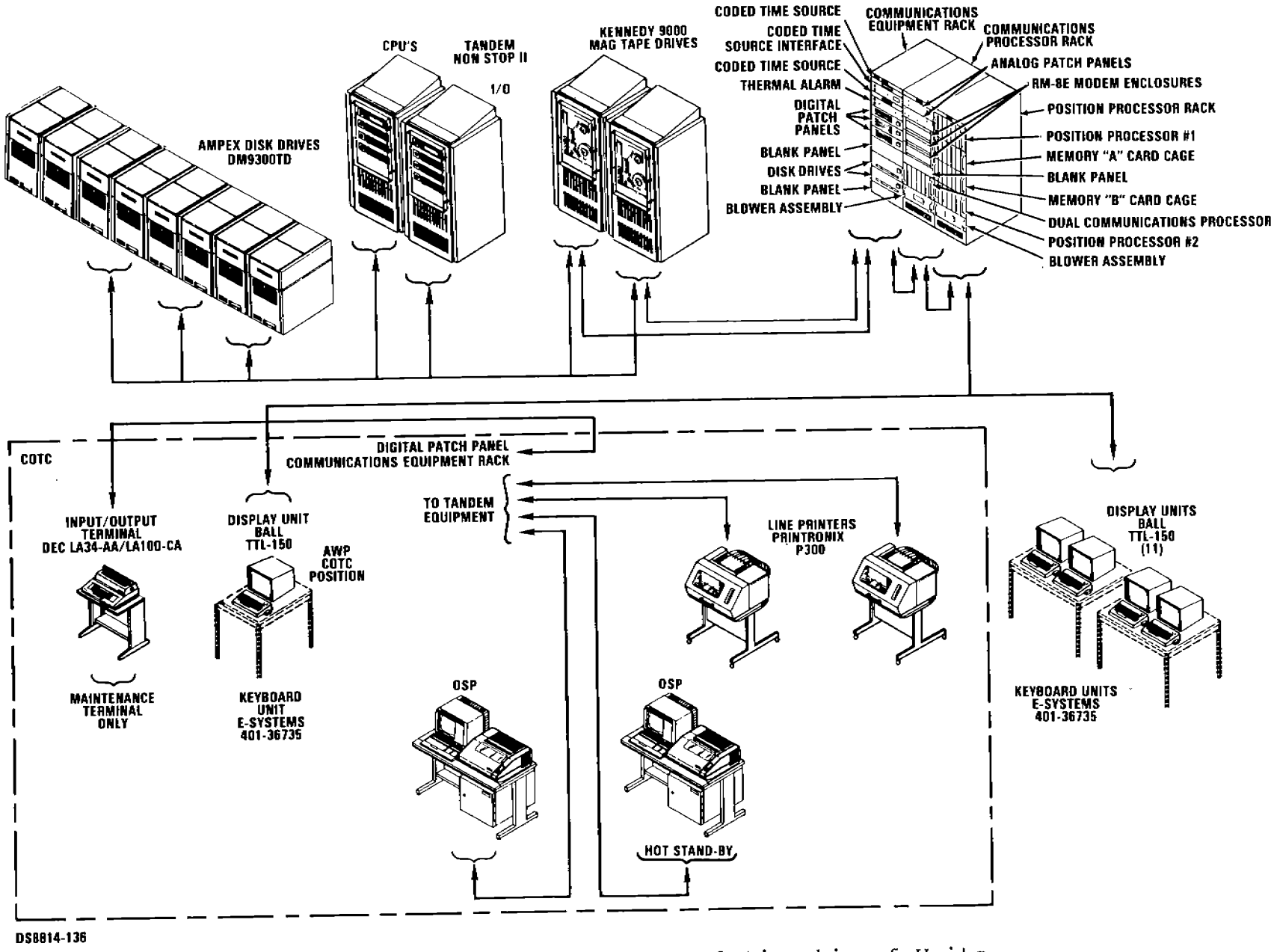

Figure 1-7. M1FC AWP Relationship of Units

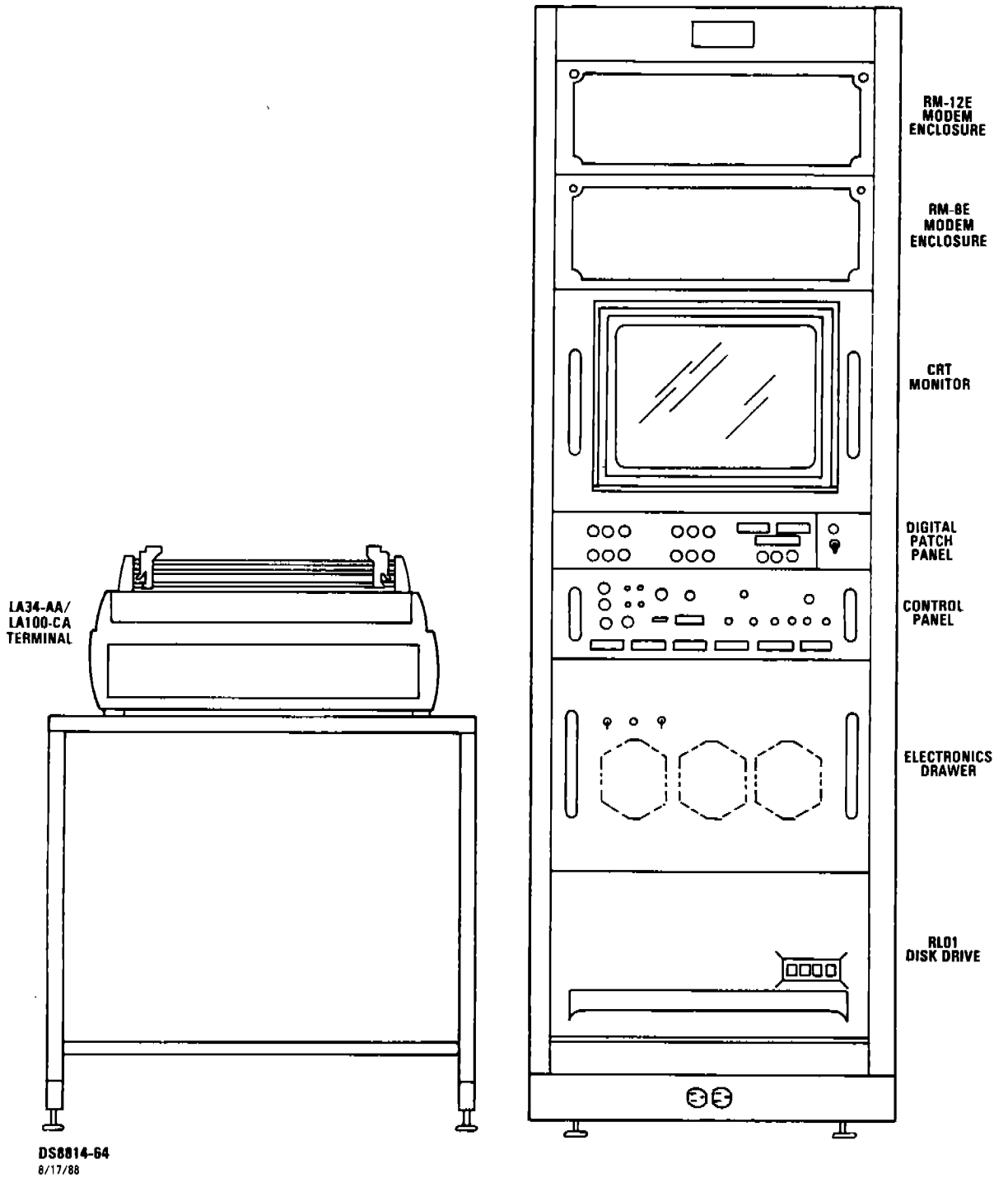

Figure 1-8. Maintenance and Diagnostic Test Set

1.4.1.1 Ampex Disk Drive Relationship.- Each FSDPS contains eight DM9300TD Disk Drives: two redundant drives per processor subsystem. Interface is provided by T16/3106 Disk Controllers and a T16/7504 Patch Panel. To prevent daisy-chain failure from bringing down the data base, each of two disk drives is connected to two disk controllers which simultaneously provide alternate access paths to each disk drive.

1.4.1.2 Kennedy Magnetic Tape Drive Relationship.- Two T16/5103 Magnetic Tape Drives are provided; each one is interfaced through a T16/3202 Magnetic Tape Controller. Each dual-port controller handles up to two independently connected tape drives without the conventional requirement for daisy-chaining. If a single processor failure occurs, then the dual-port controller is powered from the second processor. Similarly, a faulty tape drive cannot corrupt a processor since the address and count words are held in the Input/Output (I/O) C Table, not the tape controller.

1.4.1.3 Printronix Line Printer Relationship.- The Computer Operator Terminal Console (COTC) includes two printers. Each printer interfaces to the processors through a T16/7501 Asynchronous Patch Panel, a T16/6304 Asynchronous Extention Board, and a T16/6303 Asynchronous Controller.

1.4.1.4 Digital Equipment Corp. (DEC) LA34-AA/LA100-CA Input/Output Terminal (IOT) Relationship.- The LA-34-AA/LA100-CA Input/Output Terminal (IOT) is a hard copy terminal used for maintenance purposes in LSI-11 support. It is not interfaced with the application software, and is not an operational piece of hardware. Interface to the system is via the digital patch panel.

1.4.1.5 Tandem Operations and Service Processor (OSP) Relationship.- Each FSDPS has two Operations and Service Processors (OSPs). This system provides operator interface with the operating system, and the capability to perform detailed diagnostic tests on any one of the four Tandem processors while the selected processor is on-line. The second OSP is provided as a "hot standby." Each processor has a display, a keyboard, and a line printer. Interface to the Tandem processors is via the Processor Maintenance Interface (PMI).

1.4.1.6 Two Position A/N Local Terminal Relationship.- This position consists of two Ball monitors. One functions as the local AFSS COTC and the other functions as a FSDPS COTC. Both monitors have keyboards. The Tandem Non Stop II interface is via BIT Synchronous Controller T16/6203.

1.4.1.7 Communications Switching Rack Relationship.- The maximum configured FSDPS communications switching rack equipment consists of a thermal alarm unit, a coded time source interface unit, six Dynatech digital patch panels, a DEC RL01-AK/RL02-AK Disk Drive, two coded time source (CTS) units (Model 60-DC WWVB Synchronized Digital Clocks), and a circuit breaker AC junction box.

The two CTS units interface with the CTS interface unit. The CTS interface unit in turn interfaces via digital patch panel to a asynchronous patch panel of the Tandem processing system. The CTS interface unit also interfaces with the SMMC contact closure.

The digital patch panels interface the modems to the synchronous patch panels of the Tandem processing system. Also, the digital patch panel provides the COTC equipment interface with the Tandem processing system.

The RL01-AK/RL02-AK Disk Drive interfaces with the communications processor in the COTC processor rack via the RLV12 Disk Controller. The disk drive is a separate disk subsystem which provides direct memory access (DMA) to the communications processor. The disk drive includes closed-loop track following which eliminates all calibration requirements.

The thermal alarm unit interfaces with alarm sensors in the COTC processor rack. The thermal alarm unit monitors the differential rack temperature, and gives audible/visual warning when the exhaust air temperature is not within specifications.

1.4.1.8 Communications Equipment Rack Relationship.- The communications equipment rack contains the FSDPS modems, modem power supplies, and a plain AC junction box which supplies power to the modem power supplies. These modems interface the Tandem processors at the FSDPS with up to eight associated AFSSs via communication lines.

1.4.1.9 COTC Processor Rack Relationship.- The COTC Processor rack at the FSDPS contains one communications processor and one position processor. These processors handle the message traffic to and from the data base and the COTC display terminals.

Four analog patch panels and one fan AC junction box are provided in the maximum configured COTC processor rack. The analog patch panels interface data to/from the AFSSs and AWPs with the FSDPS. Service B data is interfaced with the FSDPS by using a government furnished 1200 bps modem. The fan AC junction box provides AC power to the rack equipment.

1.4.2 Maintenance and Diagnostic Test Set (MADTS)

Relationship.- The MADTS is an LSI-11 based system which provides diagnostic testing and or troubleshooting capability for certain Line Replaceable Units (LRUs). These LRUs are listed in the MADTS Instruction Book, TI 6490.41. The MADTS is a stand alone test set and is located at designated FAA maintenance facilities.

1.4.3 Relationship of AFSS Equipment.- Each AFSS consist of at least three equipment racks, one DEC LA34-AA/LA100-CA IOT, two Printronix P300 Line Printers and up to 48 Specialists display units with keyboards. The equipment racks are the communications equipment rack, the communications processor rack, and from one to three position processor racks.

Data communications between the M1FC FSDPS and each M1FC AFSS is provided by four dedicated voice grade circuits. Each line is connected through an analog patch panel. This arrangement results in four parallel redundant communication channels, any of which can fail without causing a system failure. A failure in either of the circuit paths is detected at the FSDPS automatically; no operator action is required for all communication to be routed to an alternate path. Additional redundancy in the modems and the dial backup capability is also provided.

1.4.3.1 Communications Equipment Rack Relationship.- The communications equipment rack contains a thermal alarm unit, an analog patch panel, two digital patch panels, three RL01-AK/RL02-AK Disk Drives, and a circuit breaker AC junction box.

The thermal alarm unit interfaces with alarm sensors in the communications processor rack and the position processor rack. The thermal alarm unit monitors the differential rack temperature and gives audible/visual warning when the exhaust air temperature is not within specifications.

The analog patch panel interfaces the FSDPS communication lines (lines 0-3 and dialup lines) to the modems. The digital patch panel interfaces the modems to the communications processors via multiplexers. Also the digital patch panels interface the COTC equipment to the communications processors.

1.4.3.2 Communications Processor Rack Relationship.- There are three communications processors located in this rack which establish handshakes to interface incoming data from the FSDPS. Modems and modem sharing devices are also included in this rack. The modems include four 9600 bps modems for interfacing with the four dedicated lines between the FSDPS and AFSS (line 0-3), and a 4800 bps modem for interfacing the dial-up line between the FSDPS and AFSS. The modem sharing devices connect each of the modems as well as two line printers to all three communications processors.

The communications processor rack also provides three multiplexer interface assemblies, three power supply assemblies, a blower assembly and a fan AC junction box. The multiplexer interface assemblies interface the communication processors with the modem sharing devices. The power supply assemblies provide DC voltages to the communication processor card cages. The blower assembly provides cooling air through the equipment rack. The fan AC junction box provides AC power to the blower assembly and power supply assemblies.

1.4.3.3 Position Processor Rack Relationship.- Each AFSS contains from two to six position processors, each made-up of card cages containing three major groups of modules. These groups are the DMA interfaces, the LSI-11 processor group, and the alphanumeric group. The memory boards for the processors are contained in separate card cages. The position processors handle the message traffic to and from the communication lines and the data base via the communications processor and provide the necessary interfaces with the monitor displays.

Each position processor rack contains four power supply assemblies and a blower assembly. Two serial I/O panels are provided in each position processor rack to interface the two position processors with the LA34-AA or LA100-CA Input/Output Terminal (IOT). A keyboard junction box is provided in each position processor rack to interface the two position processors with a maximum of 16 keyboards.

1.4.3.4 DEC LA34-AA/LA100-CA (IOT) Relationship.- Each AFSS has a DEC LA34-AA or LA100-CA (IOT) which is used for maintenance purposes in LSI-11 support. It is interfaced with the operational software to provide an audible alarm. Interface to the system is via a digital patch panel.

1.4.3.5 Printronix P300 Line Printer Relationship.- The AFSS includes two P300 Line Printers. Each printer interfaces to the communications processors via a digital patch panel.

1.4.3.6 Ball Display Monitor Relationship.- The display monitors, with keyboards, interface the specialists at an AFSS with the M1FC FSAS system via the position processors. One of these monitors, assigned as part of the COTC, allows the operator to status the system, validate operations, and reconfigure the equipment for maintenance purposes.

1.4.4 Relationship of AWP Equipment.- Each AWP consist of a Tandem Group, three equipment racks, one DEC LA34-AA/LA100-CA IOT, two Printronix P300 Line Printers and 12 display positions with keyboards. The equipment racks are the communications equipment rack, the communications processor rack, and position processor rack.

Data communications between the M1FC AWP and each M1FC FSDPS is provided by two dedicated voice grade circuits. The AWP is also connected to Service A and Service A backup lines (WMSC) with a 2400 baud modem which is government furnished and Service B and Service B backup lines using a government furnished 1200 baud modem. Each line is connected through an analog patch panel. This arrangement results in two parallel redundant communication channels either of which can fail without causing a system failure.

1.4.4.1 Tandem Equipment Group Relationship.- The Tandem Equipment Group in the AWP is identical to the FSDPS Tandem Equipment Group with the addition of two Byte Sync Controllers, T16/6202, connected to the Service A communication lines. The bit synchronous controllers are used to interface to the FSDPSs instead of the AFSSs.

1.4.4.2 Communications Equipment Rack Relationship.- The communications equipment rack in the AWP contains a thermal alarm unit, an analog patch panel, three digital patch panels, two RL01-AK/RL02-AK Disk Drives, two coded time sources, a coded time source interface, and a circuit breaker AC junction box.

The thermal alarm unit interfaces with alarm sensors in the communications processor rack and the position processor rack. The thermal alarm monitors the differential rack temperature to ensure that the exhaust air temperature remains within specifications.

The digital patch panel interfaces the communications processors with the Tandem equipment and selected peripheral equipment. Also the digital patch panel interfaces the position processor with the LA34-AA/LA100-CA Input/Output Terminal (IOT).

1.4.4.3 Communications Processor Rack Relationship.- There are two communications processors located in this rack which establish handshakes to interface incoming data from the Tandem group. Modems are also included in this rack. The modems include nine 9600 bps modems for interfacing the Tandem Group/communications processors communications and nine 9600 bps fast-poll modems for interfacing the AWP/FSDPS communications.

The communications processor rack also provides two multiplexer interface assemblies, two power supply assemblies, a blower assembly and a fan AC junction box. The multiplexer interface assemblies interface the communication processors with the 9600 bps modems. The power supply assemblies provide DC voltages to the dual communications processor card cage. The blower assembly provides cooling air through the equipment rack. The fan AC junction box provides AC power to the blower assembly and power supply assemblies.

1.4.4.4 Position Processor Rack Relationship.- The AWP contains two position processors; each made-up of card cages containing three major groups of modules. These groups are the DMA interfaces, the LSI-11 processor group, and the alphanumeric group. The memory boards for the processors are contained in separate card cages. The position processors handle the message traffic to and from the communication lines and the data base via the communications processor and provide the necessary interfaces with the monitor displays.

The AWP position processor rack contains four power supply assemblies and a blower assembly. Two serial I/O panels are provided in each position processor rack to interface the two position processors with the LA34-AA or LA100-CA Input/Output Terminal (IOT). A keyboard junction box is provided in each position processor rack to interface the two position processors with 12 keyboards.

1.4.4.5 DEC LA34-AA/LA100-CA (IOT) Relationship.- The AWP AFSS has a DEC LA34-AA or LA100-CA (IOT) which is used for maintenance purposes in LSI-11 support. It is interfaced with the operational software to provide an audible alarm. Interface to the system is via a digital patch panel.

1.4.4.6 Printronix P300 Line Printer Relationship.- The AWP contains two P300 Line Printers. Each printer interfaces the communications processors via a digital patch panel.

1.4.4.7 Ball Display Monitor Relationship.- The display monitors, with keyboards, interface the display positions at the AWP with the operating system via the position processors. One of these monitors, assigned as part of the COTC, allows the operator to status the system, validate operations, and reconfigure the equipment for maintenance purposes.

1.5 EQUIPMENT SPECIFICATION DATA.- The M1FC FSAS system consists of recently designed equipment and modified-off-the-shelf equipment supplied by E-Systems and other off-the-shelf-equipment supplied by various manufacturers. Refer to table 1-1 for a listing of supplied equipment manuals to obtain specification data on related equipment. See the M1FC FSAS Equipment Instruction Book, TI 6490.37, for detailed information concerning E-Systems equipment.

1.5.1 External Power Requirements.- The FSDPS, AWP, and AFSS require a main distribution panel, with circuit breakers at each equipment area for a power source. Shown below are typical power requirements.

FSDPS/AWP Equipment Area	26.50 KVA
AFSS Equipment Area	10.17 KVA

NOTE

See the applicable Installation Planning Report for exact power requirements of a particular site.

1.5.2 Environmental Characteristics.- The M1FC FSAS system, which includes the FSDPS, AWP, and the AFSSs, is designed to operate in a area maintained at an ambient temperature of +15 to +32 degrees Celsius and a relative humidity between 20 and 80 percent. The equipment heat load is as follows:

FSDPS	86,903 BTU/HR
AFSS	23,402 BTU/HR
AWP	101,802 BTU/HR

NOTE

Heat load varies by site

No special equipment ducting is required. All forced air cooling required within equipment cabinets is accomplished using internal fans.

1.6 EQUIPMENT AND ACCESSORIES SUPPLIED.- Table 1-2 lists the equipment supplied for the typical FSDPS; table 1-3 lists equipment supplied for a typical AFSS; table 1-4 lists the equipment supplied in an AWP; table 1-5 lists the required test equipment for the M1FC FSAS; table 1-6 lists the recommended tools for M1FC FSAS; table 1-7 list the recommended cable repair tools; and table 1-8 lists the M1FC FSAS equipment options.

1.7 SIGNAL EQUIPMENT REQUIRED BUT NOT SUPPLIED.- The FAA provided hardware in this group is defined as:

a. Service A and associated modem
b. Service B and associated modem
c. Leased lines

All of the items listed are required at the FSDPSs. In addition, leased lines are required at the AFSSs.

1.7.1 Service A.- The FAA supplies each FSDPS with a modem interfaced to a Service A leased line. This modem is a Bell 201 series or equivalent operating at 2400 baud, full duplex, synchronous and conforming to EIA RS-449.

1.7.2 Service B.- The FAA supplies each FSDPS with a modem interfaced to a Service B circuit. The modem is a Bell 202C or equivalent operating at 1200 baud, full duplex, asynchronous and conforming to EIA RS-449.

1.7.3 Leased Lines.- Leased lines are provided between a FSDPS and its associated AFSSs. Two lines per AFSS are required. Each line has sufficient conditioning to support a transmission rate of 9600 baud with an error rate of less than one in one hundred thousand.

Table 1-2. Equipment Supplied - FSDPS

Description	Unit Number	Model	Mfg.
Tandem Group		401-42690	Tandem
Disk Drives		DM9300TD	Ampex
Communications Switching Rack	FA-10017/1	401-37622	E-Systems
Communications Equipment Rack	FA-10017/2	401-37623	E-Systems
COTC Processor Rack	FA-10017/3	401-37624	E-Systems
Line Printers		P300	Printronix
Operations and Service Processors (OSP)		T16/3910	Tandem
OSP Video Display Terminals		T16/6530	Tandem
OSP Line Printers		T16/5520	Tandem
CRT Monitors		401-37290-01	Ball/ E-Systems
Keyboard Assemblies		401-36735-03	E-Systems
Keyboard Power Supplies		5305-000-423	Ault
Input/Output Terminal		LA34-AA/ LA100-CA	DEC

Table 1-3. Equipment Supplied - AFSS

Description	Unit Number	Model	Mfg.
Communications Equipment Rack	FA-10018/1	401-37614	E-Systems
Communications Processor Rack	FA-10018/2	401-37615	E-Systems
Position Processor Rack(s)	FA-10018/3	401-37616	E-Systems
Line Printers		P300	Printronix
CRT Monitors		401-37290-01	Ball/ E-Systems
Keyboard Assemblies	FA-10018/8	401-36735-03	E-Systems
Keyboard Power Supplies		5305-000-423	Ault
Input/Output Terminal		LA34-AA/ LA100-CA	DEC

Table 1-4. Equipment Supplied - AWP

Description	Unit Number	Model	Mfg.
Tandem Group		401-42690	Tandem
Disk Drives		DM9300TD	Ampex
Communications Equipment Rack	FA-10020/1	401-12301	E-Systems
Communications Processor Rack	FA-10020/2	401-12302	E-Systems
Position Processor Rack	FA-10020/3	401-12303	E-Systems
Line Printers		P300	Printronix
Operations and Service Processors (OSP)		T16/3910	Tandem
OSP Video Display Terminals		T16/6530	Tandem
OSP Line Printers		T16/5520	Tandem
CRT Monitors		401-37290-01	Ball/ E-Systems
Keyboard Assemblies		401-36735-03	E-Systems
Keyboard Power Supplies		5305-000-423	Ault
Input/Output Terminal		LA34-AA/ LA100-CA	DEC

Table 1-5. Recommended M1FC FSAS Test Equipment

ITEM/DESCRIPTION	AFSS	FSDPS/AWP	FAA Technical Center/ Academy	FAA Repair Depot	FAA Sector Maint. Facility
Oscilloscope Dual Channel (Tektronix 2236 or equivalent with Tektronix K212 Portable Instrument Cart	1	1	1	1	3
Digital Multimeter (Fluke 8062A or equivalent)	1	1	1	1	3
Protocol Analyzer (Hewlett-Packard 4951A or equivalent with 18180A Interface Unit)	1	1	1	1	1
SPECIAL TEST EQUIPMENT					
Maintenance and Diagnostics Test Set (MADTS) (E-Systems)	0	1	1	1	1
Modem Eliminator Model 3 ARK Electronics Inc.	0	1	1	0	0
Asynchronous Loop Back Cable (INMAC Mfg., P.N. 40351)	0	8	1	8	0
Disk Exercizer, Model DDX900B Ampex	0	1	1	1	1

Table 1-6. Recommended M1FC FSAS Tools List

ITEM/DESCRIPTION	PART NO.	QTY*	MANUFACTURER
Sector Facility			
PC Card Extender	T50507	1	Tandem
Card Extender (Card Cage)	3302153-01	1	Ampex
Card Extender (Pwr. Supply)	3308053-01	1	Ampex
Head Install Tool	3303728-01	1	Ampex
Torque-Limit Screwdriver	3302778-01	1	Ampex
Head Position Tool	3302377-01	1	Ampex
Head Spring Tensioner	3302379-01	1	Ampex
Filter Pressure Gauge	3300937-01	1	Ampex
Disk Pack	-	1	Ampex
Retaining Ring Pliers	-	1	Ampex
Skewmaster Tape	154-0036-001	1	Kennedy
Card Extender	190-2224-001	1	Kennedy
Speed Tester	190-4536-001	1	Kennedy
Alignment Tool	154-0006-001	1	Kennedy
300 MByte CE Disk Pack	Dysan	1	Dysan
Q-Bus Extender Board	XTNDR-4	1	Technical Magic

*Quantities are for one facility only. In this case, a set of these tools are required for the Sector Maintenance Facility, the FAA Technical Center and FAA Academy.

Table 1-7. Recommended M1FC FSAS Cable Repair Tools

ITEM/DESCRIPTION	PART NO.	QTY*	MANUFACTURER	USE
Crimp Tool	KTH-1000	1	Kings	BNC
Die	KTH-2001	1	Kings	BNC
Insertion Tool	229384-1	1	Ampex	CHAMP
Extraction Tool	230238-1	1	Ampex	CHAMP
Crimp Tool	M22520/2-01	1	Daniels	D-Type
Positioner	M22520/2-08	1	Daniels	D-Type
Extraction Tool	91067-2	1	Ampex	D-Type
Extraction Tool	91136-1	1	Ampex	Audio
Crimp Tool	90363-1	1	Ampex	Audio
Insertion Tool	455830-1	1	Ampex	Wiring AC J-Box
Extraction Tool	458994-1	1	Ampex	Wiring AC J-Box
Crimp Tool	90296-1	1	Ampex	Wiring AC J-Box
Extraction Tool	30518	1	Ampex	Ampex Disk Cables
Insertion Tool	91002	1	Ampex	Ampex Disk Cables
Crimp Tool	90277-1	1	Ampex	Ampex Disk Cables

*Quantities are for one facility only. In this case, a set of these tools are required for the Sector Maintenance Facility, the FAA Technical Center and FAA Academy.

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Table 1-8. M1FC FSAS Equipment Options

Equipment	Option	Options Provided
LSI-11/23 Processor	Fixed Point Instructions	Yes
MRV11-C Memory MSV11-LF Memory KPV11-B	Floating Point Instructions	Yes
	Extended Instruction Set	Yes
LA34-AA/LA100-CA Terminal	Roll Paper Holder - LAX34-RL	Yes
	Numeric Keypad - LAX34-KL	Yes
	Tractor - LAX34-AL	Yes
	Printer Stand	Yes
RL01-AK Disk Drive	BC20JI/O Cable Chassis Slide and Mounting Hardware - RL01A	Yes
	RL01-A (drive) RK01K-DC (cartridge) -RL01-AK	No
	RL01 Data Cartridge - RL01K-DC	Yes
	RL01-AK, RLV12 Controller BC80M, Terminator	Yes
	DWLB w/H9514-A Top Cover H9603-EE, H9601-ED	No
	DWHB Complete Hiboy Cabinet H9602-EB, H9600-EA	No
	SWHB Option Arrangement Dwg., H9600-EB, HB9602-B-0	No
	DWHB Option Arrangement Dwg., H9600-A-0	No
	SWLB Option Arrangement Dwg., H9600-B-0	No
	DWHB Option Arrangement Dwg., H9600-A-0	No

Table 1-8. M1FC FSAS Equipment Options (Continued)

Equipment	Option	Options Provided
RL02-AK Disk Drive	BC20JI/O Cable Chassis Slide and Mounting Hardware - RL02A	Yes
	RL02-A (drive) RK02K-DC (cartridge) -RL02-AK	No
	RL02 Data Cartridge - RL02-DC	Yes
	RL02-AK, RLV12 Controller BC80M, Terminator -RLV22-AK	Yes
	DWLB w/H9514-A Top Cover H9603-EE, H9601-ED	No
	DWHB Complete Hiboy Cabinet H9602-EB, H9600-EA	No
	SWHB Option Arrangement Dwg., H9600-EB, HB9602-B-0	No
	DWHB Option Arrangement Dwg., H9600-A-0	No
	SWLB Option Arrangement Dwg., H9600-B-0	No
	DWHB Option Arrangement Dwg., H9600-A-0	No
RLV12 Disk Controller	Cable BC20J-206m (20 Feet)	No
	Cable BC20J-4012m (40 Feet)	No
	Cable BC20J-6018m (60 Feet)	No

Table 1-8. M1FC FSAS Equipment Options (Continued)

Equipment	Option	Options Provided
DMA-QB Direct Memory Access Controller	See Appendix A, DMA Configuration Specifications	
8S Eight Channel Serial Interface	See Appendix A, 8S Eight Channel Serial Interface	
RM-8E Multiple Modem System	See Appendix A, RM-8E Multiple Modem System	
Model 9000 Tape Drive		
P300 Line Printer	Forms Length Selector	Yes
	Compressed Print	Yes
	Multi-mode Print	Yes
	OCR High Resolution	No
	PROMs OCR A and B Sets	No
	Slow Close Cover	No
	Quick Access Cover	Yes
	Pedestal and Paper Stacker	Yes
Digital and Analog Patch Panel	None	
Display Monitor P/N 401-37290-01	None	
Keyboard Unit P/N 401-36735	None	

Table 1-8. M1FC FSAS Equipment Options (Continued)

Equipment	Option	Options Provided
Model 60-DC Coded Time Source	External Oscillator	Yes
	IRIGH	No
	Parallel BCD Time Output Assembly	No
	IRIG B DC Level Shift	No
	Coded Format (Field Conversion)	No
	Slow Code (Field Conversion)	No
MM43 Regulated Power Supply	None	
M200 Matrix Printer	Pedestal Assembly	No
	TCVFU Assembly and Control Panel Assembly	No
	DPC Long-Time Parallel Interface Circuit Card Assembly	No
	Serial Interface Circuit Card Assembly EPROM Kit 2708	Yes
	DPC Centronics - Compatible Interface Circuit Card Assembly	No
	Adapter Cable Assemblies	Yes
	DPC Short-Line Parallel Interface Circuit Card Assembly	No
	Optional Header	Yes
	Rear Forms Load	Yes
	6/8 Lines Per Inch Switch	Yes
	Condensed Print Switch	Yes

Table 1-8. M1FC FSAS Equipment Options (Continued)

Equipment	Option	Options Provided
M200 Matrix Printer (Cont'd)	Direct Access Vertical Format Unit (DAVFU)	No
	Parity Error Detect Enable	Yes
	Parity Odd/Even	Yes
	Fixed Perforation Skipover	Yes
	11/12 Forms Length	Yes
	Automatic Line Feed	Yes
	Seven Bits Only Word Length	Yes
	Status Display	Yes
Model 9000 Tape Drive	STD Interface	Yes
	Speed - 45 IPS	Yes
	Dual Density (800/1600 CPI)	Yes
	Tracks (9)	Yes

SECTION 2

TECHNICAL DESCRIPTION

2.1 GENERAL.- The Model 1 Full Capacity (M1FC) Flight Service Automation System (FSAS) consists of three major subsystems, the FSDPS, AFSS, and AWP. An FSDPS can communicate with up to eight satellite AFSSs and the FSDPS COTC position equipment at, and logically connected to, the FSDPS. This FSDPS COTC position equipment consists of two A/N displays with keyboards. No lease line is required for the local position equipment, even though the same modems and communications equipment is used to transmit data to and from the FSDPS and the local position equipment that is used between the FSDPS and the AFSSs.

The Computer Operator Terminal Console (COTC) provides operator control of the M1FC FSAS. The COTC at the FSDPS consists of two Operations and Service Processors (OSPs) Each OSP includes a CRT, keyboard, and line printer. One of the OSPs is a "hot stand-by". The FSDPS COTC also includes two CRT Monitors, 401-37290-01, with keyboards, 5305-000-423, and two P300 Line Printers. One of the OSPs is a "hot standby". At each AFSS the COTC consists of a designated A/N Display Terminal, an IOT (LA34-AA/LA100-CA), and two P300 Line Printers. The COTC at the AWP consists of two OSPs as well as a designated CRT Monitor, an IOT, and two P300 Line Printers.

2.2 THEORY OF OPERATION.- The M1FC FSAS system is shown in figure 2-1 and a simplified block diagram showing the three major subsystems is shown in figure 2-2. The FSDPS provides the collection, maintenance and dissemination of information related to flight services to the AFSSs. The FSDPS maintains external interfaces to WMSC (via the AWP) and Service B and internal interfaces to terminal equipment at the AFSS via dedicated line circuits. Figure 2-3 shows a typical FSDPS operational site.

2.2.1 FSDPS Hardware.- The hardware elements of a M1FC FSDPS operational system are shown in figure 2-4. The hardware consists of processing and communications equipment (supporting the operational system) and maintenance equipment for diagnostic support of the FSDPS.

The processing equipment includes the Tandem CPUs, OSP, COTC processors, and all I/O controllers and peripherals connected to the Tandem CPUs. The communications group consists of patch panels and modems necessary to complete the communication links to the AFSSs, AWPs, and Service B. The maintenance equipment consists of Tandem diagnostic hardware and other tools necessary to diagnose and repair the equipment.

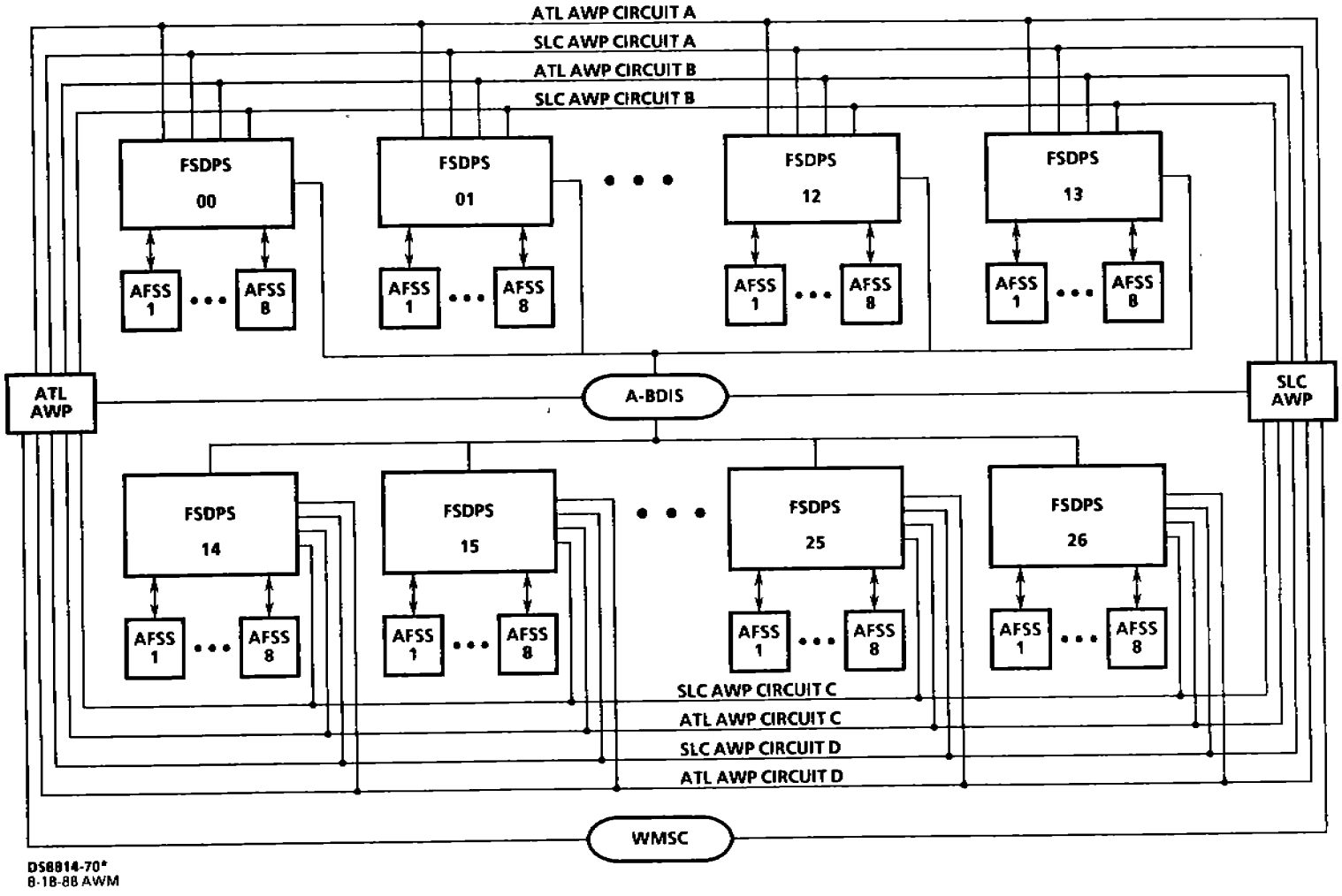


Figure 2-1. M1FC FSAS System

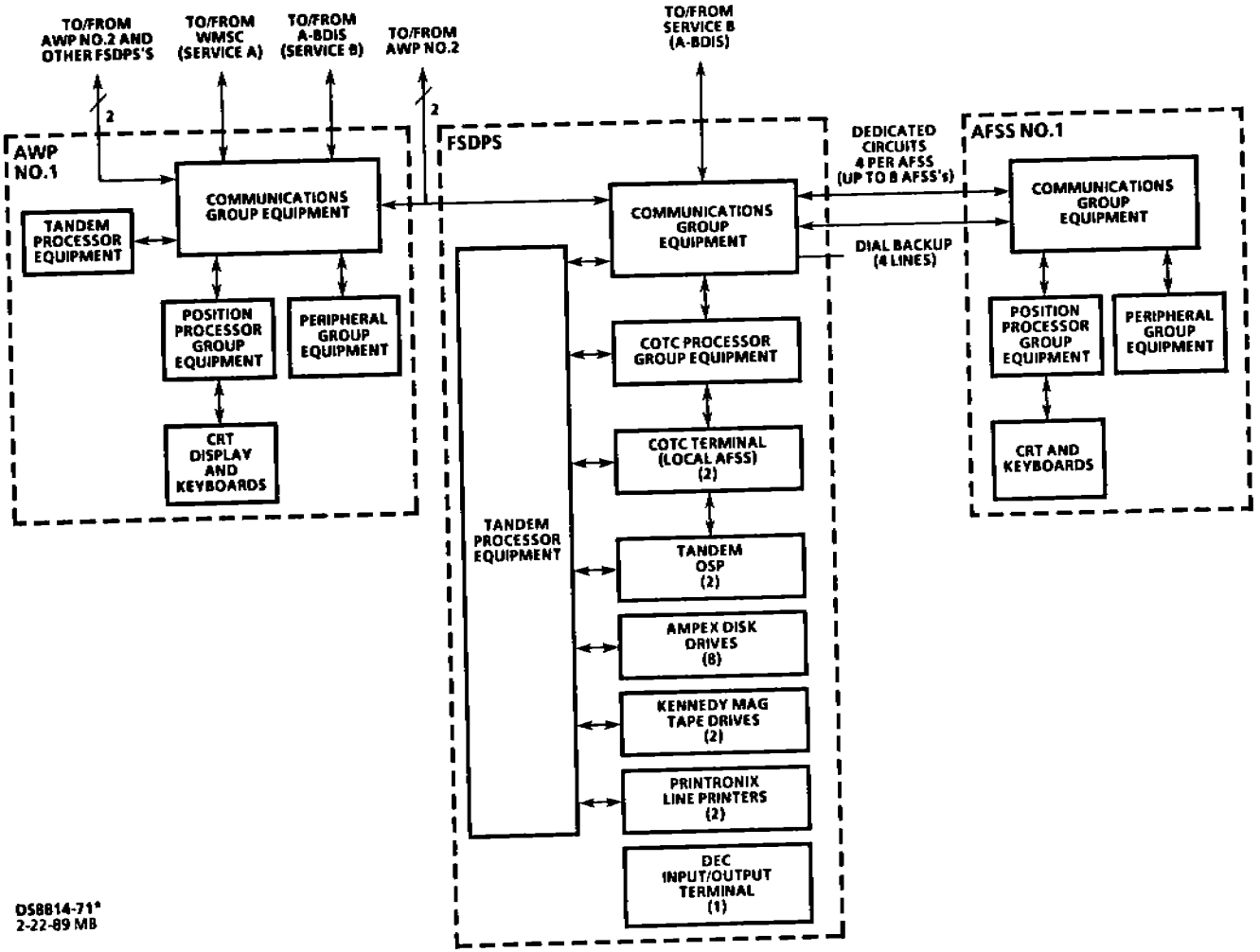


Figure 2-2. M1FC FSAS Simplified Block Diagram

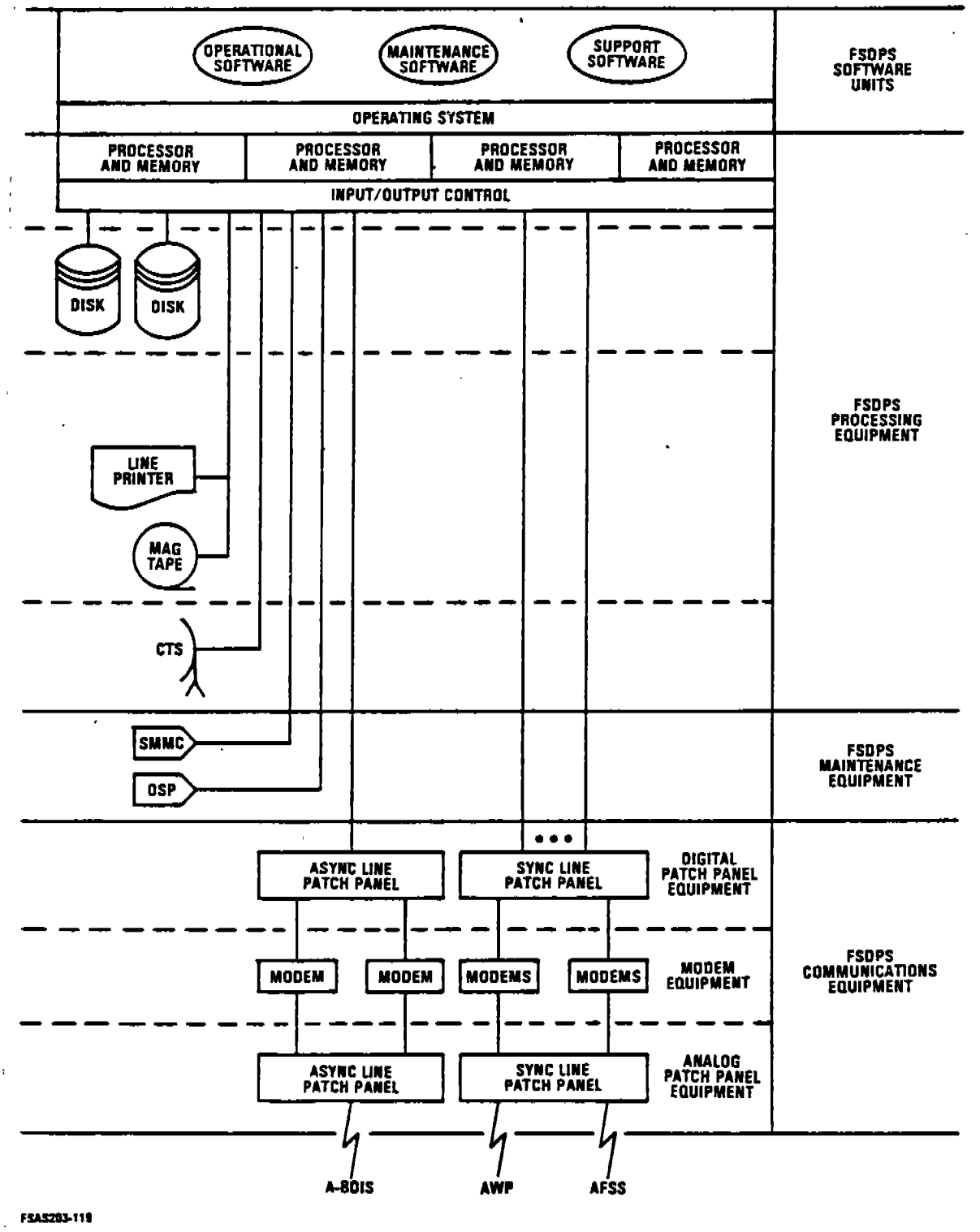


Figure 2-3. Typical M1FC FSDPS Operational Site

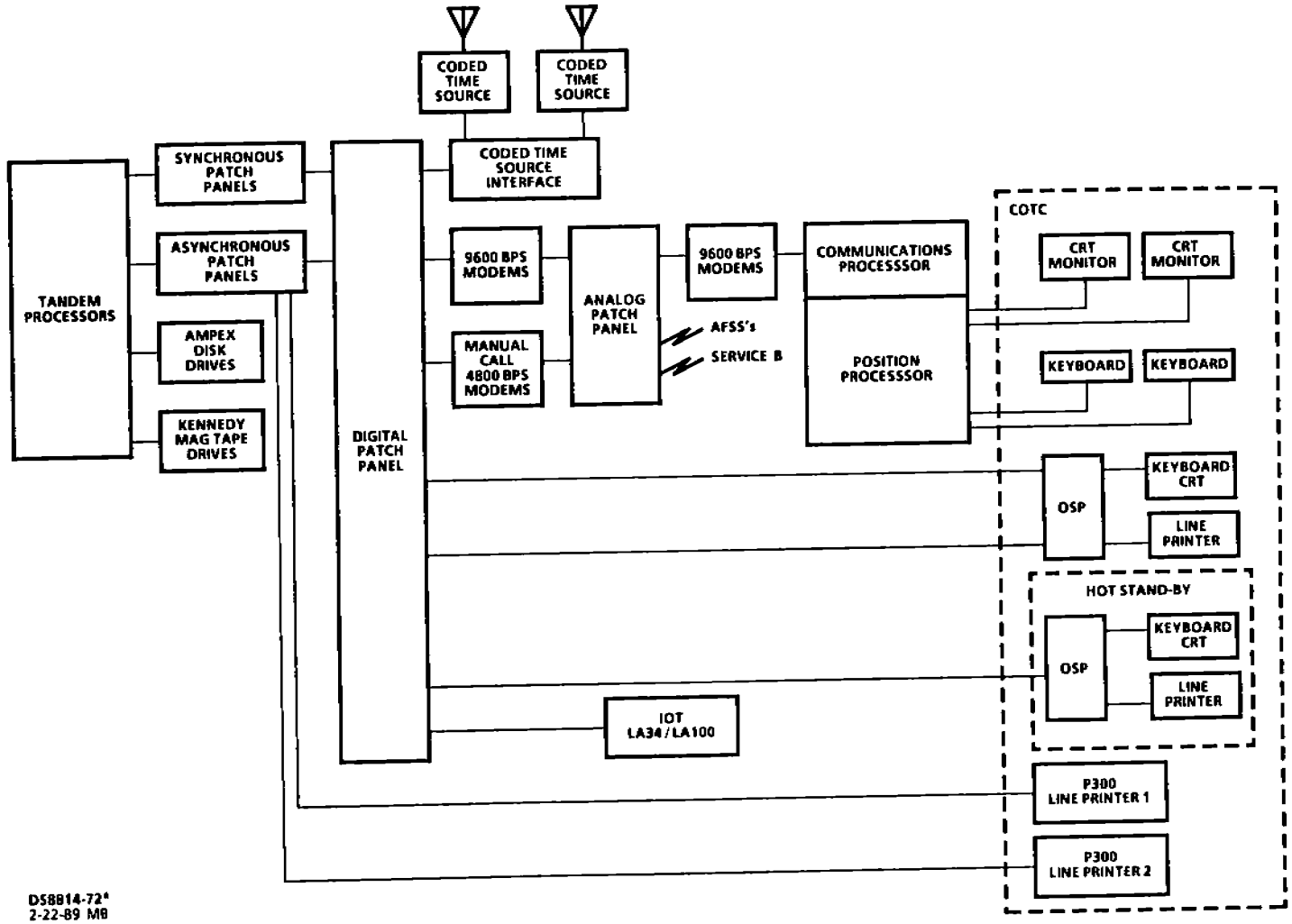


Figure 2-4. FSDPS Elements

2.2.2 FSDPS Software.- The M1FC FSDPS software consists of the following three functional categories:

1) operational software
2) support software, and
3) maintenance software.

The overall software structure concept separates operational software from support and maintenance software, where the operational software is given priority. The system is designed such that any software (with the exception of MADTS) can be executed at any given site.

The operational software is designed to operate in a load-sharing environment where, to the extent possible, all resources are used equally. Support and maintenance software is designed to operate on dedicated pieces of equipment, but may operate in a low-priority background mode. The background mode allows a sharing of resources normally used by operational software, but on an as-available noninterference basis. When support and maintenance software operate on dedicated equipment, the dedicated equipment is removed from use by the operational software. The remaining equipment is used in a load-sharing method by the operational software. If the support and maintenance software is operating in a background mode, the operational software continues to use resources equally. Support and maintenance software use the remaining resource capacity, if any.

These two methods of executing support and maintenance software lead to a revision of the definition of "off-line." The system is designed such that every AWP or FSDPS CPU or AFSS processor is operating in one of four modes. Mode 1 is the executing of operational software only. Mode 2 is the executing of operational software and executing support or maintenance software in the background. Mode 3 is the executing of support or maintenance software under the control of the same operating system used by the operational software. Mode 4 is the executing of support or maintenance software as stand alone software or under the control of an operating system other than the one used by the operational software.

The system is considered operational if at least one AWP CPU, one FSDPS CPU, and one communications/position processor pair per AFSS is operating in either Mode 1 or 2. Mode 3 is an off-line mode which is used for data base installation, weather data base reconstruction or for the execution of more exhaustive diagnostics. MADTS and the Mode 3 are used primarily to aid repair functions. Mode 4 is rarely used in the AWP, FSDPS, or AFSS configurations, but is available to isolate failures that cannot be isolated in the other modes.

2.2.2.1 FSDPS Operational Software.- The FSDPS operational software responds to requests from specialists to obtain weather briefings and to file flight plans. This software responds to these requests for action or data within a short period of time (seconds). This software supports an interface to Service B and maintains a data base of flight plan information to support the operational needs.

2.2.2.2 FSDPS Support Software.- The FSDPS support software is executed from the OSP terminal or from the Tandem terminal connected via the asynchronous controller. It prepares data for the FSDPS operational software, provides support for the development of the operational software, and prepares administrative reports for the AFSSs. This support software is not initiated from the specialists' operational terminals. It is the type of software traditionally satisfied by the batch type of processing.

2.2.2.3 FSDPS Maintenance Software.- The FSDPS maintenance software assists maintenance personnel in isolating failures to replaceable hardware elements.

The software of the FSDPS operates as an integrated unit within each of the Tandem CPUs. Each CPU can operate in one of the following five modes at any time:

1) Mode 1 - FSDPS full operational software only;

2) Mode 2 - FSDPS full operational software plus selected support and/or maintenance software;

3) Mode 3 - FSDPS partial operational software plus selected support and/or maintenance software;

4) Mode 4 - FSDPS selected support and/or maintenance software; and

5) Mode 5 - FSDPS maintenance software.

In Modes 1 through 4 the Tandem Non Stop II Guardian Operating System is operating in the CPU, while in Mode 5 the CPU is operating as a separate entity in shadow mode.

When mixed software units are operating (i.e. Modes 2, 3 and 4) CPU utilization by the respective units is controlled by executing priority. Mode 5 (i.e. shadow mode) is reserved for those diagnostic programs which require a dedicated CPU.

The M1FC FSAS maintains redundant paths for most system elements and is completely supported by the FSDPS hardware and software. Figure 2-5, M1FC FSDPS Architecture, abbreviates the

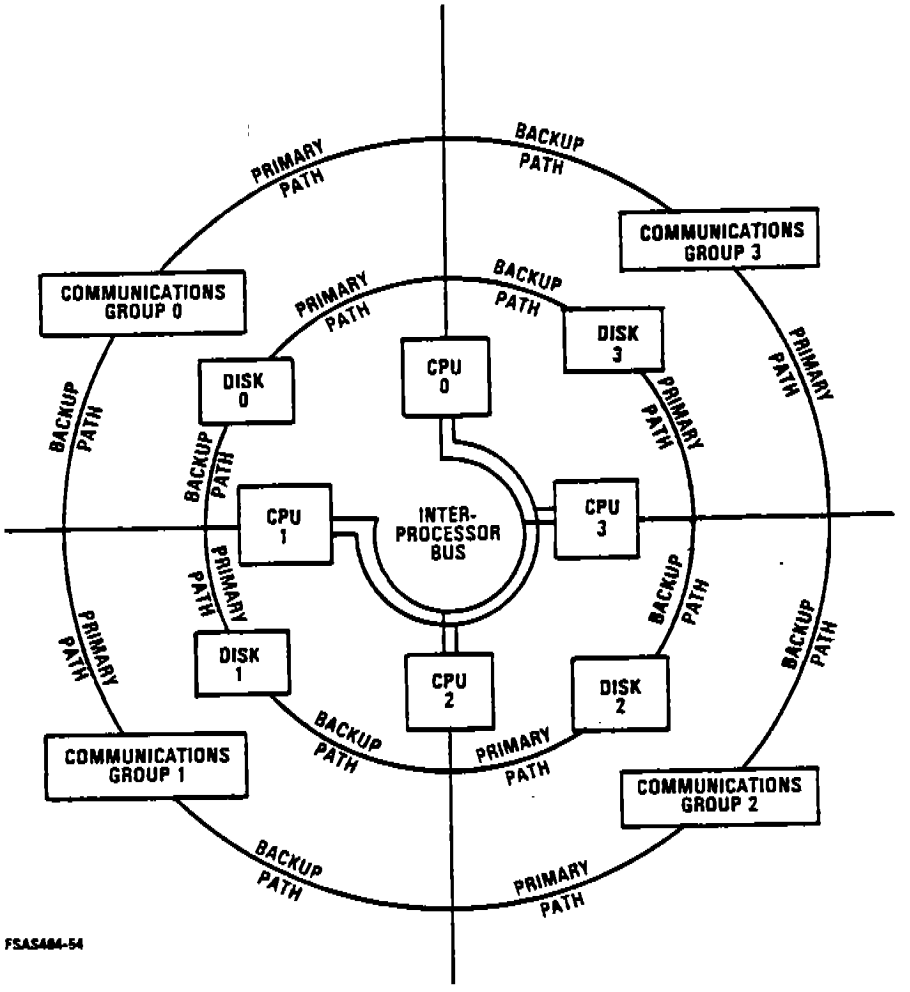


Figure 2-5. M1FC FSDPS Architecture

FSDPS configuration to illustrate the backup capabilities existing in the FSDPS. The figure shows four CPUs connected via the interprocessor bus (actually two interprocessor buses for redundancy). Disk 0 and communications group 0 are under primary control of CPU 0 with CPU 1 maintaining the backup path to these devices. In the event of a failure in the primary path to an element (disk 0 or communications group 0), CPU 0 uses the backup path through CPU 1 to the failed element. In case of a CPU failure (CPU 0), CPU 1 assumes the primary control of disk 0 and communications group 0 and continues normal processing. As the figure illustrates, the same backup relationship exists for CPUs 1 and 2, 2 and 3, and 3 and 0.

The operational software unit is composed of the following subprograms:

1) Guardian Communications Processes,
2) AFSS I/O,
3) Service A I/O,
4) Service B I/O,
5) Service A Edit,
6) Service B Edit,
7) queue management,
8) time manager,
9) event scheduling,
10) supervisory functions,
11) recovery/reconfiguration,
12) weather retrieval,
13) route processing,
14) flight plan data,
15) local weather,
16) start up/shutdown,
17) data base, and
18) historical recording.

Detailed descriptions of each of these subprograms are presented in Section 3 of this instruction book.

The support software unit consists of subprograms to perform the event reconstruction and the data base generation functions. These subprograms execute in the background mode while the operational software unit executes in the foreground mode.

The maintenance software unit consists of diagnostic subprograms for the following hardware elements:

1) CPU,
2) memory,
3) magnetic tape drive,
4) disk drive,
5) IOT,

6) line printer,
7) byte synchronous controller (AWP only),
8) bit synchronous controller, and
9) asynchronous controller.

2.2.3 AFSS Hardware.- The AFSS hardware consists of processing equipment and communications equipment required to support the flight service station specialist interaction with the FSDPS. The AFSS hardware is described in detail in section 2.3.2. Figure 2-6 shows the AFSS communications processors and the AFSS position processors in the maximum 48 position configuration. Figure 2-7 shows an AFSS position processor in a 16 position (maximum) configuration.

The communications multiplexers support the ADCCP, bit synchronous communications with the FSDPS. The HEX/IPB-11 (located in the communications processor) and the DMA-QB (located in the position processor) provide the high speed data transfer link between the communications function and the terminal display function of an AFSS.

The keyboard serial I/O circuit board (TMI-8S) allows each keyboard to enter characters to be recognized by the position processor. The position processors "echo" these characters via an alphanumeric on-the-fly (OTF) processor to the corresponding cache (refresh) memory. Every character in the cache memory is displayed on the CRT monitor.

2.2.4 AFSS Software.- The AFSS software (see section 3.3 for detailed information) has two categories: the communication processor software and the position processor software. The communications processor software performs the following four functions:

1) communications with the FSDPS,

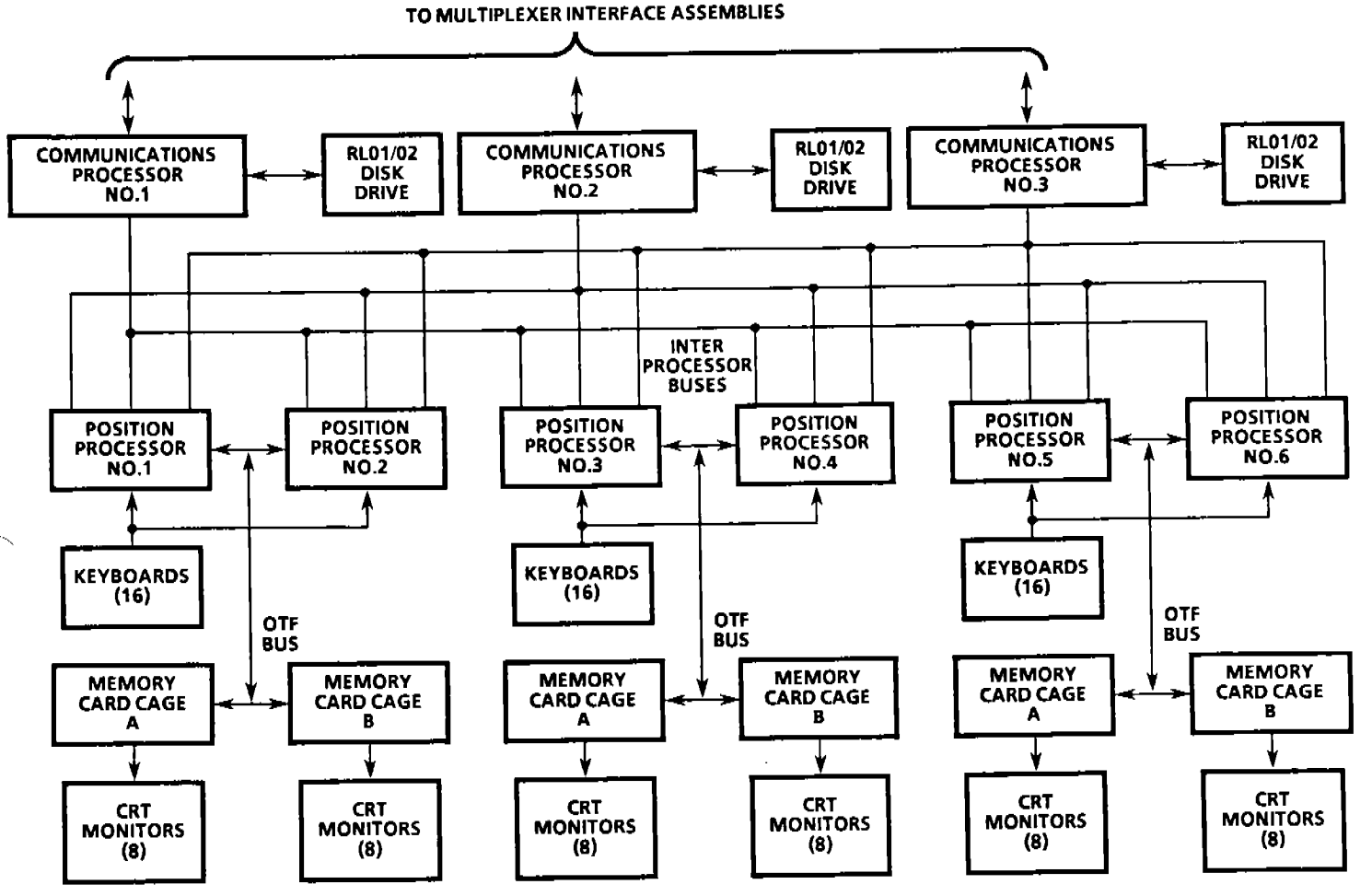
2) interprocessor control between the communications and position processors,

3) executive control including routing of transactions and failure detection and recovery, and

4) printer control.

The position processor software performs the following five functions:

1) receiving of characters from the keyboard and displaying characters on the monitor. This function includes the normal edit support functions of data entering (e.g., line insert, line delete, and character manipulation);



DS8814-73*
2-21-89 MB

Figure 2-6. AFSS Communications Processors and Position Processors

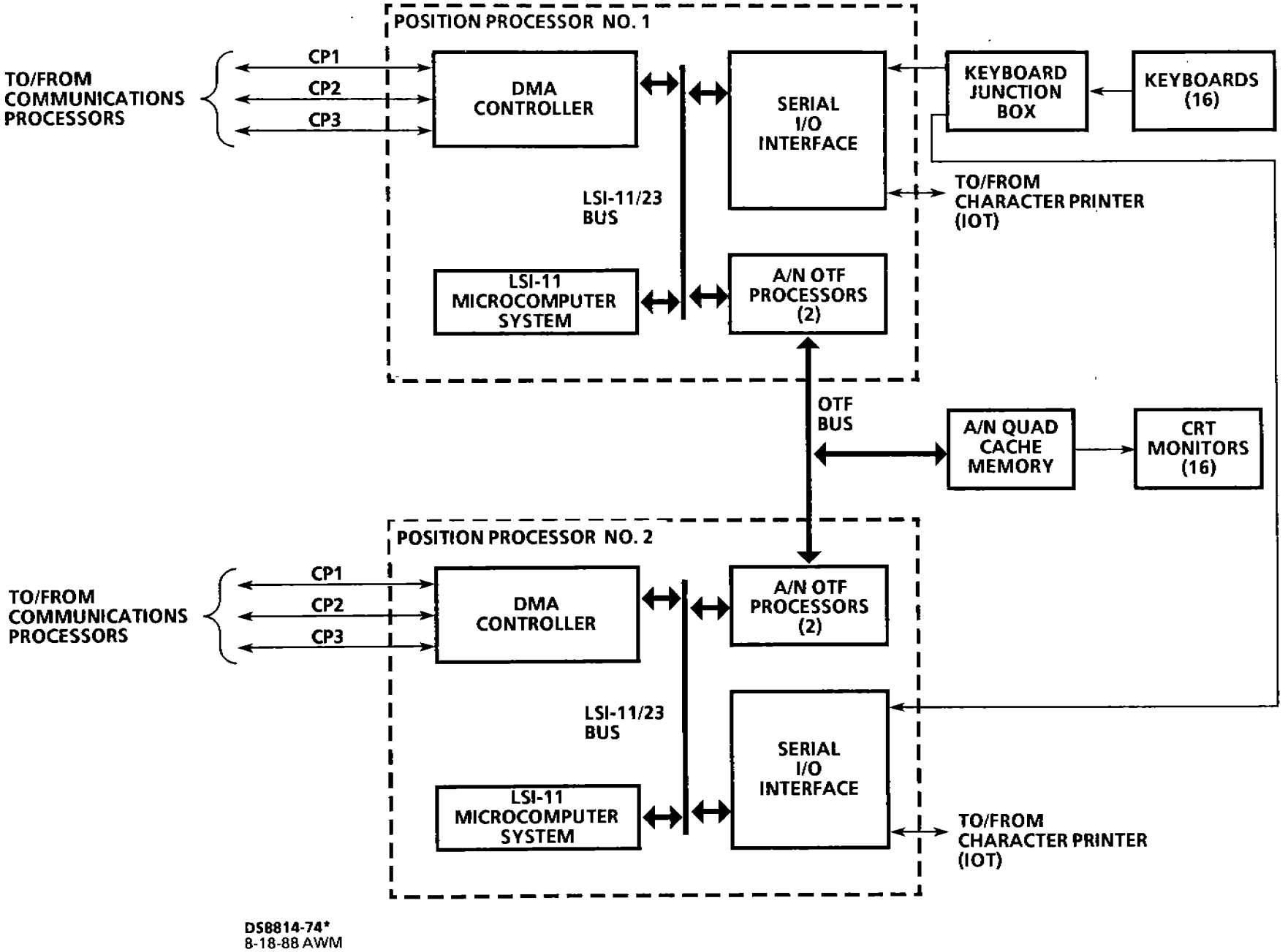


Figure 2-7. AFSS Position Processor

2) recognizing an enter command from a keyboard and routing the request to the communications processor for relay to the FSDPS;

3) receiving a response (to a terminal enter) from the communications processor and displaying the response on the CRT monitor;

4) receiving unsolicited data for display on a CRT monitor; and

5) executive control.

To support the programmable logic necessary to exercise the AFSS hardware, the software is provided in two units, each of which runs under the DFX-11 executive. The software consists of operational software and maintenance software. The operational software provides the message routing at an AFSS necessary to forward specialists' requests to the FSDPS and display responses from the FSDPS on the specialists' terminals. Software is also required to accept data from the FSDPS to be printed on one of the two line printers at the AFSS. In addition to its support of the operational requirements at an AFSS, the operational software supports the maintenance software testing.

The maintenance software resides in the AFSS software configuration as a low priority task concurrently with the operational software. Maintenance software test functions are available upon request to test the various AFSS hardware components. Requests for maintenance software initiation may be invoked from either the COTC at FSDPS or the COTC at AFSS.

Tests available at the AFSS include the following:

1) CPU - A test for CPU operability may be initiated either remotely (FSDPS) or locally (IOT) to check either the communications or position processor;

2) Memory - A test of both PROM and RAM may be initiated either remotely or locally to check either the communications processor or position processor memory;

3) MUX - A test that verifies operability of each of the four channels of the MUX interface may be initiated locally;

4) DMA Interface - A test that checks the operation of the DMA interface between the communications processor and position processor may be initiated either remotely or locally.

5) IOT - A test that verifies IOT operation at the AFSS may be initiated locally;

6) Line Printer - A test that verifies line printer operation may be initiated locally;

7) Disk - A test that verifies disk controller and disk driver operation may be initiated either remotely or locally; and

8) Keyboard/Display - A test that verifies the interaction between and operation of the keyboard and alphanumeric display may be initiated locally.

Details concerning each of these tests and their interactions are discussed in section 3.3.2, AFSS Maintenance Software.

2.2.4.1 DFX-11.- The DFX Executive is a collection of services which controls the dynamic state of the system and is interfaced to the system by the "nucleus." The nucleus consists of basic system services and procedures. A complete system consists of the DFX-11 nucleus plus all other software including: I/O drivers, operator controls, and applications tasks.

The executive administers to both static and dynamic representations of applications software. The static representation of applications software is a program and consists of machine language instructions coded according to standard reentrant techniques. As always the case with a reentrant program, one or more separate data areas are required for run-time.

The dynamic representation of applications software is called a task and consists of those run-time data areas needed by a reentrant program plus the control blocks needed by the executive management of task states.

These program and task concepts enable two features of system software applications: the ability to contain all software in read only memory, and the ability to share the same physical program code among any number of tasks.

DFX-11 consists of three independent sections:

1) system initialization control,
2) task dispatcher, and
3) service routines.

2.2.4.1.1 System Initialization Control.- System initialization may begin at any time by entry of the executive through a global entry point. This entry does not result in a system reset or a change in processor priority.

For purposes of M1FC FSAS application, initialization processing is performed as a result of a system boot. The following processing steps are performed as a function of initialization processing:

1) memory is tested and sized,

2) common is established and cleared,

3) task control blocks are established,

4) queue terminals are established,

5) task control lists used by the task dispatchers are established,

6) applications tasks are allowed to perform their initialization processing, and

7) the task dispatcher is invoked to begin system processing.

2.2.4.1.2 Task Dispatcher.- The task dispatcher is a module responsible for the assignment of system controls on a priority basis. At each system event, the task dispatcher checks to see if the currently running task still has the highest priority. If another task of higher priority has become feasible, then the task dispatcher gives it control, after saving the state of the current task.

2.2.4.1.3 Service Routines.- Six categories of service routines are used to support and manage executive processing. Each of these routine service categories is listed below with a brief functional description.

1) Program Management - Any number of programs may be present in an operational system. The existence of each program must be declared to the executive by a service call. As each program is declared, the executive incrementally builds a directory. In DFX, each program directory is called a Program Control Block (PCB). The program management service allows a PCB to be created for each program in the system.

2) Task Management - Any number of tasks may be established from the base of programs present in an operational system. To establish these tasks a definitive complex of data structures must be created; its interface to other tasks, a stack to be used by the task, and one or more workspaces to be used by the task. Task management services provide for data structure establishment. In addition, services are available to manage suspension and resumption of tasks, task status monitoring, and context switching between tasks.

3) Synchronization Management - The synchronization of tasks with each other and with external events is accomplished with a single mechanism called a semaphore. This is a flag that tracks various operations performed in task synchronization. Any number of semaphores may exist in the system, and may be used by applications tasks and executive services.

   Semaphores may be used to provide the following schemes for synchronization:

   a) resource allocation,
   b) mutual exclusion, and
   c) synchronization.

4) Communications Management - Tasks running under DFX may communicate with each other via either of two methods: global common or queueing of data buffers. Global common provides for the sharing of a data area in dynamic memory by multiple tasks, and may be regulated by semaphores in the mutual exclusion scheme. The queueing of buffers provides inter-task communication via buffers of data that are queued from task to task. Using this technique, each task may have one or more queue terminals via which data may be received. The DFX-11 Communications Management Services establish and manage the structures used to define the queue terminals. Applications tasks use two structures to pass buffer and task related data. A work request buffer (WRB) queues the buffer between two nondriver applications tasks or between applications and driver tasks that do not require queueing to the hardware device. Input/Output Blocks (IOB) interface applications tasks to device drivers that may require a queueing mechanism between the applications task and the driver. The IOB is managed by a task called Input/Output Control (IOC). Its function is to provide the queueing mechanism between the applications task and the driver.

5) Memory Management - Various memory management services are provided under DFX including: buffer allocate and deallocate, workspace and management, memory clear services, and buffer sizing.

6) List Management - DFX-11 manages task execution and controls the state of the system via the manipulation list structures. Each list is composed of tasks in similar states. The following lists are typical of those managed by DFX:

   a) The program list allows the executive to maintain control over allocated program control blocks.

   b) The feasible list is a list of tasks that are in a ready-to-run state waiting for CPU resources.

   c) The suspended list is for tasks waiting for resumption via a service call.

   d) The message list is a list of queue terminals in the system.

2.2.5. AFSS Operational Characteristics.- The AFSS system performs four basic data flows:

1) keyboard echo,
2) transmittal of requests from a keyboard to the FSDPS,
3) receipt of responses from the FSDPS for display on a monitor, and
4) receipt of data from the FSDPS for printing

Keyboard echoes are performed solely within the position processor. Keyboard characters are classified into three categories: normal, edit, and enter keys. Normal characters include the alphanumeric and special character set that are received from the keyboard and displayed on the appropriate monitor. No other actions are required. This processing entails:

1) reading a character from the keyboard controller, and identifying the position with which it is associated;

2) changing the cache identifier of the OTF controller to point to the correct position; and

3) writing the character to the OTF controller (which automatically places it in the correct cache).

Transmittals of requests are initiated when the position processor detects the ENTER character key. The position processor reads the data currently stored in the position's cache and sends it to the communications processor. The communications processor then forwards the request to the FSDPS.

Responses received from the FSDPS may be destined to a position or to a printer. If the destination is a position, the data is transferred to the position processor which writes the data to the cache. If the destination is the printer, the communications processor holds the data and writes it to the printer.

2.2.6. AWP Hardware- The hardware elements of a M1FC AWP consist of processing equipment, communications equipment (supporting the operational system), position equipment, and maintenance equipment for diagnostic support of the AWP. The elements of an AWP are shown in figure 2-8.

The processing equipment includes four Tandem CPUs and all the I/O controllers and peripherals connected to the Tandem system. The communications group consists of patch panels and modems necessary to complete the communication links to Service B, WMSC, the AWP position equipment, and the FSDPSs. The position equipment includes AFSS-type equipment to control 12 positions. The maintenance equipment consists of Tandem diagnostic hardware and special tools necessary to diagnose and repair the equipment.

2.2.7. AWP Software- The M1FC AWP software consists of the following three functional categories:

1) operational software
2) support software, and
3) maintenance software.

The AWP operational software provides the M1FC FSAS interface to WMSC for receipt and distribution of weather and NOTAM data. This software also provides the M1FC FSAS interface to Service B for receipt and distribution of general Service B data (law enforcement messages, ATCCC messages, military training routes, etc.). This software also supports the editing functions necessary to identify and correct improperly formatted reports. The operational software at each AWP provides the capability to support the entire National Data Base in the event only one AWP is operational.

The AWP support software, executed from the Operations and Service Processor (OSP) terminal or from the Tandem terminal connected via the asynchronous controller, prepares data for the AWP operational software, provides support for the development of the operational software, and prepares administrative reports for the AWP. This support software is not initiated from the specialists' operational terminals. It is the type of software traditionally satisfied by the batch type of processing.

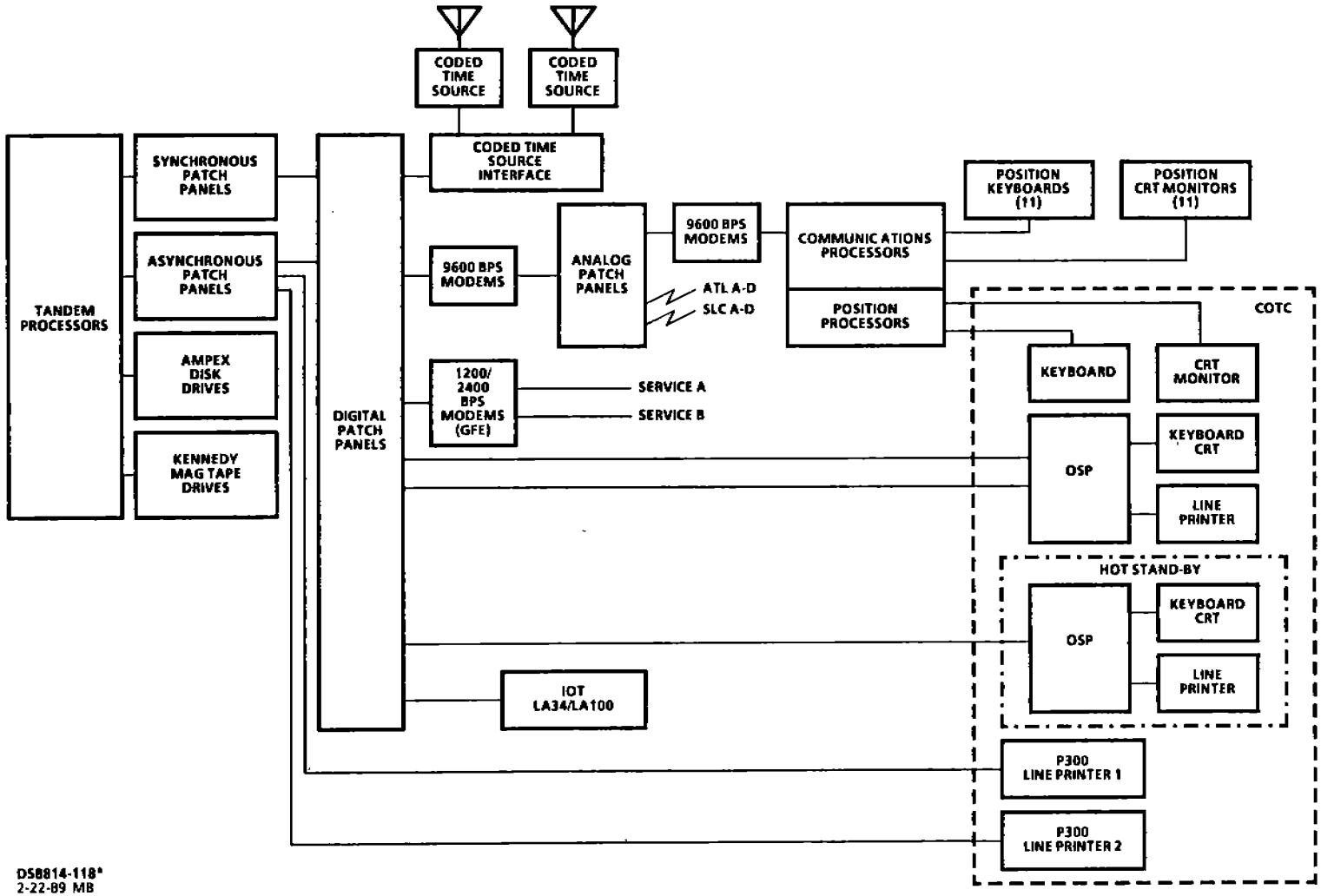


Figure 2-8. AWP Elements

The AWP maintenance software assists maintenance personnel in isolating failures to replaceable hardware elements.

2.2.8. AWP Operational Characteristics- The AWP performs the following operational functions within the M1FC FSAS:

1) Automatically accepts and stores meteorological data and NOTAMS from the WMSC;

2) automatically accepts and stores law enforcement messages, ATCCC messages, special use airspace messages, and other general Service B messages;

3) accepts and processes data base edit requests from the AWP specialists;

4) distributes messages received from WMSC and Service B to the FSDPSs to maintain a National FSAS Data Base;

5) supports FSDPS data base recovery after an FSDPS outage; and

6) provides support to the entire set of FSDPSs if one of the AWPs is out of service.

2.3 DETAILED THEORY OF OPERATION.- The following paragraphs describe the FSDPS, AFSS, and AWP in detail including: processing equipment, communications equipment, peripherals, and power distribution. Included is a description of the FSDPS maintenance equipment. Figures 2-9, 2-10, and 2-11 show configurations of an FSDPS, AFSS, and AWP, respectively.

2.3.1 Flight Service Data Processing System (FSDPS).- Each FSDPS consists of four Tandem processor subsystems, each with its own pair of disk drives/controllers and the COTC communications and position processors. Each Tandem processor has access to communication line controllers, COTC processors, CTS, SMMC, magnetic tape drives, line printers and backup paths to the disks of the other processors.

2.3.1.1 Processing Equipment.- The following sections provide detailed technical data on all elements in the processing subsystem. The processing subsystem is divided into five major areas:

1) processors (Tandem Non Stop II, OSP, COTC processors),
2) I/O controllers,
3) communications channels,
4) peripherals, and
5) DC power distribution

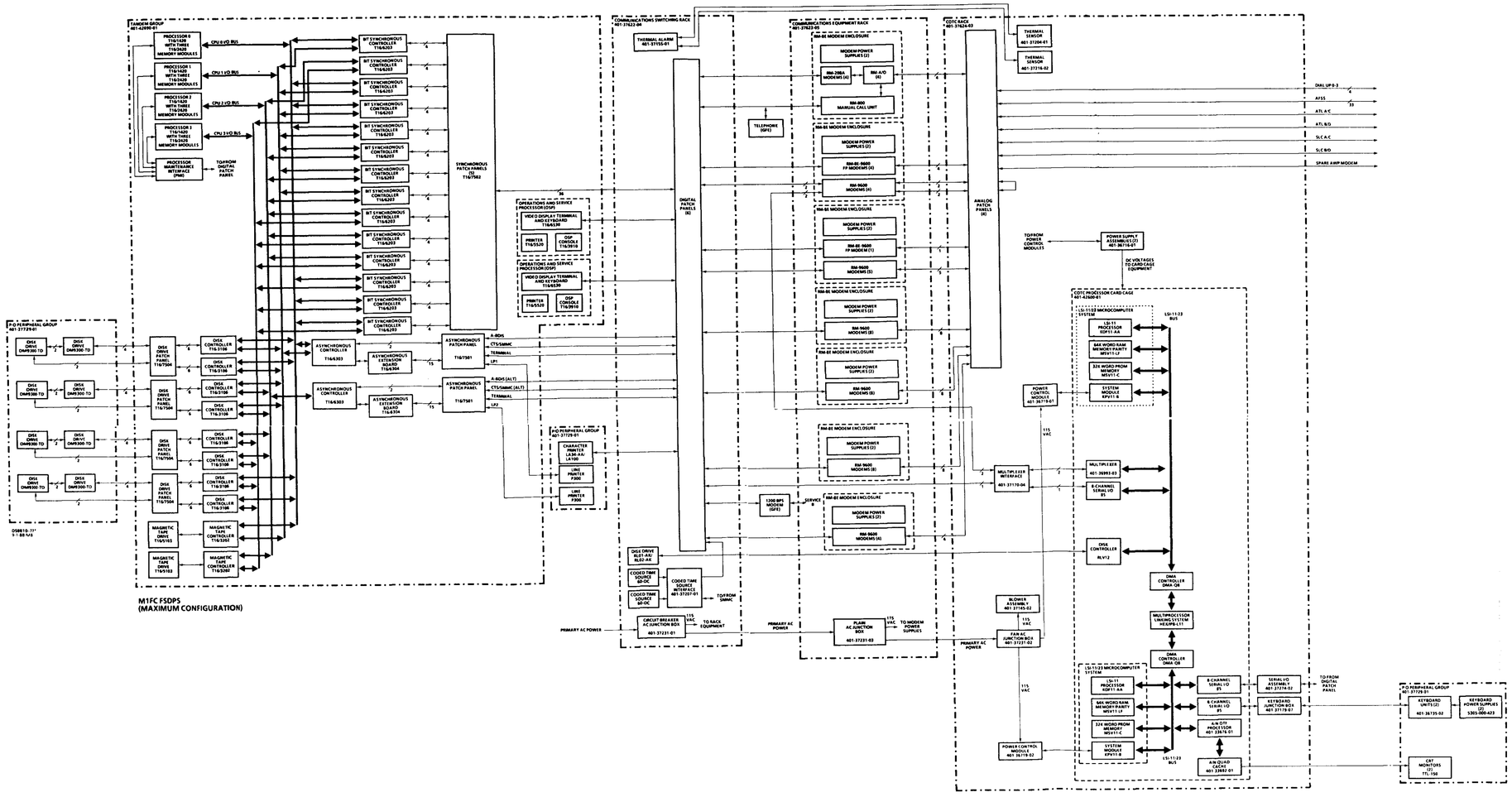


Figure 2-9. FSDPS Configuration

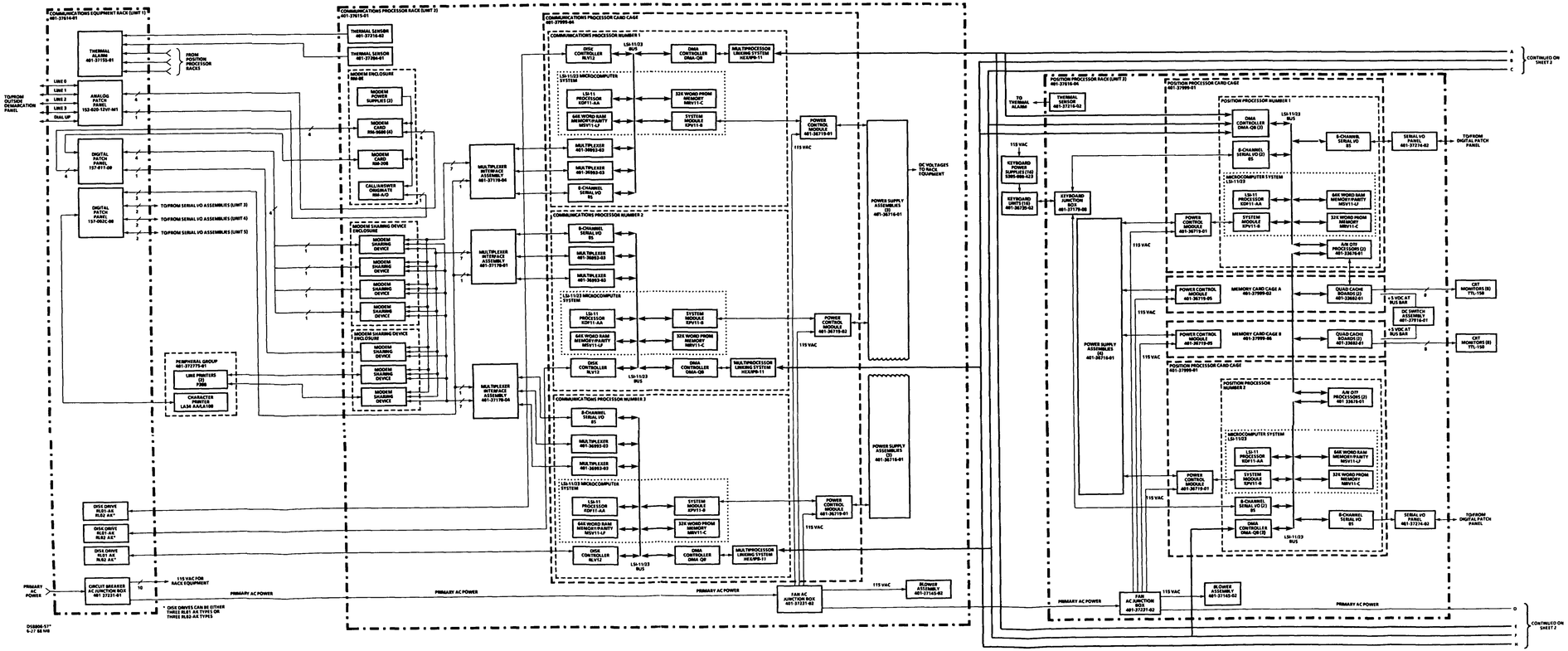


Figure 2-10. AFSS Configuration (Sheet 1 of 2)

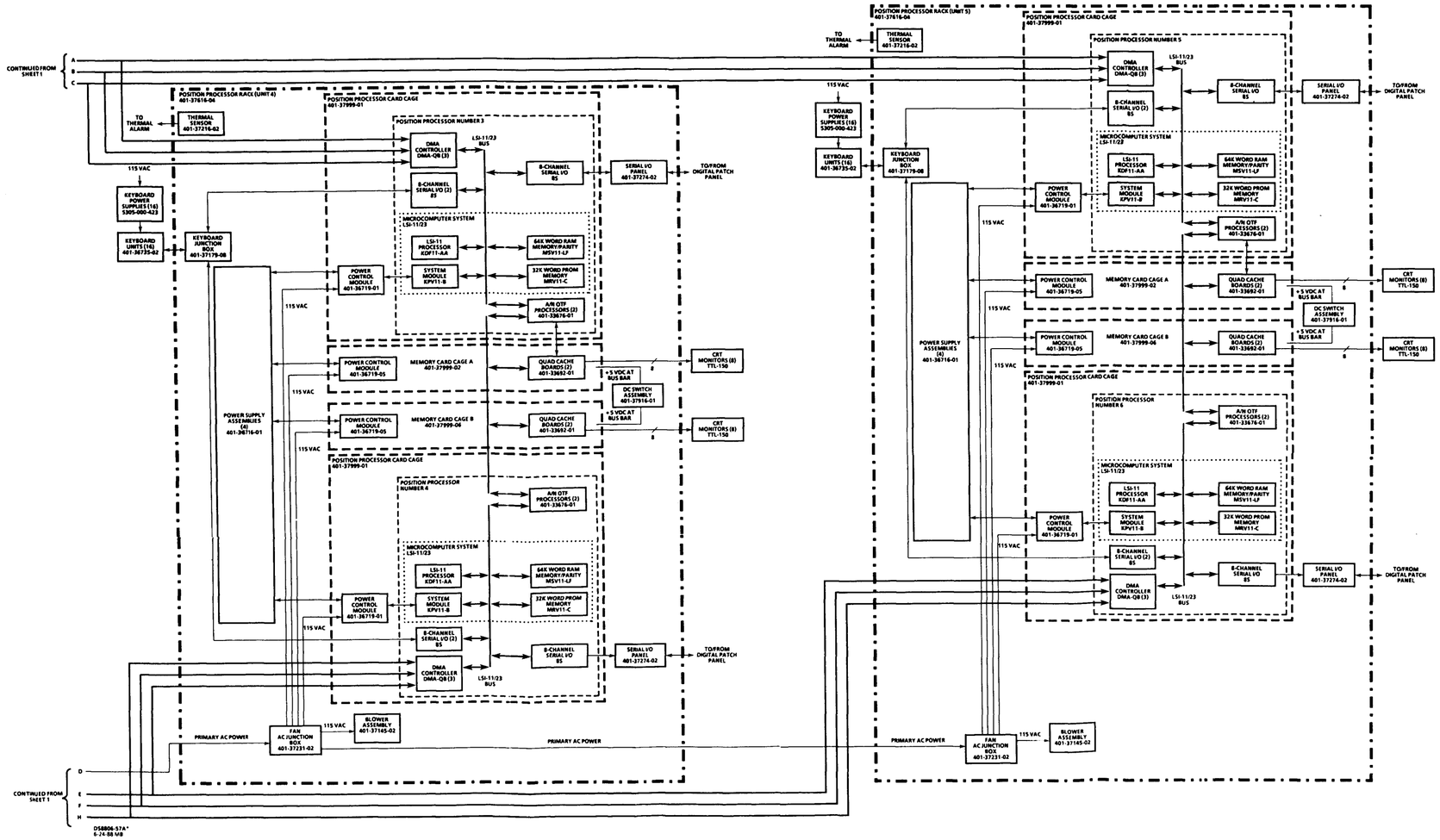


Figure 2-10. AFSS Configuration (Sheet 2 of 2)

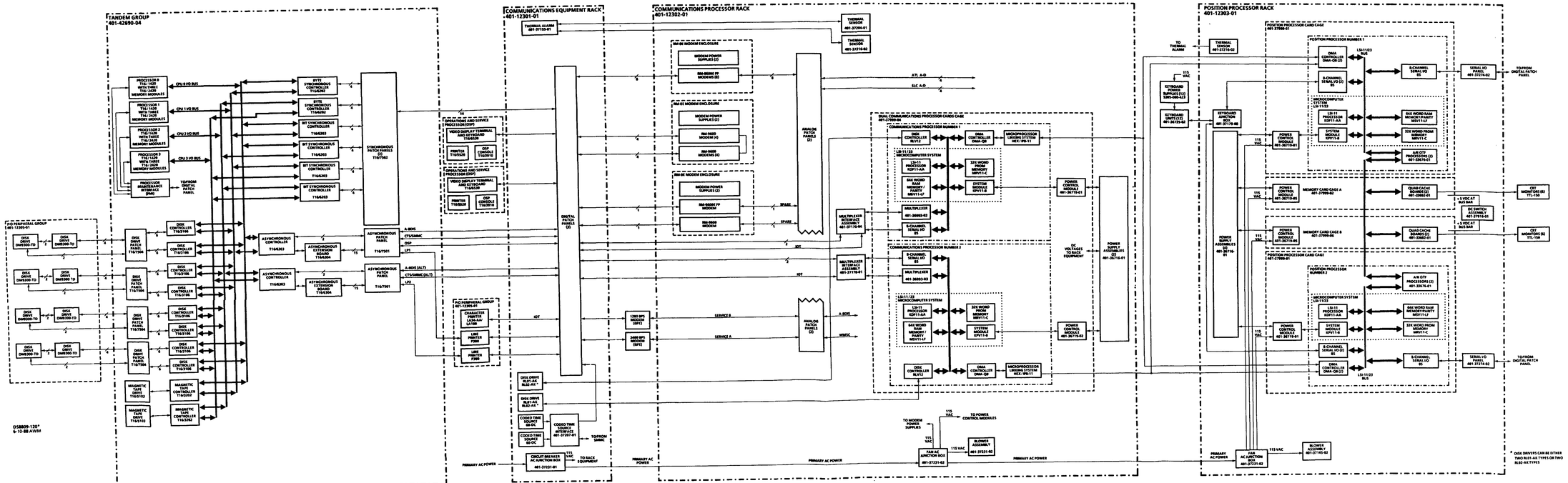


Figure 2-11. AWP Configuration

All segments of the processing subsystem except the communications channels stand alone and require no external interfacing other than AC power.

2.3.1.1.1 Tandem Non Stop II Processors.- The Tandem Non Stop II processor subsystem and functional description is organized as follows. See figure 2-12.

1) Instruction Processing Unit (IPU)
This board includes the hardware for register files, ALU shifter, microprocessor address register, instruction register, and instruction decoding. (The IPU functions as the CPU of the processor subsystem.)

2) Memory Control Board (MCB)
This board includes the hardware for memory request control, address translation map, memory ECC, address trap comparator, refresh timer, processor clock, interprocessor bus control, and interval timer.

3) Channel, Control Store, DDT (CCD)
This board includes hardware for the I/O channel, control store array, and diagnostic data transceiver.

4) Memory (Semiconductor)
This board includes the 256K x 22 (16 rows with 22 16K RAMs in each row) dynamic RAM array, drivers, and timing control.

5) Control Panel
The control panel contains panel switches, LED interfaces, and software licensing hardware.

NOTE

Subsystems 1) through 4) are mounted in their respective slots in the processor card cage of the processor cabinet. The control panel is mounted on the front door of the processor cabinet.

2.3.1.1.1.1 Instruction Processing Unit (IPU).- The Instruction Processing Unit (IPU) is the principal control unit for the processor. Controlled by a microprogram resident in the control store, the IPU communicates with the I/O channel, the memory control, the diagnostic data transceiver, the test panel (depot level use only), and the interprocessor bus. The IPU can read or write selected words of the control store under microprogram control. Through the memory control, the IPU communicates with software residing in main memory, fetching, interpreting, and executing instructions. See figure 2-13.

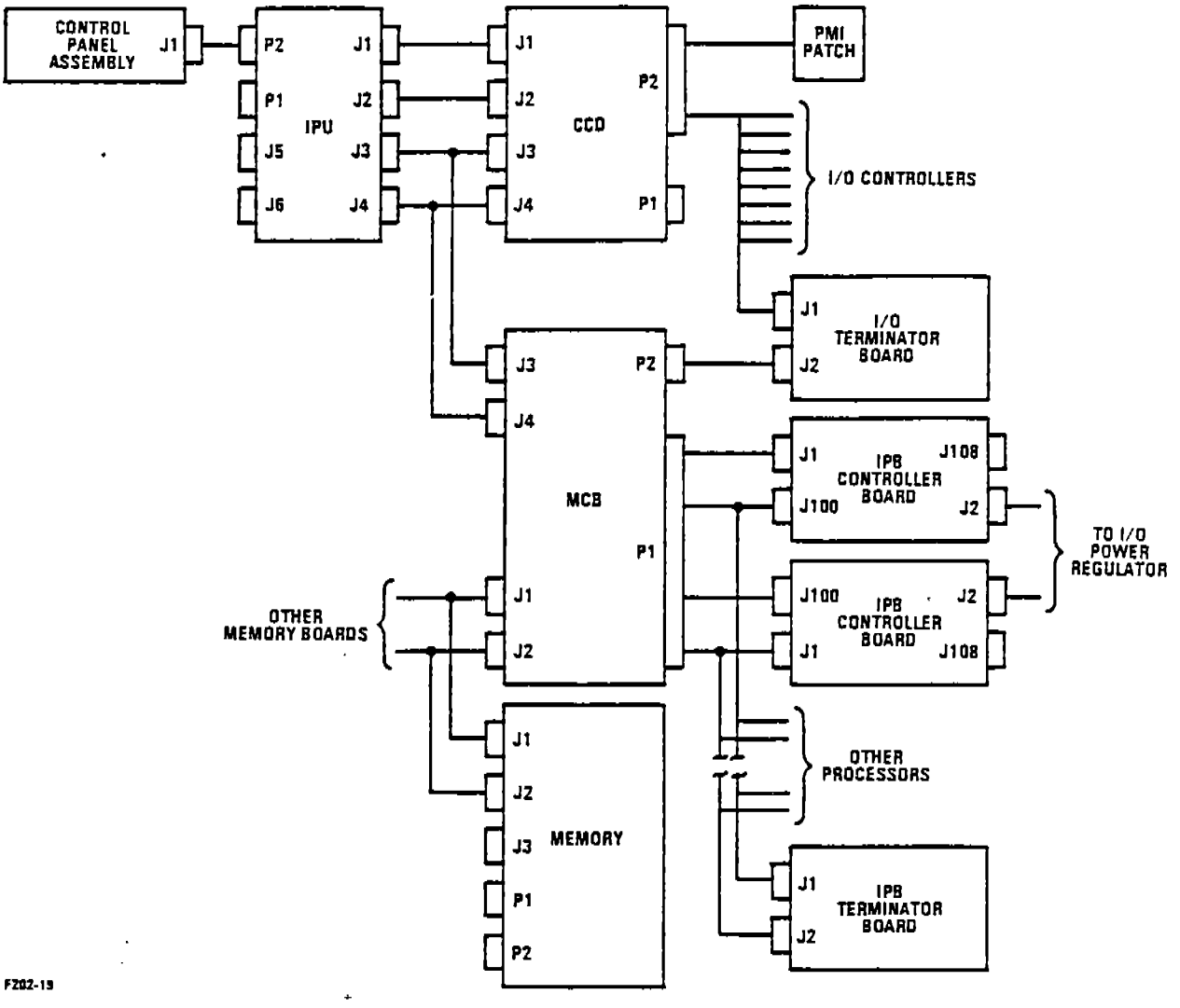


Figure 2-12. Tandem Processing Equipment

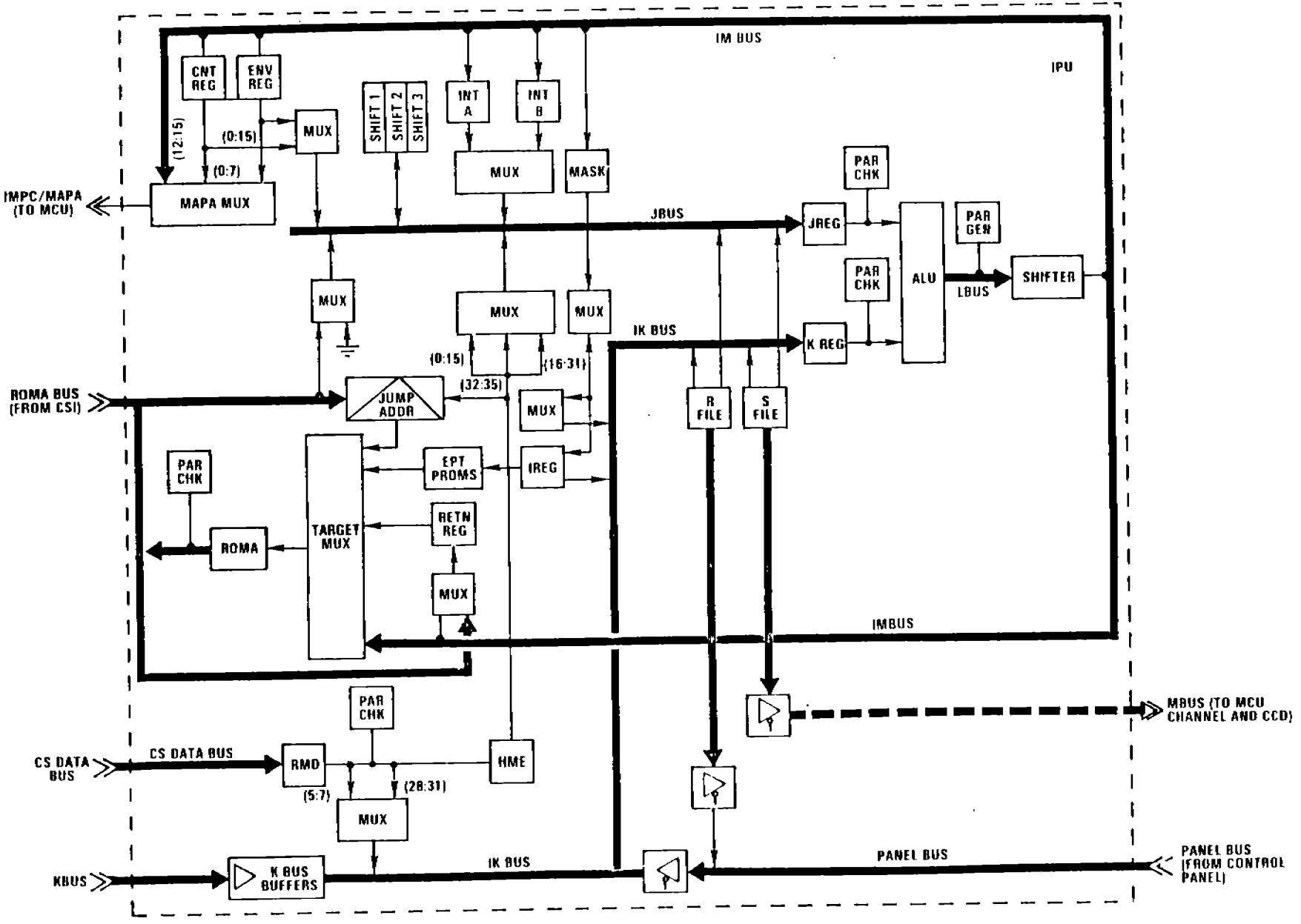


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Figure 2-13. IPU Functional Block Diagram

2.3.1.1.1.2 Internal and External Buses.- The internal and external buses of the IPU are listed in table 2-1. Refer to table 2-2 for a listing of the microprogram sequencer components and their function.

2.3.1.1.1.3 I/O Channel (Channel).- The channel allows I/O controllers on the IOBUS to communicate with the memory and with the IPU. The channel is a microprogrammed processor which functions as IOBUS controller, as a port into the memory control, and as an interface to the IPU. It can accept reconnect requests from device controllers on the IOBUS and requests for I/O service from the IPU. These requests are accepted under microprogram control only since the channel is not interruptible; the channel, however, does have the ability to interrupt the IPU to make special requests for service or to report exceptional conditions. See figure 2-14 for the channel data paths.

The channel provides status information to the Diagnostic Data Transceiver to assist in diagnosis of failures.

2.3.1.1.1.4 Channel Structure.- The I/O channel is a bus-organized microprocessing unit. It consists of the control unit and a set of registers.

2.3.1.1.1.5 Buses.- The I/O channel communicates internally over the CBUS: with the memory control via the CBUS and the CMPAPA bus, with the IPU via the MBUS and KBUS, and with the I/O controllers via the IOBUS.

2.3.1.1.1.6 Memory Control (MCB).- The memory control provides access to memory for both the channel and the IPU. It arbitrates memory requests; pipelines address, data control and error information; maps logical addresses into physical addresses; provides error checking and correction on data transfers from memory, and controls the timing of refresh operations on semiconductor memory.

The memory mapping unit maps 20-bit logical addresses into 23-bit physical addresses.

Data (16-bit) are coded by the Memory Control in a 22-bit single-error- correcting, double-error-detecting code for storage in main memory. The MCU checks parity on data and addresses from the channel and from the IPU. Parity errors are reported to the IPU, the channel, and the Diagnostic Data Transceiver.

Table 2-1. Internal/External Buses

REGISTER	FUNCTION
J BUS	JBUS. 0:15,PL,PR,PV ,within the IPU only
IK BUS	IKBUS. 0:15,PL,PR,PV ,internal K bus
KBUS	KBUS. 0:15,PL,PR ,external K bus
L BUS	Alu output BUS. 0:15 ,within the IPU only
IM BUS	Internal MBUS. 0:15,PL,PR,PV ,within the IPU only
M BUS	MBUS. 0:15,PL,PR,PV ,only drives loads external to the IPU.
ROMA BUS	ROM address bus to control store, ROMA. 0:15
MAPA BUS	Map address bus to memory control unit MAPA. 0:3
P BUS	Low asserting bidirectional bus between the control panel and IPU, PBUS. 0:15

Table 2-2. Microprogram Sequencer

REGISTER	FUNCTION
ROMA	ROM address register/counter for micro instructions.
RMD	Rank 2 control store data register where J & K microop fields are decoded and executed.
RME	Rank 2 control store data register where the microinstruction is executed.

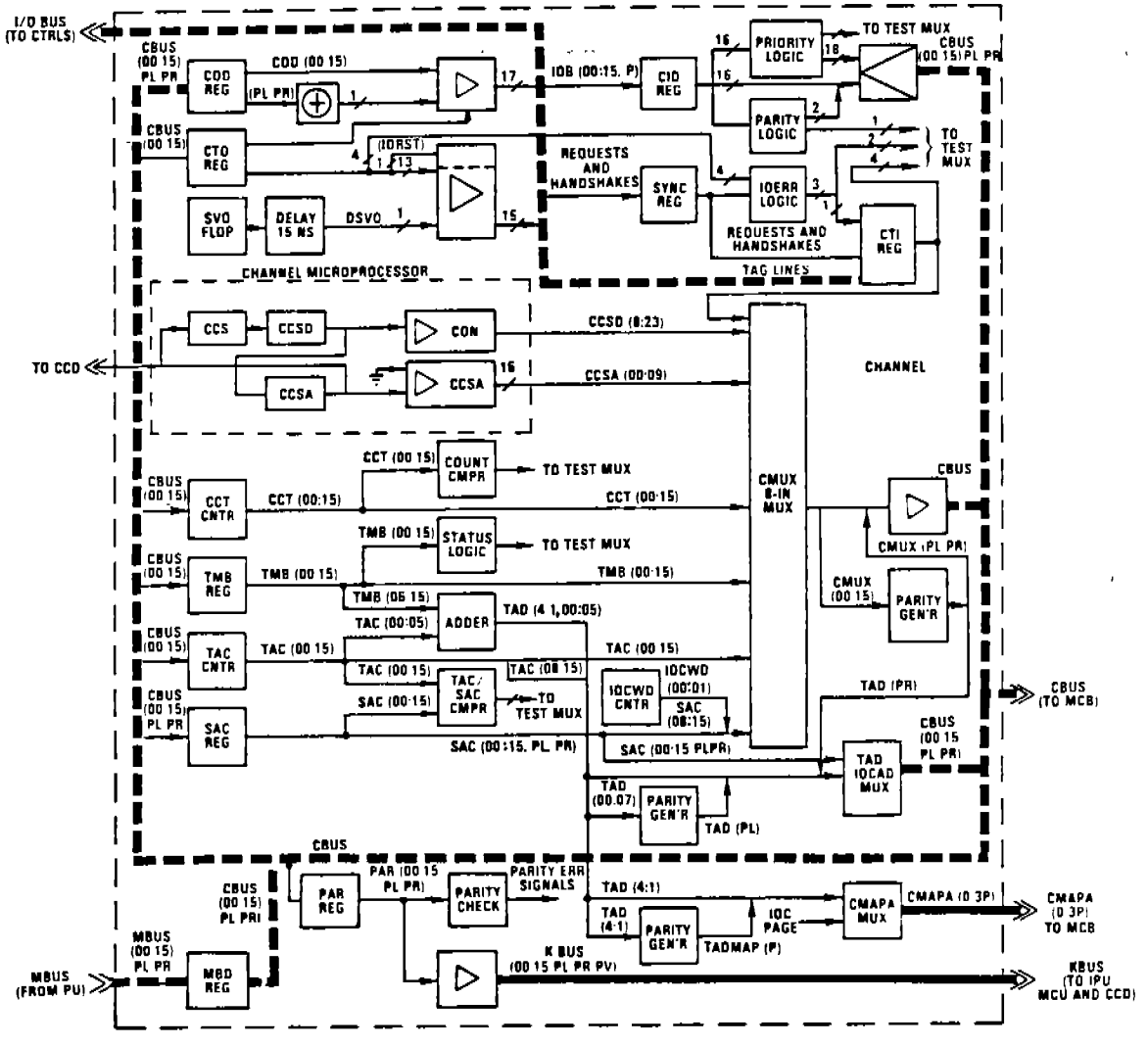

Figure 2-14. Channel Data Paths

2.3.1.1.1.7 Map/Memory Control.- The Map/Memory Control Unit (MCU), which resides on the MCB board, consists of MAP access hardware and Memory access hardware. The MAP machine arbitrates the Instruction Processing Unit (IPU) MAP requests for: MAP READS (MR), MAP WRITES (MW), PROCESSOR CODE READS (PCR), PROCESSOR DATA READS (PDR), and PROCESSOR DATA WRITES (PDW); and Channel MAP requests for CHANNEL READS (CR) and CHANNEL WRITES (CW).

The memory machine arbitrates between MAP memory requests and REFRESH memory requests (made by a timer internal to the MCB). The memory machine also does single error correction (SEC), double error detection (DED) on read data, and single error detection (SED) on memory read address. Refer to figure 2-15 for the Memory Control Unit data paths.

2.3.1.1.1.8 Interprocessor Bus (IPB) Control.- The IPB control, which also resides on the MCB board, handles the sending and receiving of packets over the two interprocessor buses (X bus and Y bus). The IPB provides separate input and output buffers for each bus and is capable of sending and receiving over the X bus and the Y bus simultaneously. See figure 2-16 for the IPB Control data paths.

2.3.1.1.1.9 Control Store (CS).- The Control Store (CS), located on the CCD board, is the storage element for the microprogram executed by the IPU. Most of the CS is Writable Control Store (WCS). It is 36 bits wide: 32 data bits and 4 data parity bits. The maximum address space is 16K. CS address parity checking is done on ROMA. 0:15. The data path is shown in figure 2-17.

2.3.1.1.1.10 Diagnostic Data Transceiver (DDT).- The Diagnostic Data Transceiver (DDT) resides on the CCD board and provides communication between the processor and the rest of the system through the PMI patch panel, which in turn provides communication with a local or remote operator through an Operations and Service Processor (OSP). The DDT permits the operator to examine processor status information which gives indication of hardware failures. It also provides two-way communication between the microprogram and the operator for system software debugging. If appropriately enabled, the DDT permits the operator to reset and cold load the processor, and permits one processor in the system to suspend the operation of other processors (under microprogram and software control). See figure 2-18 for the DDT data paths.

2.3.1.1.1.11 Memory (MEM).- Main memory is organized in 256K word modules. Up to eight Mword addressability is provided. MOS dynamic RAM technology is used, with an uninterruptible (battery) power supply to ensure memory integrity in the event of power interruptions. (Core memory is not available in a Non Stop II processor.) See figure 2-19 for memory data paths.

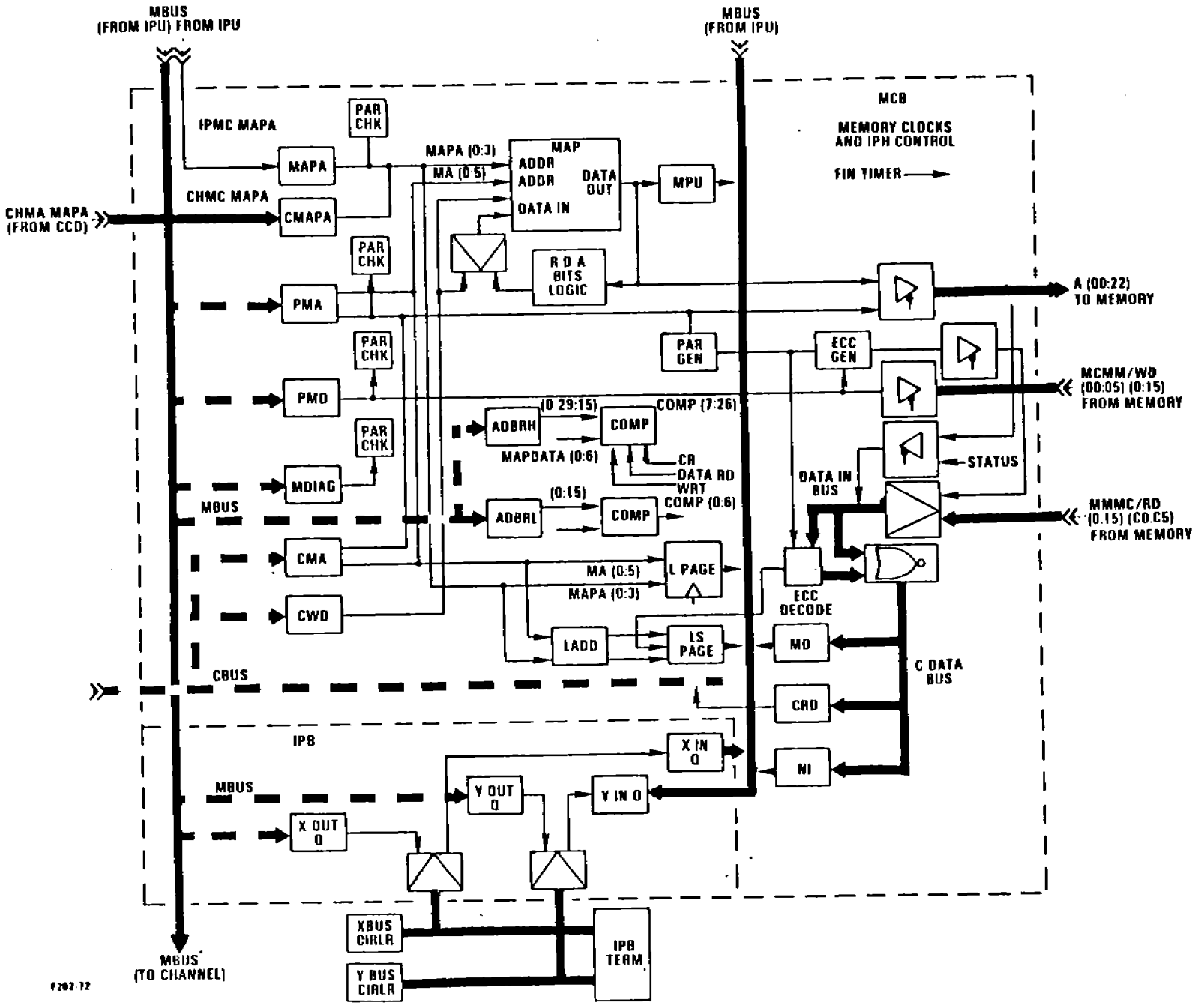

Figure 2-15. Memory Control Unit Data Paths

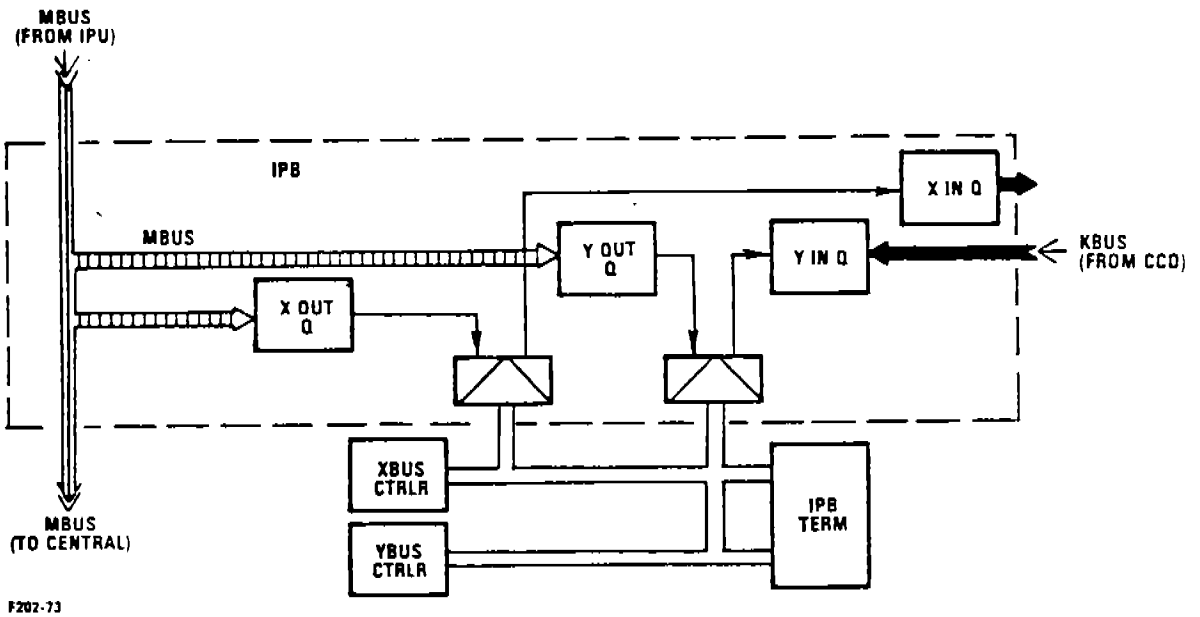

Figure 2-16. IPB Control Data Paths

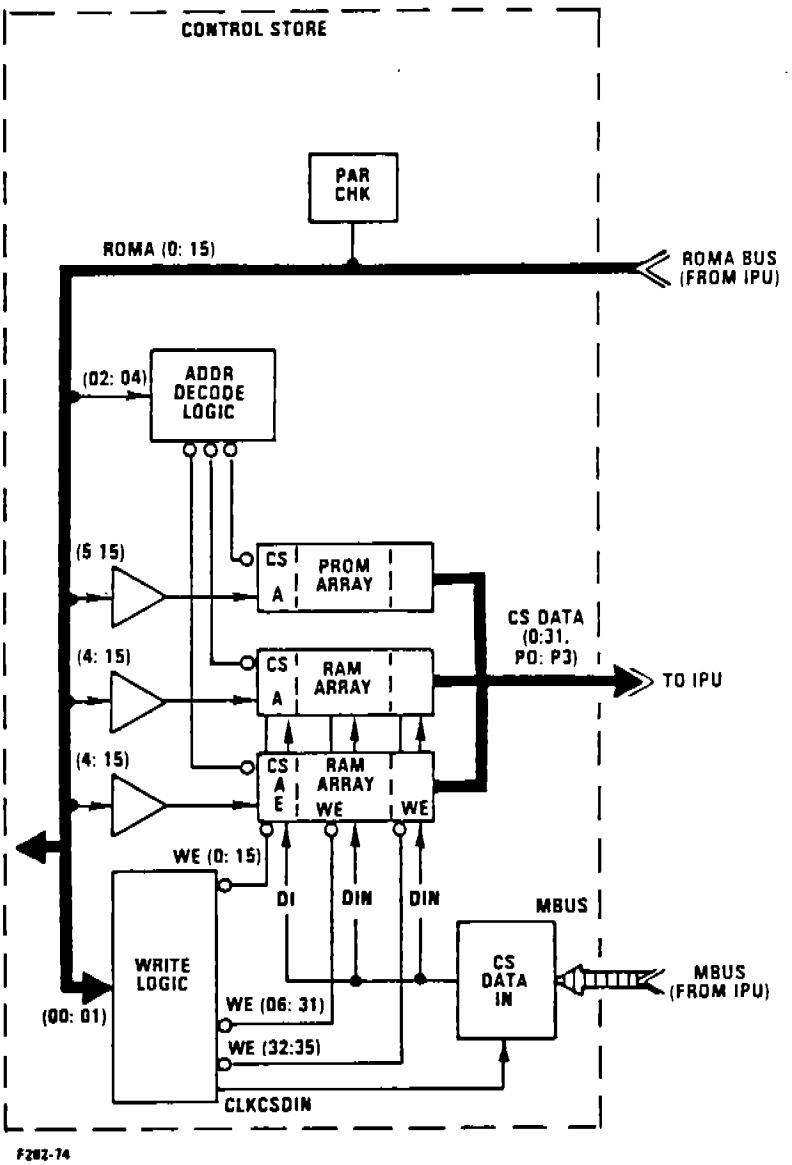

Figure 2-17. Control Store Data Path

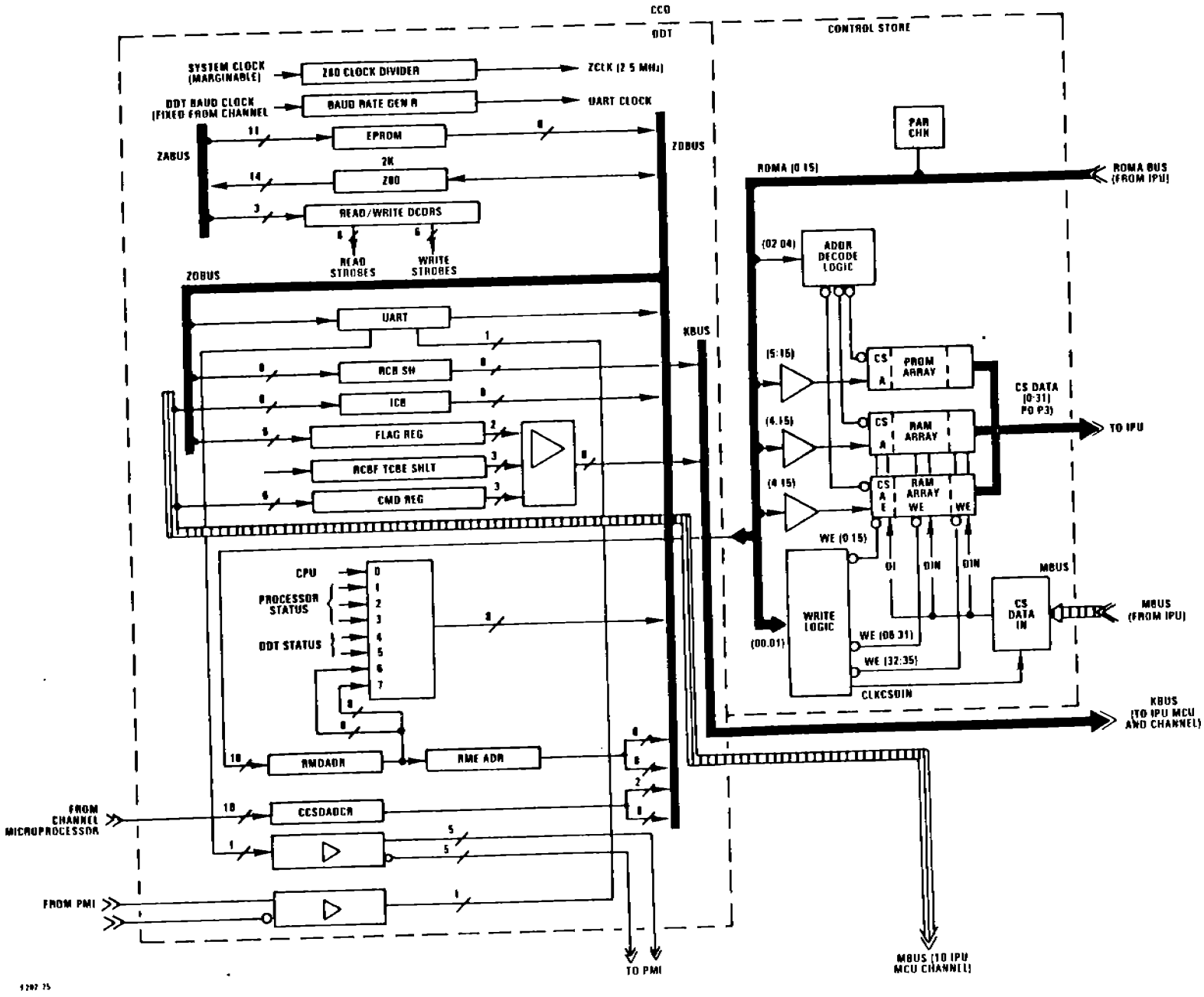

Figure 2-18. DDT Data Paths

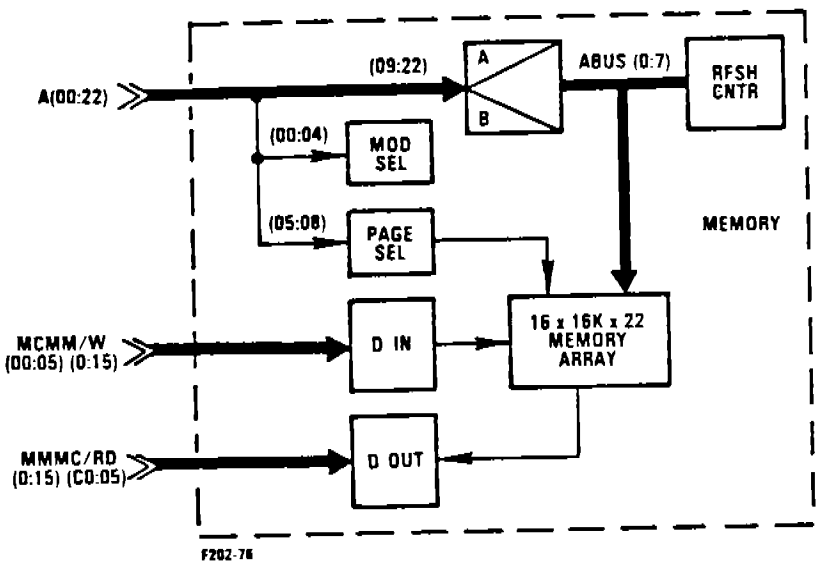

Figure 2-19. Memory Data Paths

2.3.1.1.1.12 Control Panel.- The control panel is an interface between an operator and the Non Stop II CPU. It enables an operator to reset and cold load a processor, and run some processor microdiagnostics. See figure 2-20.

The Non Stop II control panel contains the following:

1) a bank of sixteen yellow LEDs for data output,
2) a bank of sixteen toggle switches for data input,
3) a Reset/Load switch (activated by the cabinet door key),
4) a green Power LED,
5) a green Run LED, and
6) a Power Warn/Halt switch (inside door).

2.3.1.1.2 OSP.- The Operations and Service Processor (OSP) is a dedicated programmable debugging and maintenance tool which provides the operator interface to each processor in a Tandem Non Stop II System with the following:

1) local access to GUARDIAN through the Command Interpreter or LOBUG program via T16/6520 Video Display Unit (OSP-VDU);

2) local access to the SHADOW diagnostic Operating System via OSP-VDU;

3) remote access to GUARDIAN through the Command Interpreter or LOBUG program via modem;

4) remote access to the SHADOW diagnostic operating system via modem;

5) a central point for system cold loading, reloading, and running a machine room command interpreter;

6) a microcode interface for hardware interrogations; and

7) hardware status display.

NOTE

GUARDIAN need not be up for the OSP functions.

The OSP is controlled by an event-driven, multitask operating system capable of supporting a variable number of tasks, semaphore locking of system-wide resources, central disk, I/O memory management, and limited interprocess communication.

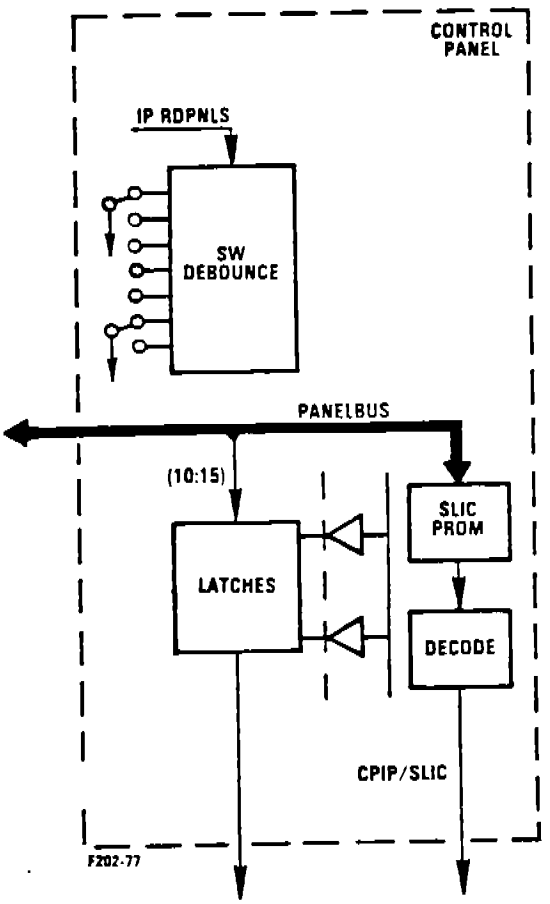

Figure 2-20. Control Panel Data Path

Access to the twelve operating modes is through the OSP-VDU. The OSP-VDU is used in both block and conversational modes. The shifted function keys each put the OSP into a different operating mode and invoke a different display page format. Within each operating mode, the unshifted function keys perform functions appropriate to that operating mode.

The OSP handles all system message functions and maintains a limited soft copy error log and a complete hard copy error log.

2.3.1.1.2.1 Physical Description.- The OSP consists of a T16/6530 Video Display Unit (OSP-VDU) and Printer, System Maintenance Processor (SMP) logic board assembly, two flexible (floppy) disk drives, two power supplies, a T16/5520 character printer, and operator console desk. The entire assembly (excluding the OSP-VDU and character printer) is housed in the operator console desk cabinet.

2.3.1.1.2.2 Console Desk.- The console desk is 53.00 inches long (134.62 cm), 29.00 inches high (73.66 cm), and 27.20 inches wide, with indicators on the front panel of the maintenance drawer. The console desk should not be located more than 20 feet (6.10 meters) from the first processor cabinet.

2.3.1.1.2.3 Front Panel.- Five indicators and five switches are on the front panel. Three of the indicators represent the power supply voltages and the remaining two indicate proper operation of the System Maintenance Processor (SMP). One of the five switches is for the AC power. The other four are selectable OSP functions. Tables 2-3 and 2-4 list the functions of these switches and indicators.

2.3.1.1.2.4 Maintenance Drawer.- Table 2-5 lists the maintenance drawer cable connections. The maintenance drawer is mounted on sliding rails in a rack behind the locked door on the lower right side of the console desk. It contains the System Maintenance Processor (SMP), disk drives, and power supplies. AC power and serial I/O cables are attached to the back panel.

2.3.1.1.2.5 System Maintenance Processor (SMP) Board.- The SMP board is clamped at the top of the maintenance drawer. It consists of a Z80A microprocessor, 64K Bytes of RAM, 4K Bytes of PROM, disk controller, five UARTs, interval timer, expansion interface and associated components on a printed circuit board (see the block diagram shown in figure 2-21).

The Z80A addresses 64K bytes of RAM and accesses the disk controller and serial ports as I/O devices. The Z80A operating code is loaded into RAM from the diskette.

Table 2-3. Front Panel Switches

SWITCH	FUNCTION
OSP AC POWER	Applies AC power to the OSP subsystem.
RESET	Resets SMP and initiates the self-test diagnostics and disk bootstrap operations.
LOCKED/ MAINTENANCE (keyswitch)	LOCKED position. The SMP functions as a conversational mode terminal with special status displayed on the 25th line. Remote and Diagnostic functions are disabled. MAINTENANCE position. Diagnostic and Remote functions are enabled. The key can be removed only in the LOCKED position.
REMOTE	Enables remote operation from a remote terminal or OSP via a modem.
DIAGNOSE	Enables the diagnostic functions of the OSP.

Table 2-4 Front Panel Indicators

INDICATOR	FUNCTION
LOGIC POWER (+5V, +12V, -12V	ON. Power supplies are operating properly.
RUN	ON. Microprocessor clocks are working and system is running.
TEST OK	ON. If the self-test is successful, remains on unless an internal error is detected.
	OFF. When the system is powered-up or reset or when the self-test diagnostics fail.

Table 2-5. Maintenance Drawer Cable Connections

CABLE ASSEMBLY NO.	FROM MAIN DRAWER	TO I/O DEVICE
24243	AC IN	AC POWER (115 VAC)
55523	J1	PMI (J2)
55520	J2	MODEM (J2)
55809	J3	OSP-VDU (J2) PRINTER (J1)

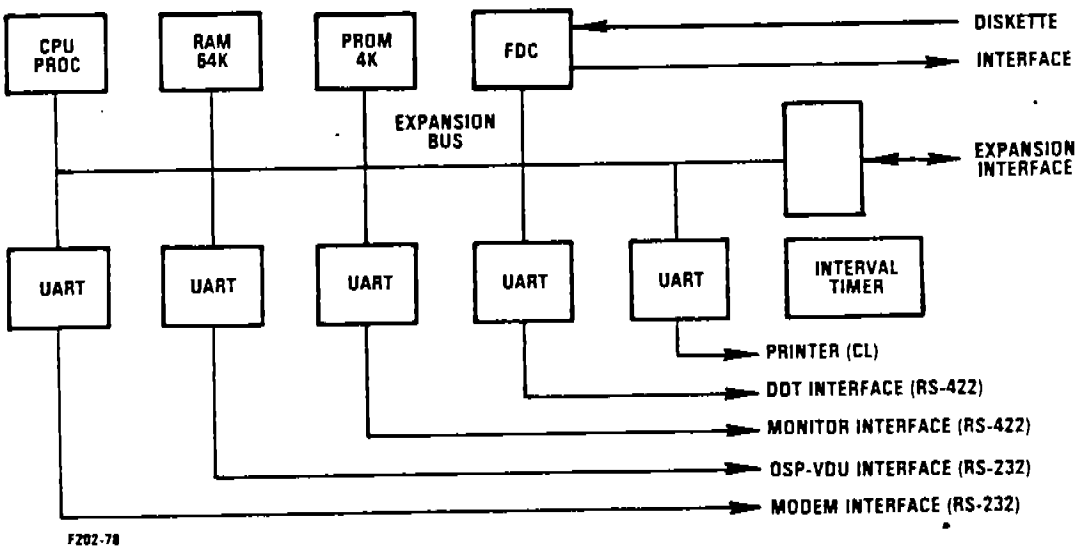

Figure 2-21. SMP Architecture

The PROM contains a resident code which is run on power-on and SMP resets. The resident code includes the following self checks of the system:

1) microprocessor self check,
2) test of all 64K of RAM,
3) checksum of the PROM,
4) soft loopback of serial I/O,
5) recalibrate and check drives for track 0,
6) boot system code from disk,
7) error reporting via indicators and OSP-VDU, and
8) RAM parity error interrupt handler and reporter.

If neither disk drive is ready, a message appears on the OSP-VDU directing the user to load the system diskette.

If self-checks are successful, the SMP OK indicator turns on and remains on. If errors are encountered, a warning message is displayed on the OSP-VDU and the SMP OK indicator turns off.

The five UARTs provide asynchronous serial ports for communicating with the OSP-VDU, PMI, OSP-line printer, and the future expansion interface.

The interval timer is used to produce ongoing output pulses. When a time-out occurs, the interval timer outputs one or more pulses which generate an interrupt to the Z80A.

2.3.1.1.2.6 Switches and Indicators.- Four LEDs (DS-F1 through DS-F4) on the SMP board display a four bit error code which identifies the malfunctions listed in table 2-6. DS-F1 is MSB and DS-F4 the LSB. When an LED is lit, it represents a one.

2.3.1.1.2.7 Disk Drives.- The 5-1/4-inch 100 TPI Flexible Disk Drive accepts a standard 5-1/4-inch diskette and rotates it at 300 RPM. A magnetic read/write head mounted to a detent assembly is positioned in contact with the surface of the diskette and effects recording and replay of data. A printed wiring assembly interfaces the control of the detent mechanism and the recording electronics to a standard TTL-compatible interface. Two drives are supplied with the OSP for backup if a drive fails.

The disk drive is mounted in a tray that facilitates access and mounting within the maintenance drawer.

2.3.1.1.2.8 Switches and Indicators.- Each disk drive has one red LED on the front to indicate drive select.

Table 2-6. SMP Four-Bit Error Codes

CODE	ERROR DESCRIPTION
0000	Improper execution of instructions.
0001	Checksum of first PROM failed.
0010	System control register not zero after reset.
0011	System Control word fails pattern test.
0100	Occurrence of unused interrupt (4).
0101	RAM parity generation circuitry failed to generate an interrupt.
0110	RAM parity detection circuitry failed to set parity error bit.
0111	Occurrence of unused interrupt (7).
1000	Parity error bit in the control word cannot be cleared.
1001	Terminal UART failed.
1010	No errors detected.

2.3.1.1.2.9 Power Requirements.- The disk drive power requirements are as follows:

Voltage	Standby	Average	Peak
+5	0.5A	0.5A	0.5A
+12	0.3A	1.0A	1.3A

Power is supplied to the drive on a 4-pin connector located on the solder side of the drive printed circuit board. The connector is an AMP Mate-N-Lok #350211-1; the mating connector is AMP 480424-0 using pins 61473-1 (loose). Refer to table 2-7.

Table 2-7. Power Connector Pin Assignment

PIN	CIRCUIT
1	+12 regulated
2	+12 return
3	+5 return
4	+5 regulated

2.3.1.1.2.10 Diskette.- The 5-1/4-inch double density flexible diskette is a removable diskette cartridge for use with the 5-1/4-inch diskette drive. The cartridge consists of a single oxide coated mylar disk contained in a vinyl jacket. The diskette has two holes punched in it. One hole is punched in the exact center and receives the mounting hub when the diskette is loaded into a drive. the other hole is punched off center and is used as an index timing marker. The jacket is lined with a treated fabric that helps keep the mylar surface clean. The jacket is constructed with cutouts which allow the recording head(s) to come into contact with the recording surface(s) and exposes the mounting and timing holes. Additional cutouts relieve mechanical stress during insertion and provide a means for write lockout.

The diskette is inserted into the disk transport mechanism which centers the media over a registration hub. When the access door is closed, the media is clamped to the hub and rotated at 300 RPM. A mechanical interlock prevents the door from being closed if the media is not correctly seated.

The operating system for the OSP and the diagnostic programs are on a single diskette.

2.3.1.1.2.11 Processor Maintenance Interface (PMI) Panel.- The PMI (Tandem Part No. 55530) is the converging point of all signals to the DDTs, control panel, and terminal. It contains enabling switches for system security, level converters for communicating with RS-232 type terminals, and indicators. The PMI is mounted on the processor bay patch panel behind the backplane. Processor connection to the PMI is with flat cables which plug into the back panel connector pins. A maximum of four CPUs may be connected to a single PMI. Multiple PMIs (refer to figure 2-22) in a system are daisy-chained together; the end of the chain leads from the processor cabinet to the OSP.

The OSP via the PMI sends commands and obtains status from the Diagnostic Data Transceiver (DDT) over an RS-422 serial link.

2.3.1.1.2.12 Diagnostic Data Transceiver (DDT)-PMI Interface.- The DDT resides on the CCD board of each processor. It provides communication between the OSP and the Instruction Processing Unit (IPU) of the processor. The OSP may be connected locally or through a modem. The PMI provides fan-out/fan-in between the DDTs of all processors in a system and the OSP or modem. Figure 2-23 shows the DDT-PMI Interface using differential (RS-422) pairs.

On the PMI, three switches per processor are provided to disable various DDT functions. One switch isolates from the OSP the serial communications lines which connect the DDT and the PMI, to prevent character transmission in either direction between processor and OSP. This permits use of the PMI and OSP even though one or more DDTs in the system may be responding improperly to commands from the OSP, or transmitting a steady stream of characters. This switch has no effect on character wraparound in the PMI.

A second switch inhibits RESETting and local HALTing of the processor, and the setting of the system halt request flag (PSHRQ) in the DDT on command from the DDT. It does not inhibit clearing of the system halt request flag from the OSP, nor does it keep software from HALTing the processor or requesting a system halt. This switch is used to permit the OSP to communicate with software in the processor without danger of accidentally crashing the processor or the system. The switch operates by controlling the state of the PMDT/ RSTEN line from the PMI to the DDT. The DDT microcode interprets assertion of this line, by convention only, as a signal that its microcode may use the RESET and HALT functions; negation of the line does not directly inhibit these functions in hardware.

A third switch disables system HALT for the processor. It disconnects both the system halt request line DTPM/SHRQ and the system halt line PMDT/SHLT from the other processors in the system.

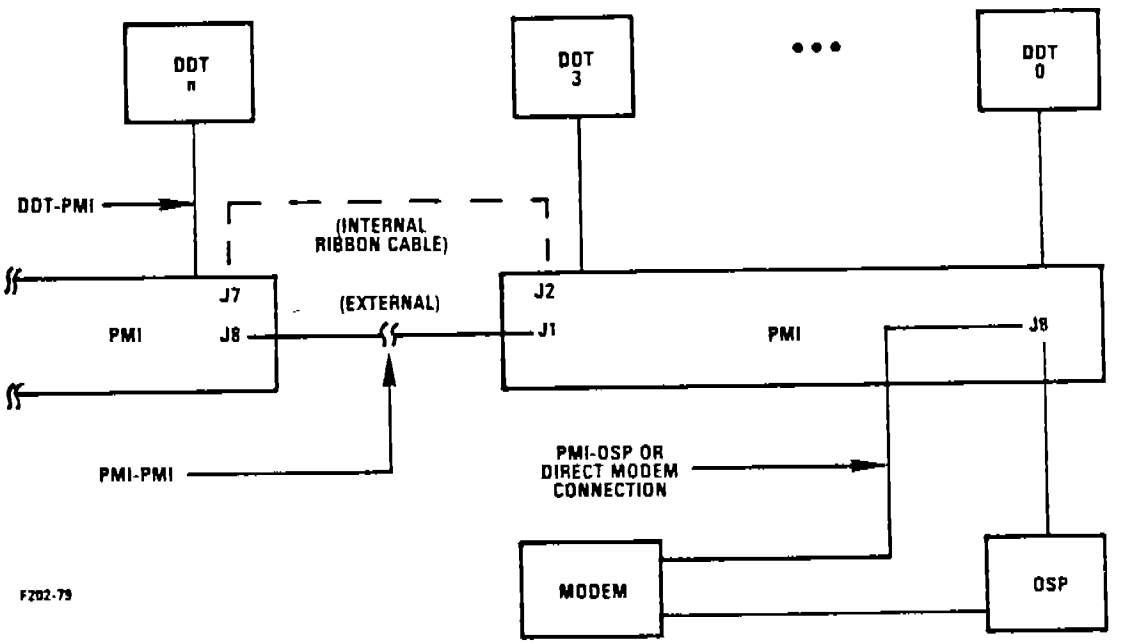

Figure 2-22. PMI Interface Cabling

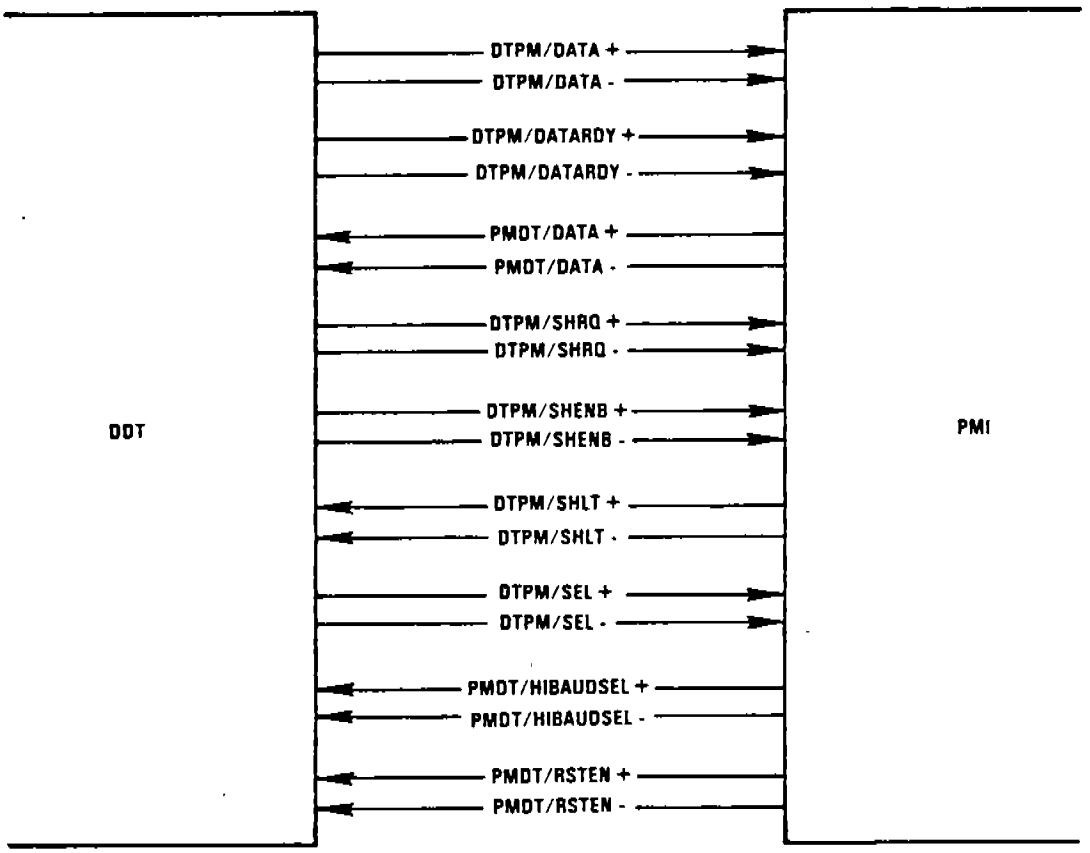

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Figure 2-23. DDT-PMI Interface

This action permits low-level access to one or more processors through the OSP without possibility of interaction with other processors in the system through the system halt facility of the PMI. This switch does not interrupt the SHRQ-SHLT wraparound logic; the processor can test the SHRQ-SHLT logic with SHENB negated regardless of the switch position. Refer to the OSP USER GUIDE (T16/8801) for more detailed DDT-PMI signal description.

2.3.1.1.2.13 PMI OSP.- The PMI-OSP interface consists of two serial communication lines: a differential (RS-422) circuit and a differential or unbalanced (RS-232 compatible) circuit, depending on the cable type that is attached. Refer to table 2-8.

NOTE

When the PMI-OSP cable is attached to J8 on the PMI, the PMI selects the high baud rate to all DDT's. If the modem cable is used, the low baud rate is selected.

Table 2-8. PMI-OSP Interface Pin Assignment

J8 PIN NO.	NAME	FUNCTION
1	Frame Ground	
2	PMMO/TD	Serial data DDT to Modem
3	MOPM/RD	Serial data Modem to DDT
4	RTS	Request to Send (always true)
7	Signal Ground	
9	PM/LOOP*	DDT to DDT data loopback
11	SMPM/PSTD+	Serial data OSP to PSM
12	SMPM/PSTD	
18	SMPM/TXD+	Serial data OSP to DDT
19	SMPM/TXD	
20	DTR	Data Terminal Ready (always true)
22	PMSM/PSRD	
23	PMSM/TXD+	Serial data DDT to OSP
24	PMSM/RXD	
25	PM/HIBAUDSEL*	High/Low Baud rate select

2.3.1.1.2.18 DDT-Processor Interface.- The DDT Interface for each processor consists of the nine differential (RS-422) circuits listed in table 2-9; the signals are described in table 2-10.

Table 2-9. DDT to Processor Signals

CCD	PMI	SIGNAL NAME	FUNCTION
J2 PIN NO.	J3-J6 PIN NO.		
55	1	DTPM/DATAn+	Serial data from DDT to OSP
56	2	DTPM/DATAn	
57	3	DTPM/DATARDYn+	DDT is ready to transmit data;
58	4	DTPM/DATARDYn	self-test has completed.
59	5	DTPM/SHRQn+	System Halt Request
60	6	DTPM/SHRQn	
61	7	DTPM/SELn+	Select; the OSP has selected DDT
62	8	DTPM/SELn	
63	9	PMDT/RSTEN+	Reset Enable
64	10	PMDT/RSTEN	
65	11	PMDT/SHLTn+	System Halt (Freeze)
66	12	PMDT/SHLTn	
67	13	PMDT/DATAn+	Serial data from OSP to DDT
68	14	PMDT/DATAn	
69	15	DTPM/SHENBn+	System Halt Enable; used to disable
70	16	DTPM/SHENBn	the Halt logic and allow self-test.
71	17	PMDT/HIBAUDSEL+	Select High (19.2K) baud rate; or
72	18	PMDT/HIBAUDSEL-	use 300 baud rate.

Table 2-10. DDT to Processor Signal Description

SIGNAL	FUNCTION
n	Denotes a processor.
SEL	Drives an LED.
DATARDY	Used by the DDT to loop a path with the serial data path to perform self-test after power-up. When DATARDY+ goes low, the self-test is completed, and an LED is lit to signify DDTOK.
SHENB	Used to self-test the system halt request logic. The PMI allows the self-test in spite of the setting of the Freeze Enable Switch. The switching of SHENB should not cause false system halt requests to other processors in the system.
HIBAUDSEL	Used to notify the DDT that the modem is connected instead of the OSP and that 300 baud rate should be used instead of 19.2K baud. The switching of HIBAUDSEL is accomplished through the use of a jumper switch in the OSP-PMI cable.

2.3.1.1.2.19 Power Supply Monitor (PSM) Interface.- The PSM Interface consists of two differential circuits used to fan out a serial multi-drop line (refer to table 2-11, n=0 to 14 and denotes a separate power supply).

Table 2-11. PSM Interface Circuits

J9-J123 PIN NO.	SIGNAL NAME	FUNCTION
1	PMPS/PSTDn+	transmit data
2	PMPS/PSTDn	
3	PSPM/PSRDn+	receive data
4	PSPM/PSRDn	

2.3.1.1.2.20 Power Requirements.- Power input to the PMI is via a 10 pin connector:

+5 volts primary (2.0 amperes, max.)	J24 pins 1, 2, 3
Ground	J24 pins 4, 5, 6, 7
+5 volts secondary	J24 pins 8, 9, 10

2.3.1.1.2.21 Switches and Indicators.- The PMI has switches and indicators for each processor; the system freeze function can be enabled via the switches. Status conditions which are affected by the switches are displayed to aid with the freeze function. Refer to tables 2-12 and 2-13 for the description of switches and indicators.

Table 2-12. PMI Switches

SWITCH	FUNCTION
DDT ENABLE	Enables the DDT to communicate with the OSP and to issue SYSTEM HALT REQUESTS TO THE PMI. Does not affect wraparound in PMI.
RESET ENABLE	Enables the resetting and halting of its processor from the OSP. Does not prevent OSP from clearing an SHRQ or software from requesting a SYSTEM HALT.
RST-HLT-FRZ ENABLE	Enables the processor to be halted by a SYSTEM HALT REQUEST from the OSP or from other processors on the system. Also enables this processor to halt other processors by means of a SYSTEM HALT REQUEST. When disabled, no SYSTEM HALT can occur. This switch does not affect a LOCAL HALT command from the OSP.

Table 2-13. PMI Indicators

INDICATOR	FUNCTION
FREEZE	ON. A processor freeze request exists in this processor. This is an outstanding request if the FREEZE ENABLE/DISABLE switch is placed in the disable position.
DDT DATA	ON. This DDT is transmitting data to SMP.
DT SELECT/DDT OK	Both DDT SELECT and DDT OK off indicates the PROM checksum self-test failed. DDT SELECT blinking and DDT OK off indicates the UART data turnaround routine failed. DDT SELECT blinking and DDT OK on indicates this DDT is selected by the SMP and that the power on self-test and idle loop tests executed successfully.
+5V POWER-ON	ON. +15V is applied to the PMI logic.
PSM TXD/PSM RXD	PSM TXD and PSM RXD indicate that the Power Supply Monitor (PSM) poll and response serial communication lines are active. These LEDs blink to reflect the mark/space condition on the lines.
SHRQ From Left	ON. A System Halt Request is originated from the PMI on the left of this panel.
Data From Left PMI	ON. The PMI to the left of this panel is sending data to the SMP.
SHRQ From Right	ON. A System Halt Request is originated from the PMI on the right of this panel.
Data From Right PMI	ON. Data from the OSP-VDU is available at the serial communication lines to the PMI-DDT.

2.3.1.1.2.22 Control Panel.- The CONTROL PANEL SWITCH REGISTER lamps report status information and error codes. Lamps indicate processor halt errors, COLD LOAD errors, and errors detected during the loading of Shadow or Stand Alone Diagnostic. Lamps also indicate which processor is involved. Refer to the OSP USER GUIDE (T16/8801) for detailed CONTROL PANEL SWITCH REGISTER decoding.

2.3.1.1.2.23 OSP-VDU (T16/6530).- The T16/6530 Video Display Unit (OSP-VDU) provides access to the 12 operating modes of the OSP. The shifted function keys, F1 through F16, are used to switch between the operating modes. The unshifted function keys modify the data displayed. The screen displays 24 lines of 80 characters each, with a specially addressed 25th line for reporting extraordinary conditions on the system. Since only one process can have control of the screen at any given time, an off-screen process receiving an error report uses the 25th line to gain the operator's attention. Independently addressable fields on the display provide reverse, halfbright, and blinking video attributes.

2.3.1.1.2.24 Interface.- The OSP-VDU interface, connector J3 of the SMP, is a RS-232C interface combined with a current-loop interface that serves a hard copy printer. Refer to table 2-14. The connecting cable (SMP-TERM) orders the signals so that the DTC-DCE relationship is maintained as listed in table 2-15. The operation of the terminal and the printer is controlled by the SMP software.

Table 2-14. OSP-VDU Interface Circuits

PIN NO.	CCITT	EIA	D/R	FUNCTION
1	101	AA	-	Frame Ground
2	103	BA	D	Transmit Data
3	104	BB	R	Receive Data
4	105	CA	D	Request to Send
5	106	CB	R	Clear to Send
6	107	CC	R	Data Set Ready
7	102	AB	-	Signal Ground
8	109	CF	R	Carrier
14			-	CL Transmit Driver (Printer)
15			-	CL Transmit Return (Printer)
17			-	CL Receiver Driver (Printer)
18			-	CL Receiver Return (Printer)
20	108	CD	D	Data Terminal Ready

Table 2-15. DTE-DCE Relationship

SMP J3 PIN		CABLE CONNECTIONS NO. 51341	PIN	TERMINAL
TXD	2	----------	3	RXD
RXD	3	----------	2	TXD
RTS	4	----------	8	CD
CTS	5	----------	5	CTS
CD	8	----------	4	RTS
DSR	6	----------	20	DTR
DTR	20	----------	6	DSR

2.3.1.1.2.25 Power Requirements.- The OSP-VDU power requirements are as follows:

1) 100 - 120 VAC at 2 amperes, 60 Hz
2) 220 - 240 VAC at 1 ampere, 50 Hz

2.3.1.1.2.26 Switches and Indicators.- OSP-VDU back panel switches include the PARITY, BAUD RATE, AND POWER switches. The function of these switches is described in table 2-16. Refer to the Programming Manual (Part Number 82047) for a description of keyboard switches.

NOTE

The status of these switches is only read normally when power is applied. If they are charged while power remains on, use of the RESET key (depressed twice) is required to read in their new settings.

2.3.1.1.2.27 OSP Printer (T16/5520).- The T16/5520 Printer provides a hard copy printout of the Tandem Non Stop II error messages. The printer is a high speed (9600 Baud) serial 7x7 dot matrix printer. Print rate is 125 lines per minute for 132 printed character columns.

2.3.1.1.2.28 OSP Power Requirements.- The OSP power requirements are as follows:

1) 110 VAC $\pm$ 10%, 50 - 60 Hz; power receptacle NEMA 5-15R or equivalent, and

2) power consumption is 66 Watts nominal.

Table 2-16. OSP-VDU Back Panel Switches

SWITCH	FUNCTION
Parity	Enables or Disables (center position) checking of parity. Selects Even (down) and Odd (up) parity.
BAUD Rate	Selects the asynchronous data speed, or in the SEL position, places the VDU in synchronous mode. The OSP-VDU baud rate is 19.2K.
Power	Turns the OSP-VDU on or off.
Volume	Controls the loudness of the "bell" character and the "key-depressed" analog click.
Brightness	Controls the intensity of characters on the display.

2.3.1.1.2.29 Operating Environment.- The OSP operating environment is as follows:

1) ambient temperature range: 0 - 50 degrees C.;

2) relative humidity: maximum 30% to 80% with no condensation.

2.3.1.1.3 COTC Processors.- The COTC Processors are located in the COTC Processor Rack at the FSDPS. There is one Position Processor and one Communication Processor. Together they handle the message traffic to and from the data base and the two COTC display terminals. They provide the capability to operate either of the COTC display terminals as a local AFSS terminal or as a COTC terminal.

When a display terminal is operated as a local AFSS, that terminal provides all the services that are provided at any AFSS. Data may be entered and or retrieved from the system in this configuration.

When a COTC display terminal is operated as the COTC, the operator may perform certain system functions such as, System start-up or execute diagnostics. Refer to Section 3 for a detailed description of the functions of either mode of operation.

The position processor and the communications processor are both LSI-11/23 based processors. Refer to section 2.3.2 on the AFSS position processors and the AFSS communications processors for a detailed description of each processor.

2.3.1.1.4 I/O Controllers.- Each controller in the Tandem Non Stop II computer system is connected to the input/output channels of two processor modules. Selective addressing is provided by DIP switches on each controller. These DIP switches are configured according to the DIP Switch Matrix Table in the Tandem System Log Manual supplied at each FSDPS. Dual-Port addressing provides redundant communication paths to I/O devices. Figure 2-24 illustrates the concept of dual-port addressing.

Although each controller has two ports and is fully capable of communicating through either I/O channel, only one channel is used during normal operation (the other channel, as far as a particular controller is concerned, is not used). The I/O channel through which communication to a particular controller occurs is said to own the controller. All input/output transfers (i.e., control and data) occur through the channel owning the controller.

Each of the two ports in a controller contains a flag bit known as the ownership bit. The state of these bits determines the channel from which the controller will accept commands. An operating system configuration parameter specifies which channel is to be the primary channel of communication for a particular controller.

The operating system only transfers data through the owned side (an attempt to communicate through the unowned side results in the EIO instruction being rejected with an ownership error). If, during the course of a data transfer, the primary path to the controller (i.e., the primary processor module, channel, or port) becomes inoperable, the operating system executes a take ownership operation (of an EIO instruction) over the alternate (backup) channel. The ownership bits in the controller switch over, to point to the alternate I/O channel. All subsequent data transfers occur through this channel.

Each port has two disable bits that are separate from its ownership bits. A disable bit, if a "1", prevents a controller from transmitting information through that port onto an I/O channel. The disable bit is set by an EIO instruction set disable command. Normally, this is used by the operating system when a controller performs some unexpected action that could affect the entire channel. The disable bit is associated with a port, so, if the malfunction is in one port, normal communication with the controller still occurs via the other port. Figure 2-25, Dual-Port Ownership, depicts a typical dual-port ownership functional layout. The following paragraphs detail the operational and physical characteristics of the I/O controllers operating in the M1FC FSAS processing subsystem.

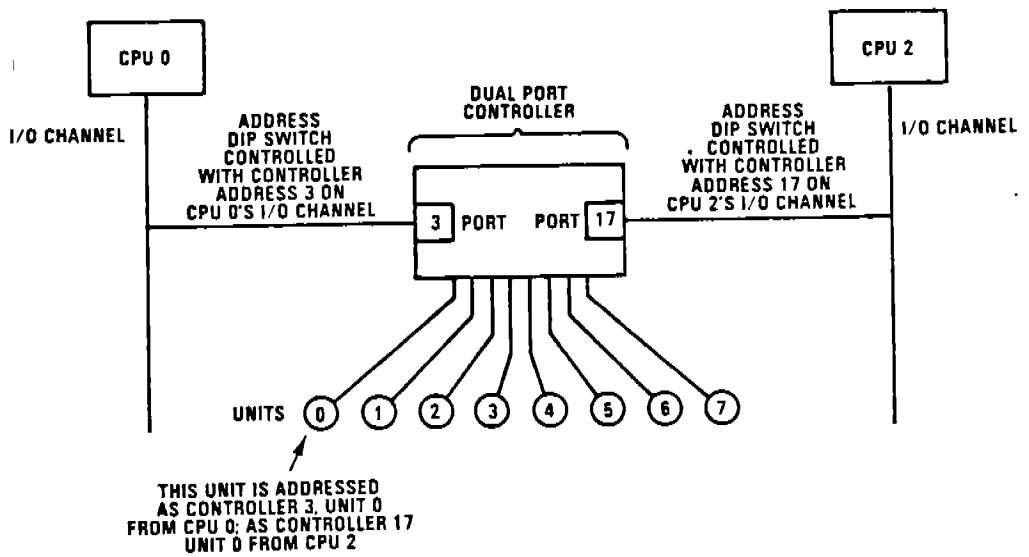


Figure 2-24. Dual Port Addressing

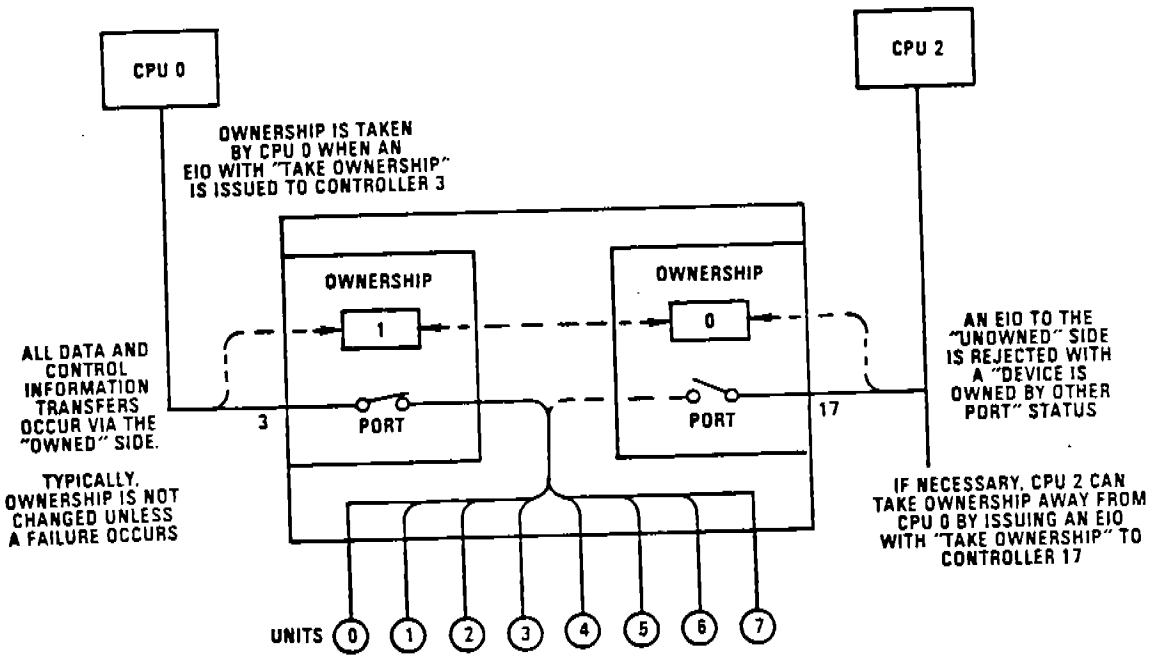


Figure 2-25. Dual Port Ownership

2.3.1.1.4.1 Disk Controller, T16/3106.- The disk controller can attach up to eight 300 Mbyte disk drives connected in a dual-ported configuration. The FSDPS contains eight disk drives. The disk controller consists of two boards, a channel interface board and a disk interface board. The disk interface board externally connects to the disk drives via the disk patch panel illustrated in figure 2-26, Disk Patch Panel. Each FSDPS is equipped with eight disk controllers configured as illustrated in figure 2-27, 300 MByte Disk Configuration. The eight drive/controller configuration requires two disk patch panels.

The Model T16/3106 Disk Controller is actually an intelligent "backend" disk processor which supports 1.92 billion bytes of on-line storage per FSDPS. In addition, it provides the hardware support for handling "mirrored" volumes found in the inscribed data base record manager. The controller connects two I/O channels simultaneously and may be powered by either processor in the event of a single processor failure.

The T16/3106 Disk Controller interfaces high technology disk drives in a way that provides fail-safe access and allows flexible system configuration. The controller will interface eight 240 MByte drives.

Significant controller features include: (1) a 4K buffer for buffering logical records between the channel and a disk unit; (2) dual recording or the ability to transfer the buffer to one or more disk units without having to retransmit on the I/O bus; (3) support of dual access disk units; and (4) read without I/O transfer which allows one disk unit to be copied to another without involving the I/O bus.

The disk controller is configured so that two controllers access the same disk unit. To prevent daisy-chain failure from bringing down the data base, the drives are connected to two controllers simultaneously providing alternate access paths to each drive.

2.3.1.1.4.2 Mag Tape Controller T16/3202.- The FSDPS is provided with two T16/3202 controllers. The FSDPS configuration interfaces one drive per controller. The controller cables directly to the magnetic tape drive. The dual-port controller handles up to two independently connected tape drives without the conventional requirement for daisy-chaining. In the event of a single processor failure, the dual-port controller is powered from the second processor.

Features of the T16/3202 are:

1) NRZI (800 bpi) and/or PE (1600 bpi) recording format and ANSI/ECMA format compatibility;

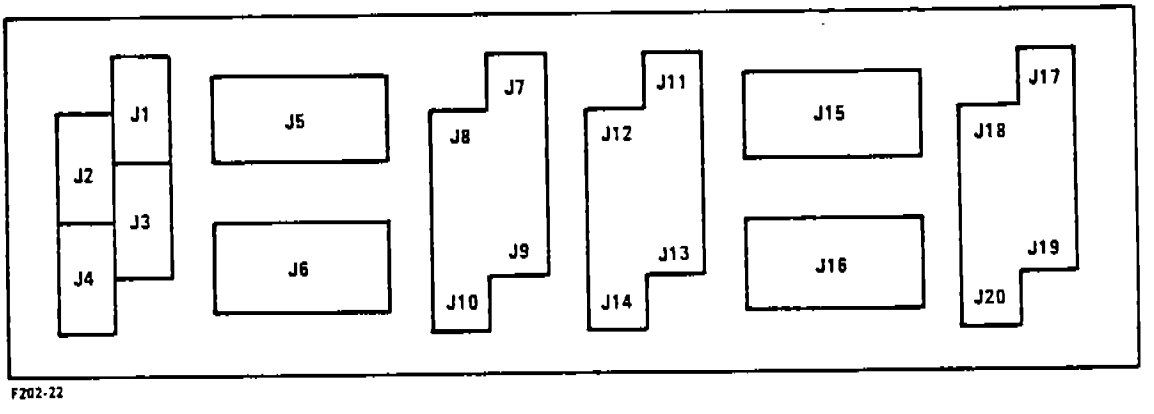


Figure 2-26. Disk Patch Panel

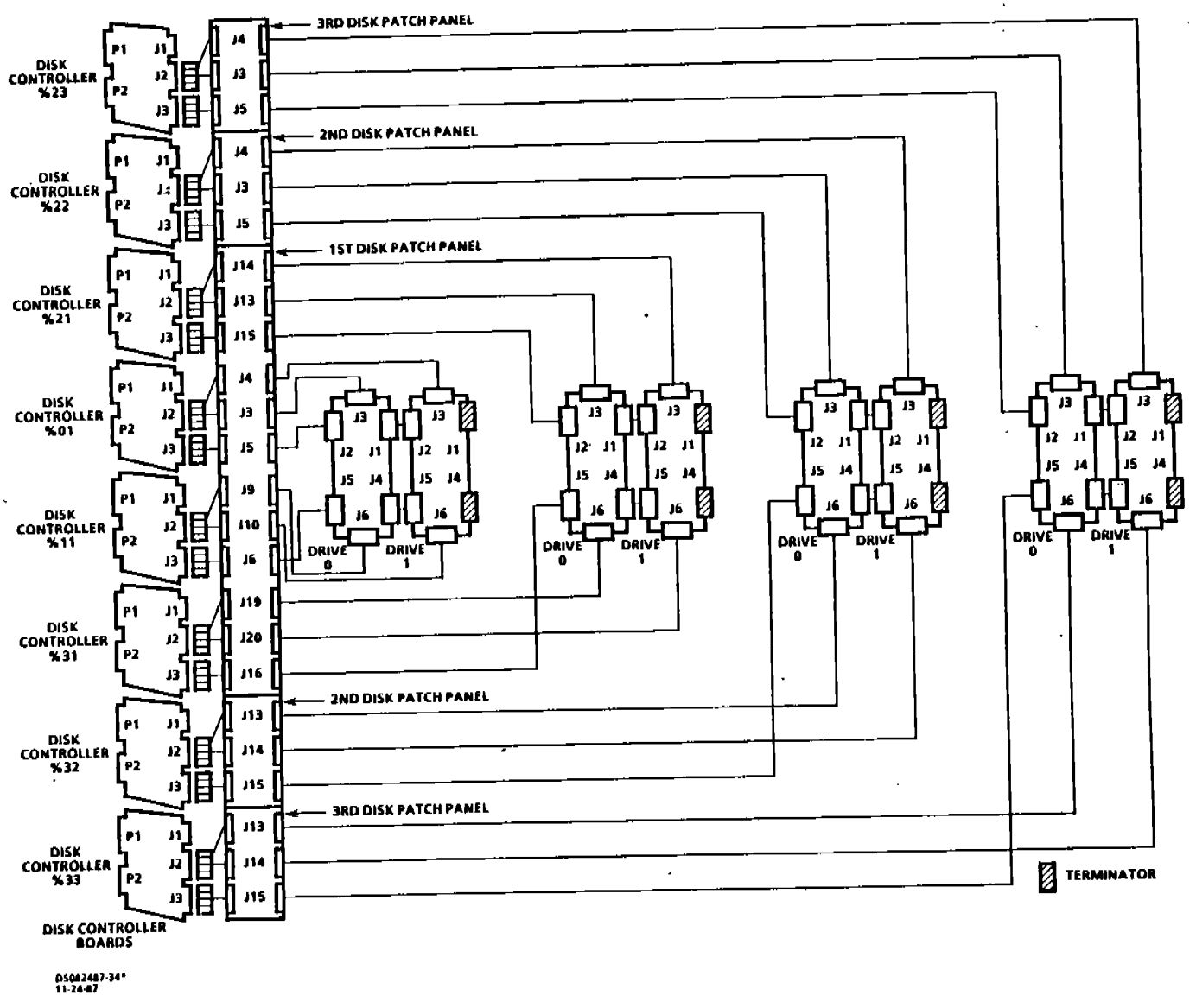


Figure 2-27. 300 Mbyte Disk Configuration

2) IBM 9-track compatible with vertical parity generation and check, longitudinal parity generation and check, CRCC generation, write echo and over-write;

3) time saving performance with speedy local or remote fastforward (150 ips), rewind (300 ips) and unload modes; and

4) economical maintainability with modular design, extensive diagnostics and self-contained diagnostic modular for off-line testing.

2.3.1.1.5 FSDPS Communications Equipment.- The FSDPS communications equipment is located in two racks of equipment. These racks are the communications switching rack and the communications equipment rack. The two racks incorporate modems, power supplies, digital patch panels, and analog patch panels. Multiplexers for the FSDPS are contained in the Tandem processor. Figure 2-28, FSDPS/AFSS Interface Block Diagram, shows the system communications equipment.

2.3.1.1.5.1 Asynchronous Communications Controller.- The Asynchronous Communications Controllers (T16/6303) are provided to support the protocol. The controller board is the front end board and provides ports for two asynchronous communication lines. In addition to the two external ports, the front end board also supports one extension board (T16/6304). The extension board provides an additional 15 external communication ports and interfaces to the Asynchronous Patch Panel (T16/7501). The port configuration is performed by the operator from the COTC. Each port is configured individually.

2.3.1.1.5.2 Asynchronous Patch Panel.- One patch panel supports 17 asynchronous ports. Each port on the patch panel is terminated with an EIA compatible 37-pin connector. The patch panel is interfaced to the asynchronous controller via external cabling. Five cables per patch panel are required. Adaptive cabling is provided so that the EIA RS-449 connectors on the patch panel will function with the EIA RS-232 connectors provided with the GFE modem.

2.3.1.1.5.3 Byte Synchronous Communication Controller.- Each synchronous controller supports four full- or half-duplex ports. The synchronous controllers Service A baud rates are determined by the modem. Each port is configured individually by the operator from the COTC.

All input/output is directly between main memory and the controller. CPU processing is interrupted only when a transfer of a message completes or a line error condition is encountered.

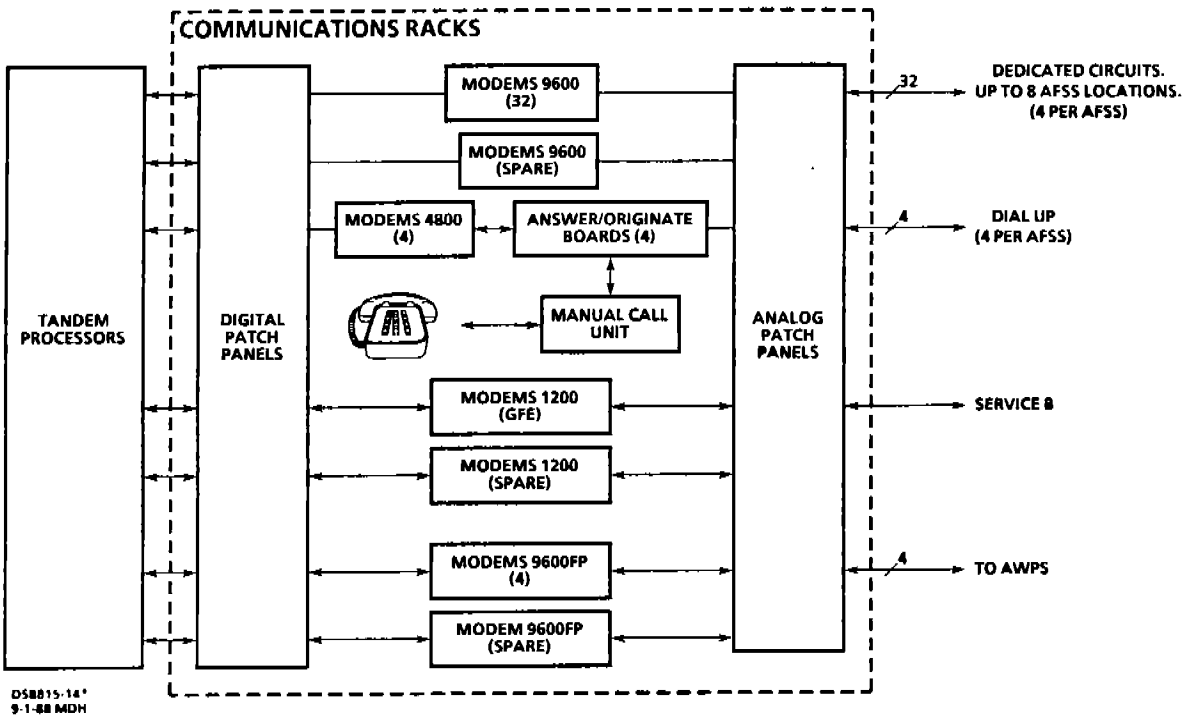


Figure 2-28. FSDPS/AFSS Interface Block Diagram

The controller generates and appends check character information upon transmission and performs error checking upon reception.

The controller automatically recognizes the transmission of transparent text. If the control sequence (DLE-STX) is encountered at the beginning of a message transfer, the controller will insert a control (DLE) character in front of a data (DLE) character when transmitting. Conversely, when receiving transparent text, the controller will delete a control (DLE) character in front of a data (DLE) character. The controller remains in the transparent text mode until an (ETB), (ETX), or (EOT) control sequence is encountered.

The controller's internal character code, as far as detecting control character sequences is concerned, is ASCII. The controller has the capability to translate ASCII code to EBCDIC code upon transmission and to translate EBCDIC code to ASCII code upon
reception. Because of this capability, application processes need deal only with the ASCII character set.

The controller has the capability to recognize a line being polled or selected. For each line, the controller stores the first byte of the station's polling address and the first byte of the station's selection address. Only when the line is polled or selected and the corresponding poll or select byte matches is CPU processing interrupted.

2.3.1.1.5.4 Synchronous Patch Panel.- One patch panel supports three synchronous controllers (12 ports). Each port on the patch panel is terminated with an EIA compatible 37-pin connector. The patch panel is interfaced to the controller via external cabling. Two cables per controller are required for the patch panel. As with the asynchronous device, adaptive hardware is provided for RS-232/RS-449 conversion.

2.3.1.1.5.5 Dedicated Communication Facilities.- The system provides the following:

1) 9600 bit per second modem operation;

2) four each 3002, voice grade, 4-wire, full duplex, GFE supplied, Telco circuits between FSDPS and AFSSs, and FSDPS and AWPs; and

3) dial backup equipment and facilities.

The 9600 bps operation uses, to its maximum, the data communication capabilities of the basic point to point, leased, voice grade link or circuit. Modulation techniques and data recovery methods incorporated in the UDS RM-9600 modem illustrate

the highest probability of satisfactory data transfer between the AFSSs and FSDPSs. The modulation technique employs a 2400 baud line signaling rate, double sideband suppressed carrier, quadrature amplitude modulation (QAM). Relatively error free recovery of the data is accomplished through the automatically controlled (retrain) equalizers. Table 2-17, Universal Data Systems Modem, illustrates the manufacturer's specifications for the RM-9600 Modems.

2.3.1.1.5.6 Dial-Up Facilities.- The dial-up facilities provide an alternate means of transferring data between the FSDPS and associated AFSSs via the DDD telephone network in the event one or more of the FSDPS-to-AFSS leased channels fail. At the FSDPS, these facilities consist of a 4800 BPS full-duplex 4-wire modem with DAA interface card (configured for call origination) for each of its associated AFSSs and at least one manual dialer (One dialer can access up to four AFSS full-duplex data communications). Dial backup data communications are initiated and completed by the FSDPS operator with no action required at the associated AFSS. To activate the dial-up feature, the FSDPS operator must first patch the AFSS data source (AFSS A, Line 1, for example) to the dial-up modem. Then the operator takes the manual call-up telephone handset off hook and dials the digit corresponding to the dial-up modem.

The operator then raises the exclusion key which connects one of the DDD subscriber lines dedicated to the selected modem's DDA interface card to the central telephone office. The central telephone office returns dial tone and the operator direct dials the first of two telephone numbers of the corresponding AFSS dial-up modem DAA interface card. When the DAA interface card at the AFSS detects the incoming call, it goes "off hook" and supplies an answerback tone to the FSDPS.

The operator then lowers the exclusion key which signals the dial-up modem DAA interface card to maintain the DDD subscriber line "off hook." The operator then places the telephone set "on hook." The operator then repeats this process once more, dialing first the selected modem number plus "1" (accessing the second DDD subscriber line), then dialing the second telephone number of the AFSS dial-up modem DAA interface card. When this process has been completed, the DDD subscriber lines are transferred to the modems (at the FSDPS and AFSS) and the terminals (at the FSDPS and AFSS) are notified to start passing data. Dial-up facilities disconnect is accomplished by dropping the Terminal Ready signal to the modems. Figure 2-29 illustrates a typical dial-up configuration.

2.3.1.1.5.7 Digital and Analog Patching Facilities.- Network management and the required access to the system communication facilities are provided by the analog and digital patch panels. Each modem is accessible on both the digital and analog

Table 2-17. UDS Modem (RM-9600)

Data Rate
9600 bps

Fall Back Rates
7200 bps, 4800 bps

(switch selectable)

Modulation
Eight-phase, four amplifier QAM per CCITT V.29

Carrier Frequency
1700 Hz

Internal Transmit Clock Frequency
9600 Hz ± 0.01%

External Transmit Clock Frequency
9600 Hz ± 0.01%

Transmit Output Level
0, -2, -4, -6, -8, -10, -12 dBm

Line Impedance
600 ohms, transformer coupled and transient protected

Operation Mode
4-Wire, full-duplex private line operation

Digital Interface
Conforms to EIA Standards RS-232C and CCITT V.24

Clear to Send
253.5 ms

Carrier Detect Level
0 to -34 dBm

Line Equalizer
Automatic Adaptive

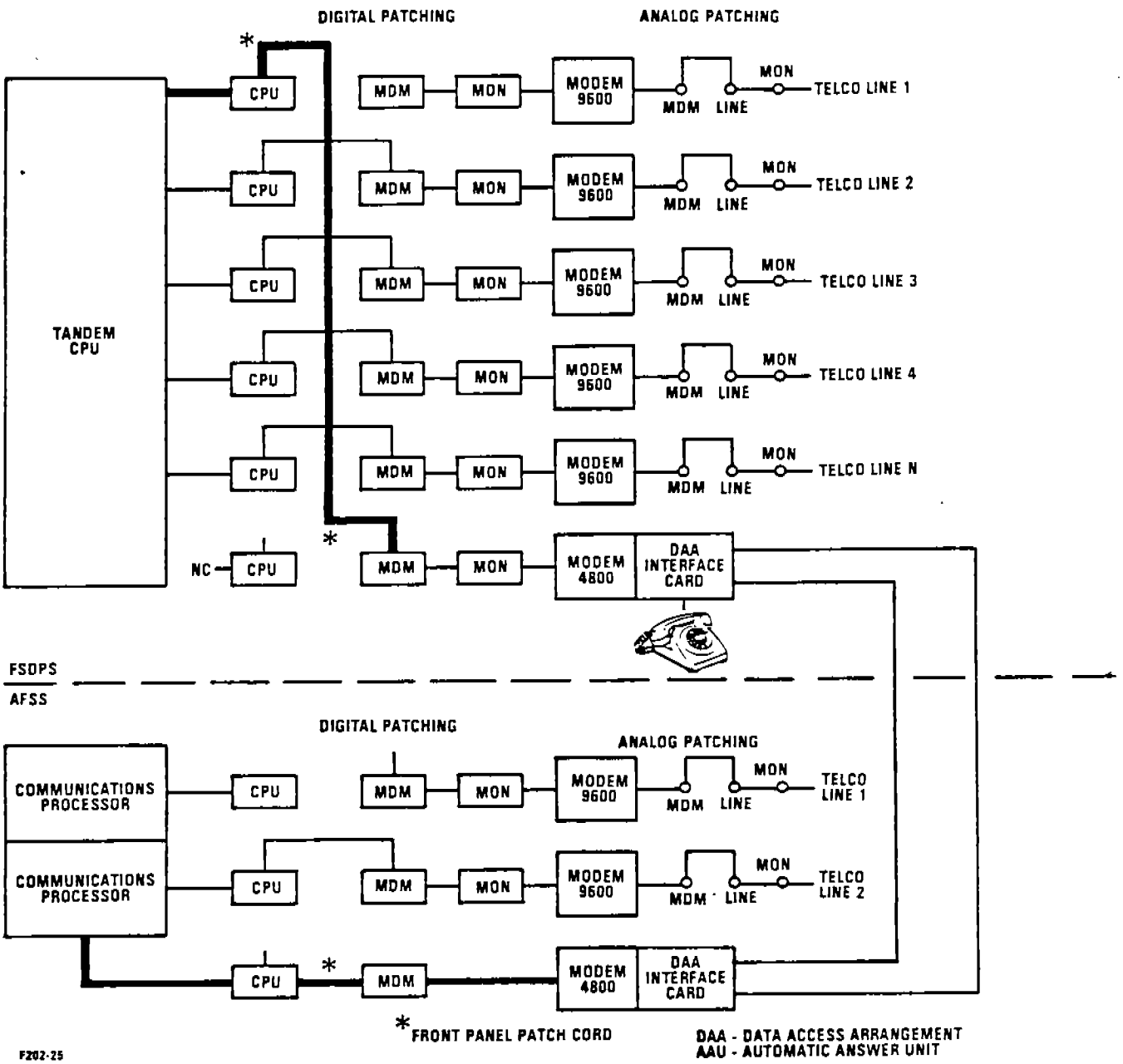


Figure 2-29. Typical M1FC Dial-Up Configuration

interfaces. Modem to line and modem to dial-up facilities configurations can be changed to provide very flexible network management.

The Dynatech VF Analog Patch Panel and the digital patch panel basic patching is shown in figure 2-30. Figure 2-31 illustrates dial-up patching between an FSDPS and the AFSSs. Both patch panels provide the system with the necessary reconfiguration flexibility with minimum and user impact.

2.3.1.1.5.8 Equipment Redundancy.- The system design provides sufficient redundancy to meet all requirements.

Modem modularity design utilizes the UDS multimodem enclosures. These enclosures (RM-8D) have the capability to house eight RM8-9600 modems. Modem power is supplied by one of two power supplies. The enclosure provides the monitoring and the switching required for continuous operation should the active (on-line) power supply malfunction. Front panel indicators alert operators/technicians of the fault. All components (modems and power supplies) are plug-in modules; all indicators and operational controls have front panel accessibility.

Each FSDPS has one modem designated as redundant and up to six modems designated for AFSS circuit dial backup. One RM-8D multimodem enclosure is installed for every eight modems. Each enclosure is equipped with two power supplies for the specified redundancy.

2.3.1.1.5.9 Government Furnished Communications Services/Equipment.- The list below documents the necessary GFE equipment. This equipment provides the primary and backup facilities which are designed into the M1FC FSAS network.

Between each AFSS and Associated FSDPS - one each 3002 voice-grade circuit per communications processor.

At each FSDPS - Modem and associated equipment for Service B, including their spares.

At each AWP - Modems and associated equipment for Service A and Service B, including their spares.

2.3.1.1.5.10 EIA RS-232C To RS-449 Adaptations.- Each E-Systems supplied EIA RS-449 interface is adaptable to interface with EIA RS-232 GFE supplied equipment. The adapter is similar to the specifications in EIA "Application Notes on Interconnection Between Interface Circuits" using RS-449 and RS-232C.

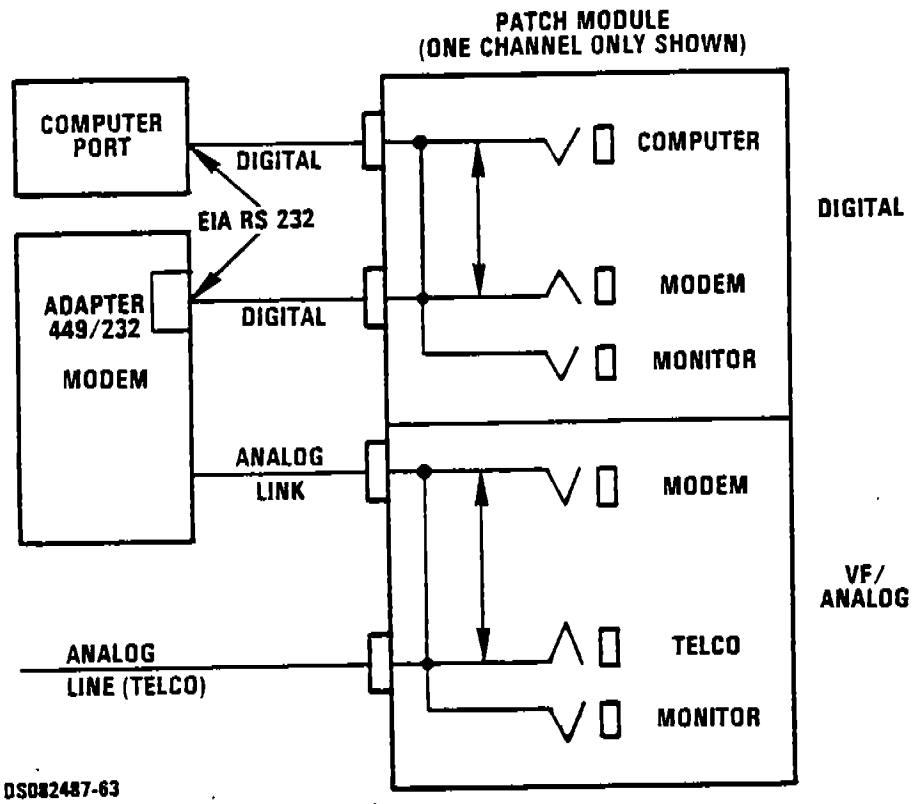


Figure 2-30. Digital and Analog Basic Patching Schematic

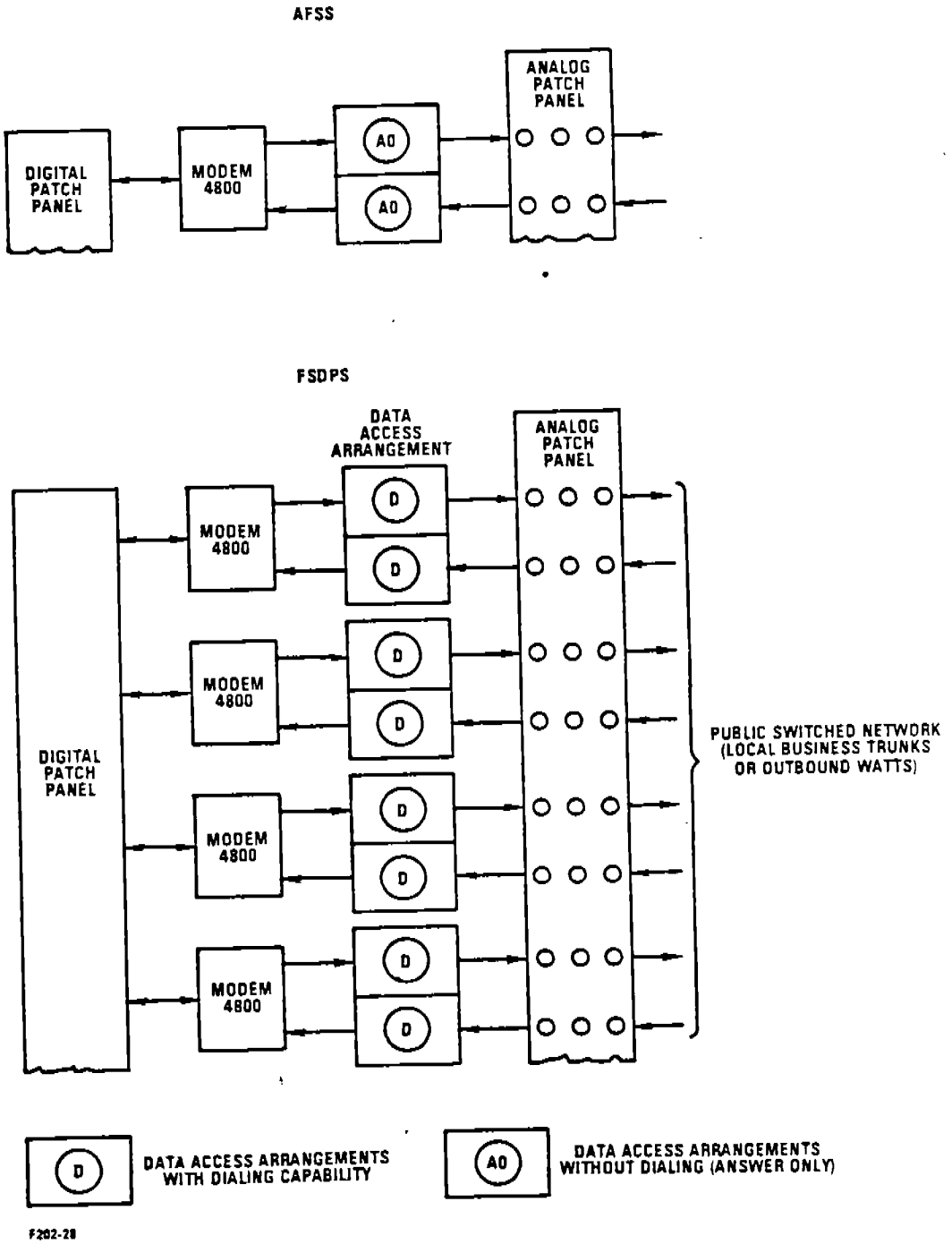


Figure 2-31. M1FC FSDPS and AFSS Dial-Up

2.3.1.1.6 Peripherals.- The following paragraphs provide a description of the peripherals provided as a part of the FSDPS processing subsystem. The units discussed in this section are:

1) disk drive,
2) magnetic tape,
3) line printer,
4) coded time source interface,
5) coded time source, and
6) thermal alarm.

All of the peripherals are free-standing except for the coded time source interface, coded time source, and thermal alarm which mount in the communications switching rack.

2.3.1.1.6.1 DM9300TDQ Disk Drive.- The M1FC FSAS system employs the Ampex DM9300TDQ, 30 Sectors per track, 300-Mbyte Disk Drive. The eight disk drives are configured as illustrated in figure 2-27, 300 MByte Disk Configuration. All drives interface to the disk panel. The Ampex DM9300 Dual-Port Disk Drive is a self-contained, single-spindle, direct-access storage device. The DM-9300 drive uses the removable IBM-3336 Model 11 20-surface disk pack, or its equivalent. Each data surface of this pack contains 815 tracks, providing a total data storage area of 815 cylinders across 19 surfaces. The 20th surface of both packs is a special prerecorded servo surface that provides track-to-track and rotational-positioning information. The data format is determined by the control unit which interfaces with the drive. Maximum disk-pack storage capacity is 300 million 8-bit bytes. Sector sparing and defect logging occur between cylinder 803 and 814. The recording technique is a modified frequency modulation (MFM) scheme.

The dual-port interface design allows two control units to attach directly to the disk drive, and gives each controller full access to the drive when the drive is not busy with the other controller. In allowing this dual access, the dual-port interface functions as a dynamic (or static) switch that routes the necessary control and data signals between the drive and the using control unit. Once the appropriate connection is made, the dual-port interface is essentially transparent. In addition to providing required signal switching, the interface also issues a special status signal, Busy, in response to the control unit attempting to select the drive when it is already selected/reserved by the partner control unit.

The stand alone configuration provides excellent user convenience and system flexibility. The drive is easily moved on its own casters, and all connections to it are plug-removable. All interconnecting cables may be located under the floor, or units may be cabled together without floor cutouts when the units are located side-by-side in a group.

A linear DC motor (voice coil) is combined with a reliable on-track servo using the track-following method with the prerecorded tracks on a special servo surface of the disk pack. This method assures that regardless of the variations possible between different disk packs on drives (e.g., a disk pack that was written on while it was installed on one disk drive at a high ambient temperature, causing an expansion of the disk, is read on a different drive at a comparatively cool ambient temperature, causing it to contract), the heads are always positioned precisely because of the servo disk.

Blowers circulate filtered air for cooling throughout the drive. Air is admitted to the drive through grillwork in the edges of the drive front panel, rather than through the bottom of the drive unit with its proximity to the dust-laden floor. Packs are installed and removed through the front-loading shroud area to minimize operator handling of the 20-pound disk packs. The hinged front cover opens automatically when the pack comes to a stop.

The Ampex disk drives are mounted in steel welded frames that have removable front, rear, and side panels. Each disk drive includes a linear positioning motor that positions the heads, carriage, and assembly; two matrix boards; and a cam tower all mounted on a precision deck plate that contains a hole through which the spindle assembly extends. The disk-pack mounts on the spindle assembly.

2.3.1.1.6.1.1 Disk Drive Specifications.- The specifications are included in the following paragraphs. They are listed in tabular form and segregated into the following categories: Table 2-18, Disk-Pack Characteristics, Table 2-19, General Operating Characteristics, and Table 2-20, Storage Characteristics.

Table 2-18. Disk Pack Characteristics

Weight:
20 pounds (9.07 Kg)

Diameter:
15 inches (381 mm)

Height:
7 inches (177.8 mm)

Storage Temperature:
-40 F to 150 F (-40 to 65 C)

Operating Temperature:
60 F to 90 F (15.6 to 32.2 C)

Table 2-19. General Operating Characteristics

Start Time:	After the START/STOP switch is set to START, it takes 15 seconds maximum to reach the point when the READY indicator is lit.
Stop Time:	After the START/STOP switch is set to STOP, it takes a maximum of 15 seconds to bring the disk pack to a complete stop. (Braking is accomplished electrodynamically by an eddy-current brake on the spindle shaft.)
Pack Rotation Speed:	3600 ± 2% rpm
Pack Rotation Period:	16.7 ms for one rotation
Average Rotation Latency:	8.35 ms
Head Positioning Access Time:	Defined as the time required to position the read/write heads from a seek initialization until the disk drive becomes ready.
One Cylinder:	10 ms
815 Cylinders DM9300:	55 ms
Average:	28 ms (The average access time is equal to the time to do all possible seeks divided by the total number of seeks possible.)
Duty Cycle (Repetition Rate):	A minimum of 4 ms (from seek end to set cylinder) between successive seeks with an average minimum of 16 ms (from seek end to set cylinder) between seeks.
Data Transfer Rate (DM9300):	1,209,600 8-bit bytes per second (which is 9.676 megabits per second).

Table 2-20. Storage Characteristics

Number of Cylinders Per Pack:	815 cylinders
Tracks Per Cylinder:	19 (The protective top and bottom disks are not used for recording. The top surface of the sixth disk - the tenth surface - is used for the prerecorded servo.)
Tracks Per Pack:	15,485
Track Density:	370 tracks per inch
Bit Packing Density:	6.038 bits per inch (bpi) maximum, inner track
8-Bit Bytes Per Track:	20,160 (unformatted)
8-Bit Bytes Per Cylinder:	383,840 (unformatted)
8-Bit Bytes Per Pack:	312,177,600 (unformatted)
Recorded Data Track Width:	0.0020 inch

2.3.1.1.6.1.2 Operator Controls and Indicators.- A control panel assembly is mounted on the front of the frame just below the disk pack. This panel contains operating controls and provides a visual indication of the drive's operational status. The operating controls and indicators are described in table 2-21.

2.3.1.1.6.1.3 Recording Method.- The recording technique generally employed with the disk drive is a modified frequency modulation (MFM) scheme. The drive is capable of writing and reading data using other recording coding techniques which employ similar frequencies of recorded pulses since the drive does not discriminate among recorded pulses being ones, zeroes, or clocks, either on a read or a write operation.

The basic recording frequency at the nominal pack rotational speed of 3600 rpm is 9.67 MHz. This provides a basic data cell period of 103 nanoseconds nominal. Write data from the control unit is synchronized with disk speed using the phase locked oscillator (PLO) signal. The PLO signal is derived from signals read from the pack's servo surface, and transmitted back to the control unit.

The recorded data information is encoded so that no greater frequency than one pulse is written during any cell period.

2.3.1.1.6.2 Magnetic Tape Drive.- The Kennedy Model 9000 Magnetic Tape Drive is mounted in a 72-inch tape cabinet. The Kennedy 9000 is an asynchronous digital tape unit, which when combined with a Tandem controller and formatter, is capable of reading and writing IBM compatible tapes. This device is used in applications requiring high reliability at moderate tape speeds. The Model 9000 is equipped with the electronics necessary for reading and writing tapes, and for controlling tape motion. The head specifications and the mechanical and electrical tolerances of the Model 9000 meet the requirements for IBM compatibility. The T16/3202 controller provides: formatting electronics, parity generator, cyclic redundancy check character (CRCC) generator, and gap control.

The Model 9000 is provided in a 9-track NRZI encoded recording configuration at 1600 cpi. The unit is switch selectable between 800 and 1600 cpi. A recording speed of 45 ips is provided.

2.3.1.1.6.2.1 Electrical and Mechanical Specifications.- Table 2-22, Magnetic Tape Drive Mechanical and Electrical Specification, provides a list of the specifications for the 9000 tape drive.

2.3.1.1.6.2.2 Controls and Indicators.- Controls and indicators provided on the Model 9000 formatted transports are shown in figure 2-32, Controls and Indicators. Each control function is explained in the figure.

Table 2-21. Operating Controls and Indicators

CONTROL/INDICATOR	TYPE	FUNCTION
MODULE SELECT	Plug	Determines the selection address of the disk drive. The plug is inserted into a receptacle on the front of the control panel. Operators may change the number of the disk drive address to the address indicated by the control unit. The plug allows for individual selection of up to 16 drives.
START/STOP	Rocker switch	When placed in the START position (and if all safety interlocks are closed), power is applied to the spindle motor. After the disk pack has attained full rotational speed, and the pack compartment is purged with filtered air, the read/write heads are positioned into the disk pack to cylinder 000. When placed in the STOP position, the positioner retracts the heads from the disk pack. When the heads are fully retracted, power is removed from the spindle motor, and dynamic braking is applied to the spindle causing the rotation to stop.
READ ONLY R/W	Rocker switch	When set at READ ONLY, the write operations are disabled. Read operations may be accomplished in the normal manner. When set at R/W, read and write operations occur in the normal manner. If the position of the switch is changed while the drive is being selected by the control unit (SELECTED indicator lit), the drive will immediately change to the new operating system.

Table 2-21. Operating Controls and Indicators (Continued)

CONTROL/INDICATOR	TYPE	FUNCTION
OPEN DOOR	Rocker Switch	When pressed, enables the electrically operated door latch to be released if the pack is not rotating. The door opens automatically when the latch is released. The switch has no effect if it is pressed when the START/STOP switch is in the START position. If the switch is pressed when the START/STOP switch is in the STOP position, and the pack is moving, the unit waits until the pack stops moving before releasing the door latch.
READY	Incandescent lamp indicator green	When this indicator is lit, each of the following are indicated: a. The pack has reached full rotation speed. b. The heads are loaded. c. The unit is ready for communication with the controller.
SELECTED	Incandescent lamp indicator yellow	When lit, this indicator shows that it has been selected by the control unit which may be performing an operation.

Table 2-21. Operating Controls and Indicators (Continued)

SELECT LOCK	Incandescent lamp indicator red	When lit, indicates that an error is sensed within the drive electronics and that ability to read and write has been disabled by the drive. With this indicator lit, the drive cannot be used for the transfer of data until after the situation has been cleared by an Unsafe Reset command from the control unit, by a power-up reset, or by following this procedure: a. Place START/STOP switch in STOP position and wait for pack to stop rotating. b. If condition was caused by an attempted write with switch in READ ONLY position, verify that correct pack was installed and place READ ONLY R/W switch in R/W position. c. Place START/STOP switch in START position. (During pack start time the drive logic is reset). d. If SELECT LOCK indicator does not turn on again, drive is operating normally. If it does, stop drive, remove select plug, and notify responsible engineer.

Table 2-22. Magnetic Tape Drive Mechanical and Electrical Specification

Tape

Width	0.5 inch (1.27 cm)
Thickness	1.5 mil (.038 mm)
Tension	8.0 ounces (227 gm)
Reel diameter	to 10.5 inches (26.6 cm)
Capacity	2400 feet (731.5 meters)
Reel hub standards	3.69 inches (9.37 cm) diaper IBM

Reel braking	Dynamic
Recording mode (IBM compatible)	NRZ1
Tape Drive	Single capstan
Tape Speed	10-45 ips (25.4-114.3 cm/sec) 25 ips (63.5 cm/sec) standard

Instantaneous speed variation	±3%
Long term speed variation	±1%
Start/Stop displacement	8.1875 inch (0.476 cm)
Start/Stop time @25 ips	15ms
Rewind speed	150 ips (381 cm) (nominal)

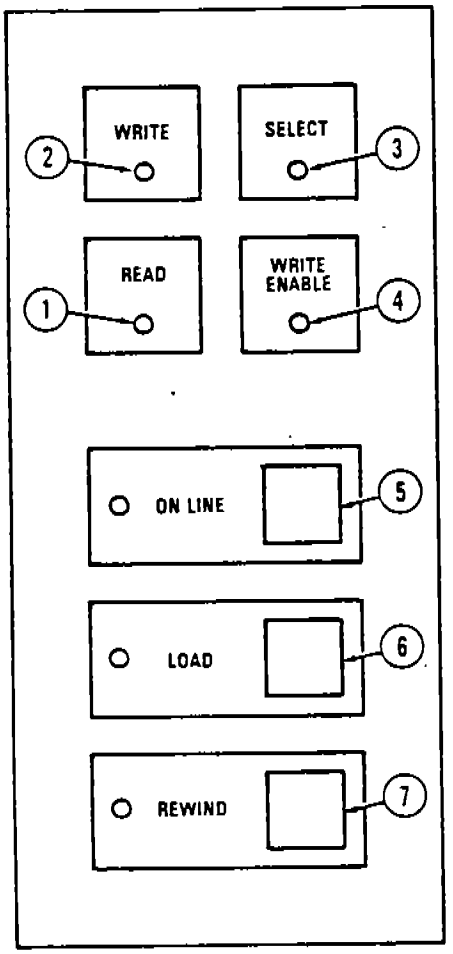
Magnetic head assembly

(Write to read gap displacement)	
Dual gap 7 track read after write	0.30 inch (0.76 cm)
Dual gap 9 track read after write	0.15 inch (0.38 cm)
Interchannel displacement error	
Write (maximum)	150 U inches (3.8um)
Read (maximum)	150 U inches (3.8um)

Erase head	Full width

Load point and end of tape reflective strip detection - Photoelectric (IBM Compatible)

Broken tape detection Photoelectric



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1 READ INDICATOR. Illuminated when tape unit is on line, selected, and read selected.

2 WRITE INDICATOR. Illuminated when tape unit is on line, selected, and write status selected.

3 SELECT INDICATOR. Illuminated when tape unit is on line and selected.

4. WRITE ENABLE INDICATOR. Illuminated whenever a reel with a write enable ring is mounted on the supply hub.

5. ON LINE. A momentary pushbutton, which functions as alternate action. When first activated the tape unit is placed in an on-line condition; when the tape unit is on line it can be remotely selected and will be ready if tape is loaded to or past the load point. When activated again it takes the tape unit off line. The indicator is illuminated in the on-line condition.

6. LOAD. The momentary pushbutton activates the reel servos (tensions tape) and starts the load sequence. The indicator is illuminated when the reel servos are activated and tape is tensioned.

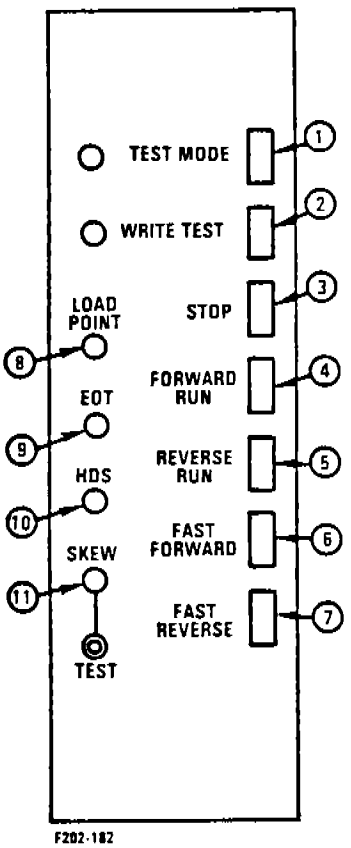
7. REWIND. The momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and unit is off line. The indicator is illuminated during either a local or remote rewind operation.

LOAD and REWIND pushbuttons are disabled when the tape unit is on.

Figure 2-32. Controls and Indicators (Sheet 1 of 2)

NOTE

Tape Transport be off line and STOP pushbutton depressed before test can become functional.



1 TEST MODE pushbutton and indicator. A momentary pushbutton selects test mode and activates test panel. When indicator (LED) is illuminated, test panel is active. (Tape unit must be off line and STOP pushbutton depressed before test panel will function.)

2 WRITE TEST pushbutton and indicator. A momentary pushbutton which programs 1's to be written on all channels in order to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator (LED) will remain illuminated while unit is in this mode.

3 STOP pushbutton. An interlocked pushbutton switch which terminates all tape motion.

4 FORWARD RUN pushbutton. An interlocked pushbutton switch that allows tape unit to proceed forward at normal speed. Depressing STOP pushbutton or EOT marker will terminate this operation.

5 REVERSE RUN pushbutton. An interlocked pushbutton switch which allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton or BOT marker will terminate this operation.

6 FAST FORWARD pushbutton. An interlocked pushbutton switch that allows tape unit to run forward at high speed. Depressing STOP pushbutton or EOT marker will terminate this operation.

7 FAST REVERSE pushbutton. An interlocked pushbutton switch that allows tape unit to run in reverse at 150 ips. Depressing STOP pushbutton or BOT marker will terminate this operation.

8 LOAD POINT indicator (LED). Indicates when tape is at load point.

9 EOT indictor (LED). Indicates when tape is at EOT.

10 HDS indicator (LED). Indicates when data is being processed by read/write electronics.

11 SKEW indicator (LED) and TEST point. Indicator lights if tape skew exceeds the appropriate skew (read or write) gate setting. an oscilloscope TEST point is available for monitoring all read pulse outputs simultaneously, displaying total bit scatter.

Figure 2-32. Controls and Indicators (Sheet 2 of 2)

2.3.1.1.6.2.3 Interface Specifications.- The interface connectors on the Model 9000 are designed for twisted-pair inputs and outputs. For each active pin there is a ground pin. Two 44-pin edge mating connectors are supplied with the tape unit for interface connections.

The tape unit responds to zero-true inputs and provides zero-true outputs. Each signal input is terminated to provide matching for twisted pair cables. Each output line is driven with an open collector driver.

The input receiver circuits, due to zero-true current sinking logic design, interprets a disconnected wire or power removal at the transmitter as a logic zero or false condition. The logic 1 (true state), requires 25 ma current sink with less than 0.4 V. The logic 0 (false state), is 3 V due to the input matching resistors. The recommended input pulse width is 2 microseconds.

The rise and fall times for pulses and levels must be less than 0.5 microsecond. Each input is enabled when the tape transport is on line and selected.

Each output line is driven with an open collector current-sinking logic-driver capable of sinking up to 40 ma in the true state. All outputs are disabled (false) when the tape unit is not on line and selected.

The tape transport capstan servo accelerates the tape to the required speed with a linear ramp. The tape is also decelerated to a stop with a linear ramp. Start and stop occur within the interrecord gaps. T ramp time is 15 ms for 25 ips and varies inversely with tape speed. The amount of tape travel during the ramp-up or ramp-down is always 0.1875 inch. These two factors must be considered when writing and gapping. A delay is required before writing to ensure that tape is up to speed to allow a read after write. Timing diagrams for pertinent commands to provide properly formatted tapes are shown in figures 2-33, 2-34, and 2-35.

Figure 2-33 shows the timing requirements for writing a block in a read after write system (dual gap head) in the write mode with read occurring immediately after writing. Figure 2-34 shows the timing requirements for forward reading of a block on a read-after-write system. Figure 2-35 shows the timing requirements for reverse reading of a block on a read after write system.

2.3.1.1.6.3 Line Printer.- The line printer is a Printronix P300, 300-line per minute device. Two printers are provided as a part of the COTC. The line printer interfaces to the T16/6304 asynchronous controller. The printer is a 300-line per minute

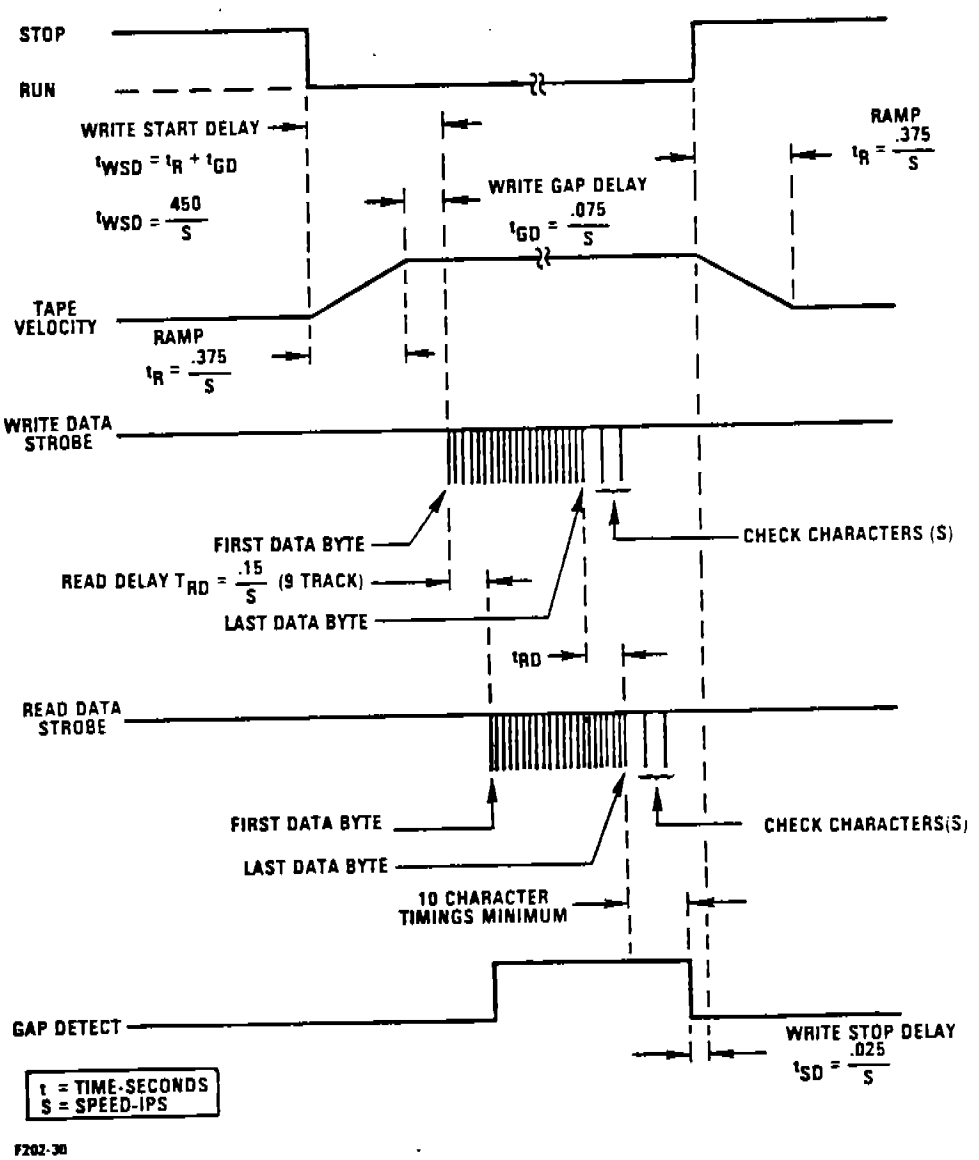


Figure 2-33. Read After Write Tape Transport Write Start and Stop Delays

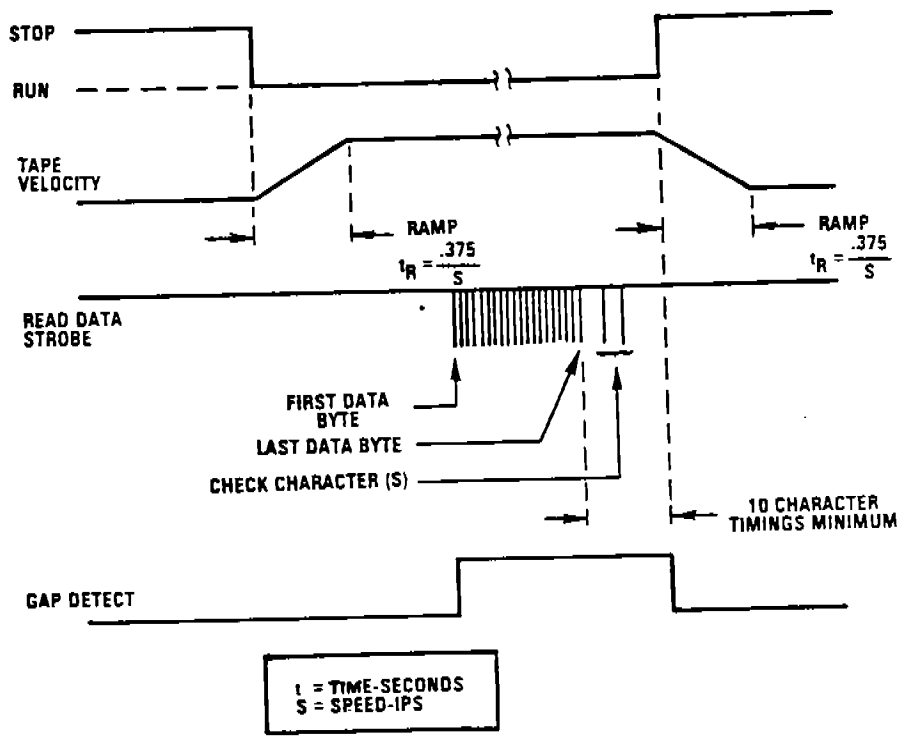


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Figure 2-34. Read After Write Tape Transport Reading Forward

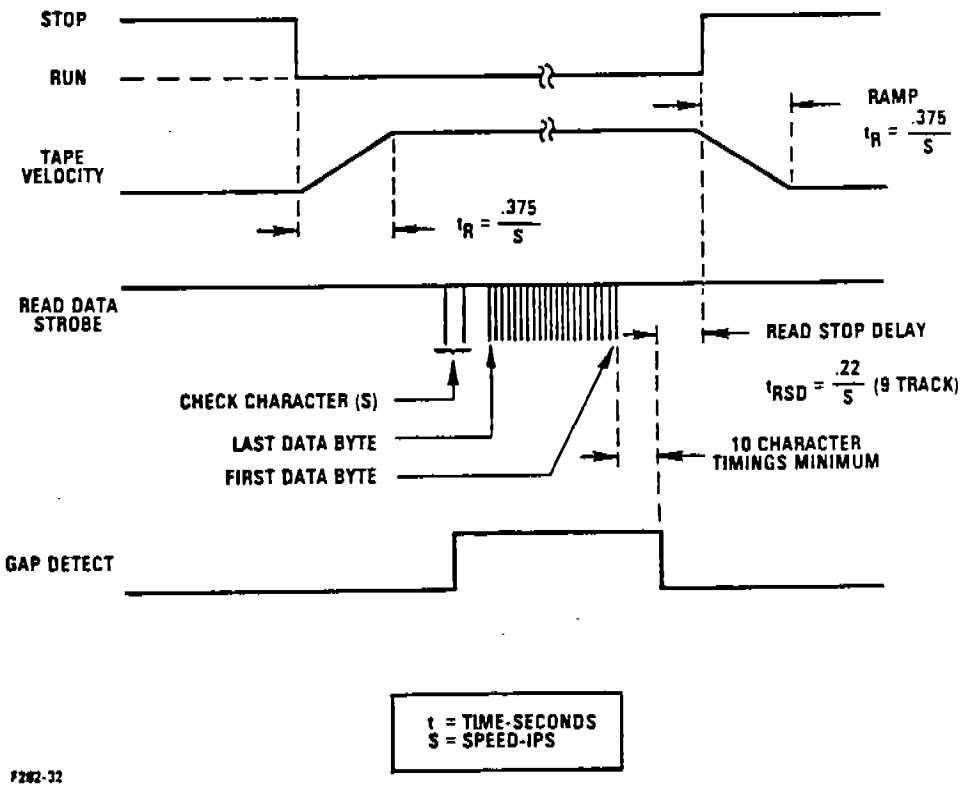

Figure 2-35. Read After Write Tape Transport Reading in Reverse

132-column dot matrix printer that prints multiple copies with a unique hammer-bank mechanism. It differs from moving-head matrix printers which print a full line of characters simultaneously.

There are 44 leaf-spring hammers positioned horizontally at every third character position which retract with a common, permanent magnet. The hammers are mounted on a shuttle which sweeps the hammers across three character positions (0.3 inch, 0.76 cm, movement). As the shuttle sweeps across, the hammers are activated at each position where a dot is required. While the shuttle is being slowed at the end of its movement and accelerated in the reverse direction, the paper-feed moves the paper one dot row increment, and the shuttle sweeps across in the reverse direction again distributing dots. This process continues through a total of seven sweeps (for standard character size) until a line of complete characters is built. The paper is then advanced a distance equal to line separation and the process is repeated.

2.3.1.1.6.3.1 P300 Line Printer Specifications.- Table 2-23 lists the specifications for the P300 Line Printer.

2.3.1.1.6.3.2 Operating Controls and Indicators.- Table 2-24, Operator Control Panel, provides a description of the printer controls and indicators located on the operator control panel.

2.3.1.1.6.3.3 Interfacing Characteristics.- The line printer interface is a buffered serial interface adaptor that converts EIA RS-232 signals into parallel formatted data. Data is received in serial form according to EIA standard, RS-232C, assembled into parallel data, stored in a buffer memory, and then routed to the printer. The serial data rate is switch selectable from 150 baud to 9600 baud. In the M1FC FSAS system the 9600 baud rate is used. Parity is switch selectable for odd, even, or parity ignore.

The RS 232 interface consists of a single printed circuit board that is plugged into the spare slot in the printer card cage. A power and a clock signal are supplied by a common bus connector. Included is a self-test mode switch. When this switch is in the run position, it will print a recycle pattern 132 columns wide on the printer. In the stop position the RS 232 interface is energized.

PERFORMANCE SUMMARY

Serial Data Rates (Baud):

9600, 4800, 2400, 1200, 600, 300, 150 Switch Selectable

Table 2-23. P300 Line Printer Specifications

Print Speed:

300 lines/min for a character set size.

170 lines/min when printing double height characters.

240 lines/min when printing underlines or characters with decenders.

Characters per line: up to 132

Line advance time: 33 ms 6 LPI (maximum)

25 ms 8 LPI (maximum)

Paper slew speed: 8 inches (20.3 cm) per second (minimum)

96 character ASCII standard
up to 160 characters optional

CHARACTER REGISTRATION

Horizontal within a line ± 0.005 inch (0.0127 cm)

Vertical within a line ± 0.005 inch (0.0254 cm)

LINE SPACING

0.167 inches (0.424 cm) ± 0.010 (0.0254 cm)
non-accumulative @6 LPI

0.125 inches (0.318 cm) ± 0.010 (0.0254 cm)
non-accumulative @ 8 LPI (switch or character code)
$(006)_8$ selectable

MATRIX

9 x 7 dot matrix (9 x 9 for lower case with descenders, 12 x 9 full width character option).

Horizontal: 5 overlapping dots on 9 centers.

Vertical: 7 overlapping dots.

ELECTRICAL CHARACTERISTICS

Voltage	100, 110, 120, 200, 220, 240, +10%, -15%
Frequency	50, 60 Hz ± 2 Hz
Power	800 Watts maximum continuous load, 450 Watts nominal continuous load, 200 Watts standby

Table 2-24. P300 Line Printer Operator Control Panel

Power Indicator: An indicator that is lit when primary power is on.

Check: A switch/indicator that is lit when:

1) the paper supply is exhausted or the form is torn below the print station,

2) platen is in the load position,

3) there is a DC power supply fault, and/or

4) there is a paper motion fault.

NOTE: The Check switch must be depressed to clear the paper motion fault logic.

Top of Form: A momentary switch/indicator that causes paper to move to the top of the next form. This switch is enabled when the printer is not on line. The indicator is lit when the VFU is loaded.

8 LPI: A momentary switch/indicator that causes the paper to be printed at 8-lines per inch. Switching to and from the 8-lpi mode can be done only when the printer is not on-line. The indicator is lit in the 8-lpi mode.

NOTE: 8 lpi is program selectable on a line basis.

On-Line: A momentary switch/indicator that enables the interface, and disables the 8-lpi, TOF, and paper advance switches. The indicator is lit in the on-line state.

Paper Advance: A momentary switch that advances paper at five inches (12.7 cm) per second as long as the switch is pressed. This switch is disabled when the printer is on-line.

Parallel Data Rate to Printer:

125,000 characters/second

Serial Data Format:

7 or 8	Data bits
1	Stop bit
1	Parity bit

Table 2-24. P300 Line Printer Operator Control Panel (Continued)

Buffer:

1024 character first-in, first-out buffer.

Power:

+30 Volts @ 50 ma
+5 Volts @ 900 ma
-30 Volts @ 50 ma
Power is supplied thru J2

2.3.1.1.6.3.4 Electronic VFU.- The Electronic Vertical Format Unit (EVFU) is a reliable, software-operated vertical formatter. The EVFU is loaded and operated entirely by software, without operator intervention - a significant advance in reliability, convenience, and performance.

The EVFU accommodates up to 14 VFU channels, permits variable form lengths up to 22 inches, sets vertical tab stops, and controls slewing within the form.

The computer program causes the EVFU semiconductor memory to be automatically loaded through the data lines. Subsequent channel codes cause paper to advance in steps that define the vertical format of the form as it is printed.

The EVFU is automatically reloaded for a different form. Paper is simply advanced to the top of the next form, and the new form is printed automatically. No shut-down, no paper tapes, and no lost time.

The EVFU may be used in three different ways, as follows:

1) to simply establish different form lengths;

2) using Channel 12 as a vertical tab stop to slew within the form; or

3) using the full multi-channel capability of the EVFU.

2.3.1.1.6.4 Coded Time Source (CTS) Interface.- The CTS interface resides in the communications switching rack and performs the following three functions:

1) accepts parallel data from the CTS clock output and serializes the data for input to a Tandem asynchronous port;

2) provides a continuous time comparison of the two CTS clock inputs with its internal clock. If a discrepancy is detected, an error code is sent to the Tandem; and

3) provides the relay contact closures for the SMMC.

Four connectors are provided for cabling the clocks and asynchronous port. LED's located on the CTS chassis provide a parallel read-out of station time currently being read by the Tandem.

Figure 2-36 is a block diagram of the CTS interface illustrating the main functional area. The CTS interface is designed to operate at a baud rate of 300 bps.

2.3.1.1.6.5 Coded Time Source.- The CTS is a Model 60-DC WWVB Synchronized Clock manufactured by True Time Instruments. The CTS receives the National Bureau of Standard radio station WWVB, which transmitts on 60 kHz. Two CTSs provide the time information to the coded time source interface, and a visual time read out on the front panel.

2.3.1.1.6.6 Thermal Alarm.- The Thermal Alarm monitors the exhaust air temperature of the equipment racks to ensure that the temperature remains within specifications. The Thermal Alarm Unit provides both a visual and an audible alarm system.

2.3.1.1.7 FSDPS Power Distribution.- The power distribution is divided into AC and DC power descriptions.

2.3.1.1.7.1 AC Power.- E-Systems provides all branch circuit cables for the FSDPS equipment. These power cables are installed in accordance with the National Electrical Code and are routed under raised floors. All but one of the branch circuits for the M1FC FSAS originate at a GFE provided power panel. The single exception is a 20 ampere, single pole circuit which is located in a GFE pull box under the raised floor. This circuit is used for the convenience outlets located in the bases of the E-System Position Equipment (EPE) racks.

The FSDPS requires a minimum service capacity of 45 KVA, 125 amperes per leg to ensure satisfactory operation. This estimate of service capacity is based on OEM handbooks and preliminary system design data. The estimate also assumes the strict use of system start up procedures which require sequential turn on of equipment to prevent excessive in-rush of current. (The disk drives must be manually turned on in sequence rather than allowing the automatic power sequencing devices to operate. Use of automatic sequencing would result in three drives activated simultaneously, one in each of the three pairs, and an in-rush current of 76 amperes per leg above the existing load.)

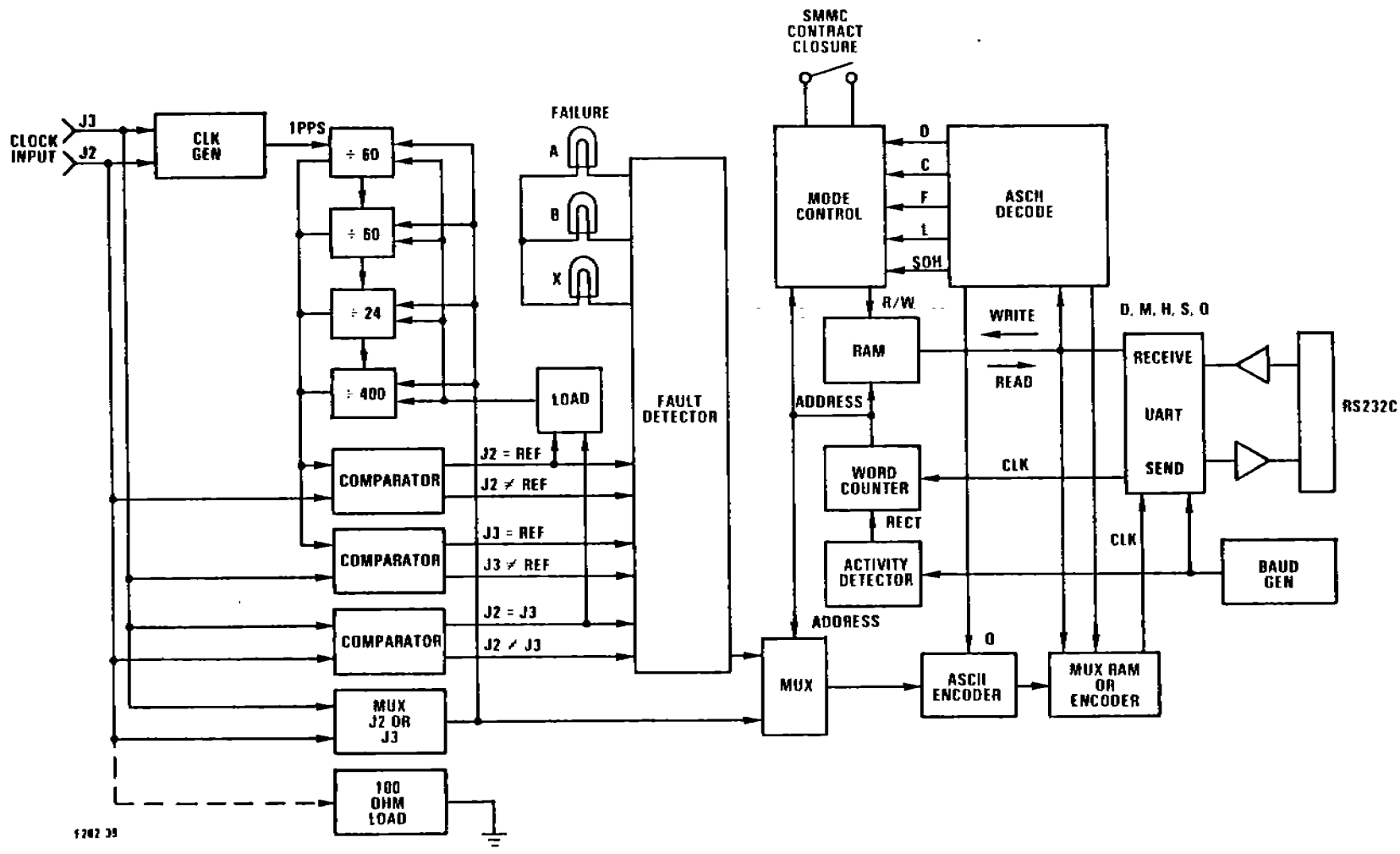

Figure 2-36. Coded Time Source Interface

The Government is required to provide and reserve the power panel CM-1, and provide in the power panel, circuit breakers as follows:

40 ampere, three pole - four each
30 ampere, three pole - three each
30 ampere, single pole - three each
20 ampere, single pole - eight each

(These breakers will conform to FED-SPEC W-C-375.)

Figure 2-37 shows an arrangement for balancing the loads within the panel. The specific load distribution is provided in the as-built drawings for each FSDPS.

The Government also provides one 20 ampere circuit in a pull box under the raised floor for essential power connection.

For detail electrical layout refer to Section 7, figure 7-5.

2.3.1.1.7.2 DC Power.- The DC power distribution is depicted in Figure 2-38, DC Power Distribution. It has the following attributes:

1) separate power supply for each processor module,

2) Separate uninterruptible power source (battery pack) for each semiconductor memory processor, and

3) power switching between two independent power sources for I/O controllers and IPB controllers.

AC power is distributed to the T16/7301 Power Modules, the UPS Battery Packs, the fans, and the T16/5103 Magnetic Tape Unit by the AC Distribution Unit.

The DC voltages provided by the T16/7301 Power Module are:

+5 VDC IPS/IPS @ 100 amperes
+5 VDC UPS/IPS @ 18 amperes
+12 VDC UPS @ 4 amperes (semiconductor memory)

IPS = Interruptible Power Source
UPS = Uninterruptible Power Source

DC power is delivered to each processor module by a processor DC power bus, which consists of five individual buses laminated together to form a single unit. The bus delivers +5 VDC IPS, +5 VDC UPS, +12 VDC UPS, DC ground, and memory ground to the processor.

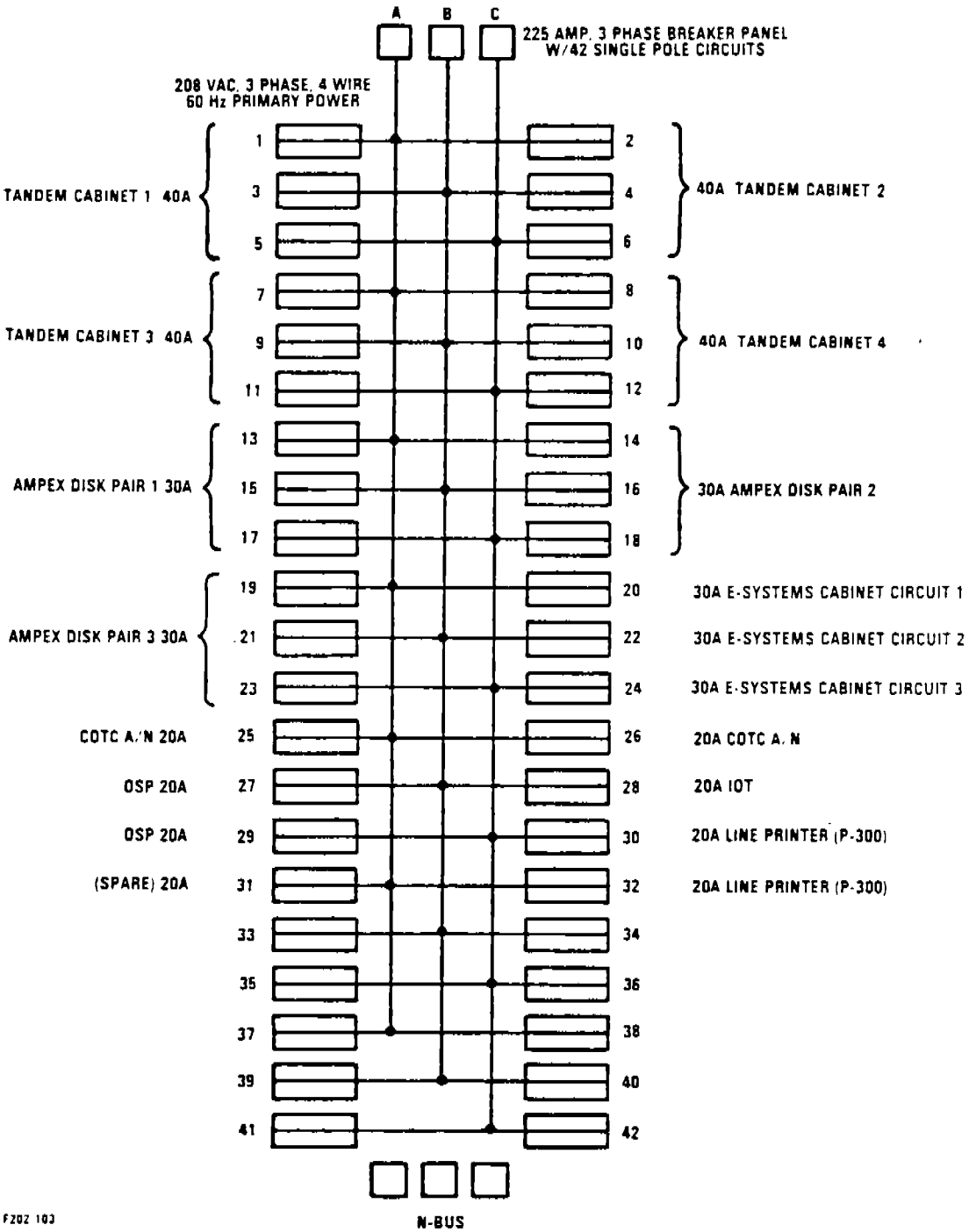

Figure 2-37. Main Power Distribution Panel, M1FC FSDPS

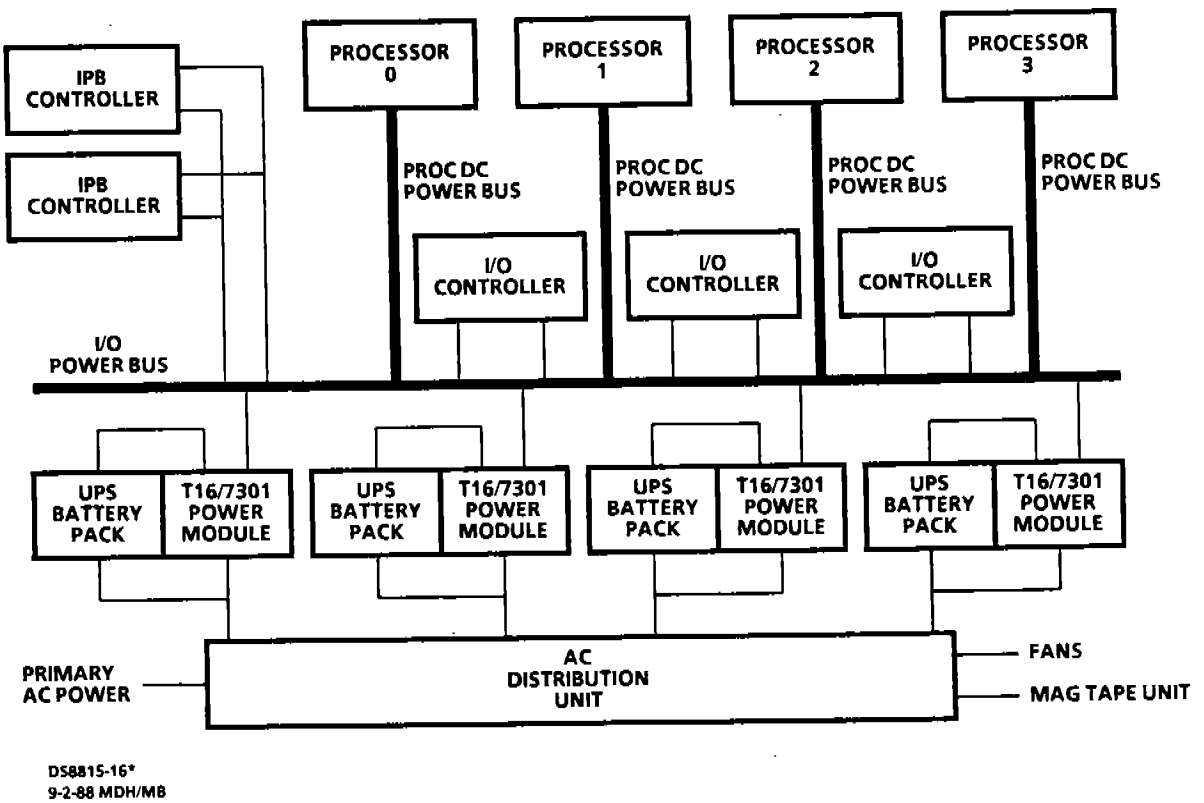

Figure 2-38. DC Power Distribution

A single I/O DC power bus delivers DC power from the +5 VDC IPS supply to the I/O controllers. The bus consists of nine individual buses that are laminated together to form a single unit. Voltage is supplied to the bus from each T16/7301 Power Module. Voltage taps along the bus allow the I/O controllers and IPB controllers to be electrically distributed among the power modules. DC power switching takes place on the I/O lower backplane board. These electronic switches deliver +5 VDC IPS from either of two power modules to the I/O controller boards. If a failure occurs in either power module, the switch transfers to the operational power module. A single switch delivers DC power to two I/O slots.

This section contains a detailed description of the DC power modules which support the processors, I/O controllers, and communications controllers. Three power modules are required to support the Tandem processors and controller.

These modules are manufactured by Tandem and are:

1) T16/7900 Power Module,
2) T16/7301 I/O only Power Module, and
3) T16/7303 Battery Module.

The following sections describe these modules and their functions in the processing subsystem.

2.3.1.1.7.2.1 Power Module T16/7900.- The T16/7900 Power Module furnishes all of the DC voltages required for a processor module. The IPB controllers and I/O controllers are connected to draw primary and backup DC power from two independent power modules. The following DC voltages are generated by a power module:

+5 VDC IPS @ 100 amperes
+5 VDC UPS @ 18 amperes
+12 VDC UPS @ 4 amperes (semi-conductor memory)
+15 VDC IPS @ 6.5 amperes (core memory)

Refer to figure 2-39, T16/7900 Power Module Block Diagram. The rectifier supplies unregulated +34 VDC to the main inverter which generates the +5 VDC IPS output. It also supplies +60 VDC to the UPS inverter which generates the +5 VDC UPS output. The linear amplifier uses +20 VDC from the UPS inverter to generate the memory voltage output of either +12 VDC UPS or +15 VDC IPS.

If power fails, +48 VDC is supplied to the UPS inverter from the UPS Battery Pack (semiconductor memory processors only). The UPS inverter and linear amplifier remain operational, and data in semiconductor memory is preserved.

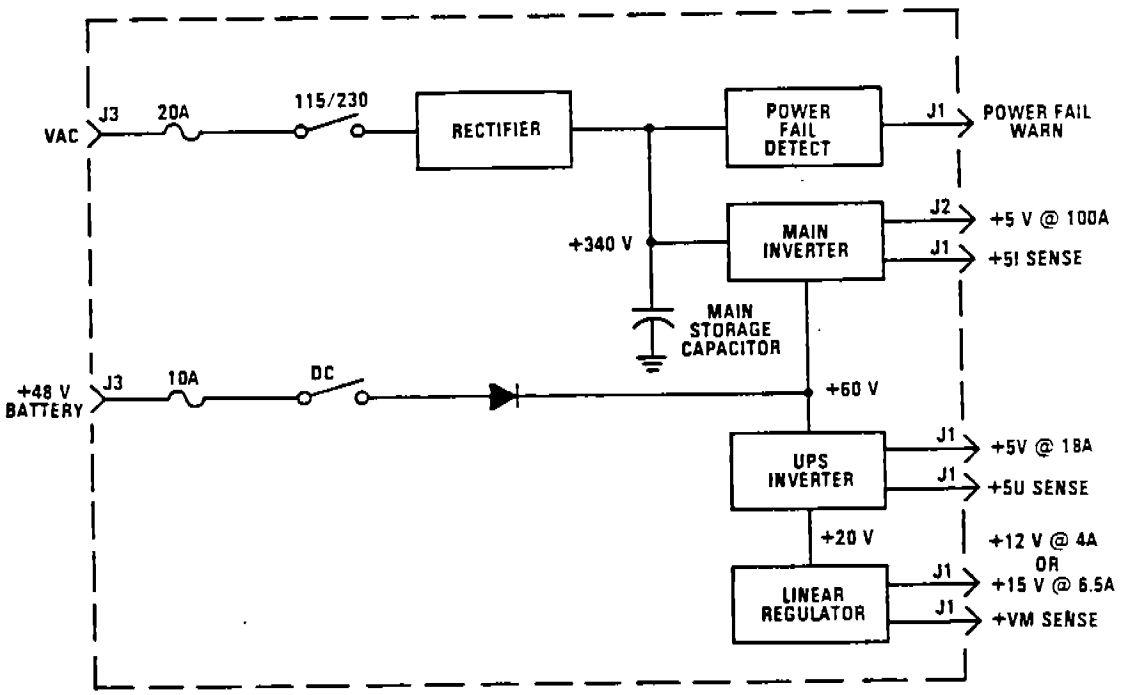

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Figure 2-39. T16/7900 Power Module Block Diagram

The power-fail detect circuit constantly monitors the charge on the main storage capacitors. The circuit is adjusted so that the Power-Fail Warn (PWARN) signal goes active 5 milliseconds before the main inverter becomes inoperative due to a loss of the rectifier output. This allows the operating system in the processor to perform its power-fail interrupt procedure before the +5 VDC IPS supply is lost.
The following controls and indicators are located in the T16/7900 module:

1) 115V POWER switch - Controls primary power to the rectifier;

2) DC POWER switch - Controls the +48 VDC battery source to the UPS supplies. When set to ON, +48 VDC from the UPS Battery Pack is applied to the UPS circuits. When OFF, the +48 VDC battery source is disconnected;

3) 5V/18A indicator - When lit, indicates that +5 VDC UPS is available at connector J2;

4) 5V/18A indicator - When lit, indicates that +5 VDC UPS is available at connector J1; and

5) 12V/15V Indicator - When lit, indicates that +12 VDC UPS is available at connector J1.

2.3.1.1.7.2.2 I/O Only Power Module T16/7301.- This module is identical to the T16/7900 except that it provides only +5 VDC at 100 amperes and does not have power-fail detection circuitry. The T16/7301 is used to support the I/O power bus when the T16/7900 module does not provide sufficient power to support the I/O load. The power I/O module has a 115 VAC power switch and a 5V/100A indicator.

2.3.1.1.7.2.3 Battery Module T16/7303.- Battery packs are installed for semiconductor memory processors only. The battery pack supplies +48 VDC to the T16/7900 Power Module during periods of ac power loss. This +48 VDC source allows the power module to sustain its UPS power supplies (+5 VDC UPS and +12 VDC UPS) if AC power fails. If the batteries are fully charged, the UPS voltages can be sustained for up to 80 minutes, based on a semiconductor memory processor with two memory boards (768 Kbytes).

See figure 2-40, UPS Battery Pack Block Diagram. During normal operation, the charge on the batteries is maintained by a charger on the UPS Control Board. When fully discharged, the batteries can be recharged to 90 percent of full-charge in approximately 8 hours and to 100 percent in approximately 15 hours. The nominal charge voltage (with batteries near full charge) is +55 VDC. If this voltage rises above +60 VDC, a crowbar circuit is activated and the 2 ampere fuse on the UPS Control Board blows. The charger is current limited at 1.4 amperes of charge current.

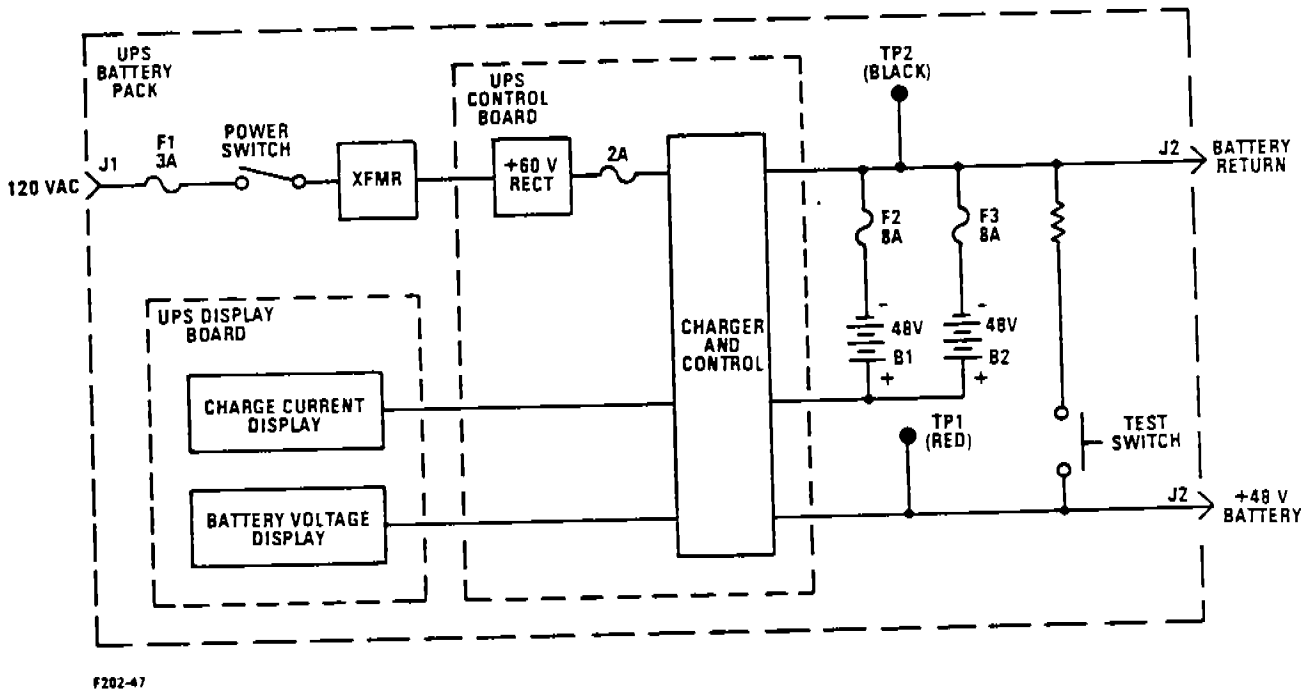

Figure 2-40. UPS Battery Pack Block Diagram

The UPS Display Board contains LED displays for both charge current and battery voltage. The displays permit the customer engineer (CE) to quickly check the operation of the battery pack. The following switches and indicators are provided on the battery module:

1) POWER switch - When set to ON, AC power is applied to the UPS Control Board. DC voltages are developed on the UPS Control Board for the charger control circuits and the UPS Display Board;

2) TEST Switch - By placing a 5 ampere resistive load across the batteries the switch tests the batteries and the operation of the charger. While ON, the CHARGE CURRENT indicators should register 10 (approximately 1.4 amperes), and the BATTERY VOLTAGE indicators should not drop below 6 (approximately 40 VDC);

3) CHARGE CURRENT Indicators - Twelve LED's indicate the level of charge current being supplied to the batteries in 140 milliamp steps. Since the charger control circuits are set to current limit at 1.4 amperes, these indicators should never register above 10. The indicators are inoperative during AC power outages; and

4) BATTERY VOLTAGE Indicators - Twelve LED's indicate the battery charge voltage from 30 VDC to 6 uV in 2.5 VDC steps. When the batteries are near full charge, these indicators should register 10 (55 VDC). They should never register below 6 (40 VDC). The indicators are inoperative during AC power outages.

2.3.1.1.7.2.4 I/O Power Bus Connections.- DC power (+5 VDC IPS) is delivered to the I/O board slots from the I/O DC power bus. Each pair of I/O board slots is fed from two independent sources (power modules). Power switching for each pair of I/O board slots takes place on the I/O lower backplane boards. If a power module fails, these switching circuits transfer to the operational power module.

The DC power switching circuits for a pair of I/O board slots are depicted in figure 2-41, I/O Power Switching Functional Diagram; all components are located on the I/O lower backplane board. Note that each I/O board slot may be powered-down independently for maintenance purposes. In addition, each power source and each I/O board slot is separately fused.

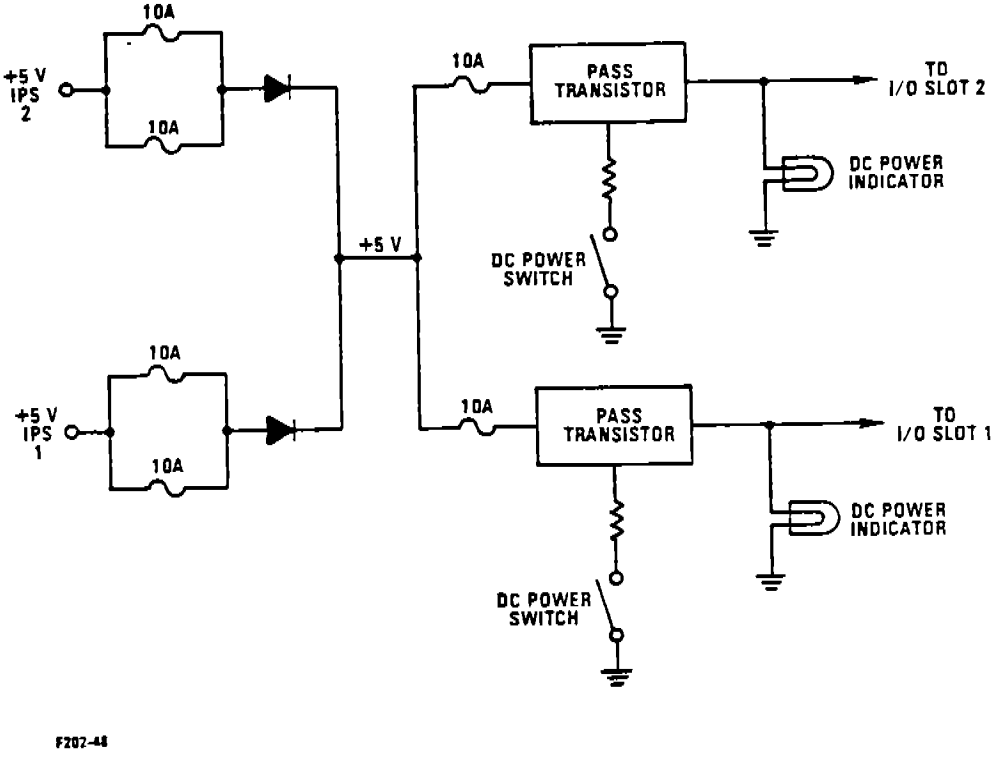

Figure 2-41. I/O Power Switching Functional Diagram

2.3.1.1.7.2.5 Interprocessor Bus (IPB) Power.- DC power (+5 VDC IPS) is delivered to the IPB controllers from the I/O DC power bus. Power-switching between two independent power sources (power modules) takes place on each IPB controller board. If a power module fails, these switching circuits transfer to the operational power module.

The DC power switching circuits are depicted in figure 2-42, IPB DC Power Functional Diagram. Note that each power source is separately fused and that each IPB controller can be powered-down independently for maintenance purposes.

2.3.1.1.7.2.6 Power Supply Assembly.- The Power Supply Assemblies, 401-36716-01, are LH Research MM43 Power Supplies which have been modified for placement in M1FC FSAS equipment racks. The power supplies supply the following DC voltages to the E-Systems card cages.

+12 VDC
-12 VDC
+5 VDC
signal ground

The power supplies and card cages are located in the COTC position processor rack at the FSDPS. All other equipment located in the E-Systems equipment racks contain internal power supplies. For detail description refer to the individual equipment manuals listed in table 1-1.

2.3.1.2. Maintenance Equipment.- To support the maintenance of the hardware supplied for the M1FC FSAS, diagnostic equipment is provided as a part of the total system configuration. The OSP is provided for the testing of the Tandem Computer system. The A/N terminals are provided for running diagnostics on the E-Systems Position Equipment (EPE) as is the IOT. The MADTS is provided for testing LRUs off line.

Local and remote testing of communications hardware is supported by loop-back capabilities built into the modem hardware. The support hardware falls into two areas; processing subsystem test and computer test. For computer testing refer to the Tandem OSP User's Guide and the Diagnostic Operating Procedures (T16/8803).

2.3.1.2.1 Maintenance and Diagnostic Test Set (MADTS).- The MADTS consists of a RM-8E Modem Enclosure, a TTL-150 Monitor, a digital patch panel, a control panel, an electronic drawer, and an RL01 Disk Drive. An LA34-AA or LA100-CA terminal is also included as part of the MADTS. See figure 2-43.

The MADTS includes two unique controllers for exercising the Ampex disks and Kennedy tape drives.

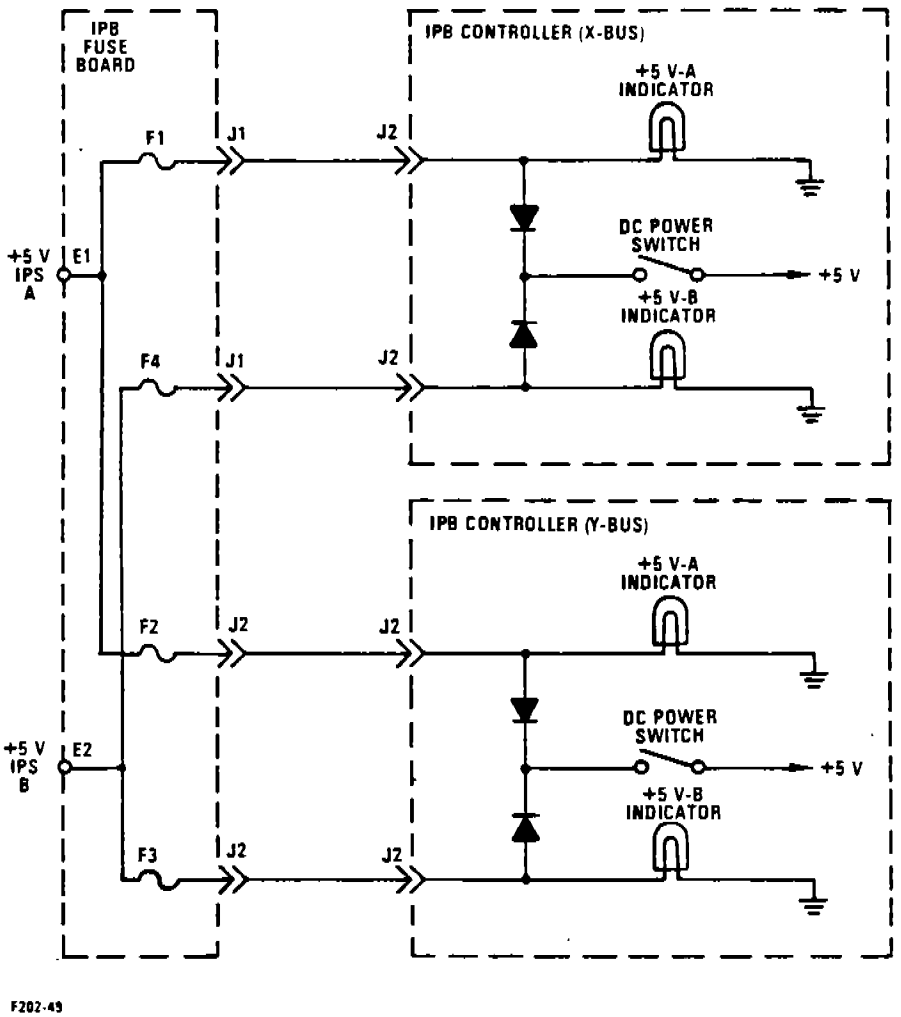

Figure 2-42. IPB DC Power Functional Diagram

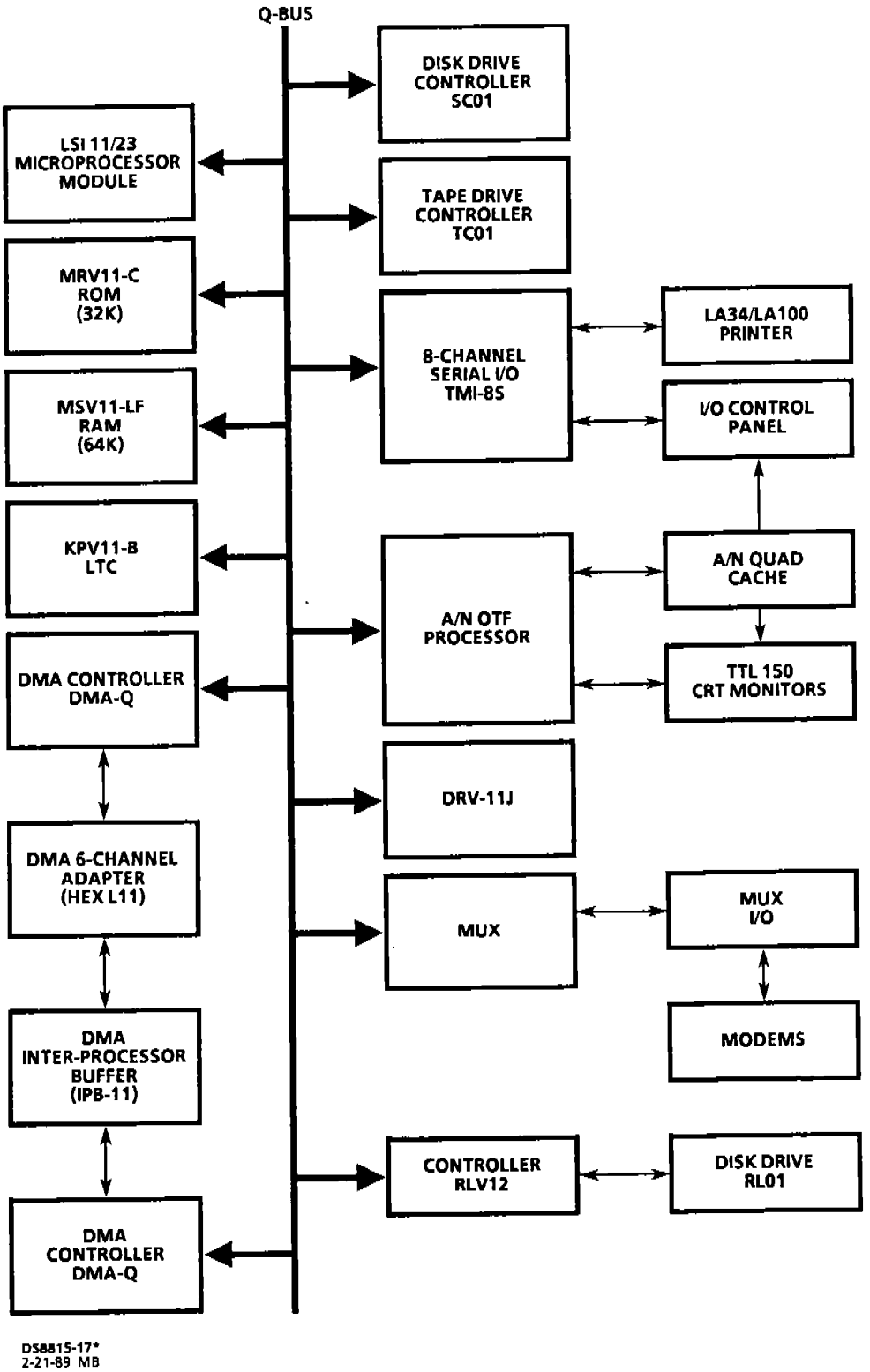

Figure 2-43. MADTS Block Diagram

Asynchronous serial interfaces are provided to support testing of the following peripherals:

1) line printer,
2) IOT,
3) AAU (Automatic Answer Unit), and
4) keyboards.

Synchronous and asynchronous interfaces provide testing capabilities for all communications hardware, including ADCCP protocols.

The MADTS is an LSI-11 based system which provides diagnostic testing and/or troubleshooting capability for certain Line Replaceable Units (LRUs). These LRUs are listed in the MADTS Instruction Book (TI 6490.41).

2.3.2 Automated Flight Service Station (AFSS).- The following paragraphs describe the communications equipment rack, the communications processor rack, the position processor rack, and peripherals at the AFSS. The communications equipment rack provides communications and patching capability for the AFSS system. The processors designed by E-Systems enhance the capabilities of the vendor equipment through redundancy, simplicity of design, and thorough automated circuitry checks. The functional block diagram for AFSS is shown in figure 2-10.

2.3.2.1 Communications Equipment Rack.- The communications equipment rack consists of a thermal alarm panel, an analog patch panel, two digital patch panels, and three disk drives. The communication equipment provides communications and patching capability for the AFSS system. Communications protocol between the M1FC FSDPS and the M1FC AFSS is under Advanced Data Communications Control Procedures (ADCCP). Four dedicated lines between the FSDPS and the AFSS are used. Each line is connected through the analog patch panel. This arrangement results in four parallel redundant communication channels, any of which can fail without causing a communications failure between FSDPS and AFSS. A failure in any of the redundant communication paths is detected at the FSDPS automatically; no operator action is required for all communications to be routed into a different path. Backup dial capability is also provided.

2.3.2.1.1 Analog and Digital Patching Facilities.- Network management and the required access to the system communications facilities are provided by the analog and digital patch panels. Each modem is accessible on both the digital and analog interfaces. Modem to line, modem to controller, and modem to dial-up facility configurations can be changed to provide flexible network management and reconfiguration flexibility with minimum end user impact.

2.3.2.1.2 Disk Drives.- The disk subsystem consists of a disk drive controller (DEC RLV12) and a 5.2 megabyte disk drive (DEC RL01-AK) or a 10.4 megabyte disk drive (RL02-AK). The disk controller monitors and reports hardware error and status information for both the controller and the disk drive. Average access time is 60 to 65 milliseconds. The RL01/RL02 also includes closed-loop track following, which eliminates all calibration requirements. The RL01/RL02 system is direct memory accessed.

2.3.2.1.3 Thermal Alarm.- The Thermal Alarm Unit, 401-37155-01, monitors thermal sensors located in the communications processor rack and position processor rack(s). Both a visual and audible alarm are observed at the thermal alarm unit when an overtemperature condition exists in the racks.

2.3.2.2 Communications Processor Rack.- Three communications processors reside within the communications processor rack. Each communications processor is a stand alone unit even though two are housed in the same card cage. There is a bi-directional, parallel direct memory access (DMA) data transfer between one communications processor and one position processor.

The communications processor rack also includes modem equipment and modem sharing devices (MSDs). The communications processor establishes handshakes to interface incoming data to the LSI-11 bus, performs cyclic redundancy checks as required by the ADCCP protocol, and directs alphanumeric products to the selected processor. It contains a communications multiplexer, an LSI-11 group, an interprocessor communications bus controller, and a DEC RLV12 Disk Controller. The communications processor contains a 32K word PROM memory board for the operating system and a 64K word RAM memory board for the temporary storage of alphanumeric products. The four primary duties of the communications processor are:

1) the switching and distribution of alphanumeric messages;

2) the storage, retrieval, and distribution of alphanumeric products;

3) Advanced Data Communications Control Procedures (ADCCP) protocol generation; and

4) interprocessor communications control.

Incoming data from the FSDPS is received through the multiplexer, which provides the necessary interface between the DEC Q bus and the patch panel equipment. After being multiplexed, incoming data is placed on the communications processor internal Q bus. The data on the Q bus is routed by the LSI-11/23 either to the communications multiplexer or over the interprocessor buses to the

position processor. The interprocessor communications is a multidrop system using parallel direct memory access (DMA) channels. Processor communication selection is handled on a daisy-chain priority interrupt protocol.

Each processing subsystem includes a system support module. This module combines the functions of real time clock, bootstrap loader, bus termination, and power-fail and restart circuitry. This combined function module achieves more efficient use of backplane space than do the separate elements provided by DEC. Down-line load software may be installed in the PROM Bootstrap area of this board as well as other DMA handlers and system start-up application programs. The communications processor execution is event driven, and does not require a real time clock. However, certain periodic functions required in an AFSS center create a need for timekeeping ability. Termination is required on both ends of the LSI-11 sub-unibus.

The communications architecture is structured around a control/data or A bus and an input/output (I/O) bus. DMA data transfer is interlocked so that data is transferred from the communications processor to the position processor. The position processor is identified by decoding three identifier bits in the control register. The communications processor generates all required protocol, such as: bus handshaking, bus time out, interrupt request, and interrupt vectoring. The communications processor has a self-contained bootstrap loader. External interrupts are initiated by:

1) a flag condition initiated by an interrupt request from the position processor,

2) an external power failure or shut-down,

3) a predefined bus error, and

4) a word count zero condition.

The DMA interface supports two basic types of interrupts (internal and external), and contains separate enable logic for each type. An external interrupt is an interrupt that is generated by a flag from the interprocessor buffer. An internal interrupt is the result of either the byte counter reaching a zero condition or of a delay in the response of an address which permits the bus time-out counter to cycle. Either one of these interrupts sets an interrupt request flip-flop located on the DMA interface. The interrupt request flip-flop then generates a bus interrupt request signal. The bus request signal remains in effect until a bus request grant is initiated by the interrupt service routine. The bus request grant resets the bus request flip-flop until a subsequent interrupt request is received.

The DMA transfer request occurs at the interprocessor buffer. The DMA interface, however, determines the size and direction of the transfer. The interprocessor buffer is merely the transfer medium. The interprocessor buffer makes a DMA transfer request. For example, the communications processor fetches the data from its memory, then makes a DMA request to the receiving position processor, and makes the fetched data available for it to write into its memory. When the position processor has completed its operation, the interprocessor buffer reinitiates the cycle. This process is repeated until the communication processor fails to respond to a DMA request. This usually happens because the byte count has been exhausted.

The status of the byte count is monitored by examining a special purpose register called the byte count register. The byte count register (located on the DMA interface) is loaded with the complement of the number of bytes to be transferred, prior to a DMA transfer. Each time a word is transferred, this register is incremented by two. When the ultimate count of 177777 (octal) is obtained, further DMA transfer is inhibited. If the internal interrupt system is enabled, an interrupt is generated.

2.3.2.2.1 Multiplexer.- Communications multiplexing is handled by an E-Systems multiplexer board installed in the communications processor. The E-Systems multiplexer board is a four channel intelligent communications interface for the Digital Equipment Corporation LSI-11 computer. The circuits are implemented on a"quad size" board using the standard DEC form factor and bus pin assignments. The logic required is contained in 103 integrated circuits of the SSI, MSI, and LSI densities, all contained in dual in-line packages. The interface to the LSI-11 Q-bus is through the four connectors on the bottom of the board. The interface for the four communications channels is through two 50 pin ribbon cable connectors near the top edge of the board. The 50 pin ribbon cables are terminated at the multiplexer I/O board, which contains four 37 pin connectors conforming to RS-449. A connector is provided for each serial communications port.

Most multiplexer functions are controlled by a microprocessor, the 8085A. The 8085A is the heart of a complete microcomputer which consists of RAM, E-PROM, four serial I/O channels, timer/counters, parallel I/O and a diagnostic display. The diagnostic display is used by the 8085A to pass information, such as self-test error codes to a maintenance technician. The parallel I/O provides control lines to various functions on the board and status information from certain circuits. The serial channels are capable of handling all communications protocols now in common use, including HDLC and SDLC. Hardware performs such functions as zero bit insertion and CRC generation/checking automatically.

Each channel is independently programmable for both mode and baud rate. External timing may also be selected under program control. E-PROMs are used to stop firmware instructions used by the 8085A CPU. The RAM is used to store message data and CPU variables. The RAM and E-PROM can be mixed in a variety of configurations by mixing IC types in the six universal memory sockets. Up to 32 Kbytes of memory can be accommodated.

The interface to the Q-bus is handled by a sequencer called the Q-bus controller, or QBC. The QBC is a slave to the 8085A for all operations except access to the control-status register by the LSI-11, in which case it responds to certain bus signals. The QBC sequences through sets of "instructions" contained in PROMS to perform the required tasks. The QBC operates at 9.12 MHZ and can perform data transfers to and from the LSI-11 main memory at the rate of four words in less than 10 microseconds. The QBC has 21 status inputs and 32 control outputs. By selecting the appropriate status input the QBC can make decisions to either increment to the next address or branch to a new address. The outputs are used to control LSI-11 bus signals and various logic on the multiplexer board.

In operation, the multiplexer board is commanded to initialize itself by the host LSI-11 in one of several selectable modes. The host can configure the four channels to be compatible with the required external device (modem, printer, etc.). A few interprocessor communications tasks are handled via the control-status register (CSR), but most operations are tasked through the LSI-11 main memory. The host sets up a control-status area in memory and then issues an interrupt to the 8085A. The 8085A then reads the designated area of memory to determine what action to take. Message data is passed in the same manner. Once a message has been transferred to the multiplexer memory, the 8085A takes care of required transmission tasks. Received messages are processed in the same way: data is collected in multiplexer RAM, passed to the LSI-11 main memory, and the LSI-11 is notified via an interrupt.

The multiplexer board can be configured to operate at any standard data rate from 50 BPS up. Four channels are supported operating at 9600 BPS each.

2.3.2.2.2 Modems.- AFSS to FSDPS communications are handled through Universal Data Systems modems. These modems operate at a data rate of 4800 or 9600 bps depending upon the specific application. Modems dedicated to FSDPS data communications operate at 9600 bps (RM-9600). Figure 2-44 illustrates the AFSS to FSDPS communications equipment including modem utilization. The 9600 bps operation utilizes, to its maximum, the data communication capabilities of the basic point to point, leased,

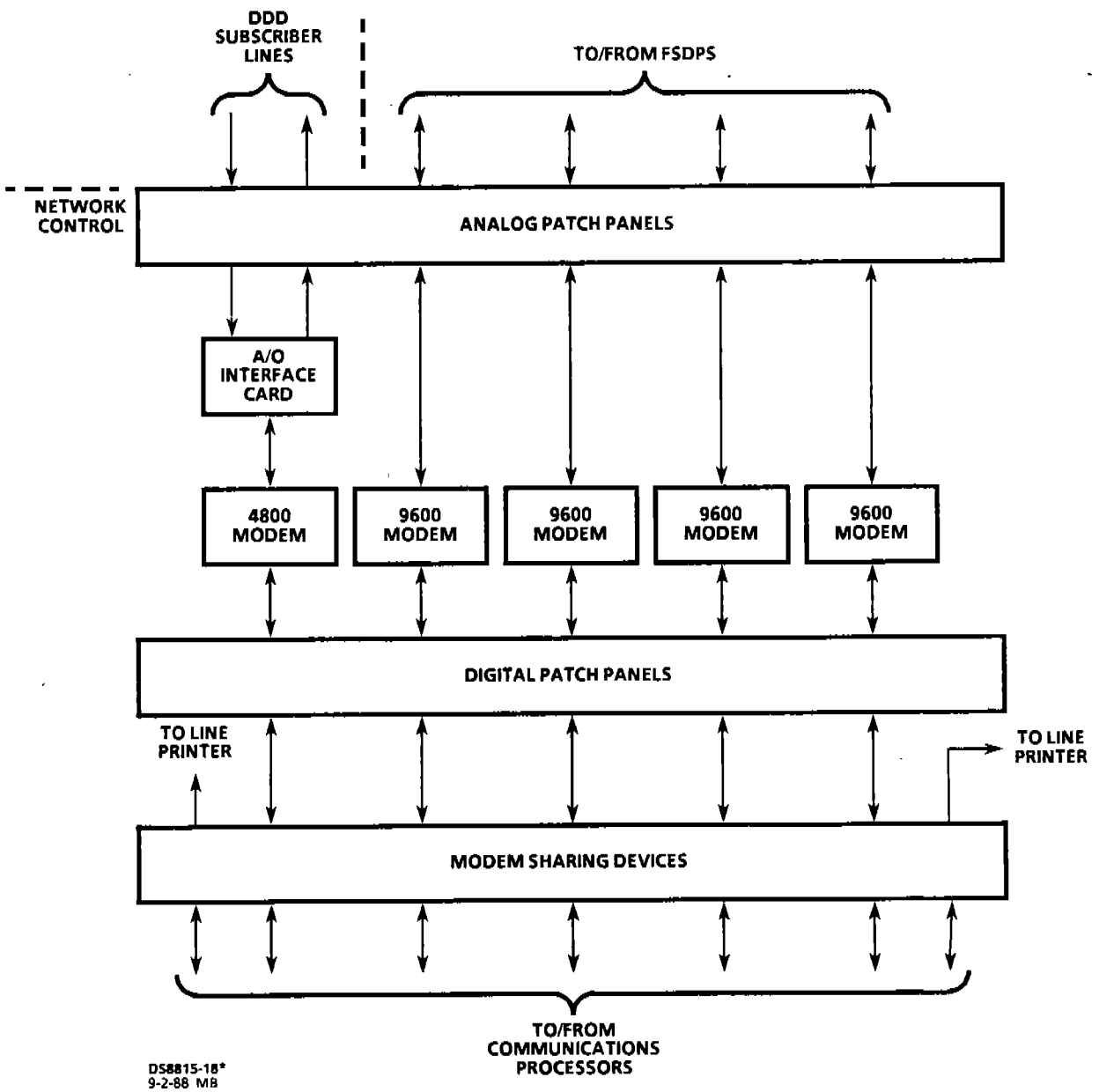

Figure 2-44. AFSS Communications Equipment

voice grade link or circuit. Modulation techniques and data recovery methods incorporated in the UDS RM-9600 Modem illustrates the highest probability of satisfactory data transfer between the AFSS and FSDPS. The modulation technique employs a 2400 baud line signalling rate, using double sideband suppressed carrier, Quadrature Amplitude Modulation (QAM). Relatively error free recovery of the data is accomplished through the automatically controlled (retrain) equalizers. The use of the UDS RM-9600 Modem provides the network with reliable operation.

2.3.2.2.3 Alternate Communications.- The dial-up facilities provide an alternate means of transferring data between the FSDPS and associated AFSSs via the DDD telephone network in the event one or both of the FSDPS-to-AFSS leased channels fail. At each AFSS, these facilities consist of a 4800 BPS full-duplex 4-wire modem with DAA interface card (configured for automatic answer). The DAA interface card connects to 2 DDD telephone network subscriber lines (2 lines required for full-duplex data communications). Dial back-up data communications are initiated by the FSDPS operator with no action required at the associated AFSS. Refer to paragraph 2.3.1.1.4.6 for the dial-up sequence performed by the FSDPS operator. Incoming calls on the DDD subscriber lines are detected by the AFSS DAA interface card which go "off hook" and supply an answer tone back to the FSDPS. When both calls have been established, the DDD subscriber lines automatically transfer to the modems (at the FSDPS and AFSS) and the terminals (at the FSDPS and AFSS) are notified to start passing data. Dial-up facilities disconnect is accomplished by dropping the Terminal Ready signal to the modems. Table 2-25, UDS RM-A/O DAA interface card specifications, identifies the basic unit specifications.

2.3.2.2.4 Modem Sharing Devices.- The communications processor rack contains seven Universal Data Systems (UDS) modem sharing devices (MSDs) which are contained in two RM-4E MSD Enclosures. These MSDs allow multiple remote data terminals to communicate by phone line using data modems without providing a dedicated modem for each remote data terminal. Each MSD provides the necessary logic, buffers, and circuitry to accept one I/O port from a synchronous modem and provides connections for four ports to external devices such as remote terminals. The incoming data to the MSD will be processed on a first-come-first-served basis from any of the four remote data terminals served.

2.3.2.3 Position Processor Rack.- There are four different configurations of position processor racks. Each rack configuration differs from the other in the type of PROMs each rack uses and/or the number of quad cache boards each rack

Table 2-25. UDS RM-AAU Auto Answer Specifications

Data Rates:

Insensitive

Mode:

Half Duplex for each DAA (CBS type)

Full Duplex with 2 DAA's (CBS type)

Auto Answer:

Circuit 1 (Call #1)
23 sec to 2 minutes abort timer

Circuit 2 (Call #2)
2nd call answer after 1st ring (if 1st call ringing)
switch modem from dedicated circuit to dial up network.

Call Termination:

DTE TR (Terminal Ready) (TR OFF)
causes immediate disconnect

Analog Interface:

-9DBM TX level

Enclosure RM-8D or RM-16 DC

contains. The different configurations are required because the number of display positions can vary from one AFSS to another AFSS. Refer to table 7-6 in Section 7 for actual rack configurations and the number of display positions each rack will support.

Each position processor rack consists of two position processors. Figure 2-45, AFSS Terminal Display Equipment, shows the relationship of this equipment. The equipment provides the command and control for data entry, retrieval, and display. There is one Peritek DMA-QB interface circuit card in each position processor. Each position processor contains an interface for each keyboard. The keyboard interface structure is completely redundant. If a processor fails, the remaining processor still has communications interface to all of the keyboards at the terminal display equipment. Associated with a position processor is a memory chassis. Each alphanumeric cache memory supports four alphanumeric terminal display positions. The maximum M1FC configuration requires three communications processors and six position processors to support 48 positions. See figure 7-19 for a 48 position AFSS.

The two position processors consist of the following modules:

1) DMA Interface - This module provides a direct memory access (DMA) data transfer from a host communications processor via the interprocessor communications bus to the position processor Q bus. The module is a Peritek DMA-QB interface board.

2) LSI-11 Group - This module contains all LSI-11 associated components that are common to the communications processor. Specifically, the LSI-11 group includes the KDF11-AA LSI-11/23 processor, MSV11-LF 64K words of system RAM, the system support module, a MRV11-C module which can contain up to 32K words of PROM, and a TMI 8S eight-channel asynchronous serial interface. Each computing group contains a KPV11-B system module which includes power failure-restart, line time clock and bus termination circuitry.

3) Alphanumeric - This group contains a minimum of two alphanumeric on-the-fly (OTF) processor cards (401-33676). The actual number of alphanumeric OTF cards is n/8 (rounded up), where n is the total number of alphanumeric display units.

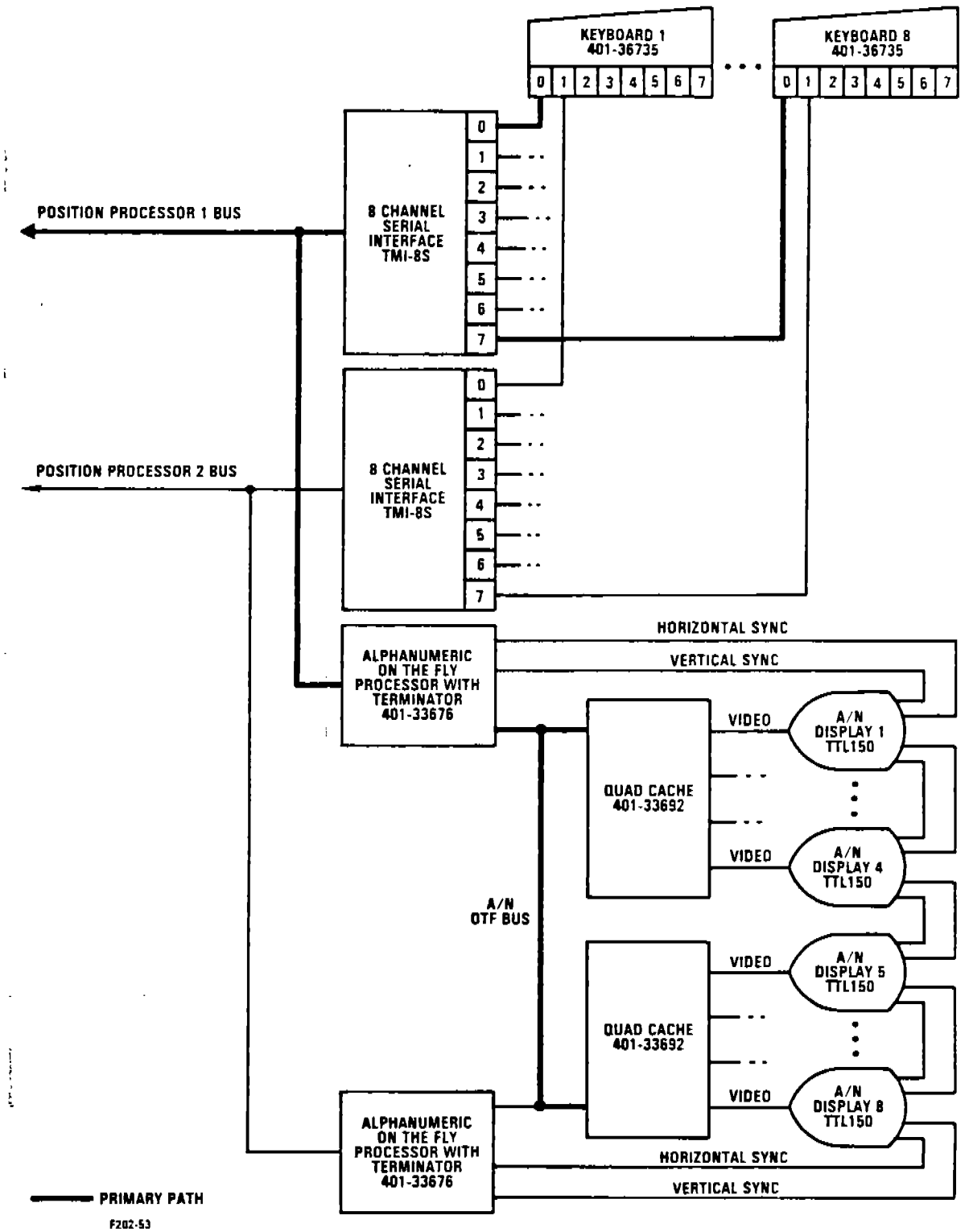

Figure 2-45. AFSS Terminal Display Equipment

The position processor employs alphanumeric quad cache memories to control the CRT displays. A cache I/O with mapping, read/write, and refresh capability controls a 2K X 16 display cache for each CRT display unit. An E-Systems Pico Processor (EPP) outputs control signals and provides horizontal and vertical synchronization signals. The EPP is crystal controlled for frequency stability and is located on the alphanumeric OTF assembly. Each cache circuit board drives four CRTs.

2.3.2.3.1 Processor Interface.- Processor interface is handled by Peritek DMA-QB interface cards. See figure 2-46, DMA-QB Block Diagram. The DMA-QB is a high performance direct memory access interface for the LSI-11. It handles all the hardware protocol of the Q bus interface: bus handshaking, bus timeout, interrupt request and vectoring, DMA request/grant, and data transfer. Sockets are provided on the interface card for two 32 X 8 Bipolar PROMs. This allows the DMA-QB to be set up for a 32 word program in the PROMs for bootstrap or other purposes. The extended addressing capability of the DMA-QB allows larger bulk memories to be mapped down to the 16-bit addressing capability of the LSI-11. Interrupt logic incorporated in the DMA-QB allows the external device power failure or shutdown. It also generates interrupts due to bus error and byte count zero conditions. The DMA modules between each communications processor and position processor handle the message traffic to and from the communications lines and the data base. These modules communicate with each other by parallel DMA transfers on the interprocessor bus. This DMA interface operates in the single cycle, synchronous mode. This means that cycle stealing is done on every other memory cycle, so that interface of computing and DMA are ensured. This is important so that processing of information by the CPU will continue. The transfer rate of the DMA-QB multiprocessor linking subsystem is approximately 800K words per second. Table 2-26, DMA-QB Specification, defines the interface requirements.

2.3.2.3.2 Bus Communication.- Bus communication is via a HEX-L11 card used as a multiprocessor linking system for the LSI-11. The HEX-L11 controller is capable of transferring 16-bit words, and can also be used in a byte mode (8-bit words). It creates a combined DMA and PIO data path between processors. It is organized to allow one processor to select and perform bi-directional transfer via direct memory access with another processing unit. Transfer status and control information is exchanged via a set of specially structured mailbox registers. Control bits within these registers are interlocked to synchronize operation. Data moving between CPUs passes through an intermediate buffer stage in the HEX-L11. Interrupt channels for each of the satellite units are incorporated to handle requests for data, request grant, and operation complete data.

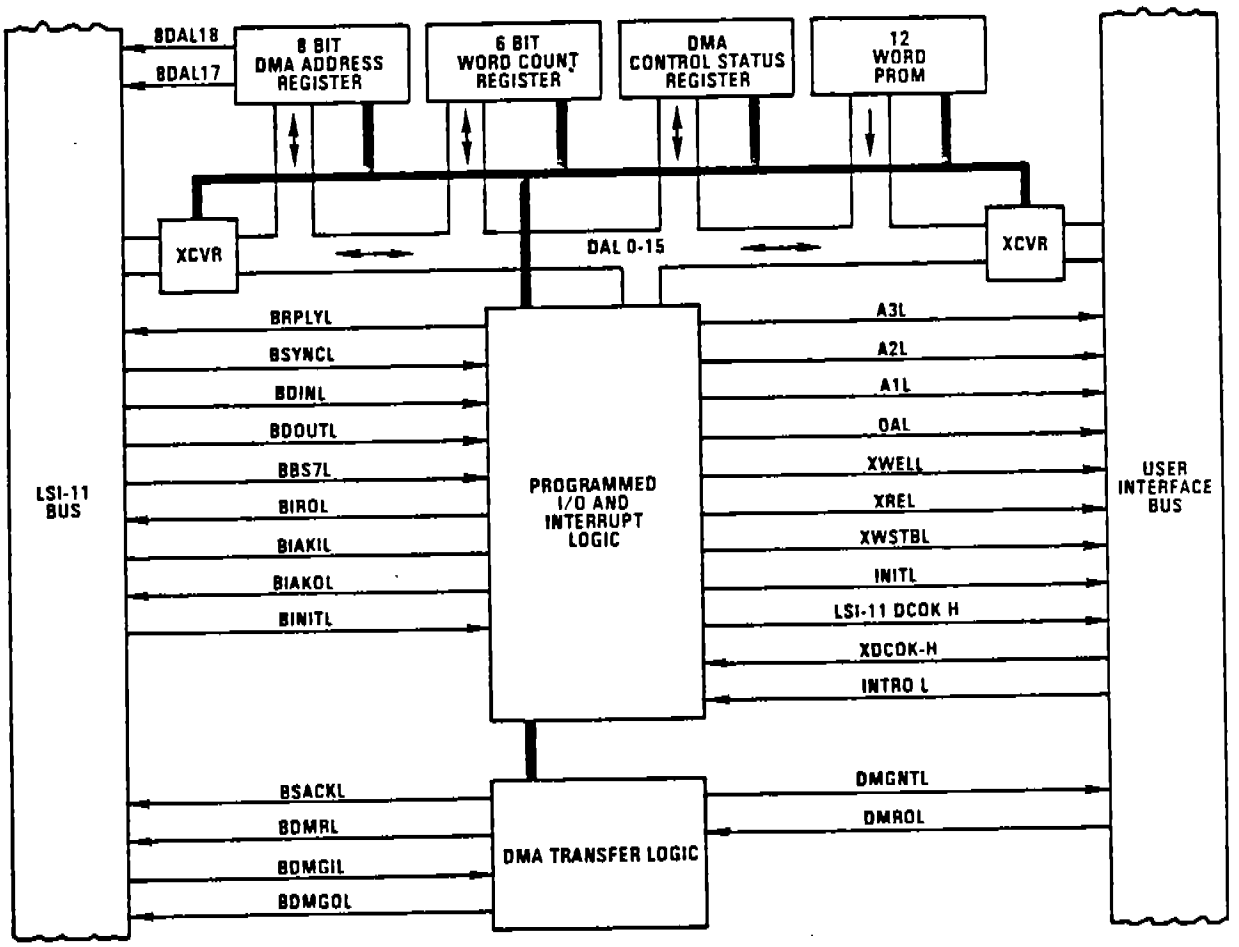

Figure 2-46. DMA-QB Block Diagram

Table 2-26. DMA-QB SPECIFICATIONS

PHYSICAL

Board Size	Dual-height, 5.2" x 8.9" x .4"
Power Requirements	+5V : 5%, 2.0A Typical
Temperature operating	5° to 50°C.
Temperature storage	55° to 125°C
Relative humidity	-0.95%, Non-condensing -
LSI-11 Bus loading	1 Bus load

ON-BOARD (PROM) INTERFACE

Type Bipolar, 82S123 or Equiv.
Size 32 word x 16 BIT
Control Enable/disable, jumper selectable
Address Base address + 000_8-0077_8

INTERRUPT INTERFACE

Priority levels	4, Jumper-selectable
DMA-L11 interrupts	Bus timeout error, byte count zero
Device interrupts	External flag, external power off
Vector address range	000_8-374_8

DMA INTERFACE

General configuration Single-cycle, request/grant
Transfer rate To 800K transfers/sec
Data bus 16-BIT, bidirectional
Interface level TTL, Logic '0' = .5V
Logic '1' = 2.5V
Mode Byte or word transfer, jumper-selectable
Addressing range 18-BIT (256 KB)
Board base address range 160000_8 to 177600_8, 1 of 64, jumper selectable

PROGRAMMED I/O INTERFACE

General configuration External register R/W
Data Bus Parallel bidirectional
Interface level TTL
Mode Word Transfer (16 BIT)

2.3.2.4 AFSS COTC.- The AFSS COTC consists of an LA34-AA or LA100-CA IOT, two P300 Line Printers and an A/N display unit with keyboard. The designated display unit and keyboard are identical to the specialists' display units and keyboards except for special software which allows this position to: status the system at the AFSS, validate operations, and reconfigure the equipment for maintenance purposes. The IOT is provided for maintenance purposes only.

2.3.2.4.1 Line Printer.- The AFSS uses the same P300 Line Printer as the FSDPS. It is described in detail in paragraph 2.3.1.1.6.3.

2.3.2.4.1.1 Printer Interface.- The Printronix P300 Printer is interfaced with the communications processor via an RS-232 interface circuit board installed in the printer card cage. This interface board provides a buffered serial interface that converts EIA RS-232 signals into parallel form. Data is received in serial form; assembled into parallel form; stored in a buffer memory, and then output to the printer. The serial data rate is switch selectable from 150 baud to 9600 baud. Parity is switch selectable for odd, even or parity ignore.

Power is supplied by a common bus connector. The interface to the printer is provided via jumper cable. A self-test mode switch is provided on the circuit board. When this switch is in the run position, it prints a recycle pattern 132 columns wide on the printer. In the stop position both of the interfaces are energized. The major functions of the RS-232 interface are:

1) voltage/current loop operation,

2) buffering of input data,

3) internal/external bit rate capability,

4) word length selection,

5) parity selection,

6) protocol selection,

7) user definable control characters, and

8) self-test capability.

Figure 2-47, RS-232 Block Diagram, shows a simplified view of major interface logic flow. The serial data interface converts RS-232 voltage levels or current loop signals to/from logic levels. Data and control signals are provided by the serial data

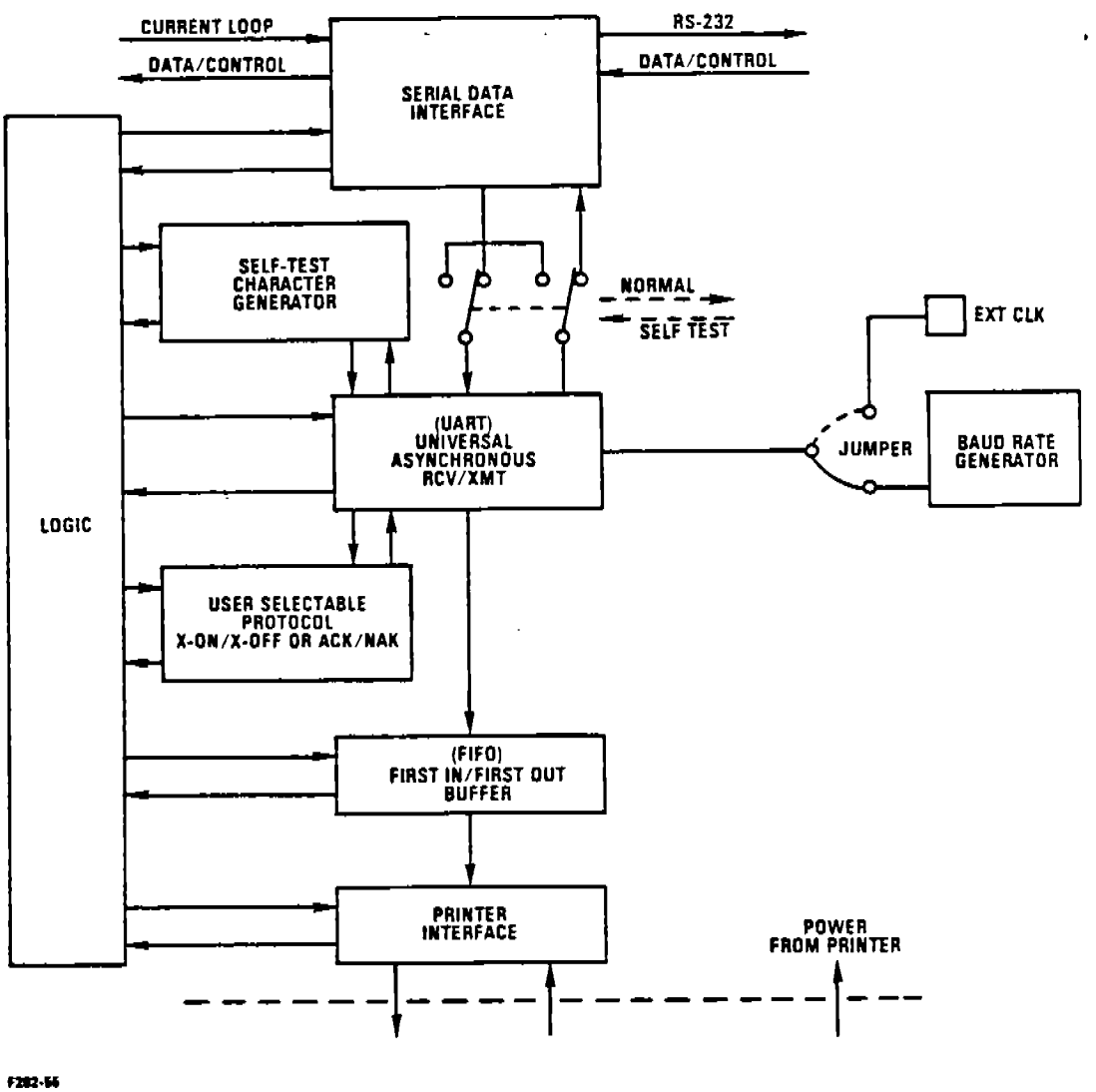

Figure 2-47. RS-232 Block Diagram

interface to the Universal Asynchronous Receiver/Transmitter (UART). The UART performs serial/parallel and parallel/serial conversions. Received characters are stored in the First In/First Out (FIFO) memory. The FIFO acts as a data buffer with a standard size of 1024 bytes. The buffer size can be optionally increased to 2048 bytes. A buffer almost full (BAFL) signal is generated when a user selectable threshold is reached. The range of thresholds between almost full and almost empty constitute a hysteresis condition. The user can select the optimum amount of hysteresis based on the input data rate and the protocol being used. Characters stored in the FIFO are output to the printer at a rate which is compatible with the print rate.

2.3.2.4.2 Display Monitor.- The A/N Display Monitor (E-Systems 401-37290-01) is a Ball TTL-150. The monitor is a solid state raster scan display for data terminal application. The TTL-150 provides high quality display of alphanumeric dot characters. The monitor has a 15 inch diagonal screen size CRT with a 110 degree deflection angle. The data monitor requires three separate TTL compatible input signals for operation (vertical drive, horizontal drive, and video). These three separate TTL input signals eliminate costly redundancy associated with the mixing and stripping operation required in a composite (single input) monitor.

The interface to the monitor is provided by the A/N OTF/Cache subsystem. The video signal is 2 volts peak-to-peak with zero volts equal to OFF and 2 volts equal to maximum brightness.

The video signal is applied to the CONTRAST control which reduces the brightness to normal viewing conditions. The normal position of the contrast control is approximately mid-range; typical video level applied to the input of the monitor is approximately one volt.

The horizontal and vertical sync signals are chained to all monitors run by a A/N processor group (A/N OTF is position processors 1 & 2). The typical level is approximately two volts, negative true.

The monitor uses P39 phosphor refreshed at 80 Hz interlaced for a frame rate of 40 FPS. 525 lines total and 480 visible lines are displayed. Each line is divided into 640 pixels along the horizontal axis. The ratio of 640 to 480 is consistent with the 4:3 aspect ratio of the CRT bulb. The CRT bulb includes a safety shield etched to 90 percent transmissity for glare reduction.

The functional operation of the display monitor is depicted in figure 2-48, TTL-150 Block Diagram. Horizontal and vertical sync signals are provided by the alphanumeric OTF in the position processor. Video amplification is provided by Q101 and Q102. The dynamic range capability of the amplifier is 48V which provides

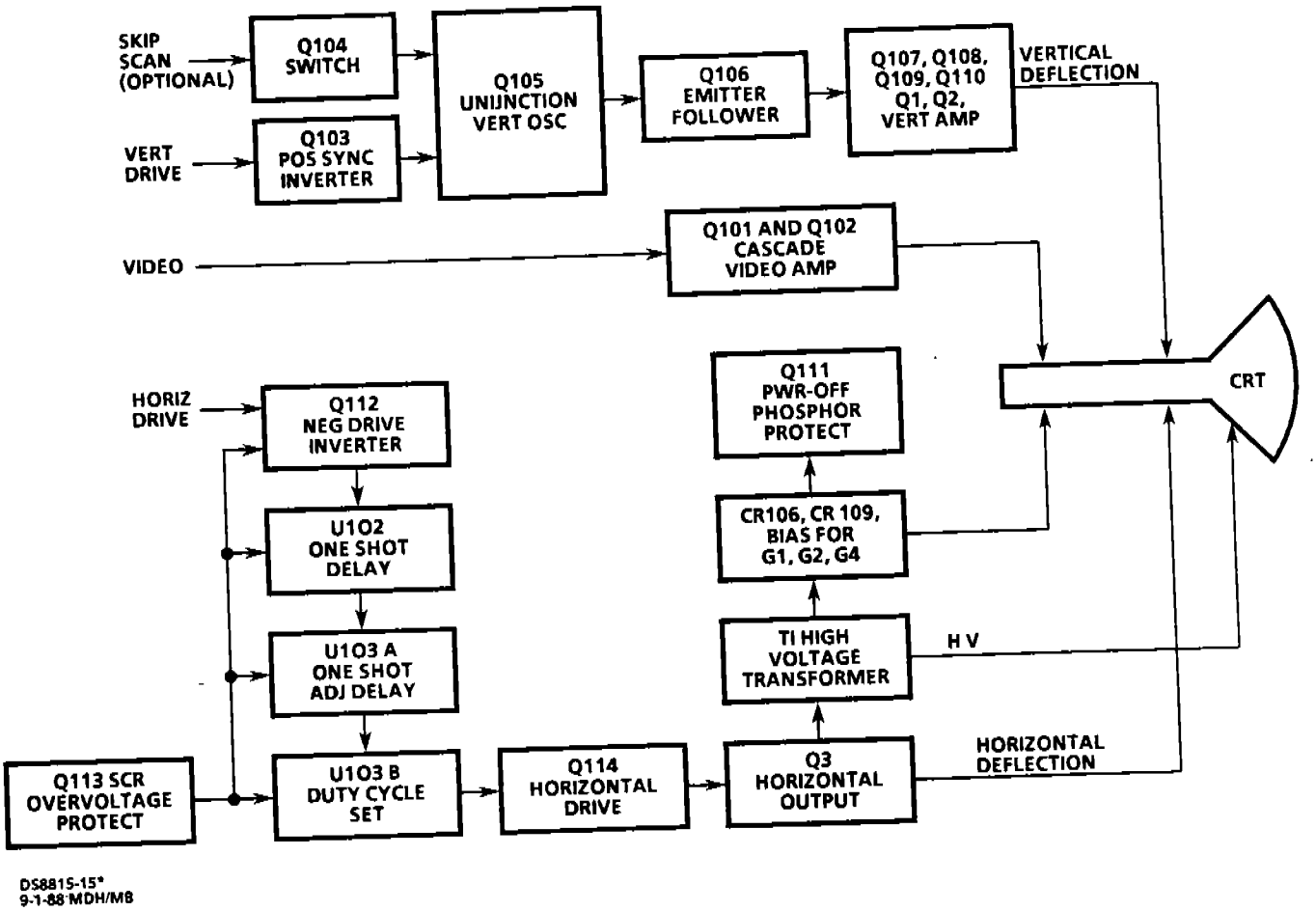

Figure 2-48. TTL-150 Block Diagram

more than adequate head room to meet the normal viewing brightness requirement of 18 to 30 volts of modulation. High frequency peaking is provided by a filter network resulting in a nominal bandwidth of 22 MHz.

The vertical electronics circuit consists of a positive sync inverter, a vertical oscillator, an emitter follower, a vertical output amplifier, and a vertical deflection coil. A programmable unijunction transistor operates as a free-running relaxation sawtooth oscillator. The incoming sync pulse forces the oscillator to run at the incoming frequency as long as the vertical sync control is adjusted to produce a free-running frequency slightly lower than the incoming frequency.

One shot delays provide an adjustable horizontal line drive delay which permits the video to be centered horizontally within the raster and generates the proper duty cycle for the horizontal output transistor. The horizontal output stage supplies the yoke with the necessary scanning current and developes the CRT anode voltages. Refer to table 2-27, TTL 150 Input Signal Requirements, for further data on the display monitor.

2.3.2.4.3 Keyboards. - The keyboard consists of a Maxi-Switch keyboard unit and E-Systems housing assembly. Also provided with each keyboard is a wall-type regulated 5 VDC power supply. See figure 2-49 and refer to the Operation and Maintenance Manual, Keyboard Unit (TI 6490.16) for functional diagrams and schematic.

The keyboard provides the specialist with an interface to the M1FC system. Special keywords are used by the specialist to perform specific tasks. Each keyword is listed in section 3 of this instruction book.

Power Supply This unit is similar to calculator-type charging units. There is no high voltage in the keyboard; only a single voltage is required within the unit. The power supply connects to the keyboard with a three wire circuit: 5 VDC, common and AC protective ground. The power supply plugs into a standard grounding type 115 VAC outlet.

Keyboard The keyboard is microprocessor controlled. Programmed functions include auto-repeat on certain keys, two-speed auto-repeat for cursor controls, and assignments for the function keys located on the top rows of the keyboard. These have been installed in mask-programmed ROM.

The keyboard uses RS-422 protocol, a differential signal technique, for extremely long runs without data errors. Multiple outputs for redundant reception of keyboard data are provided. Eight circuits are returned in the keyboard cable to the position processing equipment.

Table 2-27. TTL-150 Input Signal Requirements

	VIDEO
AMPLITUDE:	High - 4.0V±2.0V into an external 500 ohm or less contrast control. 2.0V max at J101-8 to prevent video amplifier saturation. Low - 0.0±0.4V
POLARITY:	Negative
PULSE WIDTH:	40 ns min
RISE AND FALL TIME:	Less than 12 nsec (10% to 90%)
	HORIZONTAL DRIVE
HORIZONTAL FREQUENCY:	15,250Hz min to 21,000Hz max 15,750Hz 500Hz (Standard)
AMPLITUDE:	High - 4.0V±1.5V Low - 0.0V±0.4V
POLARITY:	Standard - Positive edge triggering Optional - Negative edge triggering
PULSE WIDTH:	2.5usec min to 30usec max
RISE AND FALL TIME:	Less than 100nsec (10% to 90%)
	VERTICAL SYNC
VERTICAL FREQUENCY:	46 Hz min to 63 Hz max
AMPLITUDE:	High - 4.0V±1.5V Low - 0.0V±0.4V
POLARITY:	Standard - Negative edge triggering Optional - Positive edge triggering
PULSE WIDTH:	75usec min to 1.4msec max
RISE AND FALL TIME:	Less than 100nsec (10% to 90%)

Table 2-27. TTL-150 Input Signal Requirements (Continued)

	SKIP SCAN
AMPLITUDE:	High - 4.0V±1.5V Low - 0.0V±0.4V
POLARITY:	Skip high
PULSE WIDTH:	3usec min to 10usec max
RISE AND FALL TIME:	Less than 100nsec (10% to 90%)

Reset Switch The reset switch is located on the rear panel of the keyboard. The switch opens the +5 VDC line to the microprocessor. This allows re-start of a replaced keyboard without affecting other keyboards plugged into the same AC circuit.

2.3.2.5 Input/Output Terminal.- The DEC LA-34-AA/LA100-CA is provided for LSI-11 support. It can be connected to any of the communications processors via patch panel for maintenance purposes. The LA34-AA/LA100-CA is an advanced teleprinter designed to offer fast reliable operation at 30-cps operating speed. The true 30-cps through-put is accomplished by a 60 cps catch-up mode which is activated anytime more than one character is present in the 16-character buffer.

The LA34-AA/LA100-CA is mounted on a pedestal which provides easy access to the typewriter style keyboard.

2.3.2.5.1 IOT Specifications.- The unit is pedestal mounted and has the following general characteristics:

		H	W	D
1)	Dimensions (in)	33.5	22	16.4
	(cm)	85	55.9	40

2) Weight: 22 lbs (10 kg)

3) Heat Output: 1024 Btu/hr (258 kcal/hr)

4) Power Requirements 90-132 volts, 60 Hz (± 1), single phase; 3.1 amps at 120 volts.

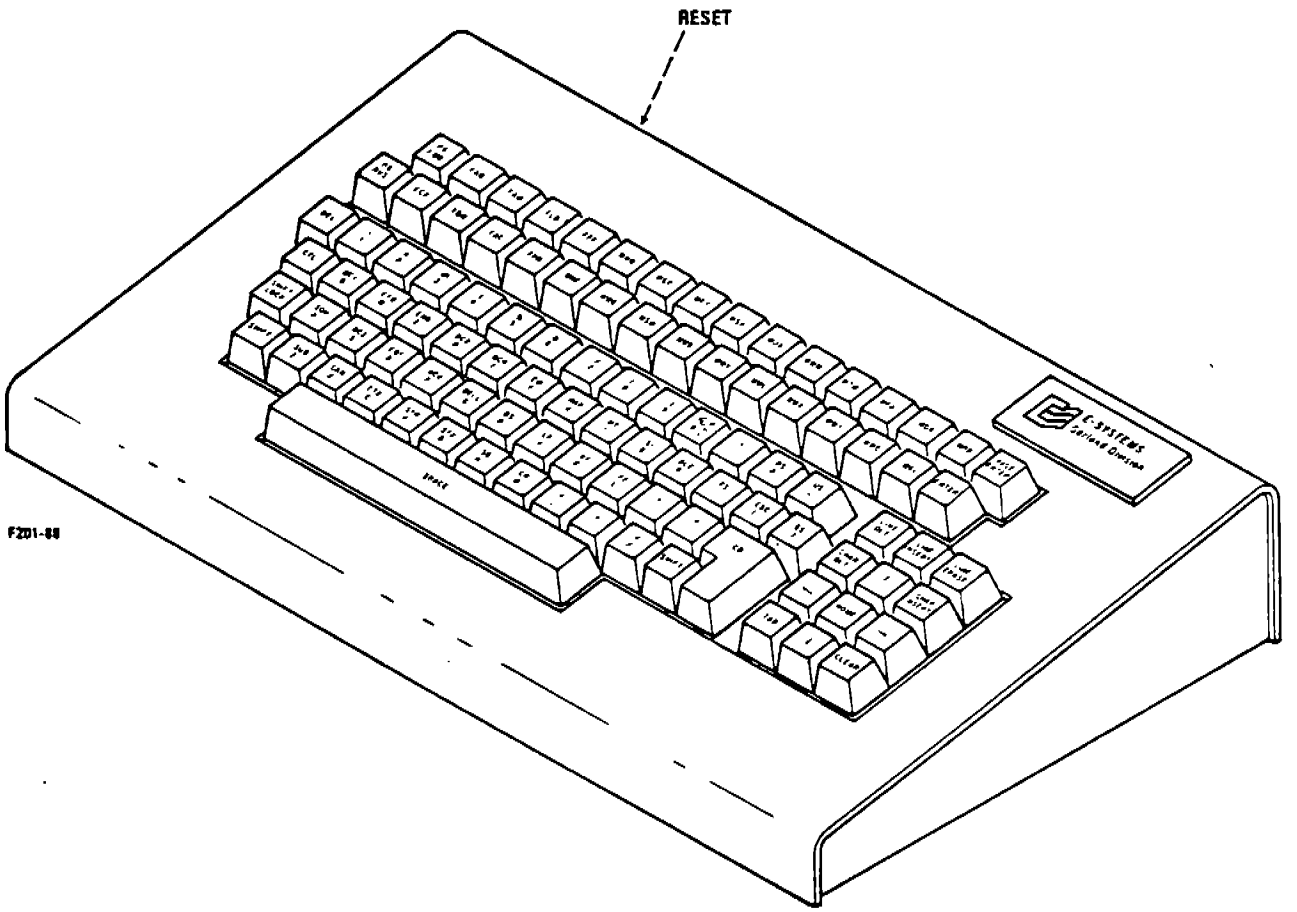

Figure 2-49. Display Monitor Keyboard

Table 2-28, LA34-AA/LA100-CA Specifications, lists the primary specifications of the LA34-AA/LA100-CA.

2.3.2.6 AFSS Power Distribution. - The powers distribution is divided into AC and DC power descriptions.

2.3.2.6.1 AC Power. - The AFSSs use existing power breaker boxes. The power requirements at a typical AFSS consist of a 100 ampere, 120/240 volt single phase, 3-wire box with 12 breaker positions. The required branch circuit breakers in this panel are three 30 ampere breakers and two 20 ampere breaker. These circuits terminate in the communications equipment rack except for one of the 20 ampere circuits, which is routed to the IOT. In the operations area, all of the alphanumeric terminals use existing power circuits whose outlets are within six feet of the terminals. All AFSS equipment located in this area and in the Training Room use NEMA type 5-15R or equivalent 120 volt, three-prong outlets. At each position, one outlet is for the monitor and one is for the keyboard. The total load on the two outlets is 1.6 amperes.

The two line printers each require one 20 ampere circuit because of the surge current. Each printer operates on a steady state current of 7.8 amperes.

2.3.2.6.2 DC Power. - The Power Supply Assemblies (401-36716-01) supply the following DC voltages to the E-Systems card cages.

+12 VDC
-12 VDC
+5 VDC
signal ground

The power supplies and card cages are located in the communications processor rack and the position processor rack(s). All other equipment located in the E-Systems equipment racks contain internal power supplies. For detail description refer to the individual equipment manuals listed in table 1-1.

2.3.3 Aviation Weather Processor (AWP). - The following paragraphs describe the communication equipment rack, communications processor rack, position processor rack, Tandem Group, and peripherals at the AWP. A functional block diagram of the AWP is shown in figure 2-11.

Table 2-28. LA34-AA/LA100-CA Specifications

PRINTING	Switch selectable, 10 or 30 char/sec throughput with 60 char/sec catch-up mode.
LINE LENGTH	132 character maximum line length.
SPACING	10 char/in (horizontal) 6 lines/in (vertical)
CHARACTERS	96 Upper/lower case (ASCII) 5x7 dot matrix (0.07 X 0.10 in.)
PAPER	Variable with -3- 14-7/8 in. Up to 4-part forms - 0.020 in. maximum pack thickness Tractor-drive, pin feed.
KEYBOARD	Standard ANSI Keyboard layout. Multi-key roll-over.
INTERFACE	EIA/CCITT

2.3.3.1 Communications Equipment Rack. - The communications equipment rack consists of a thermal alarm panel, three digital patch panels, two disk drives, two coded time source (CTS) units, a coded time source interface, and a circuit breaker AC junction box.

2.3.3.1.1 Thermal Alarm. - The Thermal Alarm Unit, 401-37155-01, monitors thermal sensors located in the communications processor rack and position processor rack. Both a visual and audible alarm are observed at the thermal alarm unit when an overtemperature condition exists in the racks.

2.3.3.1.2 Digital Patch Panels. - The three digital patch panels in the AWP provide an interface for data interchange between the Tandem Group and the two communication processors, between the position processors and the IOT, and between the 1200 and 2400 bps GFE modems and the Tandem Group.

2.3.3.1.3 Coded Time Source (CTS) Interface. - The coded time source interface in the AWP performs the same function as the CTS interface in the FSDPS, which is described in paragraph 2.3.1.1.6.4.

2.3.3.1.4 Coded Time Source (CTS). - The coded time source (CTS) in the AWP performs the same function as the CTS in the FSDPS, which is described in paragraph 2.3.1.1.6.5.

2.3.3.2 Communications Processor Rack. - Two communications processors reside within the communications processor rack. Each communications processor is a stand alone unit, even though they are both housed in the same card cage. There is a bi-directional, parallel direct memory access (DMA) data transfer between one communications processor and one position processor.

The communications processor rack also includes modem equipment, analog patch panels, a fan AC junction box, and a blower assembly. A complete description of a communications processor is provided in section 2.3.2.2.

2.3.3.2.1 Analog Patch Panels. - The communications processor rack in the AWP contains two analog patch panels. These analog patch panels interface data interchange between the AWP and another AWP, the AWP and the FSDPSs, and the AWP and Service B and WMSC.

2.3.3.3 Position Processor Rack. - The position processor rack in the AWP performs identically to the AFSS position processor rack supporting 12 positions. Refer to section 2.3.2.3 for a detailed description of the position processor rack.

2.3.3.4 Tandem Group. - The Tandem Group in the AWP is identical to the FSDPS Tandem Group (minimum configuration) with the addition of two Byte Sync Controllers, T16/6202, connected to the Service A communications lines. Refer to section 2.3.1.1.1 for a detailed description of the Tandem Group equipment.

2.3.3.5 AWP Peripheral Group. - The peripheral group equipment in the AWP is identical to that in the AFSS. This peripheral equipment includes 12 CRT monitors, 12 keyboard units, 12 keyboard power supplies, one LA34-AA/LA100-CA Input/Output Terminal (IOT), two P300 Line Printers, and eight DM9300-TD Disk Drives. All of this equipment except the disk drives is described in section 2.3.2.4. Refer to paragraph 2.3.1.1.6.1 for a detailed description of the disk drives.

2.3.3.6 AWP Power Distribution. - The power distribution for the AWP is identical to the power distribution for the FSDPS and is described in section 2.3.1.1.7.

SECTION 3

OPERATION

3.1 GENERAL.- The initial hardware start-up procedures for the MIFC FSAS is described below for the FSDPS, AFSS, and AWP.

3.1.1 Hardware Start-Up Procedure - FSDPS.- The initial power-up sequence is as follows:

a. Ensure that all equipment is properly connected to its power sources and power switches are in OFF position.

b. Close all circuit breakers at main distribution panel.

c. Check for proper voltage at main distribution panel.

d. Power-up Tandem computers by referring to Tandem operating procedures manual.

e. Power-up Ampex disk drive units sequentially. Refer to Ampex operating procedures manual.

f. Power-up Kennedy mag tape drives. Refer to Kennedy operating procedures manual.

g. Power-up communications switching rack, communications equipment rack and COTC processor rack by placing the four circuit breakers (CB1 thru CB4) in the back of cabinet 1 , communications switching rack, in ON position. Refer to RL01/RL02 Disk Drive operating procedures manual and UDS modem operating procedures manual for their power-up procedures.

h. Power-up all other peripheral equipment by placing power switches in ON position. Refer to related equipment manuals for each peripheral unit.

3.1.2 Hardware Start-Up Procedure - AFSS.- The initial power-up sequence is as follows:

a. Ensure that all equipment is properly connected to its power sources and power switches are in OFF position.

b. Close all circuit breakers at main distribution panel.

c. Check for proper voltages at main distribution panel.

d. Power-up AFSS by placing the four circuit breakers (CB1 thru CB4) in back of cabinet 1, communications equipment rack, in ON position. Refer to RL01/RL02 Disk Drive operating procedures manual and UDS modem operating procedures manual for their power-up procedures.

e. Power-up all other peripheral equipment by placing power switches in ON position. Refer to related equipment manuals for each peripheral unit.

3.1.3 Hardware Start-Up Procedure - AWP.- The initial power-up sequence is as follows:

a. Ensure that all equipment is properly connected to its power sources and power switches are in OFF position.

b. Close all circuit breakers at main distribution panel.

c. Check for proper voltage at main distribution panel.

d. Power-up Tandem computers by referring to Tandem operating procedures manual.

e. Power-up Ampex disk drive units sequentially. Refer to Ampex operating procedures manual.

f. Power-up Kennedy mag tape drives. Refer to Kennedy operating procedures manual.

g. Power-up communications equipment rack, communications processor rack and position processor rack by placing the four circuit breakers (CB1 thru CB4) in the back of cabinet 1 , communications equipment rack, in ON position. Refer to RL01/RL02 Disk Drive operating procedures manual and UDS modem operating procedures manual for their power-up procedures.

h. Power-up all other peripheral equipment by placing power switches in ON position. Refer to related equipment manuals for each peripheral unit.

3.1.4 FSDPS/AFSS and FSDPS/AWP Communications.- In normal operating mode, no operator interface is necessary to establish communications between FSDPS and an AFSS or FSDPS and an AWP. The Analog and Digital Patch Panels at the FSDPS, AFSS, and AWP contain normal through jack receptacles. Under normal operating conditions no patching is required due to internal contacts.

3.1.4.1 Manual Reconfiguration.- The analog and digital ports at the FSDPS, AWP, and AFSSs are routed through manual patch panels. These patch panels allow any modem to support any communications path for which it is compatible.

Each patch panel provides full duplex circuit interfaces. All serial communications, whether remote or local, are routed through the communications patch panels. With the aid of the supplied patch cords, the normally routed data flow may be interrupted and rerouted, via patch cords, to alternate or spare data sources or drops. Plugging one end of the patch cord into the upper jack of the given channel diverts the source data to the patch cord. Plugging the other end of the patch cord into the middle normal through jack of the alternate or spare channel interrupts the normally routed drop data flow for this channel and routes the source data, now sourced through the patch cord, to the drop connected to the alternate or spare channel. This procedure effectively reroutes data flow around defective equipment, be it a defective data source or drop. Application of this feature allows rerouting of data paths to accommodate failed controllers, ports, modems, and telephone lines.

An additional feature permits monitoring/test at both the analog and digital interfaces without interruption of on-line traffic. This is accomplished by connecting high impedance monitor/test equipment via patch cords to the monitor (bottom) jack. Patching cables for both analog and digital patching are provided.

3.1.4.2 Dial Backup Configuration.- In addition to the four dedicated 9600 baud modems provided for the AFSS communications, an additional modem is provided for dial-up operations at 4800 BPS. A maximum of four dial-up modems are provided at the FSDPS and one is provided at each AFSS.

Each FSDPS is provided with at least one manual call-up telephone handset which operates in conjunction with a manual dialer located in the same rack with the 4800 bps modems. To activate the dial backup feature, the operator must first patch the AFSS data source (AFSS A, Line 1, for example) to the dial-up modem. Then the operator takes the manual call-up telephone handset off hook and dials the digit corresponding to the dial-up modem. The operator then raises the exclusion key which connects the communication line (to the DDD network) dedicated to the selected modem to the telephone set, thereby providing DC current loop closure to the telephone central office. The telephone central office then returns dialtone where upon the operator direct dials the first of two telephone numbers of the corresponding AFSS dial-up modem. When the automatic answer card at the AFSS detects the incoming call, it goes off hook and supplies an answer-back tone to the FSDPS. The operator then lowers the exclusion key which signals the dial-up

modem originate card to maintain the communications line "off hook". The operator then places the telephone set "on hook". The operator then repeats this process once more, dialing first the selected modem number plus "1", then dialing the second telephone number of the AFSS dial-up modem. When this process has been completed, the communication lines are transferred to the modems, at the FSDPS and AFSS, and the terminals at the FSDPS and AFSS are notified to start passing data.

3.2 SYSTEM SOFTWARE.- Software for the M1FC FSAS is composed of ~~the software for the~~ FSDPS and AWP subsystems and firmware for the AFSS and AWP subsystems. Refer to the following documents for an explanation of the software operation:

User's Manual for AWP	416-32146
User's Manual for FSDPS/AFSS	416-32147
Operator's Manual for AWP	416-32149
Operator's Manual for FSDPS/AFSS	416-32150

SECTION 4

PERIODIC MAINTENANCE

4.1 GENERAL.- Periodic maintenance at each FSDPS, AFSS, and AWP is essential to ensure optimum performance, minimize service interruptions, and avoid major equipment failures.

Preventive maintenance is limited to reviewing console messages concerning the system status, inspecting backup battery indicators, alignment and adjustment of electromechanical hardware and replacement of air filters, paper supplies and ribbons. It also entails cleaning exposed surfaces and inspecting the equipment for worn mechanisms and frayed or chafed cables including the grounding system cables. Table 4-1 lists a recommended preventive maintenance schedule for the FSDPS and table 4-2 lists a schedule for the AFSS, and table 4-3 lists a schedule for the AWP.

All periodic maintenance instructions for the equipment which comprises the M1FC FSAS are contained in the related equipment manuals which are listed in table 1-1.

Table 4-1. Scheduled Preventive Maintenance Tasks - FSDPS

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
Tandem Non Stop II Processor		Maintenance Manual Processor Subsystem T16/82809 Section 6
OSP		Maintenance Manual OSP T16/8846 Section 6
a. Once each eight hours of operation		
(1) Review	OSP Console Messages. This provides information about the status of the system.	Refer to the OSP User Guide (82801) Section 3.2 for detailed procedures.
(2) Interpret	OSP Console Message to determine if any errors have occurred in the past 8 hours.	Refer to the OSP User Guide (82801) APPENDIX H.
	If errors are detected	Refer to OSP User Guide (82801) Section 3.3.
Magnetic Disk Drive Ampex DM9300TDQ		Operation and Maintenance Manual (3314888-01) Section IV
a. Daily		
(1) Inspect	Shroud area for dirt. Disk pack door area for dirt.	

Table 4-1. Scheduled Preventive Maintenance Tasks - FSDPS (Continued)

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
b. Monthly		
(1) Inspect	Cable connections. Front operator panel. Bezel pre-filter. Heads for cleanliness.	
c. Quarterly		
(1) Inspect	Head alignment Serve Adjustment Power Supplies	
d. Semiannual		
(1) Inspect	Filter	
<u>Magnetic Tape Drive Kennedy 9000</u>		Operation and Maintenance Manual (006-9001-300C) Section IV
<u>Communications Switching Rack</u>		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	
b. Three Months		
(1) Clean	Exterior Interior	

Table 4-1. Scheduled Preventive Maintenance Tasks - FSDPS (Continued)

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
Communications Equipment Rack		
a. Monthly		
(1) Inspect	Cable Connections. All cables for fraying and chafing.	
b. Three months		
(1) Clean	Exterior Interior	
COTC Processor Rack		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	
b. Three Months		
(1) Clean	Exterior Interior Air filter	
Line Printer Printronix P300		Model 300 Printer Maintenance Manual Section: Preventive Maintenance
Input/Output Terminal (IOT) LA34-AA/LA100-CA		LA34-AA/ LA100-CA Pocket Service Guide (EK-LA34-SV-001)

Table 4-1. Scheduled Preventive Maintenance Tasks - FSDPS (Continued)

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
System Cables		
a. Monthly		
(1) Inspect	All cables for fraying and chafing, including the green grounding system cabling.	

Table 4-2. Scheduled Preventive Maintenance Tasks - AFSS

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
<u>Communications Equipment Rack</u>		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	
b. Three Months		
(1) Clean	Exterior Interior Air Filter	
<u>Communications Processor Rack</u>		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	
b. Three Months		
(1) Clean	Exterior Interior	
<u>Position Processor Rack</u>		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	

Table 4-2. Scheduled Preventive Maintenance Tasks - AFSS (Continued)

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
b. Three Months		
(1) Clean	Exterior Interior Air Filter	
Line Printer Printronix P300		Model 300 Printer Maintenance Manual Section: Preventive Maintenance
Input/Output Terminal (IOT) LA34-AA/LA100-CA		LA34/LA100 Pocket Service Guide (EK-LA34-SV-001)
System Cables		
a. Monthly		
(1) Inspect	All cables for fraying and chafing, including the green grounding system cabling.	

Table 4-3. Scheduled Preventive Maintenance Tasks - AWP

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
Tandem Non Stop II Processor		Maintenance Manual Processor Subsystem T16/82809 Section 6
OSP		Maintenance Manual OSP T16/8846 Section 6
a. Once each eight hours of operation		
(1) Review	OSP Console Messages. This provides information about the status of the system.	Refer to the OSP User Guide (82801) Section 3.2 for detailed procedures.
(2) Interpret	OSP Console Message to determine if any errors have occurred in the past 8 hours.	Refer to the OSP User Guide (82801) APPENDIX H.
	If errors are detected	Refer to OSP User Guide (82801) Section 3.3.
Magnetic Disk Drive Ampex DM9300TDQ		Operation and Maintenance Manual (3314888-01) Section IV
a. Daily		
(1) Inspect	Shroud area for dirt. Disk pack door area for dirt.	

Table 4-3. Scheduled Preventive Maintenance Tasks - AWP (Continued)

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
b. Monthly		
(1) Inspect	Cable connections. Front operator panel. Bezel pre-filter. Heads for cleanliness.	
c. Quarterly		
(1) Inspect	Head alignment Serve Adjustment Power Supplies	
d. Semiannual		
(1) Inspect	Filter	
Magnetic Tape Drive Kennedy 9000		Operation and Maintenance Manual (006-9001-300C) Section IV
Communications Equipment Rack		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	
b. Three Months		
(1) Clean	Exterior Interior	

Table 4-3. Scheduled Preventive Maintenance Tasks - AWP (Continued)

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
Communications Processor Rack		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	
b. Three months		
(1) Clean	Exterior Interior	
Position Processor Rack		
a. Monthly		
(1) Inspect	Cable connections. All cables for fraying and chafing.	
b. Three Months		
(1) Clean	Exterior Interior Air filter	
Line Printer Printronix P300		Model 300 Printer Maintenance Manual Section: Preventive Maintenance
Input/Output Terminal (IOT) LA34-AA/LA100-CA		LA34-AA/ LA100-CA Pocket Service Guide (EK-LA34-SV-001)

Table 4-3. Scheduled Preventive Maintenance Tasks - AWP
(Continued)

Maintenance Task	Reference Manual	
	Task	Maintenance Procedures
System Cables		
a. Monthly		
(1) Inspect	All cables for fraying and chafing, including the green grounding system cabling.	

SECTION 5

SYSTEM MAINTENANCE

5.1 GENERAL.- The M1FC FSAS maintenance concept revolves around the computer operating systems. The operating systems have the capability to detect malfunctions, transmit error messages, and automatically recover from hardware failures by rerouting transmittal actions.

The three operating systems are: GUARDIAN, Operations and Service Processor (OSP), and the DFX-11 operating system. Each one contains certain individual diagnostic and exerciser modules which enables the system to fault isolate to a Line Replaceable Unit (LRU).

5.2 FSDPS CORRECTIVE MAINTENANCE.- Tandem's operating systems and E-System's developed DFX-11 operating system, can automatically detect most failures within their confines. Figure 5-1 shows the FSDPS functional equipment groups. The equipment groups are divided to distinguish the equipment functioning under the Tandem operating systems from the equipment functioning under the DFX-11 operating system.

5.2.1 Tandem and Peripheral Equipment Group.- When an element or element path fails within the Tandem or Peripheral equipment group, the operating system can automatically recover by rerouting the transmittal actions. See figure 5-2 and table 5-1.

The following events occur when an element failure is detected:

1) the failed element or element path is marked-down;
2) the system recovers by rerouting the transmittal actions through a secondary path;
3) a Critical Error Condition message is generated and displayed on the OSP VDU or printed on the OSP line printer;
4) an audible alarm sounds at the OSP; and
5) an alarm lamp lights at the SMMC.

The Critical Error Condition Messages that may be displayed at the OSP are listed and explained in the Operations and Service Processor User Guide (T16/8801). This manual also provides the computer operator detailed procedures in using the OSP as a system maintenance terminal, operating under Guardian operating system, and loading and running diagnostics outside of Guardian, such as Shadow Diagnostics. Additional information on the use of the OSP can be found in the Guardian Operating System Operations Manual (T16/8075).

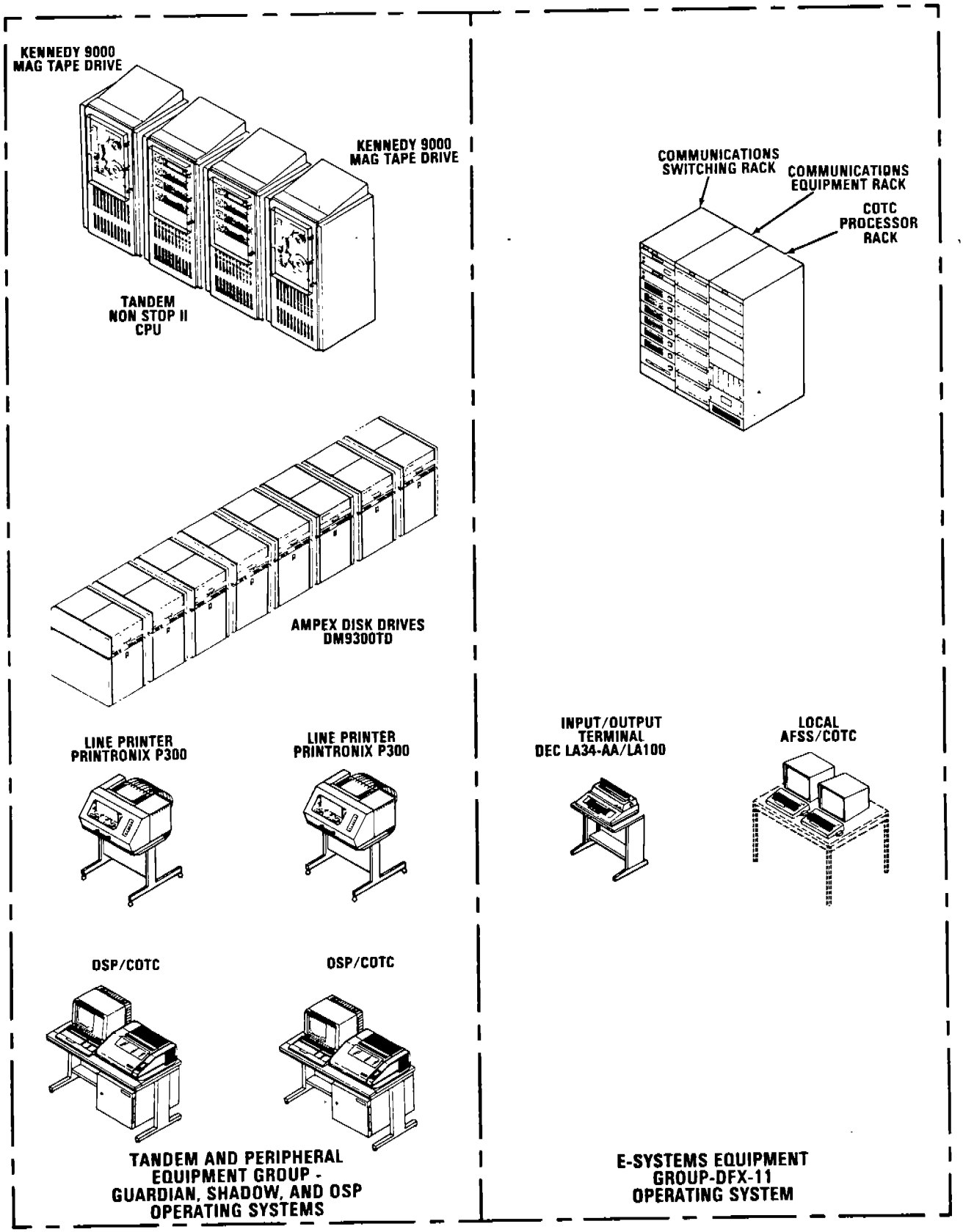

Figure 5-1. FSDPS Functional Equipment Groups

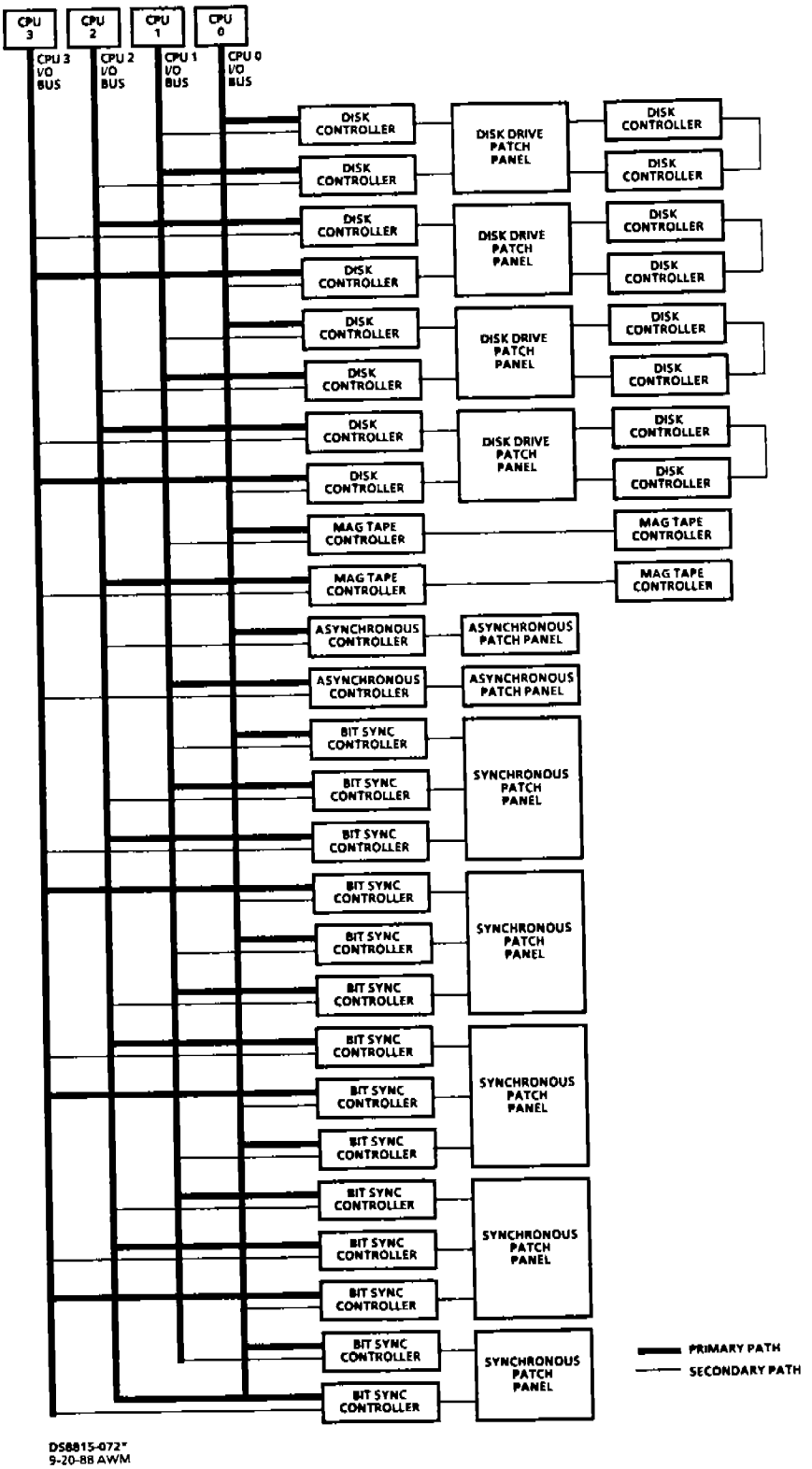

Figure 5-2. Tandem System Primary and Secondary Paths Simplified

Table 5-1. FSDPS Automatic Recovery System Elements

1. Processor, consisting of:

    a. Tandem MCB
    b. Tandem Memory
    c. Tandem CCD
    d. Tandem IPU

2. Magnetic Disk Controller, including:

    a. Disk Patch Panel

3. Magnetic Disk Drive

4. Magnetic Tape Controller, including:

    a. Magnetic Tape Drive

5. Asynchronous Controller, including:

    a. Asynchronous Patch Panel

6. Byte Synchronous Controller, including:

    a. Synchronous Patch Panel

Critical Error Condition Messages are Guardian System Messages. These messages are characterized as being important to the diagnosis of a failed processor or system. Any time a Critical Error Condition Message is displayed at the OSP an audible alarm is sounded to alert the computer operator that a failure has occurred. These messages are listed in the OSP User Guide.

Figure 5-3 shows the M1FC FSAS system failure event flow. By following this flow chart, the computer operator, using the OSP User Guide Manual can isolate a failure to a LRU. However, in some cases maintenance personnel may be required to determine the failed LRU.

The Tandem operating systems and the diagnostic software are shown in figure 5-4. The loading and running procedures for these diagnostics are described in the M1FC Users Manual for FSDPS/AFSS, 416-32147.

Maintenance personnel, when replacing a failed LRU with a spare, will perform a software diagnostic checkout on the spare LRU using the appropriate procedure as described in either the OSP User Guide or the Diagnostic Operating Procedures Manual.

5.2.2 E-Systems Equipment Group.- A failed element or element path will affect system operations within this equipment group. To restore the system to full operation, the fault must be isolated to the failed LRU, and that LRU replaced with a spare. Failures occurring within this group are reported by error messages at the OSP/COTC. These error messages are displayed in plain English and indicate what element or element path has failed. From these messages, the computer operator can determine which diagnostic test should be initiated. See figure 5-5 and refer to the M1FC Users Manual for FSDPS/AFSS, 416-32147.

Diagnostic tests are initiated at the local AFSS terminal/COTC for equipment in this group. The diagnostic test can be run concurrently with the DFX-11 operating software in most cases. Refer to note in figure 5-5 and refer to table 5-2 for the diagnostic commands.

In those cases where the on-line diagnostics isolate to a subsystem, IOT execution of the individual diagnostics is required to further isolate the failure to an LRU. The IOT is normally connected to the communications processor via the digital patch panel by a through connection. However, the computer operator should ensure that this through connection is not interrupted by an external patch cord plugged into the IOT position at the patch panel.

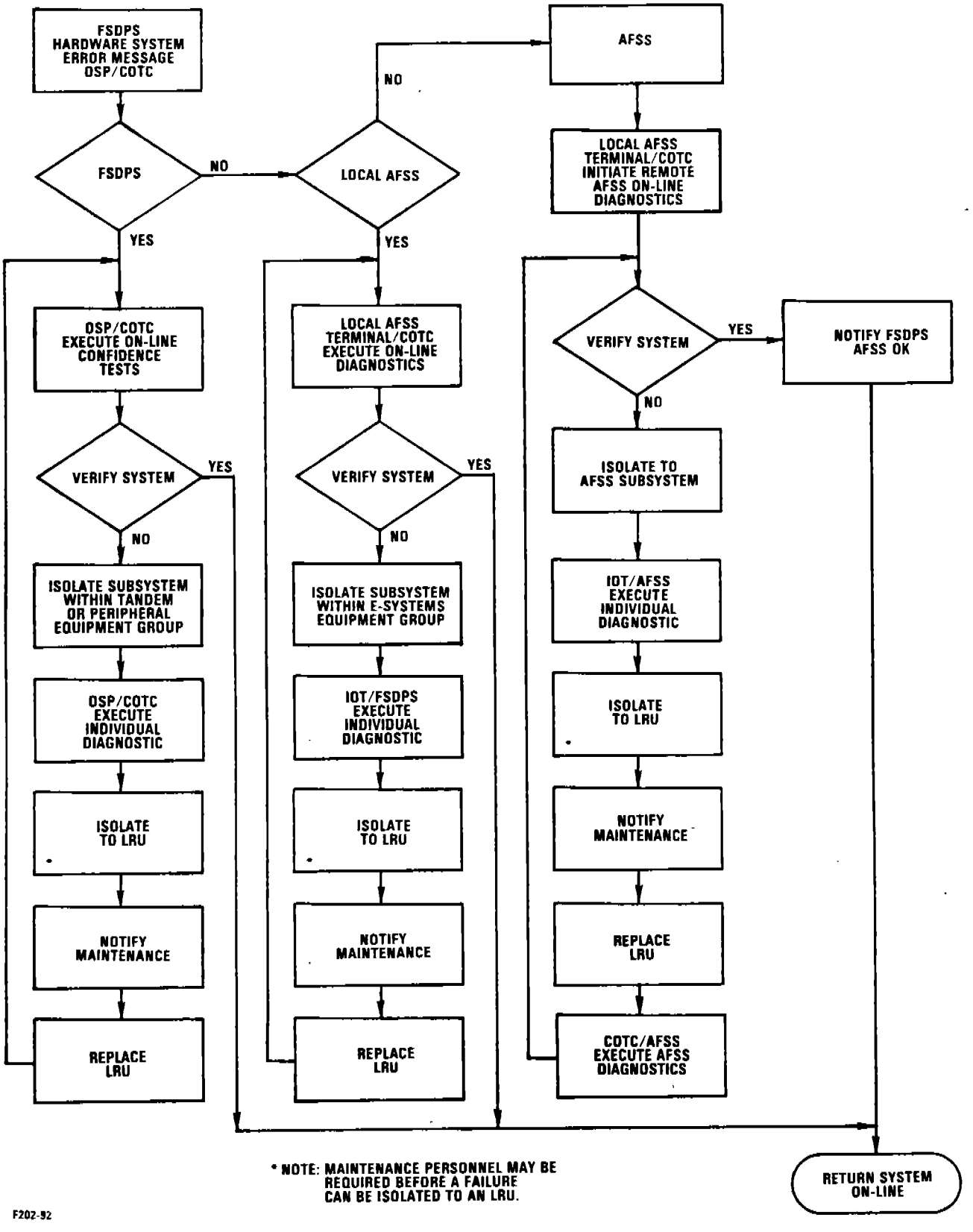

Figure 5-3. M1FC FSAS Failure Event Flow

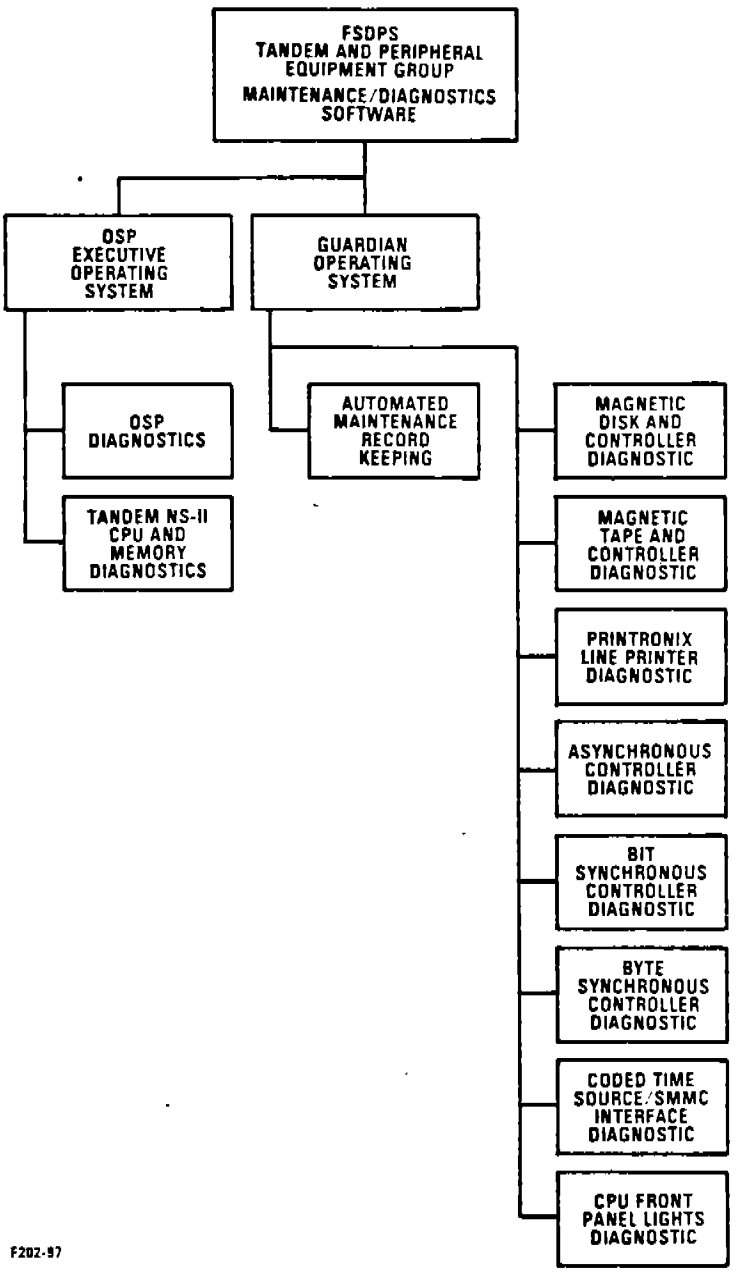

Figure 5-4. Tandem and Peripheral Equipment Group Diagnostic Software Functional Breakdown

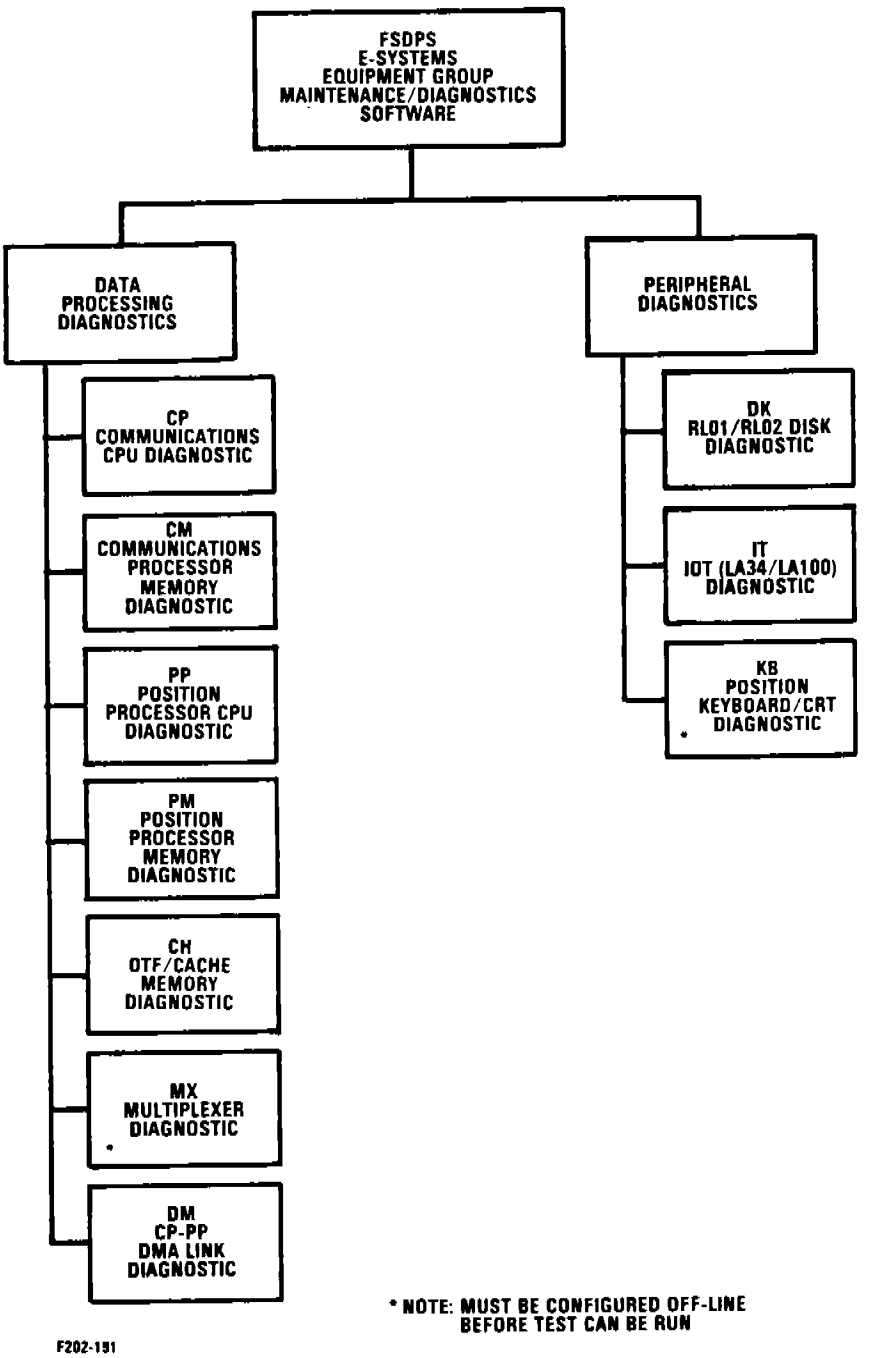

Figure 5-5. E-Systems Equipment Group Diagnostic Software Functional Breakdown

Table 5-2. E-Systems Equipment Group Diagnostic Commands

Diagnostic Commands	Point of Initiation: IOT	Point of Initiation: Local AFSS Terminal/COTC
CP - Communications Processor CPU Diagnostic	X	X
CM - Communications Processor Memory Diagnostic	X	X
PP - Position Processor CPU Diagnostic	X	X
PM - Position Processor Memory Diagnostic	X	X
CH - A/N OTF/Cache Memory Diagnostic	X	X
DK - RL01/RL02 Disk Diagnostic	X	X
DM - CP-PP DMA Link Diagnostic	X	X
IT - IOT (LA34/LA100) Diagnostic	X	
MX - E-Systems Multiplexer Diagnostic	X	
KB - Position Keyboard/CRT Diagnostic	X	

In some cases, maintenance personnel will be required to determine the failed LRU by using off-line test equipment. Maintenance personnel should refer to the Maintenance and Diagnostic Test Set Instruction Book (TI 6490.41) and the Equipment Instruction Book for the M1FC FSAS (TI 6490.37) when troubleshooting a failed system. See figure 5-3 for failure event flow for local AFSS.

Maintenance personnel, when replacing a failed LRU with a spare, will perform a diagnostic checkout on the spare LRU. Once the spare LRU is checked out, it should be configured to operational status and verified.

5.2.3 Repair of FSDPS LRUs.- All Tandem printed circuit modules are repaired at Depot and are not MADTS testable. All E-Systems and DEC LRUs are bench repaired at designated FAA maintenance facilities. Maintenance personnel are directed to the list of related equipment manuals in table 1-1 and Maintenance and Diagnostic Test Set Instruction Book (TI 6490.41).

The MADTS provides the capability for testing printed circuit modules within the E-Systems equipment group and can provide video signals for troubleshooting monitors. The MADTS is provided with disk resident diagnostic software for testing with the exception of PROM based firmware for the testing of its disk drive.

Table 5-3 provides a description, part number, and level of maintenance for all LRUs at the FSDPS.

5.3 AFSS CORRECTIVE MAINTENANCE.- At each AFSS there are three communications processors and up to six position processors. The number of position processors is dependent upon the number of specialist positions at the AFSS. Each communications processor along with its associated position processors and OTF's are referred to as a processor set. Therefore each AFSS has three processor sets. If an element or element path fails within either processor set, the Tandem operating system will detect the failure and mark-down that processor set. The system automatically recovers by rerouting the transmittal actions to another processor set. An error message is generated and displayed at the OSP/COTC at FSDPS and at the COTC at the AFSS, indicating the element path has failed.

A 9600 bps modem failure causes a similar system rerouting, as when a processor set fails. When the Tandem operating system receives no response from one of the processor sets, then that processor set is marked-down and automatic rerouting occurs through another FSDPS line. See figure 5-6 and refer to table 5-4.

Error messages pertaining to an AFSS are displayed on the Facility Supervisor Terminal (FST), on the COTC at the AFSS where the error is detected, and on the OSP/COTC at FSDPS. The error messages

Table 5-3. FSDPS LRU List

Description	Part Number	Level of Maintenance: Fault/ Isolation
CPU	T16/1420	1
CCD	54840	3
IPU	54760	3
MCB	54770	3
Cabinet/Pwr Distribution	T16/7120	1
IPB Controller	51390	3
IPB Terminator	51430	3
I/O Terminator	51440	3
PMI	45029	3
Control Panel Assy	50194	2,3
Memory Module	T16/2420	1
Disk		1
Disk Drive	DM9300TD	2,4
Disk Controller	T16/3106	2,4
Magnetic Tape		1
Mag Tape Drive	T16/5103	2,4
Mag Tape Controller	T16/3202	2,4
Bit Synch Controller	T16/6203	2,4
Asynch Controller	T16/6303	2,4
Asynch Extension Board	T16/6304	2,4
Patch Panels (PP)		4
Synchronous PP	T16/7502	4
Digital PP	157-011-00	4
Asynchronous PP	T16/7501	4
Disk Drive PP	T16/7504	4
Analog PP	153-020-VF-M1	4

(1) On Line Operational Software
(2) Off Line Diagnostic Software
(3) Off Line OSP Microdiagnostics
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

Table 5-3. FSDPS LRU List (Continued)

Description	Part Number	Level of Maintenance: Fault/ Isolation
OSP	T16/3910	3
Floppy Disk Controller	56080	3
Floppy Disk Drive	01730	3
VDU	T16/6530	3,4
SMP	55700	3
Line Printer	T16/5520	3,4
Line Printer	P300	2,5
9600 Baud Modem	RM-9600	5
9600 Baud Fast-poll Modem	RM-9600E FP	5
4800 Baud Modem	RM-208A	5
Manual Call Unit	RM-800 MCU	5
A/O Board	RM-A/0	5
P/S Module	RM8-P/S	5
Modem Enclosure	RM-8E	4
Power Module	T16/7301	1
Battery Pack PU	T16/7303	5
DMA		1
Universal I/O	T16/3401	2
DMA Controller	DMA-QB	2
LSI-11/23	KDF11-AA	1
32K PROM	MRV11-C	1
64K RAM	MSV11-LF	1
Disk	RLV12	1
Disk Drive	RL01	2
Disk Controller	P/0 RLV12	2
System Module	KPV11-B	1,2
CRT (TTL-150)	401-37290-01	4
Coded Time Source Int.	401-36264	1
Coded Time Source	60-DC	1,4
Thermal Alarm	401-37155	4

(1) On Line Operational Software
(2) Off Line Diagnostic Software
(3) Off Line OSP Microdiagnostics
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

Table 5-3. FSDPS LRU List (Continued)

Description	Part Number	Level of Maintenance Fault/ Isolation
Video		1
A/N OTF Processor	401-33676	2
Quad Cache Board	401-33692	2
Power Supply	401-36716-01	4
AC J-Box Assy	401-37231-02	4
Power Control Module	401-36719	4

(1) On Line Operational Software
(2) Off Line Diagnostic Software
(3) Off Line OSP Microdiagnostics
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

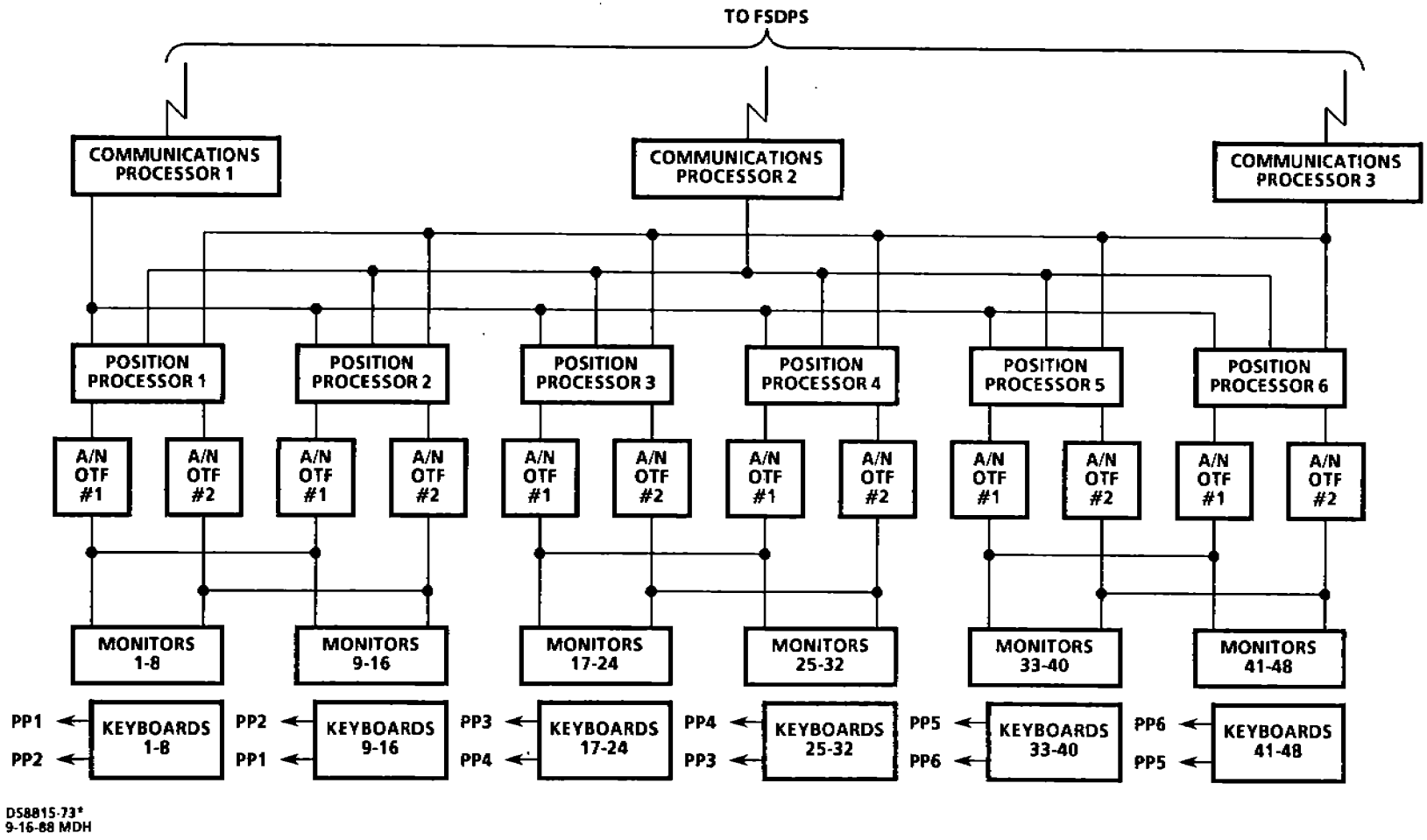

Figure 5-6. Simplified AFSS

Table 5-4. AFSS Automatic Recovery System Elements

1. Communications Processor, consisting of:

   a. DEC Processor (LSI 11/23)
   b. 64K Words RAM Module (MSV11-LF)
   c. 32K Words PROM Module (MRV11-C)
   d. System Module (KPV11-B)
   e. Disk Controller (RLV12)
   f. Disk Drive (RL01/RL02)
   g. Multiplexer (401-36993-01)
   h. Mux I/0 (401-36968)
   i. Eight-Channel Serial I/0 Module (TMI-8S)
   j. DMA I/F (DMA-QB)
   k. Multi-Processor Linking System (HEX-L11)

2. Position Processor, consisting of:

   a. DEC Processor (LSI 11/23)
   b. 64K Words RAM Module (MSV11-LF)
   c. 32K Words PROM Module (MRV11-C)
   d. System Module (KPV11-B)
   e. Eight-Channel Serial I/0 Module (TMI-8S)
   f. DMA I/F (DMA-QB)
   g. A/N OTF Processor Board (401-33676)

3. 9600 bps Modem (RM-9600)

are displayed in plain English so the operator can determine which diagnostic test should be initiated.

Remote AFSS on-line diagnostics can be initiated by the FSDPS computer operator at the local AFSS/COTC or the diagnostics can be run at the AFSS on the FST or COTC depending on the type of error message displayed. See figure 5-3 and figure 5-7.

The on-line diagnostic tests isolate a failure to a subsystem or in some cases to the failed LRU, depending on the type of failure. If the failure is isolated to a subsystem, the AFSS operator is directed to the IOT to execute the individual diagnostics to isolate to the failed LRU. In some cases, maintenance personnel will be required to determine the exact LRU that failed. Refer to table 5-5 for the diagnostic commands and to section 3.2.3.3 of this instruction book for description of each diagnostic.

Maintenance personnel, when replacing a failed LRU with a spare, will perform a diagnostic checkout on the spare LRU. Once the spare LRU is checked out, it should be configured to operational status and verified.

5.3.1 Repair of AFSS LRUs.- Bench repair of LRUs require maintenance personnel to follow maintenance procedures described in the Maintenance and Diagnostic Test Set Instruction Book (TI 6490.41). This manual gives step by step procedures for testing and troubleshooting most AFSS LRUs. For those LRUs which are not MADTS testable refer to the list of related manuals in table 1-1.

Table 5-6 list all LRUs at the AFSS including a description, part number, and level of maintenance.

5.4 AWP CORRECTIVE MAINTENANCE.- The AWP consists of a Tandem Group, communications equipment, two communications processors, two position processors, and peripheral equipment.

The Tandem Group is identical to the Tandem Group in the FSDPS with the addition of Byte Synchronous Controllers, T16/6202. Refer to paragraphs 5.2.1 through 5.2.3 for an explanation of the corrective maintenance for the Tandem Group.

The communications equipment, communications processors, and position processors are identical to AFSS equipment, with the addition of coded time sources (CTSs) and a coded time source interface. Refer to paragraph 5.3 through 5.3.1 for an explanation of the corrective maintenance for this equipment.

Table 5-7 provides a listing of the AWP LRUs.

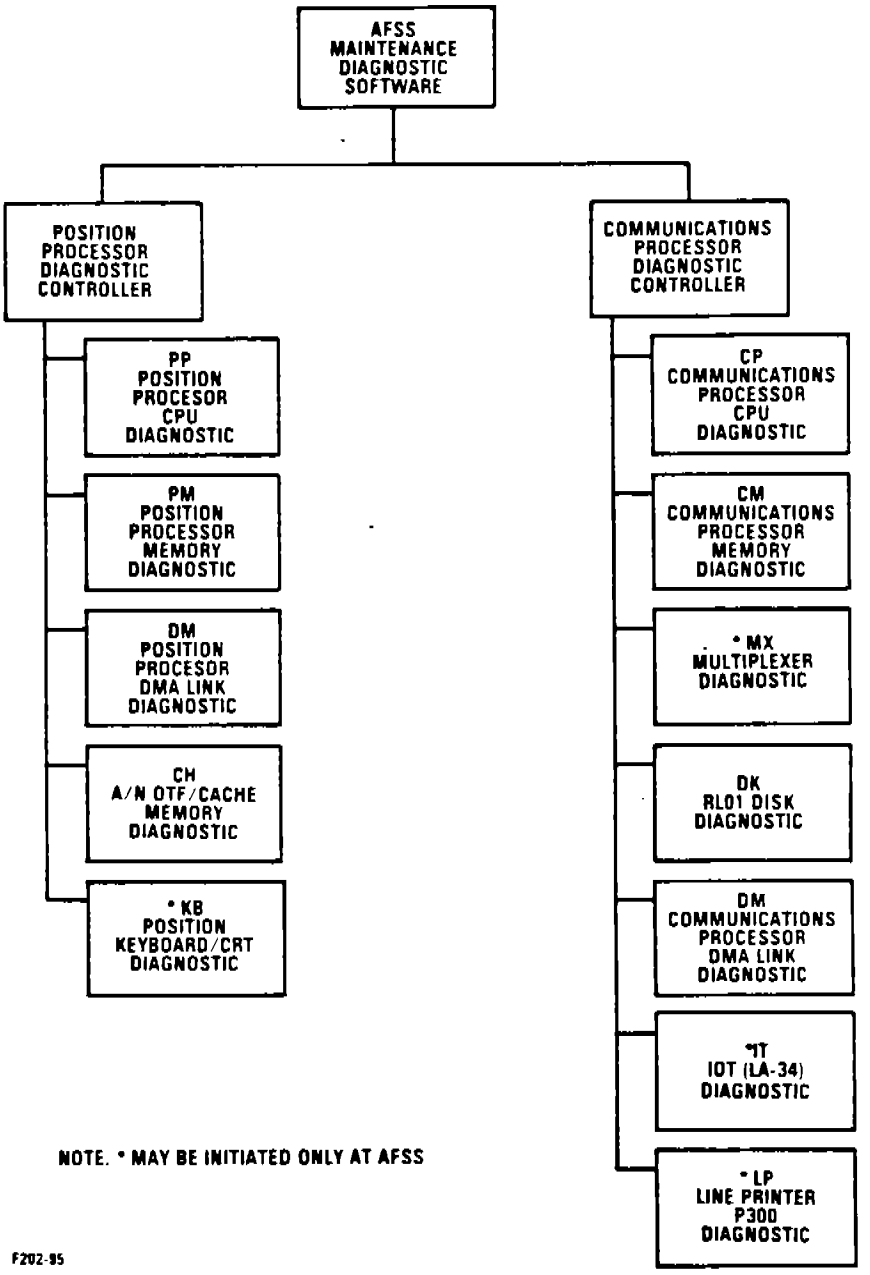

Figure 5-7. AFSS Maintenance Diagnostic Software Functional Breakdown

Table 5-5. AFSS Diagnostic Commands

Diagnostic Commands	Valid Unit Numbers	Point of Initiation: Local (AFSS)	Point of Initiation: Remote COTC (FSDPS/AWP)	Performed Off-line	Performed On-line
CP - Communications Processor CPU Diagnostic	None	X	X	X	
CM - Communications Processor Memory Diagnostic	None	X	X	X	
PP - Position Processor CPU Diagnostic	1-6*	X	X	X	
PM - Position Processor Memory Diagnostic	1-6*	X	X	X	
CH - A/N Cache Memory Diagnostic	1-48*	X	X		X
DK - RL01/RL02 Disk Diagnostic		None	X	X	X
DM - CP-PP DMA Link Diagnostic	None	X	X	X	
LP - Line Printer Diagnostic	None	X			X
IT - IOT (LA34/LA100) Diagnostic		None	X		
MX - E-Systems Multiplexer Diagnostic	None	X			X
KB - Position Keyboard/CRT Diagnostic	1-48*	X			X

*This number can vary, depending upon the number of operator positions at a given AFSS site.

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Table 5-6. AFSS LRU List

Description	Part Number	Level of Maintenance: Fault/ Isolation
Communications Processor		
LSI 11/23	KDF11-AA	1
32K PROM	MRV11-C	1
64K RAM	MSV11-LF	1
Disk	RLV12	1
Disk Controller	P/O RLV12	2
Disk Drive	RL01/RL02	2
Multiplexer	401-36993	2,5
System Module	KPV11-B	1,2
Eight-Channel Serial I/0	8S	1
DMA		1
DMA Controller	DMA-QB	2
DMA IPB	IPB-L11	2
DMA 6 CHNL Adpt.	HEX-L11	2
Power Control Module	401-36719	4
Line Printer	P300	2,5
IOT	LA-34/LA100	1,2
Position Processor		
LSI 11/23	KDF11-AA	1
32K PROM	MRV11-C	1
64K RAM	MSV11-LF	1
Video		1
A/N OTF Processor	401-33676	2
Quad Cache	401-33692	2
Eight-Channel Serial I/0	8S	1
System Module	KPV11-B	1,2
Power Control Module	401-36719	4

(1) On Line Software
(2) Off Line Diagnostic Software
(3) N/A
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

Table 5-6. AFSS LRU List (Continued)

Description	Part Number	Level of Maintenance: Fault/ Isolation
Position Terminal		
Keyboard		2
Keyboard Unit	401-36735	2
Keyboard P/S	401-36707	4
CRT (TTL-150)	401-37290-01	2
Thermal Alarm Assy	401-37155	4
9600 Baud Modem	RM-9600	5
4800 Baud Modem	RM-208A	5
Modem Enclosure	RM-8E	4
Answer/Originate Board	RM-A/0	5
Power Supply Module Board		5
Modem Sharing Device Enclosure	RM-4E	4
Modem Sharing Device	2005064	5
Patch Panels (PP)		4
Digital PP	157-011-00	4
	157-002C-00	4
Analog PP	153-020-12VF-M1	4
Power Supply	401-36716-01	4

(1) On Line Software
(2) Off Line Diagnostic Software
(3) N/A
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

Table 5-7. AWP LRU List

Description	Part Number	Level of Maintenance: Fault/ Isolation
CPU	T16/1420	1
CCD	54840	3
IPU	54760	3
MCB	54770	3
Cabinet/Pwr Distribution	T16/7120	1
IPB Controller	51390	3
IPB Terminator	51430	3
I/O Terminator	51440	3
PMI	45029	3
Control Panel Assy	50194	2,3
Memory Module	T16/2420	1
Disk		1
Disk Drive	DM9300TD	2,4
Disk Controller	T16/3106	2,4
Magnetic Tape		1
Mag Tape Drive	T16/5103	2,4
Mag Tape Controller	T16/3202	2,4
Byte Sync Controller	T16/6202	2,4
Bit Synch Controller	T16/6203	2,4
Asynch Controller	T16/6303	2,4
Asynch Extension Board	T16/6304	2,4
Patch Panels (PP)		4
Synchronous PP	T16/7502	4
Digital PP	157-011-00	4
Asynchronous PP	T16/7501	4
Disk Drive PP	T16/7504	4
Analog PP	153-020-VF-M1	4

(1) On Line Operational Software
(2) Off Line Diagnostic Software
(3) Off Line OSP Microdiagnostics
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

Table 5-7. AWP LRU List (Continued)

Description	Part Number	Level of Maintenance: Fault/ Isolation
Comm Processor		
LSI 11/23	KDF11-AA	1
32K PROM	MRV11-C	1
64K RAM	MSV11-LF	1
Disk	RLV12	1
Disk Controller	P/O RLV12	2
Disk Drive	RL01/RL02	2
Multiplexer	401-36993	2,5
System Module	KPV11-B	1,2
Eight-Channel Serial I/0	8S	1
DMA		1
DMA Controller	DMA-QB	2
DMA IPB	IPB-L11	2
DMA 6 CHNL Adpt.	HEX-L11	2
Power Control Mod	401-36719	4
Line Printer	P300	2,5
IOT	LA-34/LA100	1,2
Position Processor		
LSI 11/23	KDF11-AA	1
32K PROM	MRV11-C	1
64K RAM	MSV11-LF	1
Video		1
A/N OTF Processor	401-33676	2
Quad Cache	401-33692	2
Eight-Channel Serial I/0	8S	1
System Module	KPV11-B	1,2
Power Control Module	401-36719	4

(1) On Line Software
(2) Off Line Diagnostic Software
(3) N/A
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

Table 5-7. AWP LRU List (Continued)

Description	Part Number	Level of Maintenance: Fault/ Isolation
Position Terminal		
Keyboard		2
Keyboard Unit	401-36735	2
Keyboard P/S	401-36707	4
CRT (TTL-150)	401-37290-01	2
Thermal Alarm Assy	401-37155	4
Modem Enclosure	RM-8E	4
9600 Baud Modem	RM-9600	5
9600 Baud Fast-poll Modem	RM-9600E FP	5
Power Supply Module Board		5
Patch Panels (PP)		4
Digital PP	157-011-00	4
	157-002C -00	4
Analog PP	153-020-12VF-M1	4
Power Supply	401-36716-01	4

(1) On Line Software
(2) Off Line Diagnostic Software
(3) N/A
(4) Test Equipment (DVM, Oscilloscope, etc.)
(5) Self Test

SECTION 6

FSAS PARTS LIST

6.1. GENERAL. - This section contains the parts listing for the M1FC FSAS system, which is listed in table 6-1.

The M1FC FSAS System is broken down into three parts; the FSDPS, AFSS, and AWP. Each FSDPS and AFSS have dash numbers which indicates different configurations. Each configuration is listed in the parts list by dash number. Within each dash number, each subsystem is broken down by rack, cabinet, and major assembly. Parts breakdown for the major assemblies are contained in instruction books listed in table 1-1.

6.1.1 Parts List Configuration. - Indenture levels are used in this parts list to show the relation of a line item to the end item. A letter inserted in this block illustrates a lateral and descending relationship of each line item to and within the end item and its discrete components (units), assemblies and subassemblies.

Refer to page xxiii for FSAS Family Tree Chart.

NOTE

The FAA type numbers that appear on equipment nameplates are not item identifying in all cases. One FAA type number may represent more than one configuration of an equipment or subsystem. Therefore, the FAA type numbers should not be used to identify a specific configuration. For complete identification of specific configurations, use the part number that appears on the E-Systems nameplate and refer to the parts list in this manual.

Table 6-1. FSAS System Parts List

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	A	FSDPS	97871	401-37617-01	
Unit 1	B	Communications Switching Rack	97871	401-37622-01	
1A1	C	Coded Time Source	97871	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	
1A7	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
Unit 2	B	Communications Equipment Rack	97871	401-37623-01	
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-800)	57112	1020377	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-01	
3A1 3A2	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assy.	97871	401-37145-02	
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W16	C	AC Supply Cable	97871	401-36786-01	
3W17	C	AC Control Cable	97871	401-36785-01	
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-01	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-01	
W901 W902 W903 W904 W905 W906 W907 W911 W912 W913 W914 W915 W916	B	Cable	97871	401-37273-09	
W945	B	Cable	97871	401-37273-07	
W949- W962	B	Cable	97871	401-37273-04	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	
	A	FSDPS	97871	401-37617-02	
Unit 1	B	Communications Switching Rack	97871	401-37622-02	
1A1	C	Coded Time Source	56738	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	
1A7	C	Digital Patch Panel	25064	157-002C-00	
1A8	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
UNIT 2	B	Communications Equipment Rack	97871	401-37623-01	
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-800)	57112	1020377	
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	RM-8E	
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (4) (RM-9600E FP)	57112	2092284	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-01	
3A1 3A2	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assy.	97871	401-37145-02	
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	
3W16	C	AC Supply Cable	97871	401-36786-01	
3W17	C	AC Control Cable	97871	401-36785-01	
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-01	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-02	
W901 W902	B	Cable	97871	401-37273-09	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W903					
W904					
W905					
W906					
W907					
W908					
W911					
W912					
W913					
W914					
W915					
W916					
W917					
W918					
W919					
W920					
W945 W946	B	Cable	97871	401-37273-07	
W949-W966	B	Cable	97871	401-37273-04	
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	
	A	FSDPS	97871	401-37617-03	
UNIT 1	B	Communications Switching Rack	97871	401-37622-02	
1A1	C	Coded Time Source	56738	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	
1A7	C	Digital Patch Panel	25064	157-002C-00	
1A8	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
UNIT 2	B	Communications Equipment Rack	97871	401-37623-02	
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-800)	57112	1020377	
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Modem (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem	57112	2092842	
	D	Power Supply	57112	1020249	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (4) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-02	
3A1 3A2 3A3	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3A17	C	Blower Assy.	97871	401-37145-02	
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	
3W16	C	AC Supply Cable	97871	401-36786-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W17	C	AC Control Cable	97871	401-36785-01	
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-01	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-03	
W901 W902 W903 W904 W905 W906 W907 W908 W909 W911 W912 W913 W914 W915 W916 W917 W918 W919 W920 W921	B	Cable	97871	401-37273-09	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W922 W923 W924					
W945-W947	B	Cable	97871	401-37273-07	
W949-W966	B	Cable	97871	401-37273-04	
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	
	A	FSDPS	97871	401-37617-04	
UNIT 1	B	Communications Switching Rack	97871	401-37622-02	
1A1	C	Coded Time Source	56738	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
1A7	C	Digital Patch Panel	25064	157-002C-00	
1A8	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
UNIT 2	B	Communications Equipment Rack	97871	401-37623-03	
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-800)	57112	1020377	
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A5	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (4) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-02	
3A1 3A2 3A3	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assy.	97871	401-37145-02	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	
3W16	C	AC Supply Cable	97871	401-36786-01	
3W17	C	AC Control Cable	97871	401-36785-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-02	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-04	
W901- W928	B	Cable	97871	401-37273-09	
W945- W948	B	Cable	97871	401-37273-07	
W949- W978	B	Cable	97871	401-37273-04	
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	
	A	FSDPS	97871	401-37617-05	
UNIT 1	B	Communications Switching Rack	97871	401-37622-03	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
1A1	C	Coded Time Source	56738	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	
1A7	C	Digital Patch Panel	25064	157-002C-00	
1A8	C	Digital Patch Panel	25064	157-002C-00	
1A9	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
UNIT 2	B	Communications Equipment Rack	97871	401-37623-03	
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Modem (RM-800)	57112	1020377	
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-9600)	57112	2092264	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A5	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (4) (RM-8E)	57112	2092284	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-02	
3A1 3A2 3A3	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assy.	97871	401-37145-02	
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	
3W16	C	AC Supply Cable	97871	401-36786-01	
3W17	C	AC Control Cable	97871	401-36785-01	
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-02	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-05	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W901-W932	B	Cable	97871	401-37273-09	
W945-W948	B	Cable	97871	401-37273-07	
W949-W978	B	Cable	97871	401-37273-04	
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	
	A	FSDPS	97871	401-37617-06	
UNIT 1	B	Communications Switching Rack	97871	401-37622-03	
1A1	C	Coded Time Source	56738	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	
1A7	C	Digital Patch Panel	25064	157-002C-00	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
1A8	C	Digital Patch Panel	25064	157-002C-00	
1A9	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
UNIT 2	B	Communications Equipment Rack	97871	401-37623-04	
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-800)	57112	1020377	
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A5	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A6	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (4) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-03	
3A1 3A2 3A3 3A4	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assy.	97871	401-37145-02	
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	
3W16	C	AC Supply Cable	97871	401-36786-01	
3W17	C	AC Control Cable	97871	401-36785-01	
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-02	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-06	
W901- W936	B	Cable	97871	401-37273-09	
W945- W948	B	Cable	97871	401-37273-07	
W949- W982	B	Cable	97871	401-37273-04	
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	
	A	FSDPS	97871	401-37617-07	
UNIT 1	B	Communications Switching Rack	97871	401-37622-03	
1A1	C	Coded Time Source	56738	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	
1A7	C	Digital Patch Panel	25064	157-002C-00	
1A8	C	Digital Patch Panel	25064	157-002C-00	
1A9	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
UNIT 2	B	Communications Equipment Rack	97871	401-37623-04	
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-800)	57112	1020377	
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A5	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A6	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (4) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-03	
3A1 3A2 3A3 3A4	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assy.	97871	401-37145-02	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	
3W16	C	AC Supply Cable	97871	401-36786-01	
3W17	C	AC Control Cable	97871	401-36785-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-02	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-07	
W901- W940	B	Cable	97871	401-37273-09	
W945- W948	B	Cable	97871	401-37273-07	
W949- W986	B	Cable	97871	401-37273-04	
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	
	A	FSDPS	97871	401-37617-08	
UNIT 1	B	Communications Switching Rack	97871	401-37622-04	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
1A1	C	Coded Time Source	56738	60DC	
1A2	C	Coded Time Source Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm Assembly	97871	401-37155-01	
1A5	C	Digital Patch Panel	25064	157-002C-00	
1A6	C	Digital Patch Panel	25064	157-002C-00	
1A7	C	Digital Patch Panel	25064	157-002C-00	
1A8	C	Digital Patch Panel	25064	157-002C-00	
1A9	C	Digital Patch Panel	25064	157-002C-00	
1A10	C	Digital Patch Panel	25064	157-002C-00	
1A11	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A12	C	Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	
1W1-1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm. Cable	97871	401-37273-12	
UNIT 2	B	Communications Equipment Rack	97871	401-37623-05	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
2A1	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (RM-800)	57112	1020377	
	D	Modem (RM-208)	57112	2082278	
	D	Modem (RM-A/O)	57112	1020364	
	D	Modem Power Supply (2)	57112	1020249	
2A2	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem	57112	RM-9600	
	D	Modem	57112	RM-9600E FP	
	D	Power Supply	57112	1020249	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (5) (RM-9600)	57112	2092284	
	D	Modem (RM-9600E FP)	57112	2092842	
	D	Power Supply	57112	1020249	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A5	C	Modem Enclosure (RM-8E)	57112	2005060	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A6	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (8) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A7	C	Modem Enclosure (RM-8E)	57112	2005060	
	D	Modem (4) (RM-9600)	57112	2092284	
	D	Power Supply	57112	1020249	
2A16	C	AC Junction Box	97871	401-37231-03	
UNIT 3	B	COTC Processor Rack	97871	401-37624-03	
3A1 3A2 3A3 3A4	C	Analog Patch Panel	56657	153-020-12VF-M1	
3A5	C	COTC Card Cage	97871	401-42600-01	
3A6	C	Mux Interface Panel	97871	401-37170-04	
3A9	C	Serial I/O Assy	97871	401-37274-01	
3A10	C	Kybd. J-Box	97871	401-37179-07	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assy.	97871	401-37145-02	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3A18	C	Thermal Sensor	97871	401-37216-02	
3A19	C	Thermal Sensor	97871	401-37204-01	
3PS5 3PS6	C	Power Supply	97871	401-36716-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	+12V Cable	97871	401-36715-02	
3W5	C	-12V Cable	97871	401-36715-04	
3W6	C	+5V Cable	97871	401-36715-06	
3W7 3W8	C	Mux Int Pwr Cable	97871	401-37172-01	
3W9	C	AC Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-01	
3W11	C	Interprocessor Bus Cable	97871	401-37958-01	
3W12	C	DMA/HEX-L11 Cable	97871	401-42686-01	
3W13 3W14	C	Mux Interface Cable	97871	401-37142-01	
3W15	C	Kybd J-Box Cable	97871	401-36773-01	
3W16	C	AC Supply Cable	97871	401-36786-01	
3W17	C	AC Control Cable	97871	401-36785-01	

Table 6-1. FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W19 3W20	C	Blower Cable	97871	401-37241-01	
3W21 3W22 3W23 3W24	C	OTF/Cache Cable	97871	401-42685-01	
3W25 3W26	C	Analog Patch Cable	97871	401-37594-08	
	B	Tandem Group	97871	401-42690-02	
	B	FSDPS Peripheral Group	97871	401-37729-01	
	B	Cable Set (W800)	97871	401-42698-07	
W901- W944	B	Cable	97871	401-37273-09	
W945- W948	B	Cable	97871	401-37273-07	
W949- W990	B	Cable	97871	401-37273-04	
W991 W992	B	Cable	97871	401-37273-14	
W993	B	Cable	97871	401-37203-05	
W994	B	Cable	97871	401-37203-02	
W997	B	Cable	97871	401-37273-08	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	A	AFSS	97871	401-37618-01	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
1A1	C	Thermal Alarm	97871	401-37155-01	
1A2	C	Analog Patch Panel	56657	153-020-12VF-M1	
1A3 1A4	C	Digital Patch Panel	25064	157-011-00	
1A5 1A6 1A7	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A16	C	AC Junction Box	97871	401-37231-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
2A1	C	MSD Enclosure (RM-4E)	57112	2005061	
2A1A1- 2A1A4	D	Modem Sharing Device	57112	2005064	
2A2	C	MSD Enclosure (RM-4E)	57112	2005061	
2A2A1- 2A2A3	D	Modem Sharing Device	57112	2005064	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
2A3A3	D	Modem (RM-208)	57112	2082278	
2A3A4	D	Modem (RM-A/O)	57112	1020364	
2A3A5- 2A3A8	D	Modem (RM-9600)	57112	2092284	
2A4	C	Dual Comm Proc Card Cage	97871	401-37999-04	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	A	AFSS	97871	401-37618-01	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
1A1	C	Thermal Alarm	97871	401-37155-01	
1A2	C	Analog Patch Panel	56657	153-020-12VF-M1	
1A3 1A4	C	Digital Patch Panel	25064	157-011-00	
1A5 1A6 1A7	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A16	C	AC Junction Box	97871	401-37231-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
2A1	C	MSD Enclosure (RM-4E)	57112	2005061	
2A1A1- 2A1A4	D	Modem Share Device	57112	2005064	
2A2	C	MSD Enclosure (RM-4E)	57112	2005061	
2A2A1- 2A2A3	D	Modem Share Device	57112	2005064	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
2A3A3	D	Modem (RM-208)	57112	2082278	
2A3A4	D	Modem (RM-A/O)	57112	1020364	
2A3A5- 2A3A8	D	Modem (RM-9600)	57112	2092284	
2A4	C	Dual Comm Proc Card Cage	97871	401-37999-04	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
2W9	C	PCM DC Pwr Cable	97871	401-36786-01	
2W10	C	+5V Cable	97871	401-36715-06	
2W11	C	-12V Cable	97871	401-36715-04	
2W12	C	+12V Cable	97871	401-36715-01	
2W13	C	Interprocessor Bus Cable	97871	401-37958-01	
2W14-2W17	C	Mux Buildup Cable	97871	401-38072-01	
2W18-2W21	C	Mux IF Power Cable	97871	401-37172-01	
2W22	C	PCM AC Power Cable	97871	401-36785-02	
2W23-2W26	C	Mux Buildup Cable	97871	401-38072-02	
2W27 2W28	C	Interprocessor Bus Cable	97871	401-37958-01	
2W29-2W32	C	Mux Buildup Cable	97871	401-38072-03	
2W33	C	-12V Cable	97871	401-36715-03	
2W34	C	+12V Cable	97871	401-36715-01	
2W35	C	+5V Cable	97871	401-36715-05	
2W36	C	PCM DC Pwr Cable	97871	401-36786-01	
2W37	C	MSD Cable	97871	401-39128-01	
2W38	C	MSD Cable	97871	401-39135-01	
2W39	C	MSD Cable	97871	401-39142-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
2W40	C	MSD Cable	97871	401-39129-01	
2W41	C	MSD Cable	97871	401-39136-01	
2W42	C	MSD Cable	97871	401-39143-01	
2W43	C	MSD Cable	97871	401-39130-01	
2W44	C	MSD Cable	97871	401-39137-01	
2W45	C	MSD Cable	97871	401-39144-01	
2W46	C	MSD Cable	97871	401-39131-01	
2W47	C	MSD Cable	97871	401-39138-01	
2W48	C	MSD Cable	97871	401-39145-01	
2W49	C	MSD Cable	97871	401-39132-01	
2W50	C	MSD Cable	97871	401-39139-01	
2W51	C	MSD Cable	97871	401-39146-01	
2W52	C	MSD Cable	97871	401-39133-01	
2W53	C	MSD Cable	97871	401-39140-01	
2W54	C	MSD Cable	97871	401-39147-01	
2W55	C	MSD Cable	97871	401-39134-01	
2W56	C	MSD Cable	97871	401-39141-01	
2W57	C	MSD Cable	97871	401-39148-01	
2W58-2W64	C	MSD Power Cord Cable	97871	10096	
2W67 2W68	C	Line Printer Adapter Cable	97871	401-42624-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
UNIT 3	B	Position Processor Rack	97871	401-37616-01	
3A1	C	Position Processor Card Cage	97871	401-37999-01	
3A2	C	Memory "A" Card Cage	97871	401-37999-02	
3A3	C	Memory "B" Card Cage	97871	401-37999-06	
3A4	C	Position Processor Card Cage	97871	401-37999-01	
3A8 3A9	C	Serial I/O Panel	97871	401-37274-02	
3A10	C	Keyboard J-Box	97871	401-37179-08	
3A16	C	AC Junction Box	97871	401-37321-02	
3A17	C	Blower Assembly	97871	401-37145-02	
3A18	C	Thermal Alarm Sensor	97871	401-37216-02	
3PS1 3PS3 3PS5 3PS7	C	Power Supply	97871	401-36716-01	
3S1	C	DC Power Switch	97871	401-37916-01	
3W1	C	+12V Cable	97871	401-36715-01	
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	A/C Supply Cable	97871	401-36786-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W5	C	AC Control Cable	97871	401-36785-03	
3W6	C	+12V Cable	97871	401-36715-01	
3W7	C	-12V Cable	97871	401-36715-01	
3W8	C	+5V Cable	97871	401-36715-05	
3W9	C	A/C Supply Cable	97871	401-36786-01	
3W10	C	AC Control Cable	97871	401-36785-03	
3W11	C	+12V Cable	97871	401-36715-01	
3W12	C	-12V Cable	97871	401-36715-03	
3W13	C	+5V Cable	97871	401-36715-05	
3W14	C	A/C Supply Cable	97871	401-36786-01	
3W15	C	A/C Control Cable	97871	401-36785-02	
3W16	C	+12V Cable	97871	401-36715-01	
3W17	C	-12V Cable	97871	401-36715-03	
3W18	C	+5V Cable	97871	401-36715-05	
3W19	C	A/C Supply Cable	97871	401-36786-01	
3W20	C	A/C Control Cable	97871	401-36785-01	
3W21 3W22	C	Fan Power Cable	97871	401-37241-01	
3W23 3W25	C	DC Switch Cable	97871	401-37927-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W27	C	Power Term Cable	97871	401-37914-01	
3W28 3W31	C	Keyboard J-Box Cable	97871	401-36773-01	
3W32-3W35 3W40-3W43	C	OTF Bus Cable	97871	401-37995-01	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W930-W932	B	Disk Drive Cable	97871	BC06R-06	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
	A	AFSS	97871	401-37618-02	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-02	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
	A	AFSS	97871	401-37618-03	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-02	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W930-W932	B	Disk Drive Cable	97871	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	A	AFSS	97871	401-37618-04	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-04	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
	A	AFSS	97871	401-37618-05	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-03	
UNIT 4	B	Position Processor Rack	97871	401-37616-02	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	

Table 6-1. M1FC FSAS System Parts List (Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W926 W927	B	Digital Panel Cable	97871	401-37126-03	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	
W942	B	DMA Cable	97871	401-37986-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	A	AFSS	97871	401-37618-06	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3 UNIT 4	B	Position Processor Rack	97871	401-37616-03	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W906- W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911- W915	B	Digital Panel Cable	97871	401-37273-02	
W916- W920	B	Digital Panel Cable	97871	401-37273-01	
W921- W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W926 W927	B	Digital Panel Cable	97871	401-37126-03	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	
W942	B	DMA Cable	97871	401-37986-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	
	A	AFSS	97871	401-37618-07	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-03	
UNIT 4	B	Position Processor Rack	97871	401-37616-04	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W926 W927	B	Digital Panel Cable	97871	401-37126-03	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	

Table 6-1. M1FC FSAS System Parts List (Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	
W942	B	DMA Cable	97871	401-37986-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	
	A	AFSS	97871	401-37618-08	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-04	
UNIT 4	B	Position Processor Rack	97871	401-37616-04	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W926 W927	B	Digital Panel Cable	97871	401-37126-03	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W942	B	DMA Cable	97871	401-37986-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	
	A	AFSS	97871	401-37618-09	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-03	
UNIT 4	B	Position Processor Rack	97871	401-37616-03	
UNIT 5	B	Position Processor Rack	97871	401-37616-03	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W905	B	Thermal Alarm Cable	97871	401-37203-04	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W926 W927	B	Digital Panel Cable	97871	401-37126-03	
W928 W929	B	Digital Panel Cable	97871	401-37126-04	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W937	B	DMA Cable	97871	401-37988-01	
W938	B	DMA Cable	97871	401-37991-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	
W942	B	DMA Cable	97871	401-37986-01	
W943	B	DMA Cable	97871	401-37989-01	
W944	B	DMA Cable	97871	401-37992-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	
W949	B	DMA Cable	97871	401-37990-01	
W950	B	DMA Cable	97871	401-37993-01	
	A	AFSS	97871	401-37618-10	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-04	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
UNIT 4	B	Position Processor Rack	97871	401-37616-03	
UNIT 5	B	Position Processor Rack	97871	401-37616-03	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W905	B	Thermal Alarm Cable	97871	401-37203-04	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W926 W927	B	Digital Panel Cable	97871	401-37126-03	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W928 W929	B	Digital Panel Cable	97871	401-37126-04	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	
W937	B	DMA Cable	97871	401-37988-01	
W938	B	DMA Cable	97871	401-37991-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	
W942	B	DMA Cable	97871	401-37986-01	
W943	B	DMA Cable	97871	401-37989-01	
W944	B	DMA Cable	97871	401-37992-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	
W949	B	DMA Cable	97871	401-37990-01	
W950	B	DMA Cable	97871	401-37993-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	A	AFSS	97871	401-37618-11	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-04	
UNIT 4	B	Position Processor Rack	97871	401-37616-04	
UNIT 5	B	Position Processor Rack	97871	401-37616-03	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W905	B	Thermal Alarm Cable	97871	401-37203-04	
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W926 W927	B	Digital Panel Cable	97871	401-37126-03	
W928 W929	B	Digital Panel Cable	97871	401-37126-04	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	
W937	B	DMA Cable	97871	401-37988-01	
W938	B	DMA Cable	97871	401-37991-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	
W942	B	DMA Cable	97871	401-37986-01	
W943	B	DMA Cable	97871	401-37989-01	
W944	B	DMA Cable	97871	401-37992-01	
W945	B	DMA Cable	97871	401-37978-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	
W949	B	DMA Cable	97871	401-37990-01	
W950	B	DMA Cable	97871	401-37993-01	
	A	AFSS	97871	401-37618-12	
UNIT 1	B	Communications Equipment Rack	97871	401-37614-01	
UNIT 2	B	Communications Processor Rack	97871	401-37615-01	
UNIT 3	B	Position Processor Rack	97871	401-37616-04	
UNIT 4	B	Position Processor Rack	97871	401-37616-04	
UNIT 5	B	Position Processor Rack	97871	401-37616-04	
	B	Peripheral Group	97871	401-37275-01	
W901	B	Thermal Alarm Cable	97871	401-37203-02	
W902	B	Thermal Alarm Cable	97871	401-37203-04	
W903	B	Thermal Alarm Cable	97871	401-37203-02	
W904	B	Thermal Alarm Cable	97871	401-37203-03	
W905	B	Thermal Alarm Cable	97871	401-37203-04	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W906-W909	B	Analog Patch Cable	97871	401-37273-03	
W910	B	Analog Patch Cable	97871	401-37273-06	
W911-W915	B	Digital Panel Cable	97871	401-37273-02	
W916-W920	B	Digital Panel Cable	97871	401-37273-01	
W921-W923	B	Digital Panel Cable	97871	401-37126-01	
W924 W925	B	Digital Panel Cable	97871	401-37126-02	
W926 W927	B	Digital Panel Cable	97871	401-37126-03	
W928 W929	B	Digital Panel Cable	97871	401-37126-04	
W930-W932	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	
W935	B	DMA Cable	97871	401-37982-01	
W936	B	DMA Cable	97871	401-37985-01	
W937	B	DMA Cable	97871	401-37988-01	
W938	B	DMA Cable	97871	401-37991-01	
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	
W941	B	DMA Cable	97871	401-37983-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W942	B	DMA Cable	97871	401-37986-01	
W943	B	DMA Cable	97871	401-37989-01	
W944	B	DMA Cable	97871	401-37992-01	
W945	B	DMA Cable	97871	401-37978-01	
W946	B	DMA Cable	97871	401-37981-01	
W947	B	DMA Cable	97871	401-37984-01	
W948	B	DMA Cable	97871	401-37987-01	
W949	B	DMA Cable	97871	401-37990-01	
W950	B	DMA Cable	97871	401-37993-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
	A	AWP	97871	401-12300-01	
UNIT 1	B	Communications Equipment Rack	97871	401-12301-01	
1A1	C	Coded Time Source	56738	60DC	
1A2	C	CTS Interface	97871	401-37207-01	
1A3	C	Coded Time Source	56738	60DC	
1A4	C	Thermal Alarm	97871	401-37207-01	
1A5-1A7	C	Digital Patch Panel	25064	157-002C-00	
1A8 1A9	C	Disk Drive	15476	RL01-AK/RL02-AK	
1A10	C	Multiple Outlet Strip	22012	602	
1A16	C	AC Junction Box	97871	401-37231-01	
1W1 1W2	C	CTS Cable	97871	401-36743-01	
1W3	C	Comm Cable	97871	401-37273-12	
UNIT 2	B	Communications Processor Rack	97871	401-12302-01	
2A1 2A2	C	Analog Patch Panel	56657	153-020-12VF-M1	
2A3	C	Modem Enclosure (RM-8E)	57112	2005060	
2A3A1-2A3A8	D	Modem (RM-9600E FP)	57112	2092842	
2A4	C	Modem Enclosure (RM-8E)	57112	2005060	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
2A4A1-2A4A8	D	Modem (RM-9600)	57112	2092284	
2A5	C	Modem Enclosure (RM-8E)	57112	2005060	
2A5A7	D	Modem (RM-9600E FP)	57112	2092842	
2A5A8	D	Modem (RM-9600)	57112	2092284	
2A6	C	Card Cage	97871	401-37999-04	
2A8	C	Multiplexer Interface	97871	401-37170-01	
2A9 2A10	C	Multiple Outlet Strip	22012	602	
2A16	C	AC Junction Box	97871	401-37231-02	
2A17	C	Blower Assembly	97871	401-37145-02	
2A18	C	Thermal Sensor	97871	401-37216-02	
2A19	C	Thermal Sensor	97871	401-37204-01	
2PS5 2PS6	C	Power Supply	97871	401-36716-01	
2W1	C	+12V Cable	97871	401-36715-01	
2W2	C	-12V Cable	97871	401-36715-03	
2W3	C	+5V Cable	97871	401-36715-05	
2W4	C	AC Supply Cable	97871	401-36786-01	
2W5 2W8	C	AC Control Cable	97871	401-36785-01	
2W9	C	AC Supply Cable	97871	401-36786-01	
2W10	C	+5V Cable	97871	401-36715-06	

Table 6-1. M1FC FSAS System Parts List (Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
2W11	C	-12V Cable	97871	401-36715-04	
2W12	C	+12V Cable	97871	401-36715-02	
2W27 2W28	C	Interprocessor Bus Cable	97871	401-37958-01	
UNIT 3	B	Position Processor Rack	97871	401-12303-01	
3A1	C	Position Processor Card Cage	97871	401-37999-01	
3A2	C	Memory "A" Card Cage	97871	401-37999-02	
3A3	C	Memory "B" Card Cage	97871	401-37999-06	
3A4	C	Position Processor Card Cage	97871	401-37999-01	
3A8 3A9	C	Serial I/O Panel	97871	401-37274-02	
3A10	C	Keyboard Junction Box	97871	401-37179-08	
3A16	C	AC Junction Box	97871	401-37231-02	
3A17	C	Blower Assembly	97871	401-37145-02	
3A18	C	Thermal Alarm Sensor	97871	401-37216-02	
3PS1 3PS3 3PS5 3PS7	C	Power Supply	97871	401-36716-01	
3S1	C	DC Power Switch	97871	401-37916-01	
3W1	C	+12V Cable	97871	401-36715-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W2	C	-12V Cable	97871	401-36715-03	
3W3	C	+5V Cable	97871	401-36715-05	
3W4	C	A/C Supply Cable	97871	401-36786-01	
3W5	C	A/C Control Cable	97871	401-36785-03	
3W6	C	+12V Cable	97871	401-36715-01	
3W7	C	-12V Cable	97871	401-36715-03	
3W8	C	+5V Cable	97871	401-36715-05	
3W9	C	A/C Supply Cable	97871	401-36786-01	
3W10	C	A/C Control Cable	97871	401-36785-03	
3W11	C	+12V Cable	97871	401-36715-01	
3W12	C	-12V Cable	97871	401-36715-03	
3W13	C	+5V Cable	97871	401-36715-05	
3W14	C	A/C Supply Cable	97871	401-36786-01	
3W15	C	A/C Control Cable	97871	401-36785-02	
3W16	C	+12V Cable	97871	401-36715-01	
3W17	C	-12V Cable	97871	401-36715-03	
3W18	C	+5V Cable	97871	401-36715-05	
3W19	C	A/C Supply Cable	97871	401-36786-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
3W20	C	A/C Control Cable	97871	401-36785-01	
3W21 3W22	C	Fan Power Cable	97871	401-37241-01	
3W23 3W25	C	DC Switch Cable	97871	401-37927-01	
3W27	C	Power Terminator Cable	97871	401-37914-01	
3W28 3W31	C	Kybd J-Box Cable	97871	401-36773-01	
3W32-3W35 3W40-3W43	C	OTF Bus Cable	97871	401-37995-01	
	B	Tandem Group	97871	401-42690-04	
	B	Peripheral Group	97871	401-12305-01	
	B	Cable Set (W800)	97871	401-42698-09	
W904-W917	B	Digital Patch Panel Cable	97871	401-37273-09	
W921 W922 W924 W925	B	Digital Patch	97871	401-37126-02	
W930 W931	B	Disk Drive Cable	15476	BC06R-06	
W933	B	DMA Cable	97871	401-37976-01	
W934	B	DMA Cable	97871	401-37979-01	

Table 6-1. M1FC FSAS System Parts List
(Continued)

Ref. Design.	Indent.	Name of Part/ Description	Mfr. Code Number	Jan/Mil Mfr's Part No.	Notes
W939	B	DMA Cable	97871	401-37977-01	
W940	B	DMA Cable	97871	401-37980-01	

SECTION 7

INSTALLATION, INTEGRATION, AND CHECKOUT

7.1 GENERAL.- Each FSDPS, AWP, and AFSS is initially installed by E-Systems for the FAA. In the event that it becomes necessary to change the equipment arrangement or location at a future date, the following requirements and procedures are provided as a guide.

Installation, integration, and checkout procedures are provided for a typical FSDPS, AWP, and AFSS system. It may be necessary to refer to the M1FC FSAS Equipment Instruction Book, TI 6490.37, or to related manuals listed in table 1-1 for installation of equipment that is mounted in racks containing other equipment.

7.2 FSDPS/AWP SYSTEM.- A typical FSDPS/AWP system consists of the items listed below.

Item 1	- Central Processor Unit Cabinet	1
Item 2	- Controller Cabinet	1
Item 3	- Magnetic Tape Drives	2
Item 4	- Communications Switching Rack (FSDPS)	1
	- Communications Equipment Rack (AWP)	1
Item 5	- Communications Equipment Rack (FSDPS)	1
	- Communications Processor Rack (AWP)	1
Item 6	- COTC Processor Rack (FSDPS)	1
	- Position Processor Rack (AWP)	1
Item 7	- Disk Drives	8
Item 8	- Input/Output Terminal (IOT)	1
Item 9	- Operations and Service Processor (Includes Tandem 6530 CRT and 5520 printer for each OSP)	2
Item 10	- COTC/Local AFSS Terminals	2
Item 11	- Line Printers	2

7.2.1 FSDPS/AWP Site Requirements.- Site requirements consist of electrical and physical requirements.

The electrical requirements for a typical FSDPS/AWP is an uninterruptible power source (UPS) of 225 amperes, 120/208 volts and a power distribution panel with 42 possible single pole breaker positions.

The required breakers for the power distribution panel are as follows:

40 ampere, three pole - four each
30 ampere, three pole - four each
30 ampere, single pole - three each
20 ampere, single pole - nine each

NOTE

These breakers conform to FED-SPEC W-C-375.

A breaker arrangement for a typical FSDPS/AWP is shown in figure 7-1.

One additional power panel is required providing a 20 ampere, single pole circuit breaker for the convenience outlets at the base of the E-Systems configured cabinets.

An isolated ground plate is required in the vicinity of the main power distribution panel. The wire connecting the ground point in the equipment racks to the ground plate is insulated and at least AWG #6 in size.

The physical requirements for an FSDPS/AWP consists of a floor area of 28 feet by 26 feet. A basic floor plan for the FSDPS is shown in figure 7-2, and a basic floor plan for the AWP is shown in figure 7-3. The selected area must be maintained at an ambient temperature of +15 to +32 degrees Celsius and a relative humidity between 20 and 80 percent.

The physical characteristics of the FSDPS/AWP equipment are given in table 7-1. Table 7-2 list the dimensions and clearance requirements of the equipment along with maximum signal cable lengths.

7.2.2 Site Survey.- The installation area selected must meet the above requirements and be located when possible on a raised floor. Examine existing distribution routes for signal, power, and ground cables. Examine the amount of space available in cable ladders, ducts, troughs, and conduits. Note existing sources for power and grounds. Locate the demarcation point for telephone circuits. Identify locations of existing convenience outlets. Assess the available environmental control system capabilities.

Establish a floor plan layout (refer to figures 7-2 and 7-3). Verify facility requirements. Identify desired equipment locations. Determine routes for signal, control, power, and grounding cables. Refer to table 7-1 and table 7-2 for equipment parameters, limitations, and signal cable length restrictions.

7.2.3 Signal Cable Routing.- All signal cables provided for the FSDPS/AWP will be run under a raised floor when possible. The cables will enter and exit the subfloor plenum through holes cut in the floor tiles.

Signal cables for peripherals will exit from the bottom of the equipment racks to the subfloor and run along the subfloor in a direct path to their destinations. No cable will exceed its maximum allowable cable length.

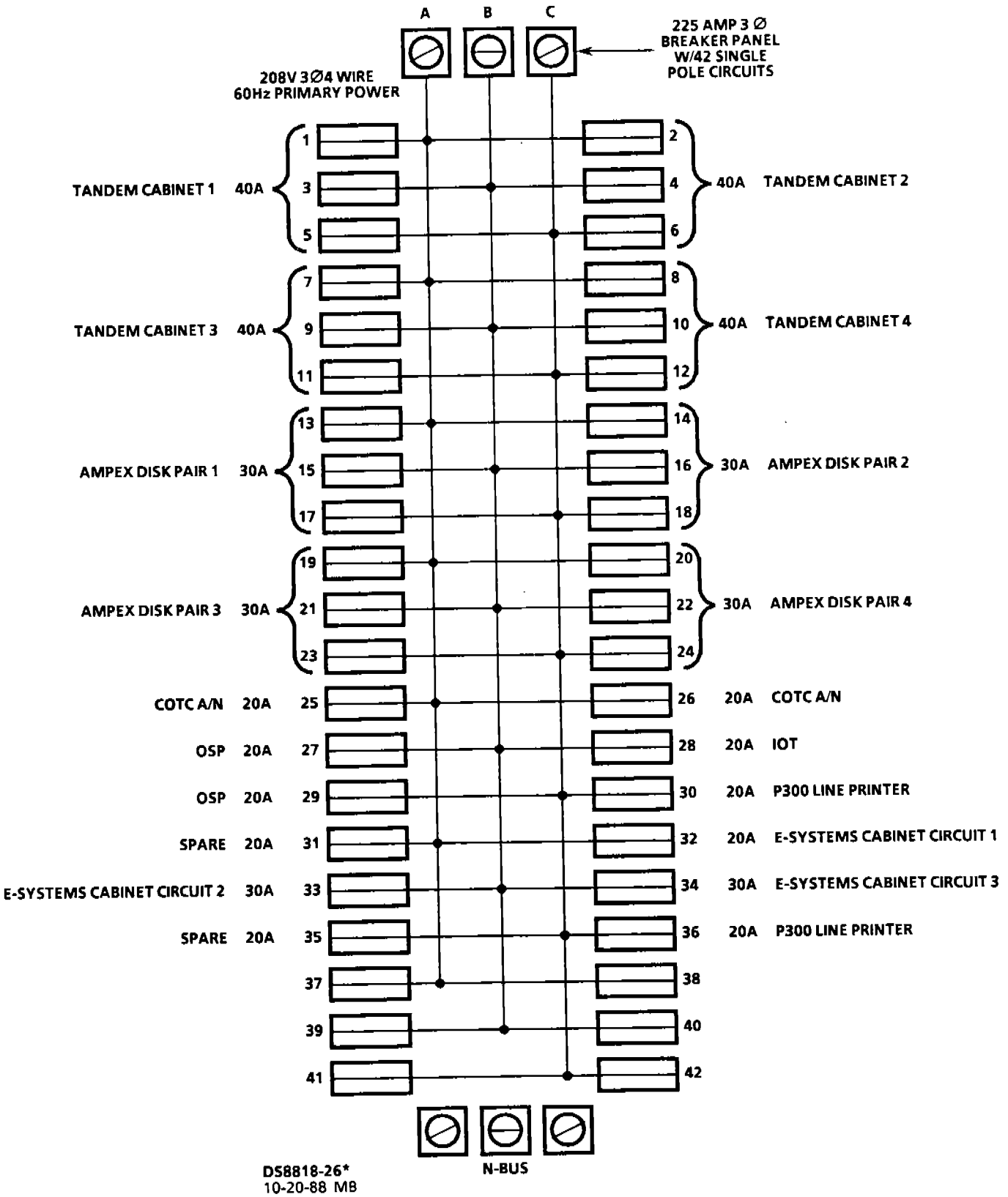

Figure 7-1. Typical M1FC FSDPS/AWP Breaker Arrangement

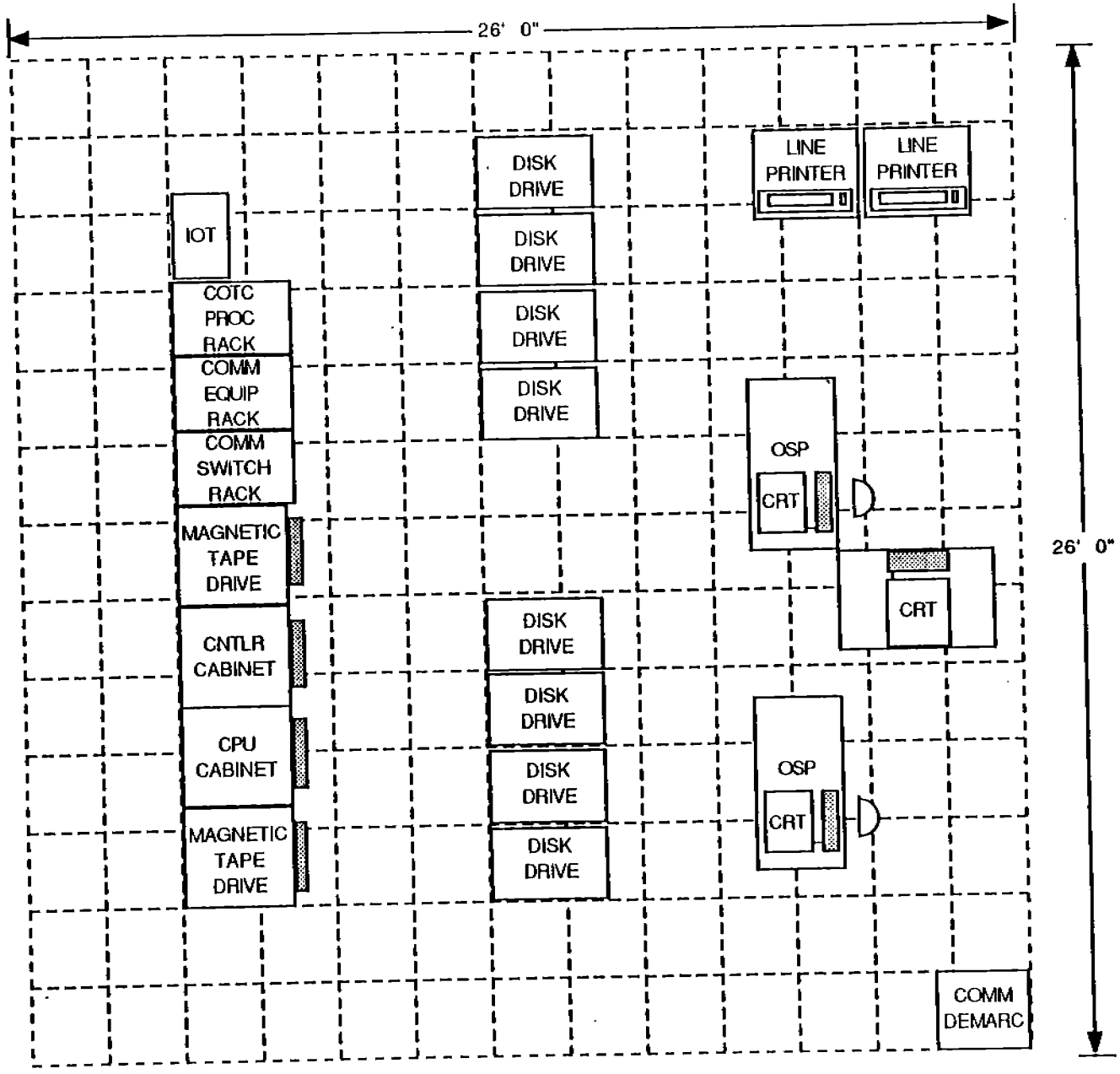

Figure 7-2. Typical M1FC FSDPS Equipment Area Floor Plan

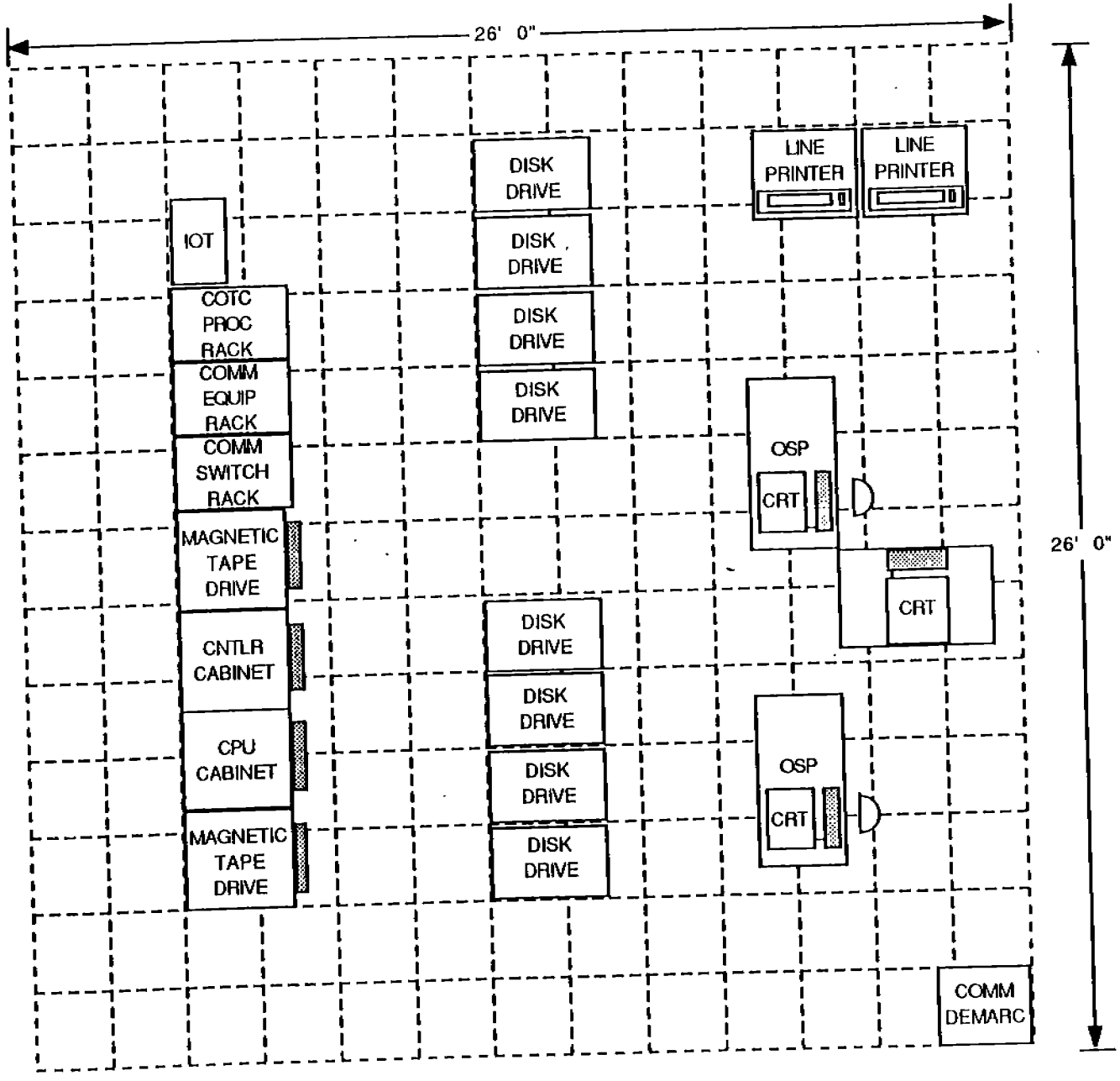

Figure 7-3. Typical M1FC AWP Equipment Area Floor Plan

Table 7-1. Equipment Parameters

NOMENCLATURE	WEIGHT LBS.	HEAT BTU/HR	PWR/REQ'D KVA	POWER PHASE
CPU CABINET (4 PROCESSORS)	437	12,500	4.31	3
CONTROLLER CABINET	365	3,978	1.38	1
MAGNETIC TAPE DRIVE	399	1,365	0.50	1
COMMUNICATIONS EQUIPMENT AND PROCESSOR RACKS	1,219	13,054	4.52	1
LINE PRINTER	185	2,187	0.94	1
DISK DRIVE (FSDPS)	465	5,800	2.00	3
INPUT/OUTPUT TERMINAL	22	1,024	0.35	1
OPERATIONS AND SERVICE PROCESSOR	180	222	0.08	1
COTC/LOCAL AFSS TERMINALS (PAIR)	80	550	0.38	1

Table 7-2. Siting Limitations

NOMENCLATURE	DIMENSIONS (INCHES)			CLEARANCE (INCHES)				MAXIMUM SIGNAL CABLE LENGTH	POWER CABLE (FEET)	NORMAL CABLE EGRESS POINT
	H	W	D	FRONT	LEFT	RIGHT	REAR			
CPU CABINET	71.5	30.25	34.5	29	30	0	29	NOT APPLICABLE	NOT APPLICABLE	BOTTOM
CONTROLLER CABINET	71.5	30.25	34.5	29	0	0	29	NOT APPLICABLE	NOT APPLICABLE	BOTTOM
MAGNETIC TAPE DRIVE	71.5	30.25	34.5	29	0	0	29	NOT APPLICABLE	NOT APPLICABLE	BOTTOM
COMMUNICATIONS EQUIPMENT RACK	70	22.5	38	21	0	0	21	NOT APPLICABLE	NOT APPLICABLE	BOTTOM OR BACK
COMMUNICATIONS SWITCHING RACK	70	22.5	38	21	0	0	21	NOT APPLICABLE	NOT APPLICABLE	BOTTOM OR BACK
COTC PROCESSOR RACK	70	22.5	38	21	0	0	21	NOT APPLICABLE	NOT APPLICABLE	BOTTOM OR BACK
LINE PRINTER	41	29.75	24.5	0	0	0	36	50 FEET FROM CONTROLLER-RS 232C	9	BOTTOM OR BACK
DISK DRIVE	36	21.75	34.3	36	0	0	36	25 FEET FROM CONTROLLER	8	BOTTOM
INPUT/OUTPUT TERMINAL	35.5	22.5	16.5	0	0	0	12	50 FEET FROM CONTROLLER	6	BACK
OPERATIONS AND SERVICE PROCESSOR	28.9	53.0	27.0	48	0	0	24	25 FEET FROM CONTROLLER	15	
COTC/LOCAL AFSS TERMINALS (PAIR) (DIMENSIONS SHOWN ARE FOR GFE TABLE)	42.5	60	30	0	0	0	0	UP TO 1500 FEET (CURRENT LOOP)	DISPLAY 9 KEYBOARD 6	BOTTOM OR BACK
ALPHANUMERIC DISPLAY	12.5	14.75	15	0	0	0	0	1500 FEET FROM DISPLAY ELECTRONICS CABINET	9	BACK
ALPHANUMERIC KEYBOARD	3.5	16.25	10	0	0	0	0	1500 FEET FROM DISPLAY ELECTRONICS CABINET	6	BACK

7.2.4 Cable Marking.- All signal cables provided with the FSDPS/AWP which enter or leave the equipment racks are marked clearly within 10 centimeters of both ends and along the cable at intervals not exceeding 5 meters.

7.2.5 Electrical Power.- The FSDPS/AWP requires a minimum service capacity of 45 KVA, 125 amperes per leg to ensure satisfactory operation. This estimate of service capacity is based on OEM handbooks and preliminary system design data. The estimate also assumes the strict use of system start-up procedures which require sequential equipment turn-on to prevent excessive in-rush of current.

All power cables will be installed in accordance with the National Electrical Code, and will be routed under the raised floor. All branch circuits except one will originate at the required UPS power panel. The single exception is a 20 ampere, single pole circuit which will originate at the required GFE power panel providing the utility power supply.

7.2.6 Grounding.- A #6 green wire will be routed from the GFE power panel CMM to the ground stud in the AC junction box located in the back of the communications switching rack in the FSDPS or communications equipment rack at the AWP. All other equipment circuits in the FSDPS/AWP will have a green wire the same size and routed with its associated branch circuit wires from the equipment's power source to the equipment. See figure 7-4.

Coaxial cables or shielded twisted pair cables will conduct the signals between the FSDPS/AWP equipment racks and the peripheral devices or the GFE telephone rack. The outer shields of these cables are grounded within the equipment racks.

7.2.7 Installation Drawings.- Wiring diagrams for the individual equipment racks and schematic diagrams of individual cables are included in the M1FC FSAS Equipment Instruction Book, TI 6490.37.

7.2.8 Installation Procedures.- The following installation procedures are for a typical FSDPS/AWP which describes a typical installation. Refer to Installation Drawings before proceeding.

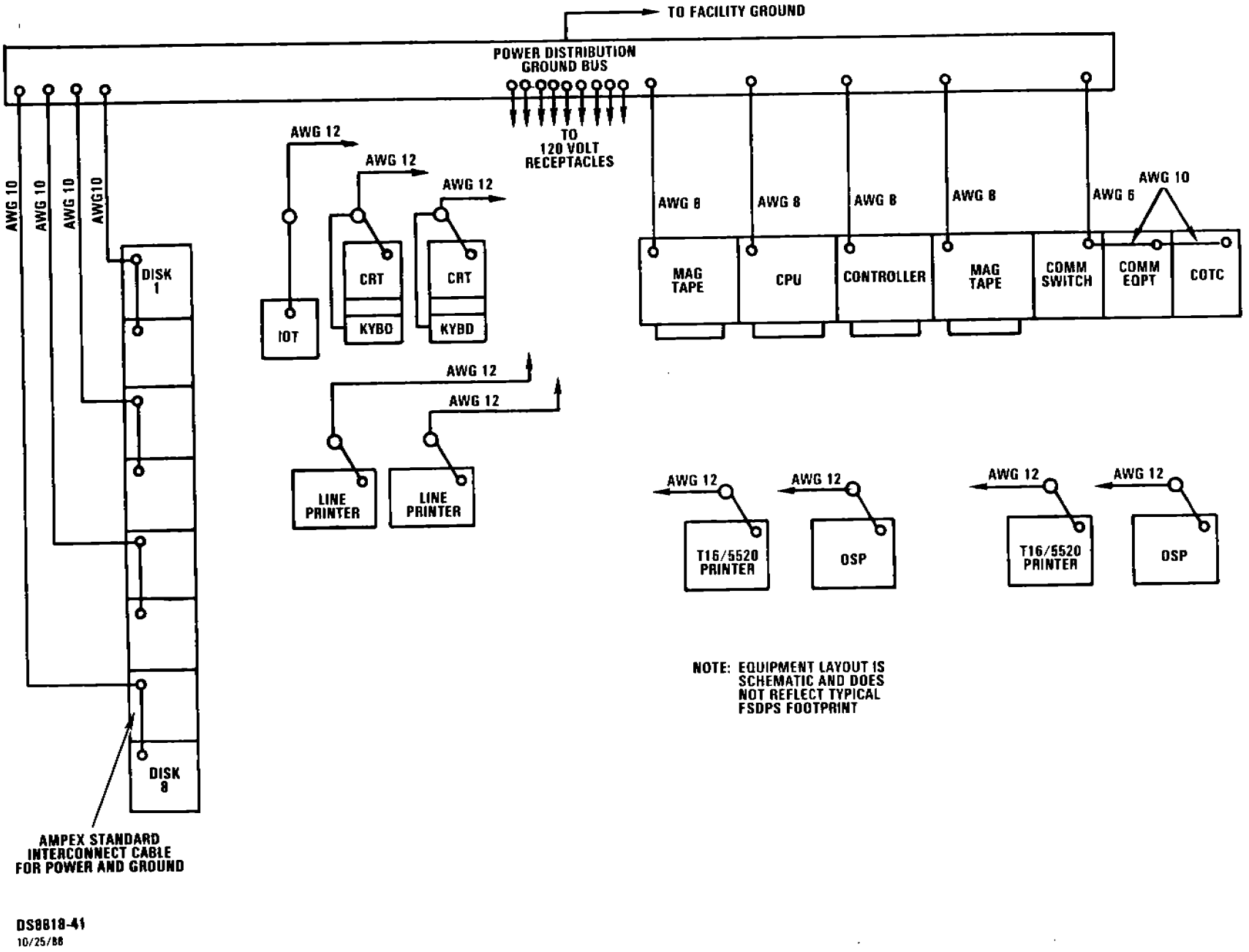

Figure 7-4. Typical FSDPS Grounding Scheme (Sheet 1 of 2)

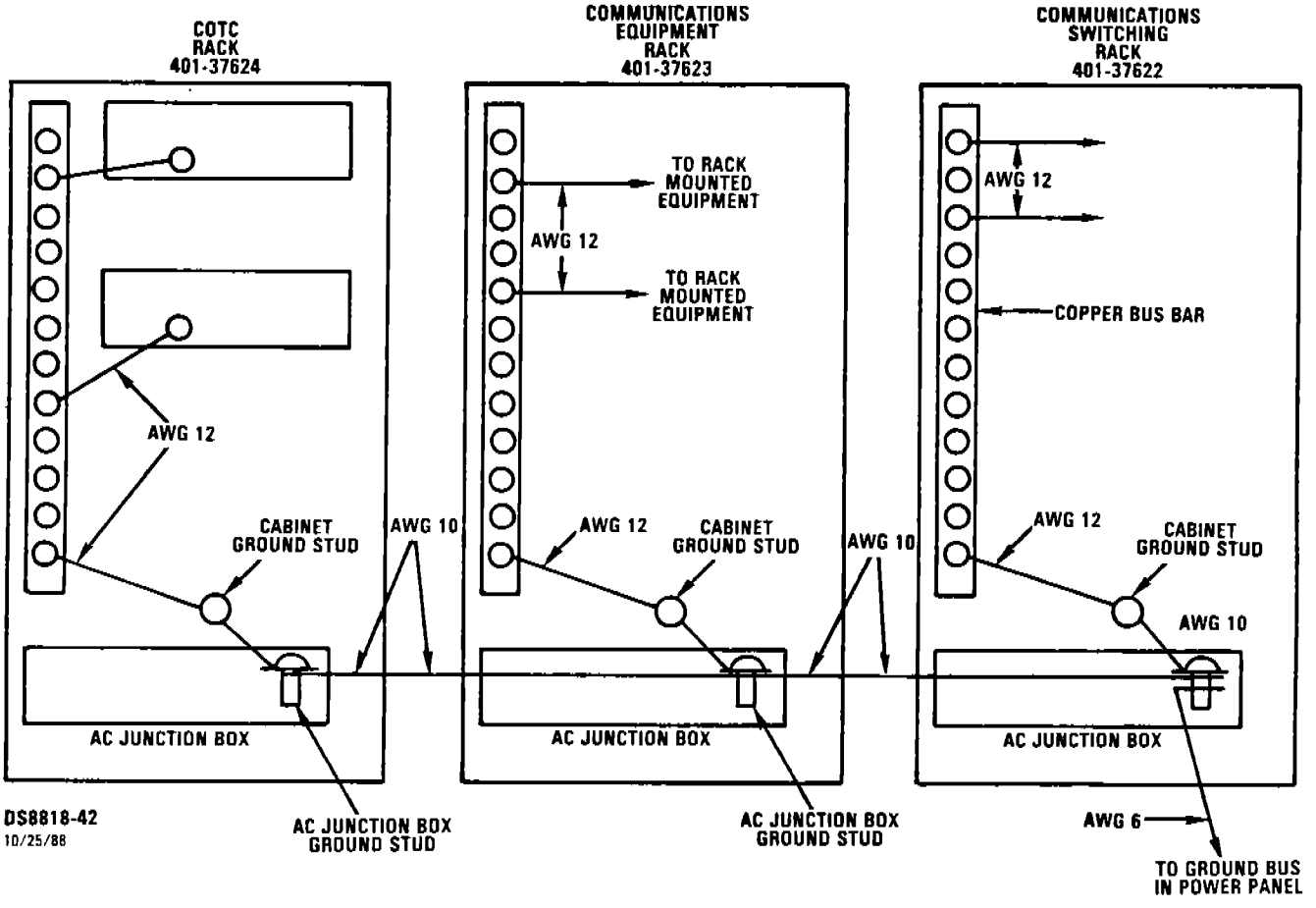

Figure 7-4. Typical FSDPS Grounding Scheme (Sheet 2 of 2)

NOTE

Any cable which is to be removed from equipment must first be checked to ensure that it is properly identified and tagged. When a cable is to be reconnected to equipment, it must be connected to the same connector from which it was removed.

7.2.8.1 Tandem Equipment Installation

a. Verify site preparation. This includes verifying the following:

(1) power distribution panels are installed, UPS and utility;

(2) floor tiles are cut for each equipment unit;

(3) Telephone demarcation rack installed; and

(4) CTS antennas installed.

b. Position precut floor tiles where equipment cabinets will be placed.

c. Position equipment cabinets in desired location according to floor plan layout.

WARNING

Danger of High Voltage. Make sure all breakers, power supplies, and controllers are turned off before performing the following steps.

d. Install AC power wiring to magnetic tape cabinet 1.

e. Bolt CPU cabinet 2 to magnetic tape cabinet 1.

f. Install AC power wiring to CPU cabinet 2.

g. Bolt controller cabinet 3 to CPU cabinet 2.

h. Install AC power wiring to controller cabinet 3.

i. Bolt magnetic tape cabinet 4 to controller cabinet 3.

j. Install AC power wiring to magnetic tape cabinet 4.

k. Install AC power wiring to OSPs.

l. Run self-tests on OSPs, including printers.

m. Install batteries in chargers.

n. Install power supplies and chargers in magnetic tape cabinet 1.

o. Connect I/O channel between cabinets.

p. Turn-on CPU cabinet AC breakers.

q. Turn-on CPU 0 power supply and measure voltages.

r. Turn-on CPU 1 Power Supply and measure voltages.

s. Turn-on CPU 2 Power Supply and measure voltages.

t. Turn-on CPU 3 power supply and measure voltages.

u. Connect cable from OSP to PMI.

v. Run general test diagnostic in CPU 0.

w. Run general test diagnostic in CPU 1.

x. Run general test diagnostic in CPU 2.

y. Run general test diagnostic in CPU 3.

z. Turn-on I/O power supply 1 and measure voltage.

aa. Turn-on I/O power supply 2 and measure voltage.

ab. Turn-on I/O power supply 3 and measure voltage.

ac. Turn-on I/O power supply 4 and measure voltage.

ad. Turn-on I/O power supply 5 and measure voltage.

ae. Remove floor tiles along path from Ampex disk drives to Tandem cabinets.

af. Remove floor tiles at rear of disk drives.

ag. Install disk drive data cables.

ah. Replace floor tiles except behind disk drives.

ai. Install disk controller cables.

aj. Install power cables to disk drives.

ak. Apply power to disk pair 1.

al. Attach disk exerciser and check head alignment on disk pair 1.

am. Install system disk on disk pair 1.

an. Power-up controller for disk pair 1.

ao. Apply power to disk pair 2.

ap. Attach disk exerciser and check head alignment on disk pair 2.

aq. Install system disk on disk pair 2.

ar. Power-up controller for disk pair 2.

as. Load operating system in CPU 0 using OSP.

at. Load operating system in CPU 1 using OSP.

au. Load operating system in CPU 2 using OSP.

av. Load operating system in CPU 3 using OSP.

aw. Run SYSEX in all CPUs.

ax. Run DISCEX on Disk pair 1 in CPU 0.

ay. Run DISCEX on disk pair 2 in CPU 1.

az. Apply power to disk pair 3.

ba. Attach disk exerciser and check head alignment on disk pair 3.

bb. Install system disk on disk pair 3.

bc. Power-up controller for disk pair 3.

bd. Run DISCEX on disk pair 3 in CPU 2.

be. Connect tape controller cables.

bf. Power magnetic tape 1 and mount scratch tape.

bg. Power-up tape controller.

bh. Run TAPEX on magnetic tape drive 1 in CPU 1.

bi. Power magnetic tape drive 2 and mount scratch tape.

bj. Power-up tape controller.

bk. Run TAPEX on magnetic tape drive 2 in CPU 2.

bl. Connect ASYNC controller cables.

bm. Run ASYNCCI in CPU 2.

bn. Connect display terminal on OSP 2 to each port and check.

bo. Connect SYNC controller cables.

bp. Connect communication cables to E-Systems racks.

bq. Connect loopback cable to modems under test.

br. Run ENVOYTST in CPU 0 for SYNC lines under test.

bs. Power-up Printronix printers.

bt. Connect cables to printers.

bu. Run PRINTST in CPU 2.

7.2.8.2 E-Systems Equipment Installation - FSDPS

WARNING

Danger of high voltage. Make sure all breakers, power supplies, and ON/OFF switches are off before performing the following steps.

a. Place communications switching rack next to magnetic tape drive cabinet 2.

b. Connect AC power to communications switching rack AC J-Box.

c. Bolt communications equipment rack to communications switching rack.

d. Connect AC power-feed to communications equipment rack.

e. Bolt position processor rack to communications equipment rack.

f. Connect AC power-feed to position processor rack.

g. Remove RL01/RL02 disk drive packing screws and head restraint.

h. Connect disk cable to communications processor.

i. Connect internal IOT cables

j. Connect internal modem cables

k. Connect COTC video and keyboard cables.

l. Power-up AC J-Box and measure voltages.

m. Plug disk drive into AC J-Box.

n. Power-up disk drive.

o. Install system disk.

p. Turn-on communications processor and verify CPU load.

q. Run communications processor diagnostics.

r. Remove printer cables from Tandem.

s. Connect printer cables to patch panel.

t. Connect all cables from patch panels to Tandem.

u. At Tandem, run PRINTST to verify patch panel connection.

v. Remove OSP cable from Tandem.

w. Connect OSP cable to patch panel.

x. At OSP, verify patch panel connection.

y. Connect TELCO cables from modem to patch panel.

z. Install loopback cable between modem 1 & 2.

aa. At Tandem, run ENVOYTST on SYNC controller 1.

ab. Connect OSP modem cable to patch panel.

TI 6490.36

7.2.8.3 E-Systems Equipment Installation - AWP

WARNING

Danger of high voltage. Make sure all breakers, power supplies, and ON/OFF switches are off before performing the following steps.

a. Place Communications Equipment Rack next to magnetic tape cabinet 2.

b. Connect AC Power to communications equipment rack AC J-Box.

c. Bolt communications processor rack to communications equipment rack.

d. Connect AC power-feed to communications processor rack.

e. Bolt position processor rack to communications processor rack.

f. Connect AC Power-feed to position processor rack.

g. Remove RL01/RL02 Disk Drive packing screws and head restraint.

h. Connect disk cable to communications processor.

i. Connect internal IOT cables

j. Connect internal modem cables

k. Connect COTC video and keyboard cables.

l. Power-up AC J-Box and measure voltages.

m. Plug disk drive into AC J-Box.

n. Power-up disk drive.

o. Install system disk.

p. Turn-on communications processor and verify CPU load.

q. Run communications processor diagnostics.

r. Remove printer cables from Tandem.

s. Connect printer cables to patch panel.

t. Connect all cables from patch panels to Tandem.

u. At Tandem, run PRINTST to verify patch panel connection.

v. Remove OSP cable from Tandem.

w. Connect OSP cable to patch panel.

x. At OSP, verify patch panel connection.

y. Connect TELCO cables from modem to patch panel.

z. Install loopback cable between modem 1 & 2.

aa. At Tandem, run ENVOYTST on SYNC controller 1.

ab. Connect OSP modem cable to patch panel.

7.3 AFSS SYSTEM.- An AFSS typical system consists of the items listed below:

Item 1 -	Communications Equipment Rack	1
Item 2 -	Communications Processor Rack	1
Item 3 -	Position Processor Rack	1 to 3
Item 4 -	Input/Output Terminal	1
Item 5 -	Display Terminals	up to 48
Item 6 -	Line Printers	2

7.3.1 AFSS Site Requirements.- Site Requirements consist of electrical and physical requirements.

The electrical requirements for the critical power require a power distribution panel located in the equipment area of the AFSS. A typical AFSS requires a 100 ampere, 120/240 volt single phase, 3-wire box with 12 breaker positions.

NOTE

These breakers conform to FED-SPEC-W-C-375

The required branch circuit breakers in this panel are three 30 ampere and one 20 ampere breakers. The three 30 ampere and one 20 ampere circuits terminate in the communications equipment rack.

In the operations area, all of the alphanumeric terminals use existing power circuits whose outlets are within six feet of the terminals. All AFSS equipment located in this area and in the

Training Room use NEMA type 5-15R or equivalent 120 volt, three-prong outlets. At each position, one outlet is for the monitor and one is for the keyboard. The total load on the two outlets is 1.6 amperes.

The two line printers each require one 20 ampere circuit because of the surge current. Each printer operates on a steady state current of 7.8 amperes.

Refer to table 7-3 for the individual equipment loads in the equipment area and in the operations area.

The AFSS facility contains one #6 green wire that runs from the GFE power panel to the ground stud in the power distribution box (AC J- Box) located in the back of the communications equipment rack.

The physical requirements for an AFSS consists of a floor area of at least 16 feet by 11 feet for placement of the equipment racks and the IOT terminal. This area is designated as the Equipment Room. A typical floor plan for the Equipment Room is shown in figure 7-5. The Equipment Room must be maintained at a relative humidity of 20 to 80 percent and an ambient temperature of +15 to +32 degrees celsius. These requirements are the same for all other AFSS equipment located at the facility.

The physical characteristics of the equipment are given in table 7-3. Table 7-4 lists the dimensions and clearance requirements of the equipment along with maximum signal cable lengths.

7.3.2 Site Survey.- The installation areas selected must meet the above requirements for the Equipment Room and all other areas where the display terminals and the two line printers are to be located.

Examine existing distribution routes for signal, power, and ground cables. Examine the amount of space available in cable ladders, ducts, troughs, and conduits. Note existing sources for power and grounds. Locate the demarcation point for telephone circuits in the designated Equipment Room. Identify locations of existing convenience outlets. Assess the available environmental control system capabilities.

Establish a floor plan layout (refer to figure 7-6). Verify facility requirements. Identify desired equipment locations. Determine routes for signal, control, power, and grounding cables. Refer to table 7-3 and table 7-4 for equipment parameters, limitations, and signal cable length restrictions.

7.3.3 Signal Cable Routing.- All signal cables provided for an AFSS may be run over head or under raised floors. The cables will enter and exit from either the top of the equipment racks or from the bottom depending on the site requirements.

Table 7-3. AFSS Equipment Parameters

NOMENCLATURE	WEIGHT LBS	HEAT BTU/HR	PWR/REQ'D KVA	POWER PHASE
COMMUNICATIONS EQUIPMENT AND PROCESSOR RACKS	1,219	13,054	4.52	1
LINE PRINTER	185	2,187	0.94	1
INPUT/OUTPUT TERMINAL	22	1,024	0.35	1
ALPHANUMERIC DISPLAY AND KEYBOARD	40	275	0.19	1

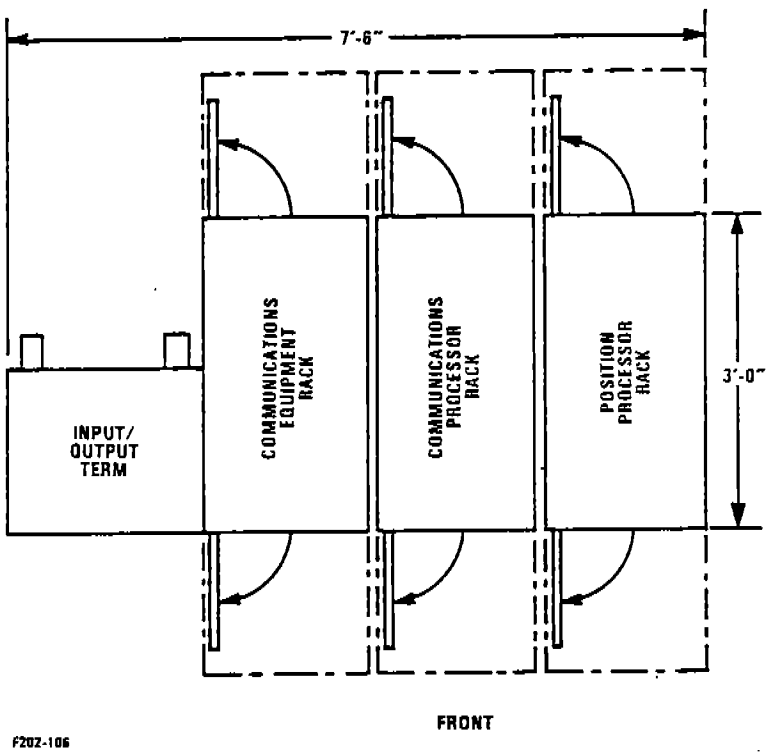

Figure 7-5. Typical M1FC AFSS Equipment Area Floor Plan

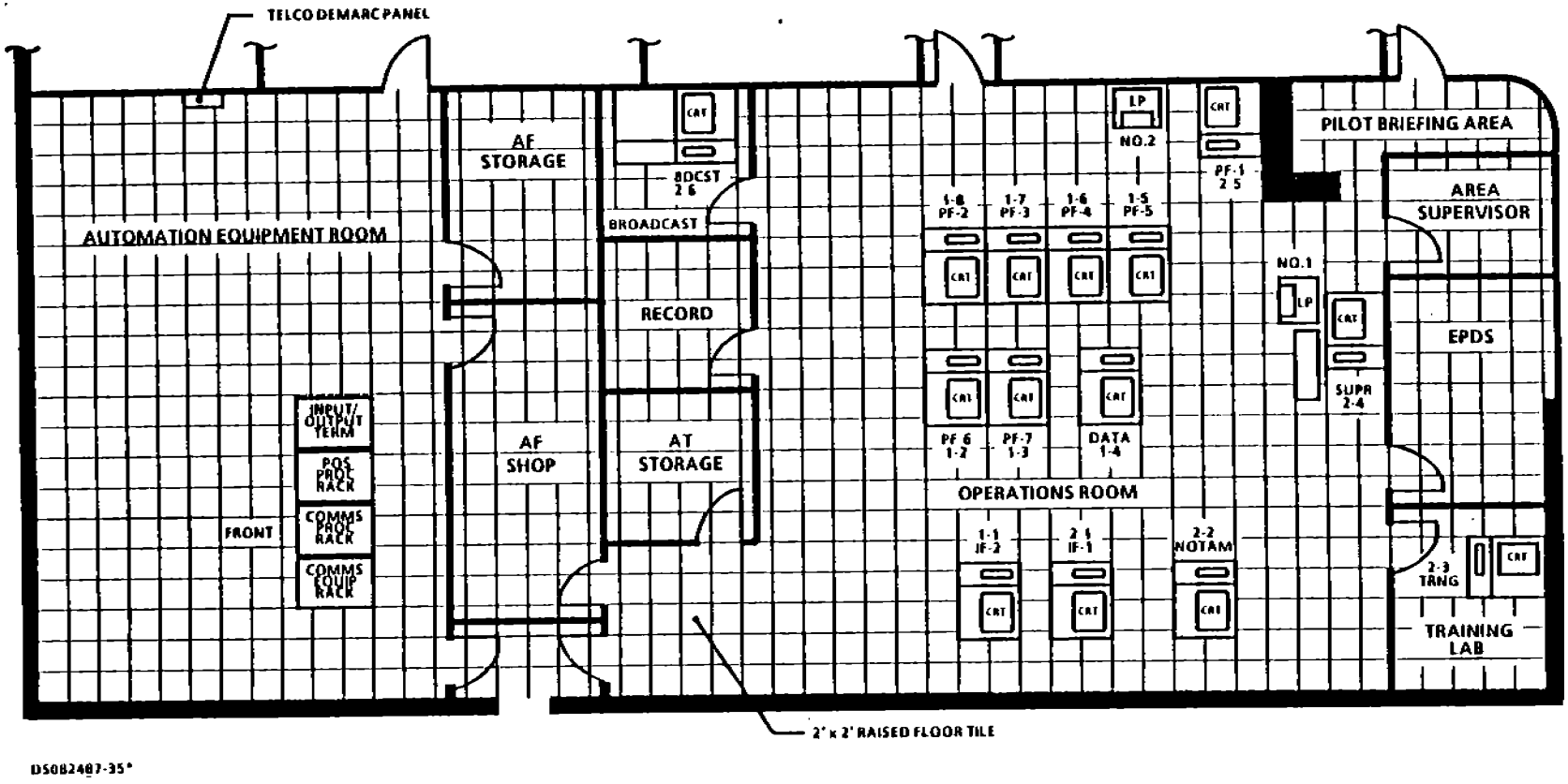

Figure 7-6. Typical M1FC AFSS Equipment Layout Drawing

Table 7-4. AFSS Equipment Siting Limitations

NOMENCLATURE	DIMENSIONS (INCHES)			CLEARANCE (INCHES)				MAXIMUM SIGNAL CABLE LENGTH	POWER CABLE (FEET)	NORMAL CABLE EGRESS POINT
	H	W	D	FRONT	LEFT	RIGHT	REAR			
COMMUNICATIONS EQUIPMENT RACK	70	22.5	38	21	0	0	21	NOT APPLICABLE	NOT APPLICABLE	BOTTOM OR BACK
COMMUNICATIONS PROCESSOR RACK	70	22.5	38	21	0	0	21	NOT APPLICABLE	NOT APPLICABLE	BOTTOM OR BACK
POSITION PROCESSOR RACK	70	22.5	38	21	0	0	21	NOT APPLICABLE	NOT APPLICABLE	BOTTOM OR BACK
LINE PRINTER	41	29.75	24.5	0	0	0	36	50 FEET FROM CONTROLLER — RS232C	9	BOTTOM OR BACK
INPUT/OUTPUT TERMINAL	35.5	22.5	16.5	0	0	0	12	50 FEET FROM CONTROLLER	6	BACK
ALPHANUMERIC DISPLAY	12.5	14.75	15	0	0	0	0	1500 FEET FROM DISPLAY ELECTRONICS CABINET	9	BACK
ALPHANUMERIC KEYBOARD	3.5	16.25	10	0	0	0	0	1500 FEET FROM DISPLAY ELECTRONICS CABINET	6	BACK

F202-105

7.3.4 Cable Marking.- All signal cables provided with an AFSS which enter or leave the equipment racks are marked clearly within 10 centimeters of both ends and along the cable at intervals not exceeding 5 meters.

7.3.5 Electrical Power.- Refer to table 7-3 for power consumption of the AFSS equipment. Total power consumption for an AFSS site will depend on the number of display terminal positions. Power for each of the two line printers require a 20 ampere circuit to prevent overload surge. The duplex outlet for each of the display terminals have to be placed at each position within six cable feet of the keyboard and within nine cable feet of the monitor. Since each terminal's power consumption is less than 2 amperes, more than one terminal can be placed on a circuit. All receptacles are NEMA5-15R type.

7.3.6 Grounding.- A #6 green wire will be routed from the GFE power panel located in the Equipment Room to the ground stud in the AC Junction Box located in the back of the communications equipment rack. All other equipment circuits in an AFSS will have a green wire the same size as its associated wires accompanying the circuit from the equipment's power source to the equipment.

All coaxial cables or shielded twisted pair cables will conduct the signals between the AFSS equipment racks and the peripheral devices or the GFE telephone rack. The outer shields of these cables are grounded within the equipment racks.

7.3.7 Installation Drawings.- Cabling diagrams for individual equipment racks and cable schematics are included in the M1FC FSAS Equipment Instruction Book, TI 6490.37.

7.3.8 AFSS Installation Procedures.- The following installation procedures are for a typical AFSS. Refer to Installation Drawing before proceeding.

NOTE

> Any cable which is to be removed from equipment must first be check to ensure that it is properly identified and tagged. When a cable is to be reconnected to equipment, it must be connected to the same connector from which it was removed.

a. Verify site preparation. This includes verifying the following:

   (1) Power distribution panel installed in Equipment Room.

(2) Floor tiles cut for each equipment unit (if required) and/or required duct work installed.

(3) Telephone demarcation rack installed.

b. Position precut floor tiles where equipment cabinets will be placed if required.

c. Position equipment cabinets in desired location according to floor plan layout.

WARNING

Danger of High Voltage. Make sure all breakers, power supplies, and ON/OFF switches are turned off before performing the following steps.

d. Connect AC power to communications equipment rack AC J-Box.

e. Bolt communications processor rack to communications equipment rack.

f. Connect AC power feed to communications processor rack AC J-Box.

g. Bolt position processor rack to communications processor rack.

h. Connect AC power feed to position processor rack AC J-Box.

i. Remove RL01/RL02 Disk Drive packing screws and head restraint.

j. Connect disk cable to communications processor.

k. Connect internal IOT cables.

l. Connect internal modem cables, patch panel cables, and telephone line cables.

m. Connect local AFSS/COTC display terminal and keyboard cables.

n. Switch to ON the AC power circuit breakers located on the GFE power distribution panel for the equipment racks.

o. Power-up AC J-Boxes in the back of each equipment rack and measure voltages.

p. Power-up the power supplies in each of the equipment racks and measure the DC voltages.

q. Power-down the power supplies in each of the equipment racks.

r. Power-down AC J-Boxes in each of the equipment racks.

s. Install printed circuit boards.

t. Repeat steps o. and p.

u. Plug RL01/RL02 Disk Drives into AC J-Box.

v. Power-up disk drives.

w. Install system disk.

x. Power-up communications processor and verify CPU load.

y. Run communications processor diagnostics.

z. Power-up position processors and verify CPU loads.

aa. Place display terminals and keyboards in desired locations.

ab. Run and connect cables between display terminals according to assigned daisy chain configurations.

ac. Connect cables from display terminals to position processor.

ad. Run and connect cables between keyboards and position processor.

ae. Plug display terminals and keyboard power supplies into 120 VAC convenience outlets.

af. Place line printers in desired locations.

ag. Run and connect printer cables to back of digital patch panel.

ah. Plug line printers into the installed 20 ampere 120 VAC circuits.

ai. Power-up all display terminals and line printers.

7.4 SYSTEM EXPANSION OR REDUCTION CAPABILITIES.

- The FSDPSs and or the AFSSs may be expanded or reduced. FSDPSs may be expanded by adding additional modem cards and a Manual Call Unit to support a maximum of eight satellite AFSSs or the system may be reduced by removing those items to support less than the maximum number of AFSSs. Refer to table 7-5.

At an AFSS, the number of positions maybe expanded to a maximum of 48 positions or the number maybe reduced to the minimum. Table 7-6 lists the required equipment to support the number of positions desired.

For example, to expand an AFSS with 16 positions to one with up to 24 positions, an additional position processor rack would be required. From table 7-6, the required rack would be a -02 position processor rack.

If the desired increase of positions were 32, then from table 7-6, the additional position processor rack would be a -04 rack.

Table 7-5. M1FC FSDPS Equipment Expansion Requirements

M1FC FSDPS Communication Equipment Rack
401-37263-01 thru -05

RACK DASH NUMBER	NO. OF AFSSs	RM-9600 MODEM	RM-9600 FP MODEM	RM-208A MODEM	RM-A/0 MODEM	RM-800 MCU
-01	1	9	5	1	1	1
-02	2-3	13-17	5	2-3	2-3	1
-03	4-5	21-25	5	4	4	1
-04	6-7	29-33	5	4	4	1
-05	8	37	5	4	4	1

Table 7-6. M1FC AFSS Equipment Expansion Requirement
AFSS Position Processor Rack
401-37616-01, -02, -03, -04

	RACK DASH NUMBER				EQUIPMENT
	-01*	-02	-03	-04	
No. of Positions	1-4	1-8	1-12	1-16	
Quantity	2	2	2	2	316-3012-001 Prog. PROM OTF U60
	-	2	2	2	316-3013-001 Prog. PROM OTF U60
	4	8	8	8	401-37994-01 OTF/CACHE Assy Adaptor Cable
	2	4	4	4	401-33676-01 A/N OTF Processor
	1	2	3	4	401-33692-01 QUAD CACHE
	4	6	6	6	8S 8 Channel Serial I/O
	4	8	8	8	401-37995-01 OTF/CACHE Bus Cable
	1	2	2	2	316-3040-001 Prog. PROM CACHE U5
	-	-	1	2	316-3041-001 Prog. PROM CACHE U5
	1	2	2	2	401-37929-01 A/N OTF/CACHE Buss Cable
	8	8	8	8	401-37925-01 Graphics Video Jumper
	28	22	22	22	401-37909-10 Buss Grant Board
	2	2	2	2	401-37909-09 Buss Grant Board
	2	2	2	2	401-37747-02 Prom Set, MRV11-C
	2	2	2	2	MRV11-C Prom (32KW) MEM
	2	2	2	2	DMA-QB DMA CONTR BD
	2	2	2	2	KDF11-AA LSI 11/23 Microcomp
	2	2	2	2	KPV11-B System Module
	2	2	2	2	MSV11-LF RAM (64KW) MEM

* NOTE: The -01 Position Processor Rack cannot be used with any other Position Processor rack.

SECTION 8

COMPUTER SOFTWARE

8.1 GENERAL. - The M1FC FSAS computer software includes: operating system software, diagnostic software, and application software. Detailed descriptions of the software are contained in the documentation listed in table 8-1.

Table 8-1. Related Software Manuals

FSAS Software	M1FC FSAS	E-Systems
Documentation:		
Computer Program Functional Specification (CPFS) for AWP/FSDPS Operational Software		406-04100
Computer Program Functional Specification (CPFS) for AWP/FSDPS Support Software		406-04101
Computer Program Functional Specification (CPFS) for AWP/FSDPS Maintenance Software		406-04102
Computer Program Functional Specification (CPFS) for Position Equipment Software		406-04103
Users Manual for the AWP		416-32146
Users Manual for the FSDPS/AFSS		416-32147
Operators Manual for the AWP		416-32149
Operators Manual for the FSDPS/AFSS		416-32150
TANDEM System	Non Stop II	Tandem
Documentation:		
GUARDIAN OPERATING SYSTEM LIBRARY		
Non Stop II System Management Manual		82069
Non Stop II System Operations Manual		82075
Guardian Operating System Messages Manual		82076
Non Stop II System Description Manual		82077
Introduction to Guardian Computer System		82003
GUARDIAN Operating System Command Language and Utilities Manual		82073
SPOOLER/PERUSE Users Guide		82093
Spooler System Management Guide		82094
GUARDIAN Operating System Programming Manual Volume 1		82096
GUARDIAN Operating System Programming Manual Volume 2		82096

Table 8-1. Related Software Manuals (Continued)

PROGRAM DEVELOPMENT TOOLS AND UTILITIES LIBRARY	
DEBUG Reference Manual	82098
TGAL Reference Manual	82026
EDIT Manual	82079
UPDATE Manual	82080
SORT/MERGE Users Guide	82091
DATA MANAGEMENT LIBRARY	
Data Definition Language Programming Manual	82034
ENFORM Reference Manual	82040
PATHWAY Programming Manual	82059
PATHWAY Operating Manual	82060
PATHWAY Programming Aids	82072
ENABLE Users Guide	82061
ENSCRIBE Programming Manual	82083
Introduction to ENFORM	82313
LANGUAGES LIBRARY	
COBOL Programming Manual	82007
FORTRAN 77 Reference Manual	82030
Transaction Application Language Reference Manual	82081
PERFORMANCE ANALYSIS AND TUNING LIBRARY	
XRAY Users Manual	82078
DATA COMMUNICATIONS LIBRARY	
EXCHANGE Reference Manual	82068
ENVOY Byte-Oriented Protocols Reference Manual	82082
AXCESS Data Communications Programming Manual, Volumes 1, 2 & 3	82084
EXPAND Users Manual	82085
ENVOYACP Bit-Oriented Protocols Reference Manual	82088
Introduction to Tandem Data Communications	82311

Table 8-1. Related Software Manuals (Continued)

SUPPLEMENTAL PUBLICATIONS LIBRARY

Master Index for the Tandem Nonstop II System	82086
Software Pocket Reference Manual	82031
Manuals Information Bulletin	82054
Tandem Technical Communications Library	82062
GUARDIAN Operating System Pocket Guide	82301
Instruction Sets Pocket Guide	82307

For additional documentation refer to section 1, table 1-1.

APPENDIX A

MODEL 1 FULL CAPACITY FLIGHT SERVICE AUTOMATION SYSTEM EQUIPMENT CONFIGURATION SPECIFICATIONS

APPENDIX A

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DMA-Q Parallel DMA	A-27
8 Channel Serial I/O TMI 8S	A-35
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I/O Character Printer LA34-AA	A-107
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Letterwriter DEC LA100-CA	A-113

CONFIGURATION SPECIFICATION

LSI 11/23 CPU

KDF11-AA

DEC M8186

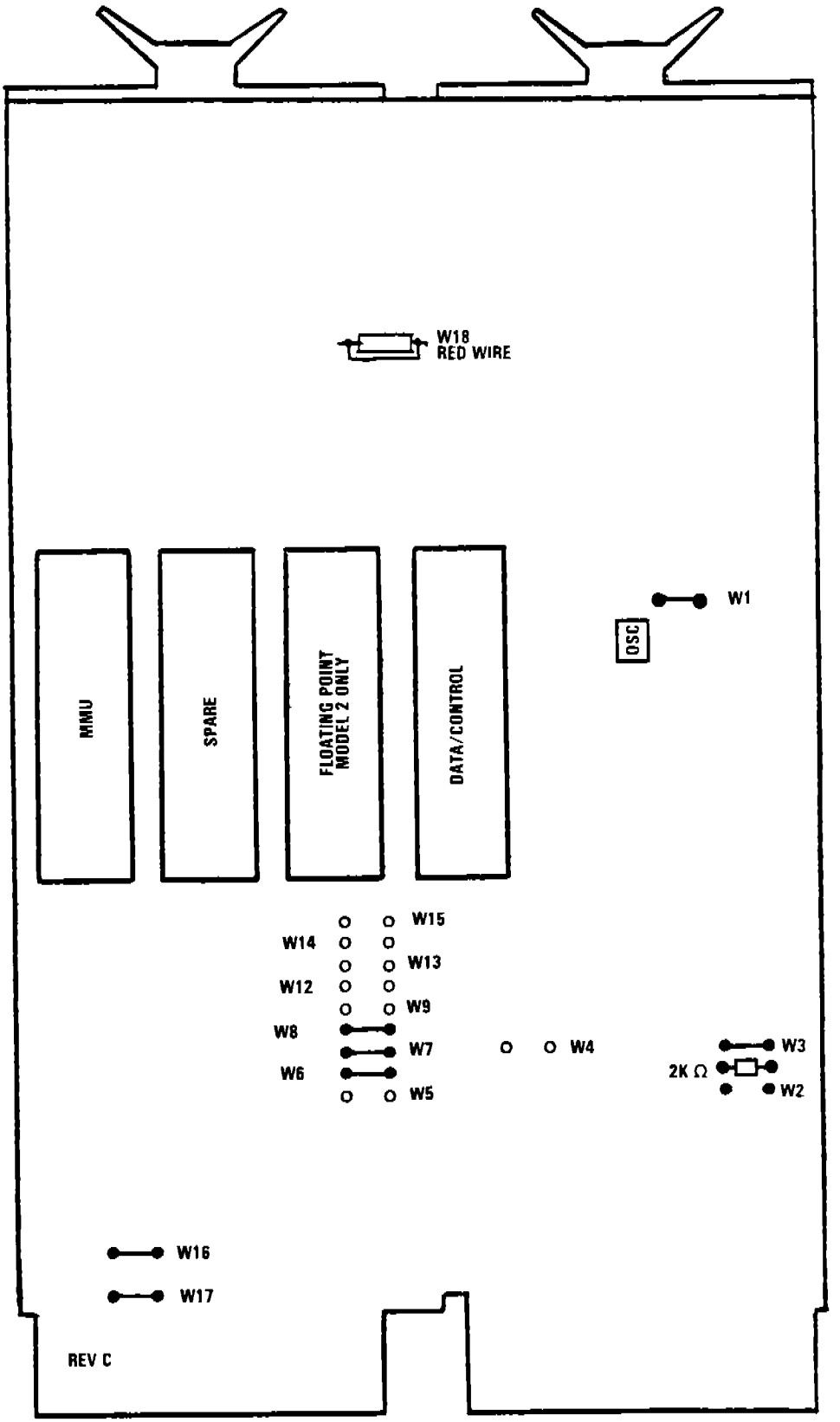
Jumper Configuration

W1	Installed	Factory - Do Not Change
W2	Removed	Factory
W3	Installed	Factory - Do Not Change
W4	Removed	Line Time Clock Enabled
W5	Removed	Power-Up Mode 2
W6	Installed	PC at Bootstrap
*W7	Installed	Halt Trap to 10_8
W8	Installed	PC at 773000
W9	Removed	Alternate Bootstrap Option - Not Used
W10	"	" " " " "
W11	"	" " " " "
W12	"	" " " " "
W13	"	" " " " "
W14	"	" " " " "
W15	"	" " " " "
W16	Installed	Factory - Do Not Change
W17	Installed	Factory - Do Not Change
W18	Installed	Disable Wake-Up Circuit

*NOTE: Install for Operation - Remove for ODT

Power-Up Mode Selection

Mode	Jumpers W5	Jumpers W6	Description
0	Removed	Removed	PC=24, PS=26 (Factory Configured)
1	Installed	Removed	ODT Microcode
2	Removed	Installed	PC at Bootstrap
3	Installed	Installed	Microcode Bootstrap Not Implemented


W18
RED WIRE
MMU
SPARE
FLOATING POINT
MODEL 2 ONLY
DATA/CONTROL
W1
OSC
W15
W14
W13
W12
W9
W8
W7
W4
W3
2K Ω
W2
W6
W5
W16
W17
REV C

F202-153

CONFIGURATION SPECIFICATION

64K WORD RAM

MSV11-LF

DEC M8059 FH

CONFIGURATION SPECIFICATION
64K WORD RAM MSV11-LF

NOTE: This circuit card assembly is factory configured.
Use this for validation only.

JUMPER CONFIGURATION

Pin Des	Installed/Removed	Function
1-2	Installed	Parity CSR Report on 16 & 17
6-7	Installed	Write wrong parity enable
10-11	Installed	Parity memory
15-16	Installed	Normal addressing
19-20	Installed	Memory Type - Parity CSR
25-26	Installed	5VDC & Power
27-28	Installed	4K I/O Page
32-33	Installed	64K Word Memory
F-H	Installed	Parity CSR
R-T	Removed	128K Addressing
A-B-C	Removed	CSR 772100

64K WORD RAM MSV11-LF
JUMPER CONFIGURATION

NOTE
CHIPS ARE POSITIONED 180° OUT OF PHASE WITH TRADITIONAL DIGITAL MEMORIES

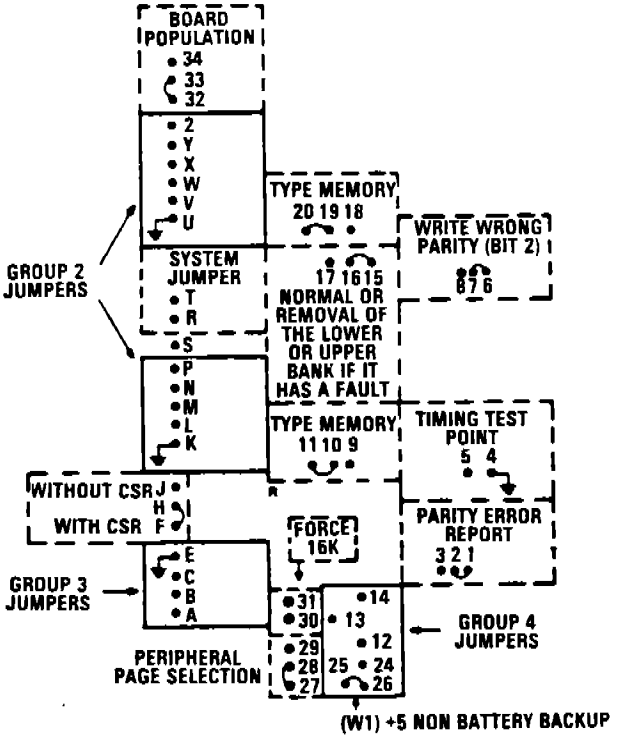
DOTTED BLOCK MEANS GROUP 1

GROUP 1 JUMPERS-GENERAL
GROUP 2, 3 JUMPERS START/CSR ADDRESS
GROUP 4 JUMPERS-POWER
- NON BATTERY BACKUP
- BATTERY BACKUP

DIGITAL DOES NOT SUPPORT BATTERY BACKUP.

MEMORY MODULES CAN NOT BE INTERLEAVED.

WIRE WRAP GUIDELINES-MAXIMUM, 2 WRAPS PER PIN.
GROUP 2 AND 3 JUMPERS MAY HAVE MAXIMUM NUMBER OF WIRE WRAPS.
- THE WRAPS MUST BE DAISY CHAINED TO IT'S OWN GROUND
- FIND OUT HOW MANY PINS MUST BE WRAPPED
- WHEN WRAPPING ALWAYS PUT THE LOWER WRAPS ON THE PINS FIRST THEN WRAP THE UPPER WRAPS



F202-152

CONFIGURATION SPECIFICATION
32K WORD PROM MRV11-C

DEC M8048

32K WORD PROM MRV11-C
WIREWRAP CONNECTIONS

Note: All addresses are in Octal.

J69-J71	Installed	Enable Low-byte MUX	

Low byte Selection

J27-J26	Installed	CSR 0	
J30-J29	"	CSR 1	
J33-J32	"	CSR 2	Window "0" page
J36-J35	"	CSR 3	number
J39-J38	"	CSR 4	

High byte Selection

J9-J8	Installed	CSR 8	
J11-J10	"	CSR 9	
J13-J12	"	CSR 10	Window "1" page
J15-J14	"	CSR 11	number
J17-J16	"	CSR 12	

Prom Window Starting Address

Model 1

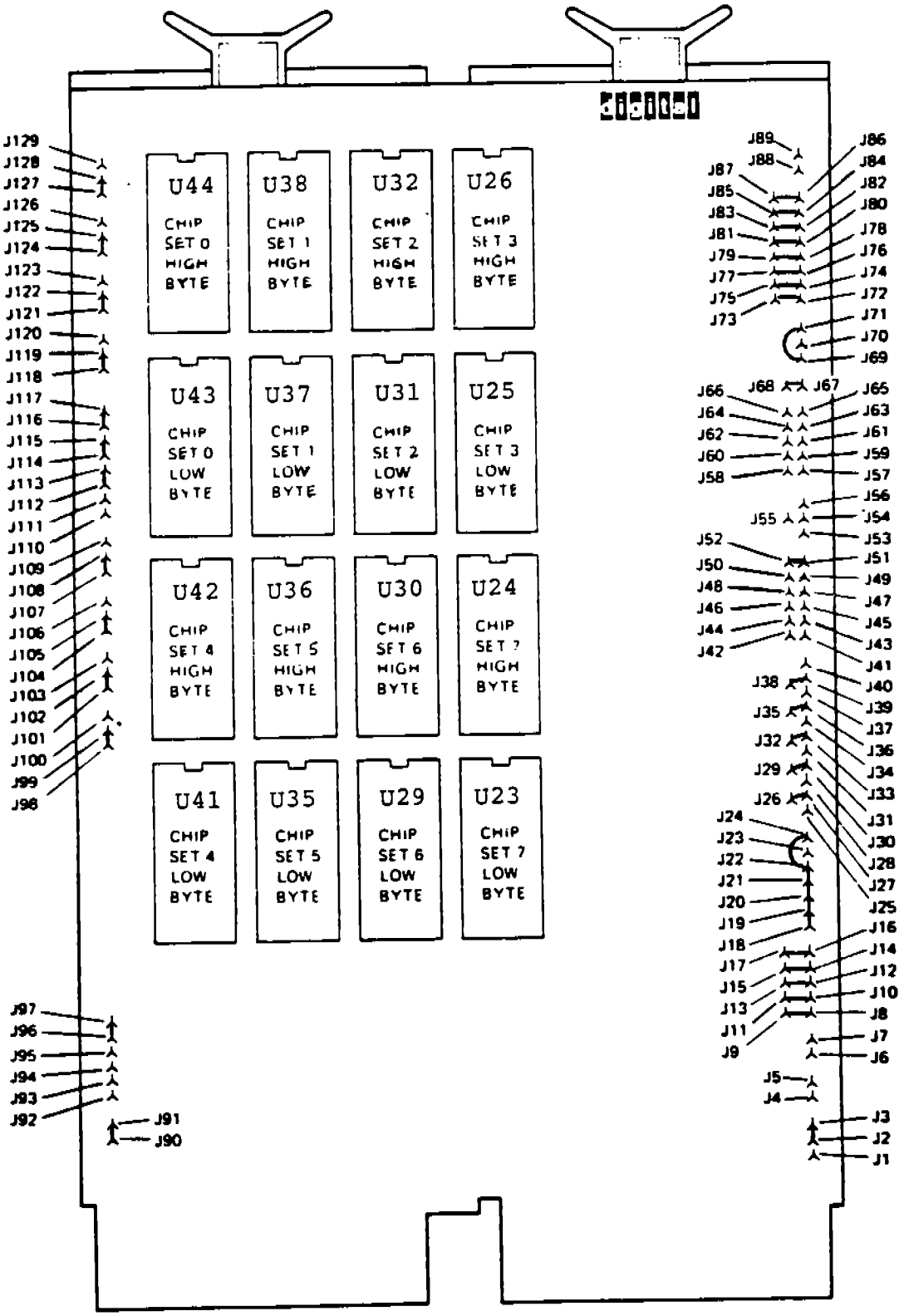
J47-J48	Installed	Bit 16	
J49-J50	"	Bit 17	Window starting
J51-J52	"	Bit 12	address 160000

Model 1 Full Capacity

J47-J48	Removed	Bit 16	Window starting
J49-J50	Removed	Bit 17	address 760000
J51-J52	Installed	Bit 12	
J86-J87	Installed	Chip Set 0	
J84-J85	"	Chip Set 1	
J82-J83	"	Chip Set 2	Chip Enable
J80-J81	"	Chip Set 3	Jumpers
J78-J79	"	Chip Set 4	
J76-J77	"	Chip Set 5	
J74-J75	"	Chip Set 6	
J72-J73	"	Chip Set 7	
J92-J93	Removed	Bit 1	
J94-J95	"	Bit 2	CSR Address *77000
J96-J97	"	Bit 3	Comm and Position and
J90-J91	"	Bit 4	COTC Processors
J92-J93	Removed	Bit 1	
J94-J95	"	Bit 2	CSR Address *77030
J96-J97	Installed	Bit 3	MADTS
J90-J91	"	Bit 4	

* Bank 7 asserted (1 for 32K words - 7 for 128K word systems)

J88-J89	Removed	Enable Bootstrap
J18-J19	Installed	Starting Address 3000 in page 31 (Fourth 512 byte's of chip set 0.)
J19-J20	"	
J20-J21	"	
J21-J22	"	
J22-J24	"	
J67-J68	Installed	Bit 15 Disable Module Enable
A12	J115-J114 and J118-J119	U43,44
	J121-J122	U37,38
	J124-J125	U31,32
	J127-J128	U25,26
	J101-J102	U41,42
	J98-J99	U35,36
	J104-J105	U29,30
	J107-J108	U23,24
A11	J113-J112	
+5 VDC	J117-J116	
	J2 - J3	200 - 450 nsec Chip Access Time



MRV11-C Wirewrap Pin Locations

32K WORD PROM MRV11-C

PAGE LOCATIONS

Chip Set	Page Range	IC Location High Byte	IC Location Low Byte
0	0-3	U44	U43
1	4-7	U38	U37
2	8-11	U32	U31
3	12-15	U26	U25
4	16-19	U42	U41
5	20-23	U36	U35
6	24-27	U30	U29
7	28-31	U24	U23

32K WORD PROM MRV11-C
PART NUMBER

COMMUNICATIONS PROCESSOR

ESY P/N	NAME	LOCATION
316-3044-X	S00C	U44
316-3045-X	S01C	U43
316-3046-X	S02C	U38
316-3047-X	S03C	U37
316-3048-X	S04C	U32
316-3049-X	S05C	U31
316-3050-X	S06C	U26
316-3051-X	S07C	U25
316-3052-X	S08C	U42
316-3053-X	S09C	U41
316-3054-X	S10C	U36
316-3055-X	S11C	U35
316-3056-X	S12C	U30
316-3057-X	S13C	U29
316-3058-X	S14C	U24
316-3059-X	S15C	U23

POSITION PROCESSOR

316-3060-X	S00P	U44
316-3061-X	S01P	U43
316-3062-X	S02P	U38
316-3063-X	S03P	U37
316-3064-X	S04P	U32
316-3065-X	S05P	U31
316-3066-X	S06P	U26
316-3067-X	S07P	U25
316-3068-X	S08P	U42
316-3069-X	S09P	U41
316-3070-X	S10P	U36
316-3071-X	S11P	U35
316-3072-X	S12P	U30
316-3073-X	S13P	U29
316-3074-X	S14P	U24
316-3075-X	S15P	U23

Note: The number of memory devices installed in the locations U23 through U44 may vary as a function of the S/W program. See PROM Set MRV11-C drawings for installation.

Note: -X represents the latest revision.

32K WORD PROM MRV11-C
PART NUMBER

MADTS

ESY P/N	NAME	LOCATION
316-3200-X	S00M	U44
316-3201-X	S01M	U43
316-3202-X	S02M	U38
316-3203-X	S03M	U37
316-3204-X	S04M	U32
316-3205-X	S05M	U31
316-3206-X	S06M	U26
316-3207-X	S07M	U25
316-3208-X	S08M	U42
316-3209-X	S09M	U41
316-3210-X	S10M	U36
316-3211-X	S11M	U35
316-3212-X	S12M	U30
316-3213-X	S13M	U29
316-3214-X	S14M	U24
316-3215-X	S15M	U23

Note: The number of memory devices installed in the locations U23 through U44 may vary as a function of the S/W program. See PROM Set MRV11-C drawings for installation.

Note: -X represents the latest revision.

32K WORD PROM MRV11-C

SYSTEM-PROM ADDRESS CROSS REFERENCE

Note: All addresses are in Octal.

System Address - (20,000 *n)		PROM Address	Word #	Byte #
0-0776		0000-0377	256	512
1000-1776	1K Words	0400-0777	512	1024
2000-2776		1000-1377	768	1536
3000-3776		1400-1777	1024	2048
4000-4776		2000-2377	120	2560
5000-5776		2400-2777	1536	3072
6000-6776		3000-3377	1792	3584
7000-7776		3400-3777	2048	4096
10000-10776		4000-4377	2304	4608
11000-11776		4400-43777	2560	5120
12000-12776		5000-5377	2816	5632
13000-13776		5400-5777	3072	6144
14000-14776		6000-6377	3328	6656
15000-15776		6400-6777	3584	7168
16000-16776		7000-7377	3840	7680
17000-17776		7400-7777	4096	8192

n = chip set #

CONFIGURATION SPECIFICATION

POWER FAIL-RESTART, LTC, TERMINATION

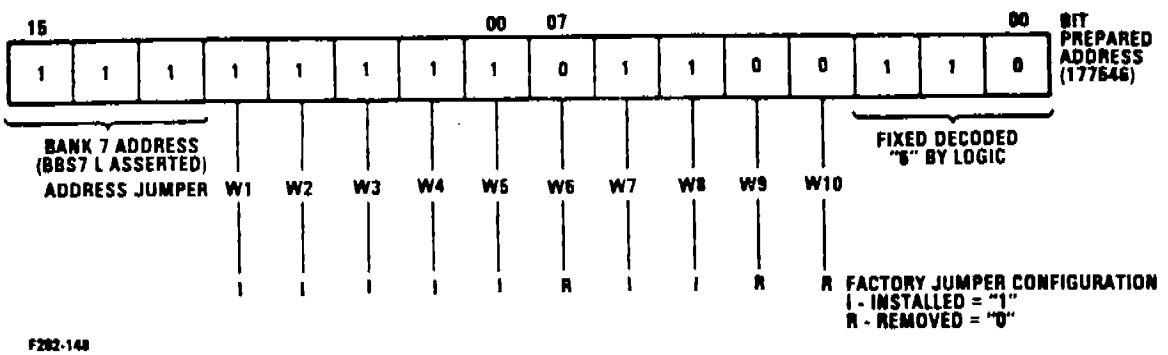
KPV11-B

DEC M8016 YB

JUMPER CONFIGURATION

W1	INSTALLED	
W2	INSTALLED	
W3	INSTALLED	
W4	INSTALLED	
W5	INSTALLED	CSR JUMPERS FOR 777546
W6	REMOVED	
W7	INSTALLED	
W8	INSTALLED	
W9	REMOVED	
W10	REMOVED	
W11	INSTALLED	FACTORY - DO NOT CHANGE
W12	REMOVED	DISABLE MANUAL LTC
W13	INSTALLED	ENABLED PROGRAMMED LTC
W14	INSTALLED	ENABLED LTC ON/OFF SWITCH
W15	INSTALLED	ALL COMMUNICATION PROCESSORS
W15	INSTALLED	ALL AFSS POSITION PROCESSORS AND ANCHORAGE FSDPS.
W15	REMOVED	FSDPS AND AWP POSITION PROCESSORS AS PER EEM 6490.16 CHAPTER 7.

DEVICE ADDRESS (LKC REGISTER) JUMPERS



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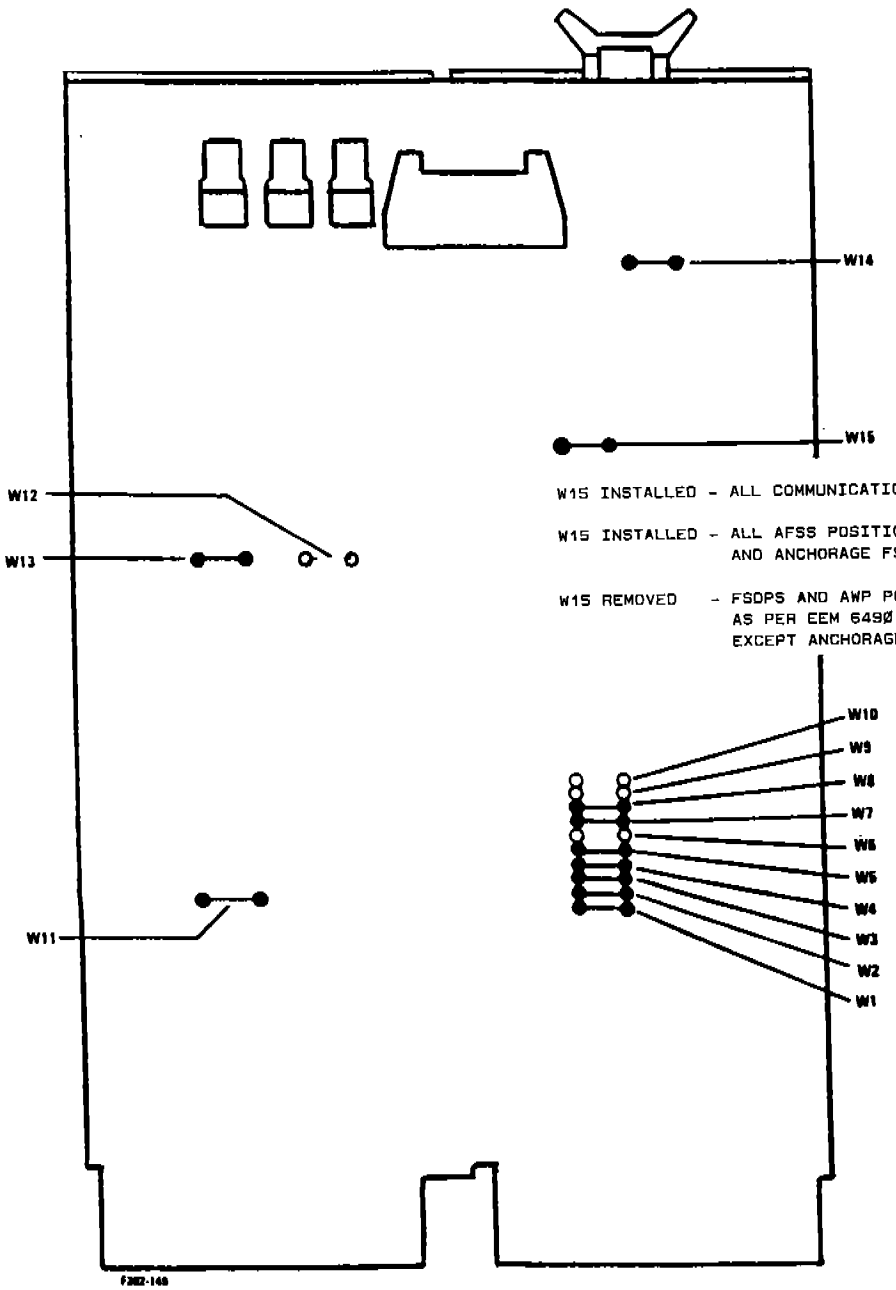
POWER FAIL-RESTART, LTC, TERMINATION KPVII-B
JUMPER LOCATIONS



W15 INSTALLED - ALL COMMUNICATION PROCESSORS

W15 INSTALLED - ALL AFSS POSITION PROCESSORS AND ANCHORAGE FSDPS

W15 REMOVED - FSDPS AND AWP POSITION PROCESSORS AS PER EEM 6490.16 CHAPTER 7 EXCEPT ANCHORAGE FSDPS

Configuration Specification

Disc Controller

DEC RLV12

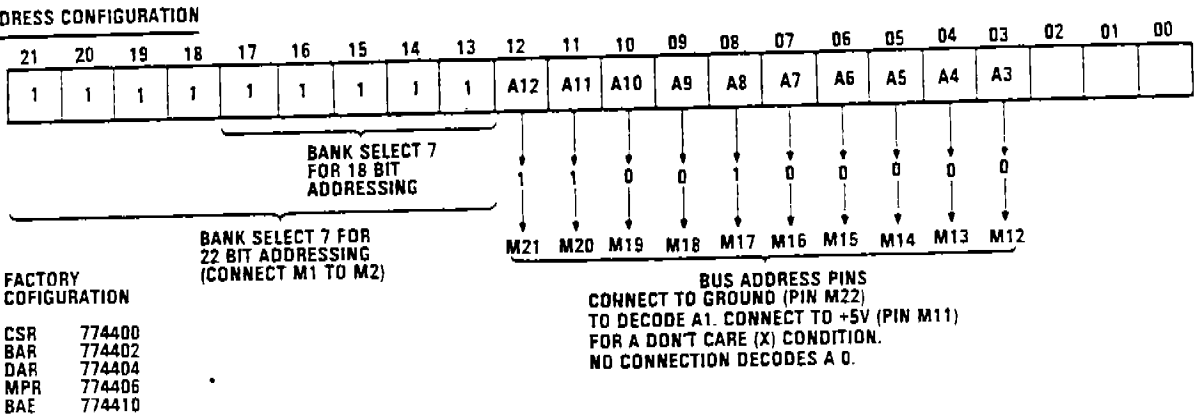
M8061

NOTE: THIS CIRCUIT CARD ASSEMBLY IS FACTORY CONFIGURED. USE THIS FOR VALIDATION ONLY.

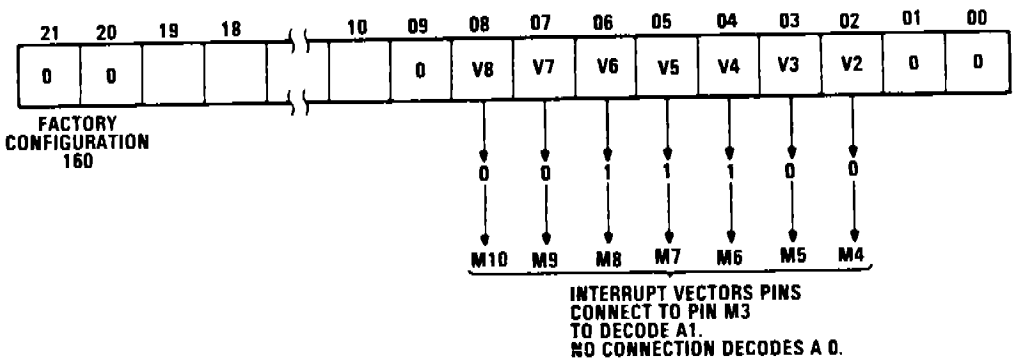
STANDARD ADDRESS ASSIGNMENTS

REGISTER NAME	18 BIT ADDRESS
CONTROL/STATUS	774400
BUS ADDRESS	774402
DISC ADDRESS	774404
MULTIPURPOSE	774406

ADDRESS CONFIGURATION



VECTOR CONFIGURATION



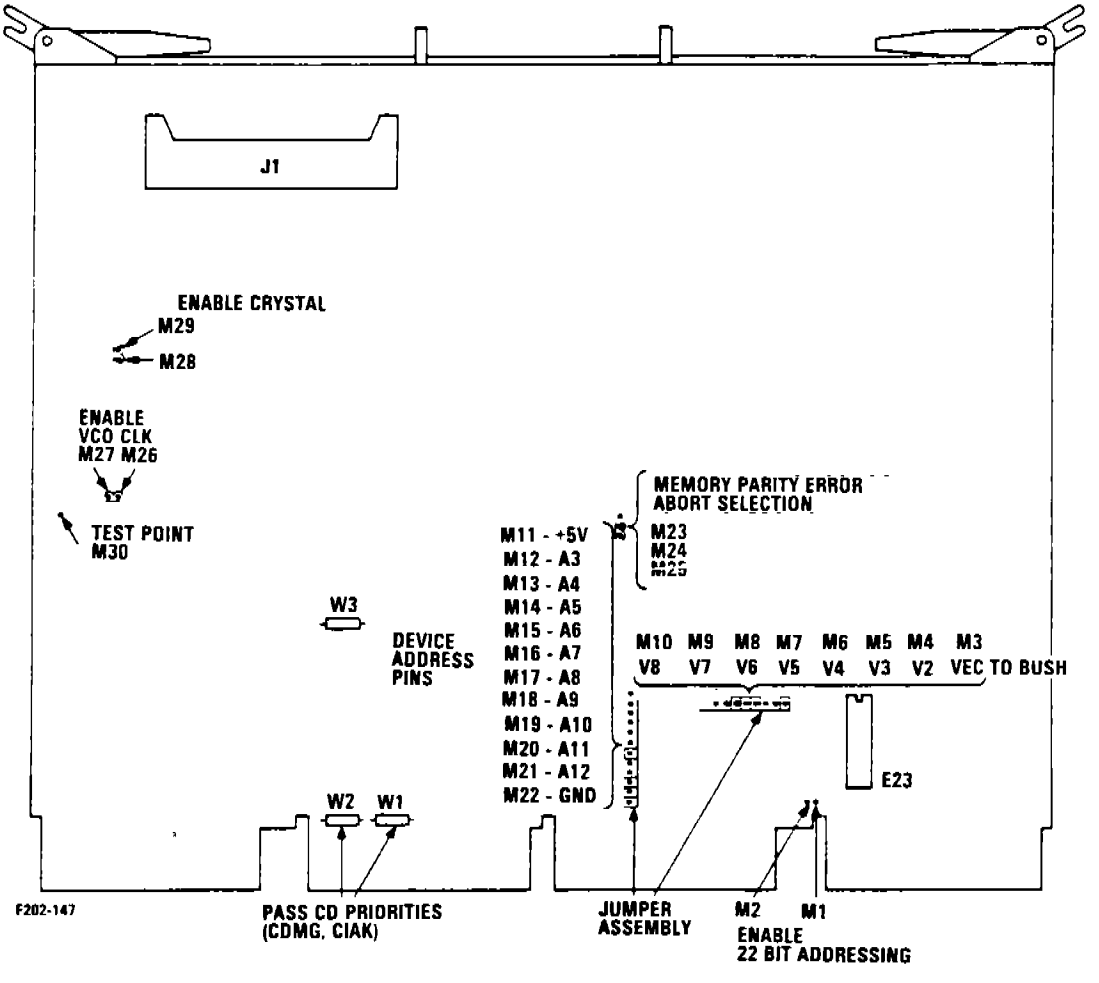
JUMPER CONFIGURATION

FUNCTION	DESCRIPTION	JUMPER CONFIGURATION
Memory Parity Error Abort	Enable Abort	No jumper between M23 to M24 Install jumper between M24 to M25
VCO Clock	Enable	Install jumper between M26 to M27
Crystal Clock	Enable	Install jumper between M28 to M29
Standard Device Address	18 Bit-774400	No jumpers between M1 to M2 Install jumper between M17 to M20 Install jumper between M21 to M22 Install jumper between M20 to M21
Standard Vector Address	160	Install jumper between M3 to M6 Install jumper between M7 to M8 Install jumper between M6 to M7

No Jumpers Installed on Pins:

M4, M5, M9, M10, M11-M16, M18, and M19

DISK CONTROLLER DEC RLV12
JUMPER CONFIGURATION



CONFIGURATION SPECIFICATION

DMA-Q PARALLEL DMA

PERITEK

JUMPER DESIGNATIONS

DMA-Q PARALLEL DMA

P-Q-R-S Group

P-R Byte Mode
R-Q Programmable Byte/Word Mode
P-S Word Mode

Configuration: R-Q

C-B-E Group

C-B PROM Enable
B-E PROM Disable

Configuration: B-E

f-h-e Group (Single/Dual Interrupt)

Configuration: f-e (Dual Interrupt)

D-A-F-E Group

D-A Word Mode
A-F Programmable Byte/Word Mode
A-E Byte Mode

Configuration: A-F

I-G-H-J-L-K-N Group (DMA Xfer Timing)

I-J, N-M	279
I-H, N-L	558
I-G, N-K	837

Configuration: I-H, N-L

7, 8, 9, 10, 11, 12 Group (Programmed I/O Address)

Dependent on DMA-Q Number. See following pages for configuration.

3, 4, 5, 6, 7 Group (Interrupt Vector Address)

Dependent on DMA-Q Number. See following pages for configuration.

JUMPER CONFIGURATION
DMA-Q PARALLEL DMA

Programmed I/O Address

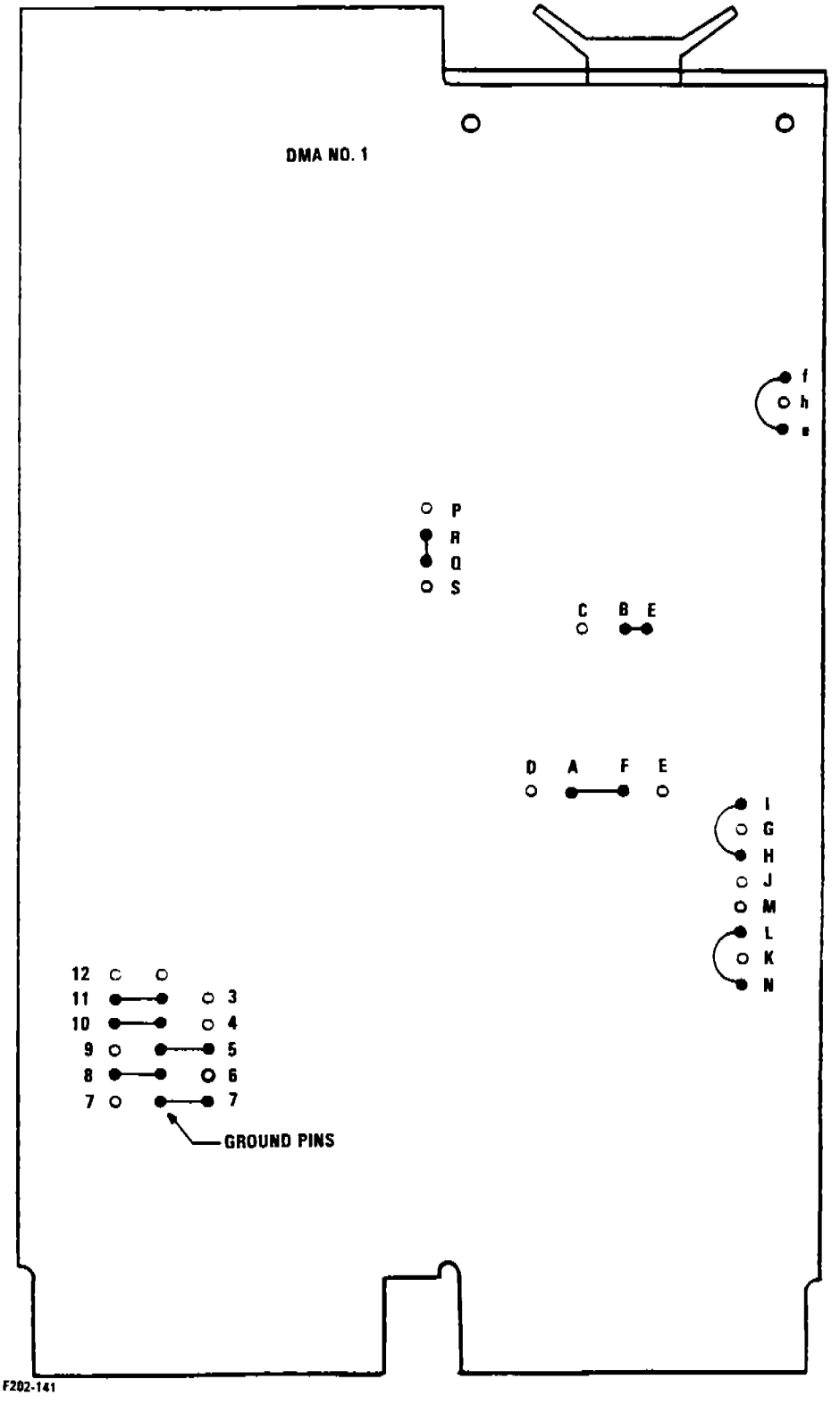
DMA-Q #	Address	Pin # 12	11	10	9	8	7
1	*71200	R	I	I	R	I	R
2	*71400	R	I	I	R	R	I
3	*71600	R	I	I	R	R	R

Interrupt Vector Address

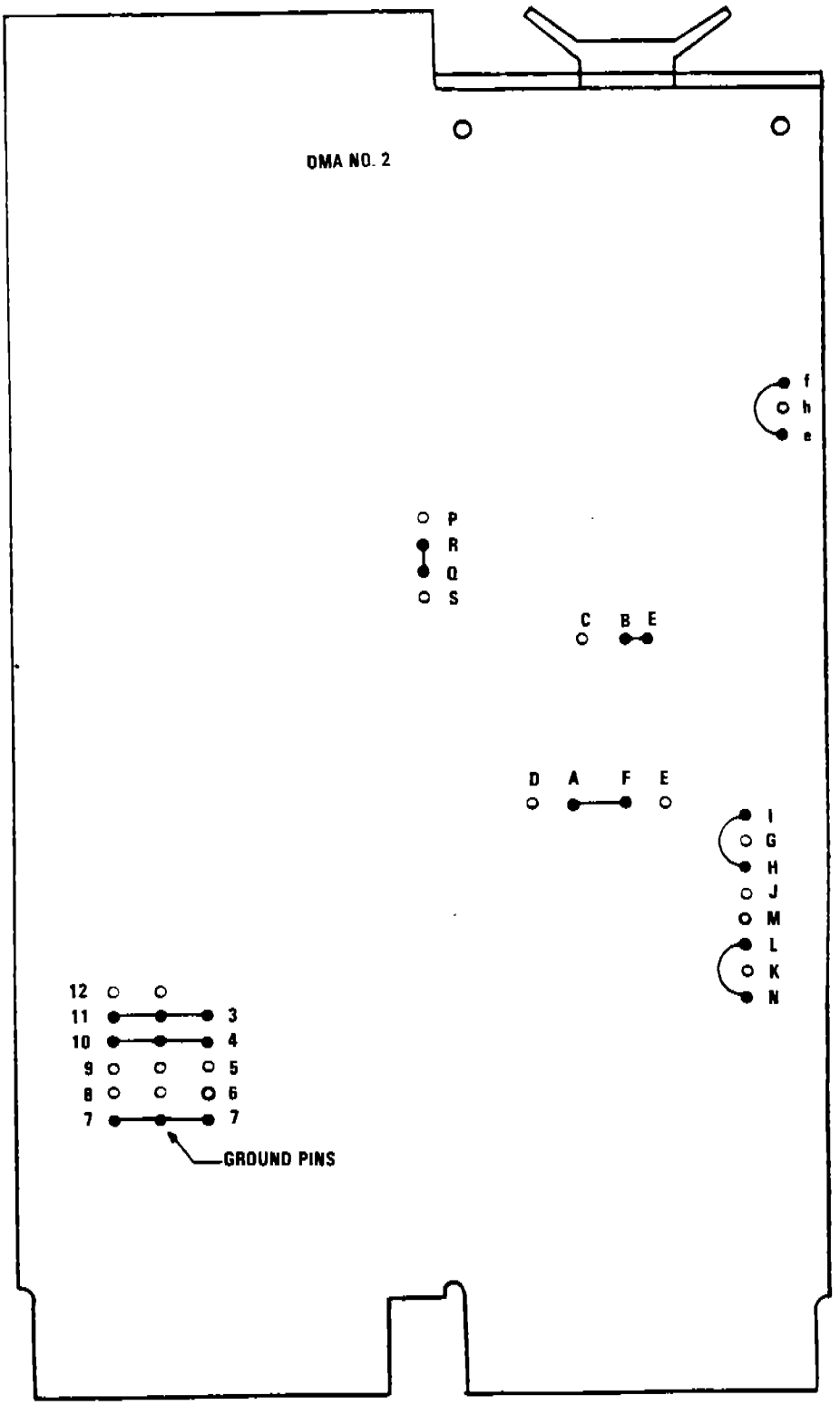
DMA-Q #	Address	Pin * 7	6	5	4	3
1	000130	I	R	I	R	R
2	000140	I	R	R	I	I
3	000150	I	R	R	I	R

I = Installed (connect to ground)
R = Removed (no jumper)

DMA-Q PARALLEL DMA
JUMPER CONFIGURATION



DMA-Q PARALLEL DMA JUMPER CONFIGURATION



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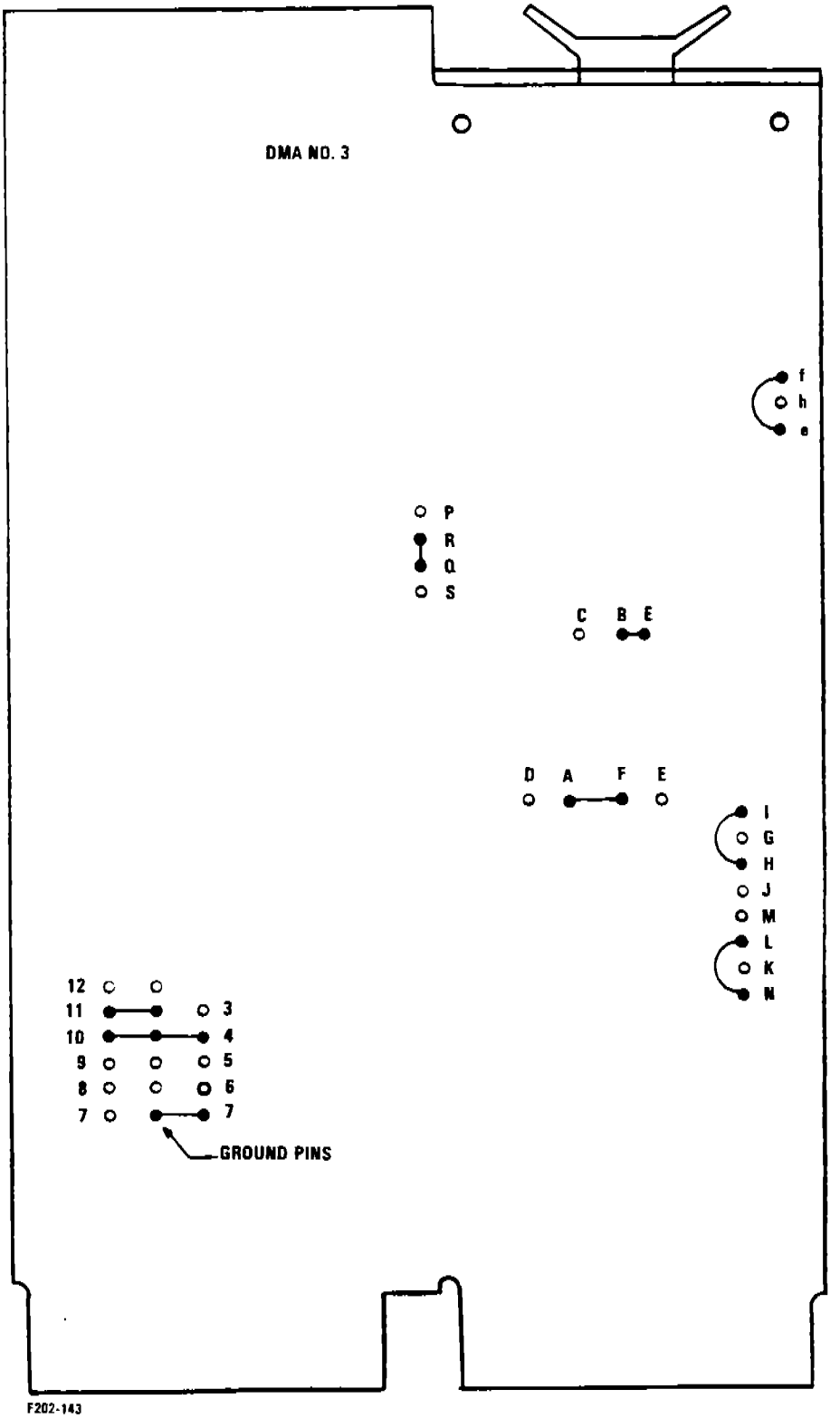
TMI 8S

COMMUNICATION CONFIGURATION - SERIAL I/O

A12	Installed	
A11	Installed	
A10	Installed	
A 9	Removed	Strapped for Device Address 776500
A 8	Installed	
A 7	Removed	
A 6	Installed	
I 9	Removed	
I 8	Removed	Strapped for Vector Interrupt 300
I 7	Installed	
I 6	Installed	
CON	Removed	Enables Console at Address 777560-777566
HALT	Removed	No action on framing error or break key
PE	Installed 8 places	Parity enabled
1S	Installed 8 places	One stop bit
7B	Installed 8 places	7 data bits
OP	Removed	Even parity

DMA-Q PARALLEL DMA JUMPER CONFIGURATION



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CONFIGURATION SPECIFICATION

TMI 8S

PART I : COMMUNICATIONS CONFIGURATION-SERIAL I/O

PART II: KEYBOARD I/O CONFIGURATION

PART III: MADTS CONFIGURATION

CONFIGURATION SPECIFICATION

TMI 8S

COMMUNICATION CONFIGURATION - SERIAL I/O

406-02160

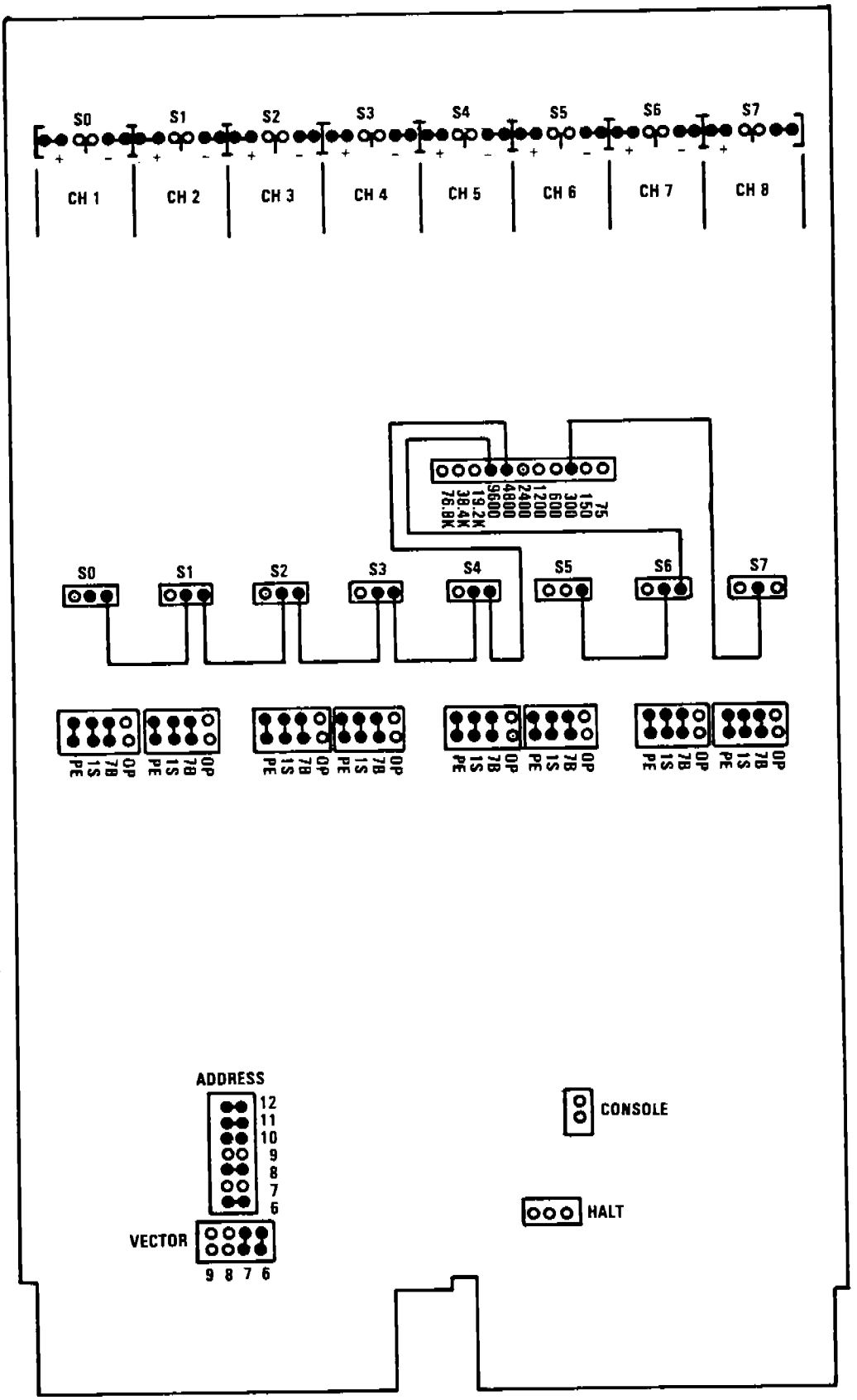
PART I

BAUD RATE SELECTION

Channel 1	Input - primary (next proc.) Output - primary broadcast	4800 baud	RS232
Channel 2	Input - primary (prev. proc.) Output - no connection	4800 baud	RS232
Channel 3	Input - secondary (next proc.) Output - secondary broadcast	4800 baud	RS232
Channel 4	Input - secondary (prev. proc) Output - no connection	4800 baud	RS232
Channel 5	Input - TSX-NET Output - TSX-NET	4800 baud	RS232
Channel 6	Input - Line Printer Output - Line Printer	9600 baud	RS232
Channel 7	Input - Prog. Workstation Output - Prog. Workstation	9600 baud	RS232
Channel 8	Input - Reserved (Non-console) Output - Reserved (Non-console)	300 baud	RS232

Note: Channels 1-8 numbered S0-S7 on the TMI-8S

COMMUNICATIONS CONFIGURATION-SERIAL I/O



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CONFIGURATION SPECIFICATION

TMI 8S

KEYBOARD I/O CONFIGURATION

PART II

KEYBOARD I/O CONFIGURATION

Address Bits							Address	Keyboard Inputs
A12	A11	A10	A9	A8	A7	A6		
I	I	R	I	R	R	R	*75000	1-8
I	I	R	I	R	R	I	*75100	9-16
I	I	R	I	R	I	R	*75200	17-64
I	I	R	I	R	I	I	*75300	25-32
I	I	R	I	I	R	R	*75400	33-40
I	I	R	I	I	R	I	*75500	41-48
I	I	R	I	I	I	R	*75600	49-56
I	I	R	I	I	I	I	*75700	57-64

*Bank (BBS7 L Asserted)

Vector Bits				Address	Keyboard Inputs
9	8	7	6		
R	I	R	R	400	1-8
R	I	R	I	500	9-16
R	I	I	R	600	17-24
R	I	I	I	700	25-32
I	R	R	R	1000	33-40
I	R	R	I	1100	41-48
I	R	I	R	1200	49-56
I	R	I	I	1300	57-64

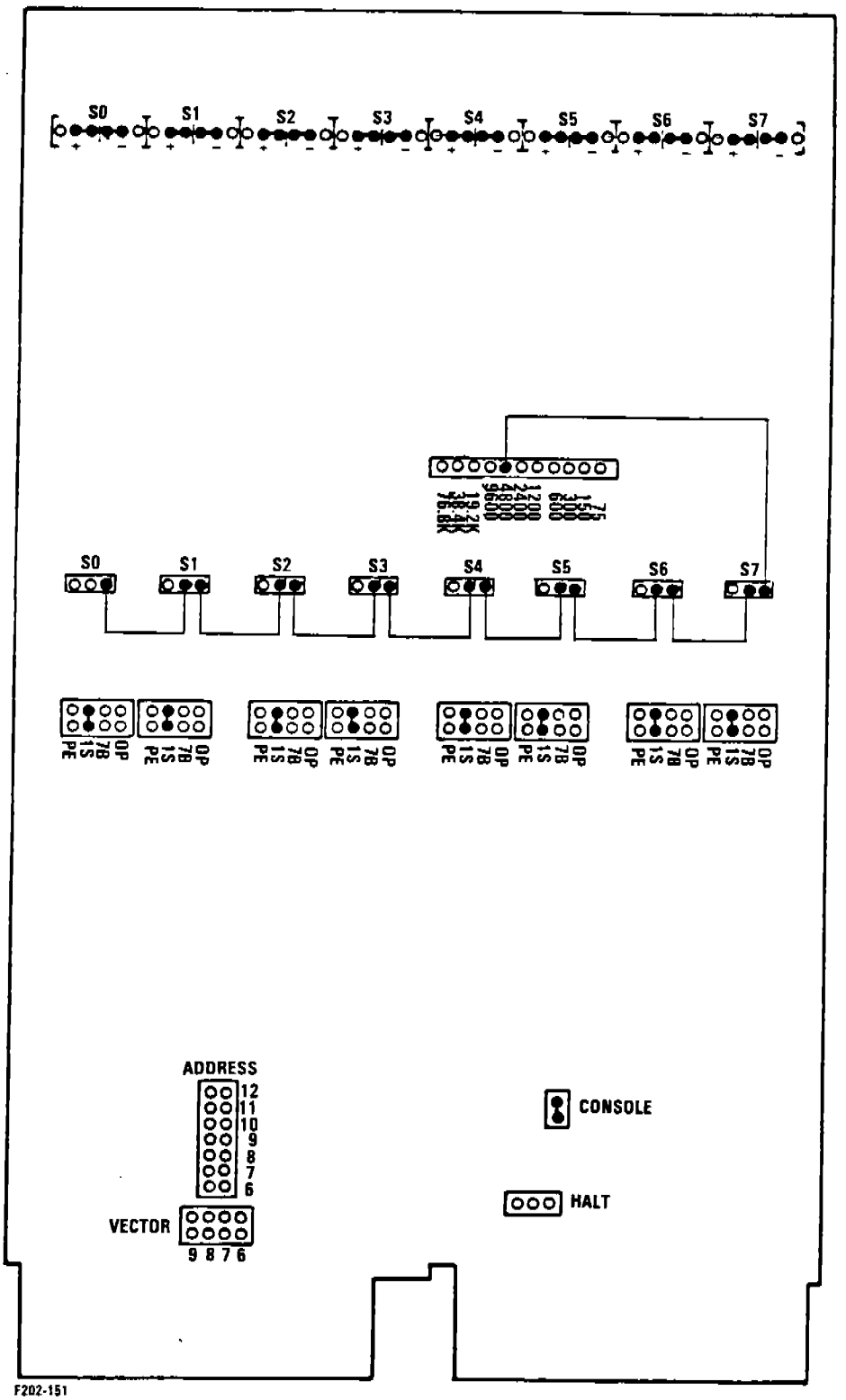
TMI 8S

KEYBOARD I/O CONFIGURATION

Channels 1 through 8
Baud Rate: 4800
Protocol: RS422

Miscellaneous Jumpers

Console	Installed	Disables console mode on channel 8
Halt	Removed	No action on framing error or break key
PE	Removed (8 places)	Parity disabled
1S	Installed (8 places)	Enable one stop bit
7B	Removed (8 places)	8 data bits
OP	Removed (8 places)	Even parity


S0
S1
S2
S3
S4
S5
S6
S7
ADDRESS
12
11
10
9
8
7
6
VECTOR
9 8 7 6
CONSOLE
HALT
F202-151

CONFIGURATION SPECIFICATION

TMI 8S

MADTS CONFIGURATION

406-02160

PART III

TMI 8S

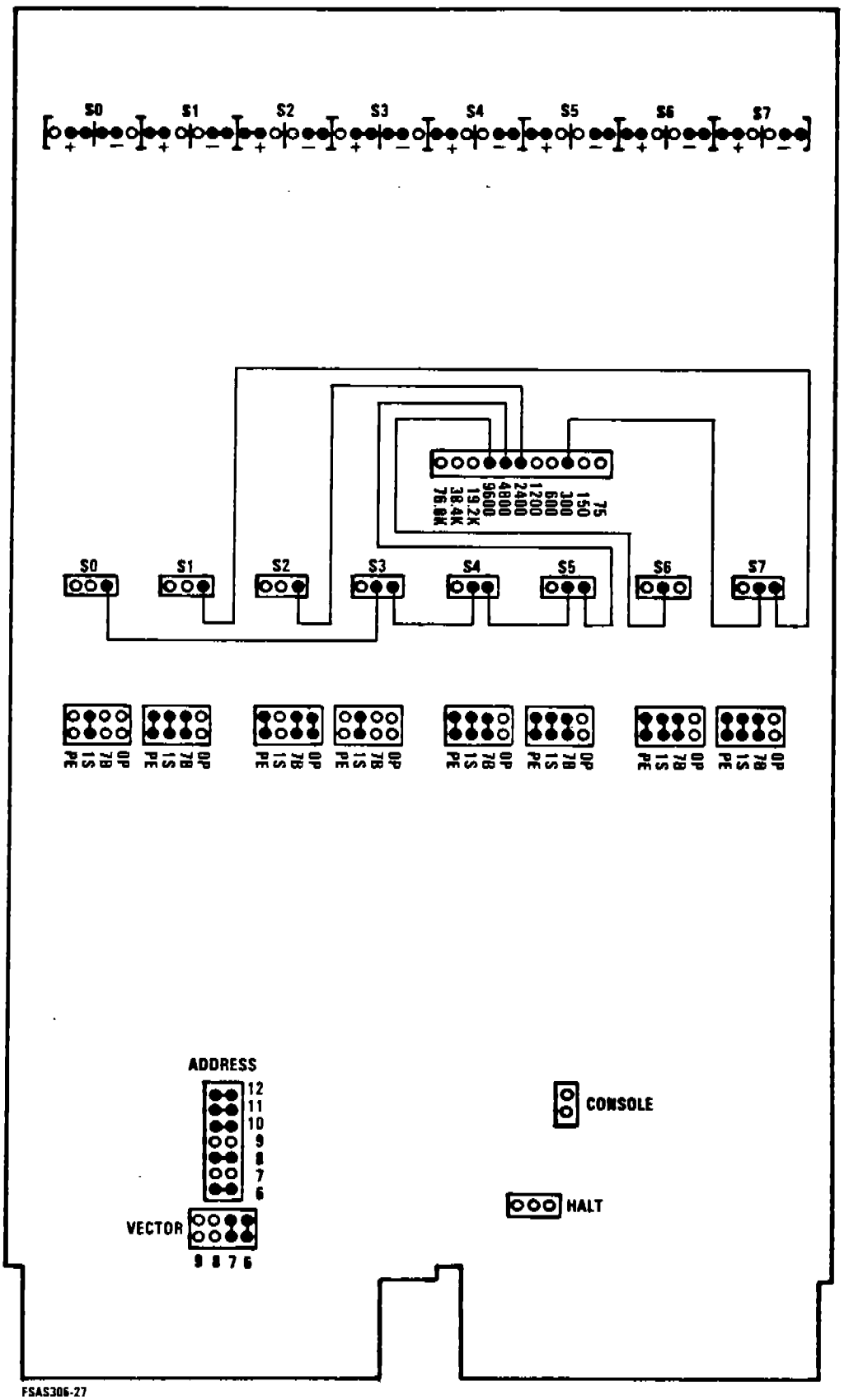
MADTS Configuration

A12	Installed	
A11	Installed	
A10	Installed	
A 9	Removed	Strapped for Device Address 776500
A 8	Installed	
A 7	Removed	
A 6	Installed	
I 9	Removed	
I 8	Removed	Strapped for Vector Interrupt 300
I 7	Installed	
I 6	Installed	
CON	Removed	Enables Console at Address 7775600-777566
HALT	Removed	No action on framing error or break key
PE	Installed 6 places	Parity enabled
1S	Installed 7 places	One stop bit
7B	Installed 6 places	7 data bits
OP	Installed 1 place	Even parity

Baud Rate Selection

Channel 1	Keyboards	4800 Baud	RS422
Channel 2	LA34	300 Baud	RS232
Channel 3	CTS Interface	2400 Baud	RS232
Channel 4	Keyboards	4800 Baud	RS422
Channel 5	TSX-NET	4800 Baud	RS232
Channel 6	Spare	4800 Baud	RS232
Channel 7	P-300 Printronix Card Reader Card Reader Data Tablet Data Table	9600 Baud	RS232
Channel 8	Console	300 Baud	RS232

Note: Channels 1-8 are numbered S0-S7 on TMI-8S


S0
S1
S2
S3
S4
S5
S6
S7
75
150
300
600
1200
2400
4800
9600
19.2K
38.4K
76.8K
PE
1S
7B
0P
ADDRESS
12
11
10
9
8
7
6
VECTOR
9 8 7 6
CONSOLE
HALT
FSAS306-27

CONFIGURATION SPECIFICATIONS
A/N OTF PROCESSOR
P/N 401-33676

A/N OTF PROCESSOR
P/N 401-33676

JUMPER OPTION CHART

Wire #	Pin Location From	Pin Location To	Function
1	5	17	MCLK -
2	3	8	MCLK +
3	8	38	MCLK +
4	16	39	ECLK +
5	6	18	ECLK -
6	18	25	ECLK -
7	25	31	ECLK -
8	10	13	DCLK -
9	14	24	DCLK +
10	21	35	LOAD +
11	22	29	ESER +
12	27	36	SCLK -
13	33	40	SLDE -
14	44	45	HSYNCH -
15	43	47	VSYNCH -
16	42	46	CSYNCH -

PROM DESIGNATIONS
A/N OTF PROCESSOR P/N 401-33676

Reference Designator: U60
Component P/N: N82S131F

ESY P/N	PROM NAME	POSITION NUMBERS
316-3012-X	APAL00.D00	00-07
316-3013-X	APAL08.D00	08-15
316-3014-X	APAL16.D00	16-23
316-3015-X	APAL24.D00	24-31
316-3016-X	APAL32.D00	32-39
316-3017-X	APAL40.D00	40-47

Explanation of PROM name APALNN.D00

AP: A/N OTF Processor
AL: Lower unit select of PROM (Address - low)
NN: Codes Addressed
.D00: Reference Description

Note: X denotes latest revision

Model 1 Full Capacity system requires a different configuration for this CCA from that used in the Model 1 systems. The following chart details the configuration differences between the two systems.

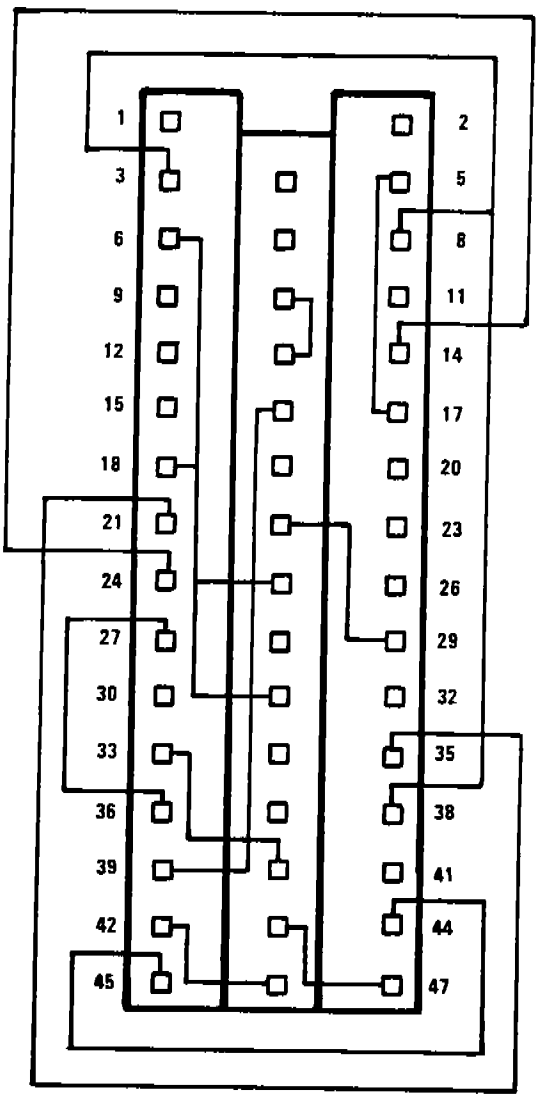
MODEL 1			MODEL 1 FULL CAPACITY		
Loc	P/N	Description	Loc	P/N	Description
U58	316-3011-X	Prom	U58	316-2586-X	Prom

Description of change:

Increases the Cache memory size from 2K words in Model 1 to 4K words in Model 1 Full Capacity. Moves the address allocation from 760000-767777 to 400000-417777

A/N OTF PROCESSOR
P/N 401-33676
WIRE JUMPER OPTIONS

A/N OTF PROCESSOR
P/N 401-33676
WIRE JUMPER OPTIONS



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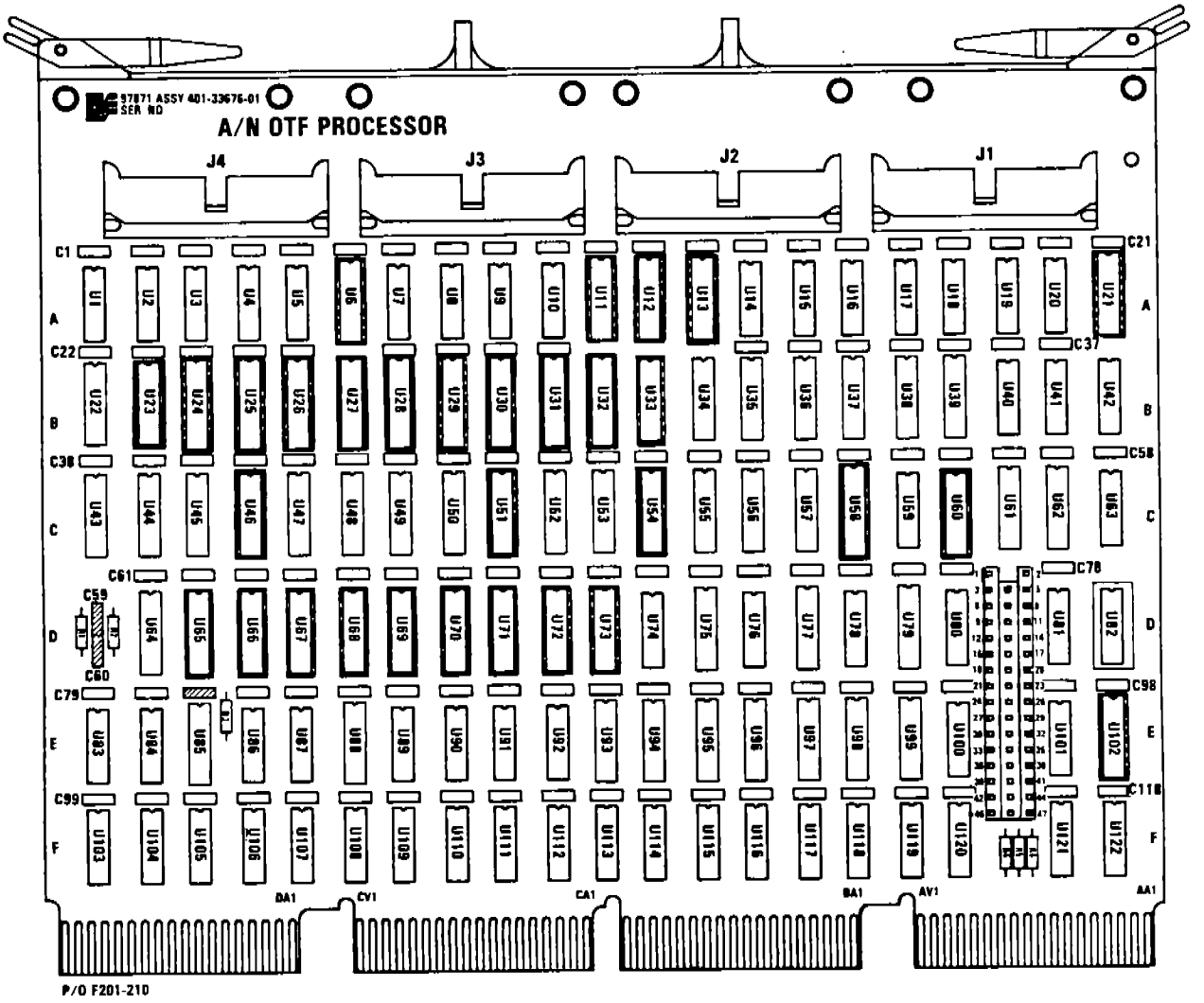
A/N OTF PROCESSOR
P/N 401-33676
PCBA



CONFIGURATION SPECIFICATIONS
QUAD CACHE
P/N 401-33692

JUMPER OPTIONS

QUAD CACHE P/N 401-33692

Wire #	Pin # From	Pin # To	Remarks
1	8	14	BLNKR2
2	14	17	BLNKR3
3	17	20	BLNKR1
4	20	21	BLNKR0
5	1	10	EMPHA1
6	10	4	EMPHA0
7	4	6	EMPHA2
8	6	16	EMPHA3
9	2	5	EMPHB1
10	5	11	EMPHB0
11	11	13	EMPHB2
12	13	19	EMPHB3

PROM IDENTIFICATION NUMBERS

PROM ID	POSITION	401-36711-XX
316-3040-X	1-1 thru 1-4	-01, -02, -03, 04-, -05
316-3041-X	1-5 thru 1-8	-01, -02, -03, 04-, -05
316-3040-X	2-1 thru 2-4	-02, -03, -04, 05-
316-3041-X	2-5 thru 2-8	-03, -04, -05
316-3040-X	3-1 thru 3-4	-04, -05
316-3041-X	3-5 thru 3-8	-05
316-3040-X	4-1 thru 4-4	-05
316-3041-X	4-5 thru 4-8	-05
316-3040-X	5-1 thru 5-4	-05

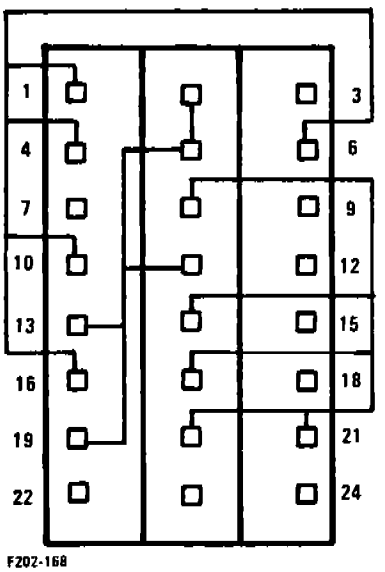
PROM ID	POSITION	401-37265-XX
316-3040-X	1-1 thru 1-2	-01

Ref Des: U5

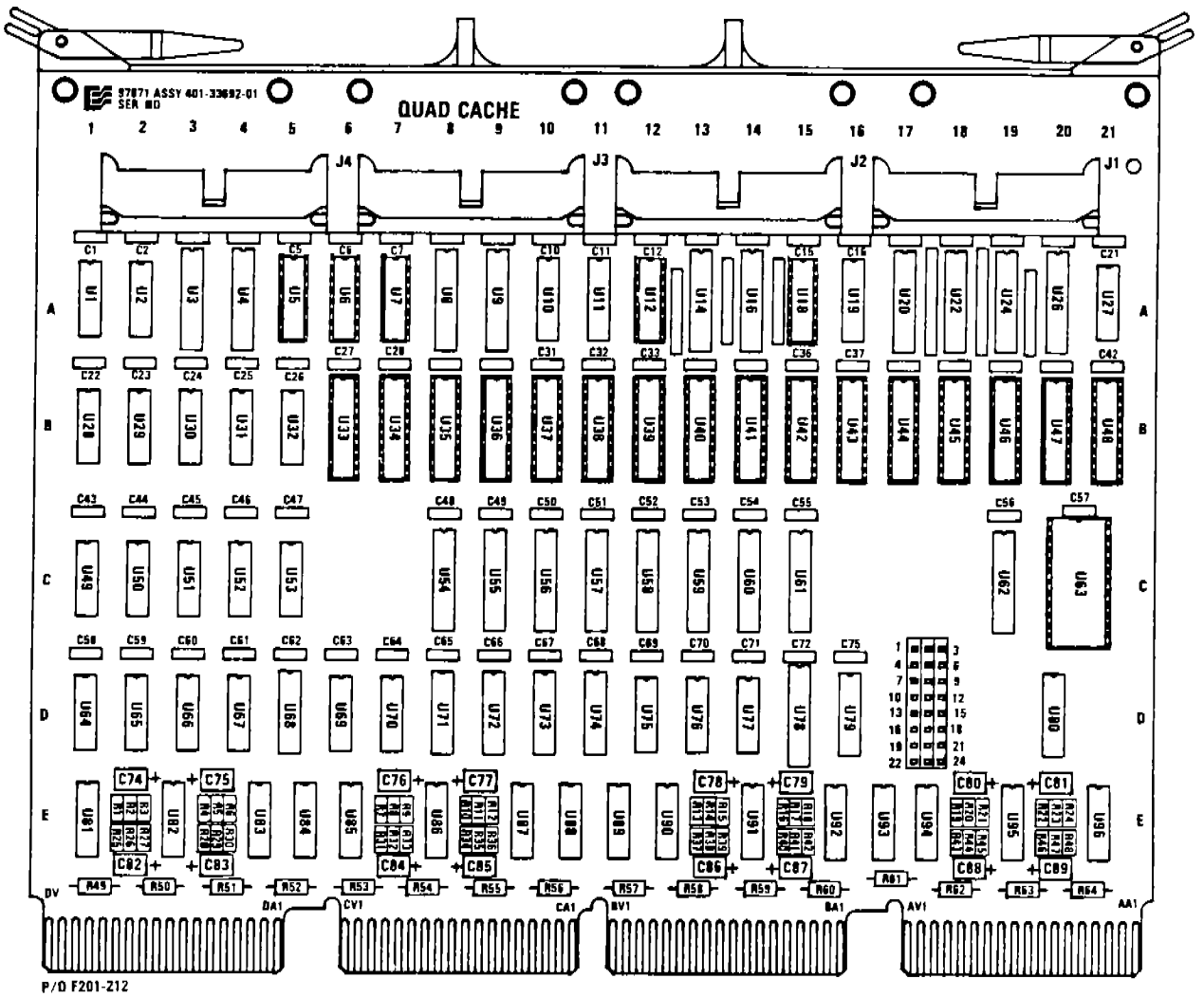
Note: X denotes latest revision

QUAD CACHE
P/N 401-33692
WIRE JUMPER OPTIONS

QUAD CACHE
P/N 401-33692
WIRE JUMPER OPTIONS



QUAD CACHE
P/N 401-33692
PCBA



CONFIGURATION SPECIFICATIONS

MULTIPLEXER

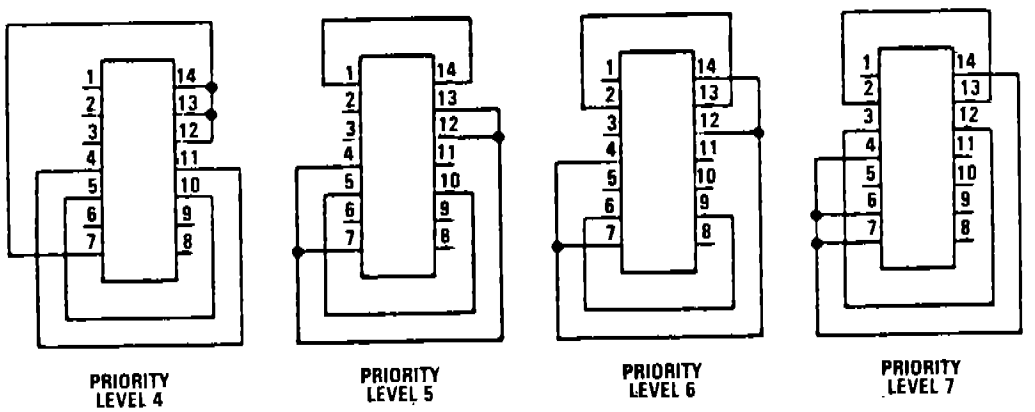
P/N 401-36993

INTERRUPT CONFIGURATION OPTION

MULTIPLEXER P/N 401-36993

OPTION PLUG - REF DES U97

PART NUMBER	PRIORITY	CONFIGURATION
* 401-37125-01	4	Position Independent
401-37125-02	5	Position Independent
401-37125-03	6	Position Independent
401-37125-04	7	Position Independent



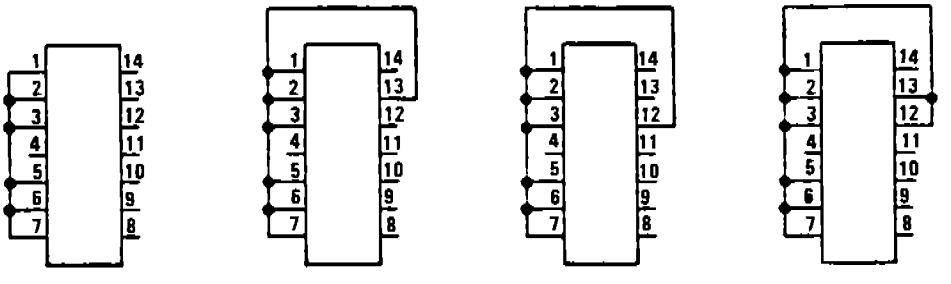
* STANDARD CONFIGURATION

MULTIPLEXER ADDRESS CONFIGURATION

MULTIPLEXER P/N 401-36993

OPTION PLUG - REF DES U93

PART NUMBER	ADDRESS	FUNCTION
401-37124-01	776600	Multiplexer Channel 0-3
401-37124-02	776602	Multiplexer Channel 4-7
401-37124-03	776604	Multiplexer Channel 8-11
401-37124-04	776606	Multiplexer Channel 12-15



OPTION 1 776600_8 | OPTION 2 776602_8 | OPTION 3 776604_8 | OPTION 4 776606_8

F202-159

LOCAL MEMORY AND I/O ADDRESS
CONFIGURATION
MULTIPLEXER P/N 401-36993

Memory Location	Socket	Jumper	Jumper Position
MEM0	U36	E4	A-B
MEM1	U37	E5	A-B
MEM2	U38	E6	B-C
MEM3	U39	E7	B-C
MEM4	U40	E8	B-C
MEM5	U41	E9	B-C

Jumpers are configured to accept the required memory devices as follows:

Memory Type	Part Number	Capacity	Jumper Position
RAM	MK4802	2k x 8	B-C
RAM	(future)	4k x 8	A-B
EPROM	D2732A-2	4k x 8	A-B
EPROM	D2764-2	8k x 8	A-B
EPROM	MK2764	8k x 8	A-B

HARDWARE CONFIGURATION OPTIONS
MULTIPLEXER P/N 401-36993

E2	E3	Communications Processor No.
o---o o A B C	o o---o A B C	1
o o---o A B C	o---o o A B C	2
o o---o A B C	o o---o A B C	3

E1	Function
o---o o A B C	Debug disable*
o o---o A B C	Debug enable

*STANDARD CONFIGURATION

Hardware configuration option E10 is not used in the current application, and therefore the jumper is removed.

MADTS CONFIGURATION
MULTIPLEXER P/N 401-36993

OPTION PLUG

U97 - P/N 401-37125-01 Installed
U93 - P/N 401-37124-01 Installed

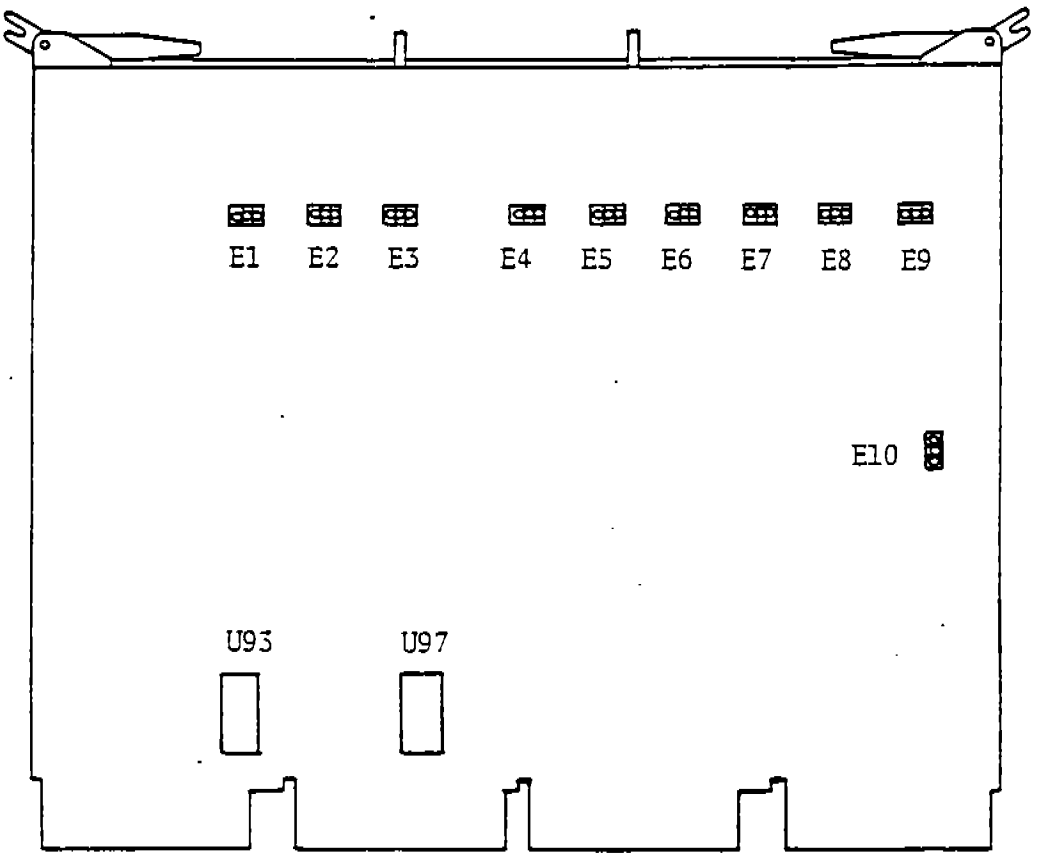
Local Memory and I/O Address Jumper	Jumper Position
E4	A-B
E5	A-B
E6	B-C
E7	B-C
E8	B-C
E9	B-C

Communications Processor No. Jumper	Jumper Position
E2	B-C
E3	B-C

Debug Jumper	Jumper Position
E1	A-B
E10	Removed

Jumper Locations

MULTIPLEXER
P/N 401-36993
PCBA



LSI-11/23 SYSTEM LEVEL CONFIGURATION SPECIFICATION FOR CONTROL, STATUS VECTOR, RAM, AND CACHE ADDRESS ASSIGNMENTS

DEFINITION OF TERMS AND SYMBOLS

Vector	Vector Interrupt Addresses
CSR	Control Status Register Addresses
RAM	Random Access Dynamic Memory Addresses
Cache	Special Purpose User Memory Addresses
Reserved	Reserved for future expansion - assigned per E-Systems or Digital convention
Unassigned	Not assigned - may be used as required
*	Bank 7 (BBS7 +) asserted plus address bits as designated (I/O page reference).
|	Change bar (in margin) - indicates change or addition since last release of specification.
o	Deletion symbol (in margin) - indicates deletion since last release of specification.

***** VECTORS *****

Addresses	Assignment
000000-000002	Constant Zero, Restart Address
000004-000006	[Vector] CPU Exception
000010-000012	[Vector] Illegal Instruction/Halt Trap
000014-000016	[Vector] BPT Instruction/T-bit Set In PS
000020-000022	[Vector] IOT Instruction
000024-000026	[Vector] Power-fail/Auto-restart (Reserved)
000030-000032	[Vector] EMT: Reentrant Service Call
000034-000036	[Vector] TRAP: Non-reentrant Service Call
000040	System Software (System ID)
000042	System Software (Version ID)
000044-000052	System Software (Reserved)
000054	Start Of RW Space (EXC$BC)
000056	End Of RO Space Not Incl Overlay Regions (0 Iff No Overlay Regions)
000060-000062	[Vector] 8S Channel #8 Input-Keyboard (Console Mode)
000064-000066	[Vector] 8S Channel #8 Output-Printer (Console Mode)
000070-000072	[Vector] Paper Tape Reader (Reserved)
000074-000076	[Vector] Paper Tape Punch (Reserved)
000100-000102	[Vector] Event/Line Time Clock (KPV11-B)
000104-000106	[Vector] Programmable Clock (Reserved)
000110-000112	[Vector] Programmable Clock (KWV11-A)
000114-000116	[Vector] Memory Parity Error Trap
000120-000122	[Vector] DMA Interface (DRV11-B)
000124-000126	[Vector] DMA Interface (DRV11-B) (MADTS)
000130-000136	[Vector] DMA-Q #1
000140-000146	[Vector] DMA-Q #2
000150-000156	[Vector] DMA-Q #3
000160-000162	[Vector] RLV12 Disc Controller #1
000164-000166	[Vector] RLV12 Disc Controller #2
000170-000176	[Vector] MADTS DMA-Q

Addresses	Assignment
000200-000202	[Vector] Line Printer
000204-000206	[Vector] Fixed-head Disk (Reserved)
000210-000212	[Vector] DEC Disk (Reserved)
000214-000216	[Vector] DEC Tape (Reserved)
000220-000222	[Vector] DEC Pack (Reserved)
000224-000226	[Vector] Mag Tape (Emulex TC01)
000230-000232	[Vector] Card Reader (Reserved)
000234-000236	[Vector] (Reserved)
000240-000242	[Vector] PIRQ - Program Int. Request (Reserved)
000244-000246	[Vector] Floating-point Exception
000250-000252	[Vector] Memory-protection Violation
000254-000256	[Vector] Disk Pack (Emulex SC01)
000260-000262	[Vector] Scanoptik DQ-11/23
000264-000266	[Vector] Floppy Disk
000270-000272	[Vector] DZV11 Multiplexer #1
000274-000276	[Vector] DZV11 Multiplexer #2
000300-000302	[Vector] 8S Channel #1 Input - Reserved
000304-000306	[Vector] 8S Channel #1 Output - Reserved
000310-000312	[Vector] 8S Channel #2 Input - Reserved
000314-000316	[Vector] 8S Channel #2 Output - Reserved
000320-000322	[Vector] 8S Channel #3 Input - Reserved
000324-000326	[Vector] 8S Channel #3 Output - Reserved
000330-000332	[Vector] 8S Channel #4 Input - Reserved
000334-000336	[Vector] 8S Channel #4 Output - Reserved
000340-000342	[Vector] 8S Channel #5 Input - TSX-NET
000344-000346	[Vector] 8S Channel #5 Output - TSX-NET
000350-000352	[Vector] 8S Channel #6 Input - Line Printer
000354-000356	[Vector] 8S Channel #6 Output - Line Printer
000360-000362	[Vector] 8S Channel #7 Input - Prog. Workstation
000364-000366	[Vector] 8S Channel #7 Output - Prog. Workstation
000370-000372	[Vector] 8S Channel #8 Input - Reserved (Non-console)
000374-000376	[Vector] 8S Channel #8 Output - Reserved (Non-console)

Addresses	Assignment
000400-000402	[Vector] Keyboard Input - Position 1
000404-000406	[Vector] (Reserved)
000410-000412	[Vector] Keyboard Input - Position 2
000414-000416	[Vector] (Reserved)
000420-000422	[Vector] Keyboard Input - Position 3
000424-000426	[Vector] (Reserved)
000430-000432	[Vector] Keyboard Input - Position 4
000434-000436	[Vector] (Reserved)
000440-000442	[Vector] Keyboard Input - Position 5
000444-000446	[Vector] (Reserved)
000450-000452	[Vector] Keyboard Input - Position 6
000454-000456	[Vector] (Reserved)
000460-000462	[Vector] Keyboard Input - Position 7
000464-000466	[Vector] (Reserved)
000470-000472	[Vector] Keyboard Input - Position 8
000474-000476	[Vector] (Reserved)
000500-000502	[Vector] Keyboard Input - Position 9
000504-000506	[Vector] (Reserved)
000510-000512	[Vector] Keyboard Input - Position 10
000514-000516	[Vector] (Reserved)
000520-000522	[Vector] Keyboard Input - Position 11
000524-000526	[Vector] (Reserved)
000530-000532	[Vector] Keyboard Input - Position 12
000534-000536	[Vector] (Reserved)
000540-000542	[Vector] Keyboard Input - Position 13
000544-000546	[Vector] (Reserved)
000550-000552	[Vector] Keyboard Input - Position 14
000554-000556	[Vector] (Reserved)
000560-000562	[Vector] Keyboard Input - Position 15
000564-000566	[Vector] (Reserved)
000570-000572	[Vector] Keyboard Input - Position 16
000574-000576	[Vector] (Reserved)
000600-000602	[Vector] E-Systems MUX 1 Service
000604-000606	[Vector] E-Systems MUX 1 Channel 0 Output
000610-000612	[Vector] E-Systems MUX 1 Channel 0 Input
000614-000616	[Vector] E-Systems MUX 1 Channel 1 Output
000620-000622	[Vector] E-Systems MUX 1 Channel 1 Input
000624-000626	[Vector] E-Systems MUX 1 Channel 2 Output
000630-000632	[Vector] E-Systems MUX 1 Channel 2 Input
000634-000636	[Vector] E-Systems MUX 1 Channel 3 Output
000640-000642	[Vector] E-Systems MUX 1 Channel 3 Input
000644-000646	[Vector] (Reserved)

Addresses	Assignment
000650-000652	[Vector] E-Systems MUX 2 Service
000654-000656	[Vector] E-Systems MUX 2 Channel 0 Output
000660-000662	[Vector] E-Systems MUX 2 Channel 0 Input
000664-000666	[Vector] E-Systems MUX 2 Channel 1 Output
000670-000672	[Vector] E-Systems MUX 2 Channel 1 Input
000674-000676	[Vector] E-Systems MUX 2 Channel 2 Output
000700-000702	[Vector] E-Systems MUX 2 Channel 2 Input
000704-000706	[Vector] E-Systems MUX 2 Channel 3 Output
000710-000707	[Vector] E-Systems MUX 2 Channel 3 Input
000714-000716	[Vector] (Reserved)
000720-000722	[Vector] E-Systems MUX 3 Service (Reserved)
000724-000726	[Vector] E-Systems MUX 3 Channel 0 Output (Reserved)
000730-000732	[Vector] E-Systems MUX 3 Channel 0 Input (Reserved)
000734-000736	[Vector] E-Systems MUX 3 Channel 1 Output (Reserved)
000740-000742	[Vector] E-Systems MUX 3 Channel 1 Input (Reserved)
000744-000746	[Vector] E-Systems MUX 3 Channel 2 Output (Reserved)
000750-000752	[Vector] E-Systems MUX 3 Channel 2 Input (Reserved)
000754-000756	[Vector] E-Systems MUX 3 Channel 3 Output (Reserved)
000760-000762	[Vector] E-Systems MUX 3 Channel 3 Input (Reserved)
000764-000766	[Vector] (Reserved)
000770-000772	[Vector] (Unassigned)
000774-000776	[Vector] (Unassigned)
001000-001002	[Vector] E-Systems Graphics Control Processor #1
001004-001016	[Vector] (Reserved)
001010-001012	[Vector] E-Systems Graphics Control Processor #2
001014-001016	[Vector] (Reserved)
001020-001022	[Vector] E-Sys. Graphics Ctrl. Proc. #3 (Reserved)
001024-001026	[Vector] (Reserved)
001030-001032	[Vector] E-Sys. Graphics Ctrl. Proc. #4 (Reserved)
001034-001036	[Vector] (Reserved)
001040-001042	[Vector] E-Sys. Graphics Ctrl. Proc. #5 (Reserved)
001044-001046	[Vector] (Reserved)
001050-001052	[Vector] E-Sys. Graphics Ctrl. Proc. #6 (Reserved)
001054-001056	[Vector] (Reserved)
001060-001062	[Vector] E-Sys. Graphics Ctrl. Proc. #7 (Reserved)
001064-001066	[Vector] (Reserved)
001070-001072	[Vector] E-Sys. Graphics Ctrl. Proc. #8 (Reserved)
001074-001076	[Vector] (Reserved)
001100-001476	[Vectors] DRV11-J (Up to 64 programmable vectors)

***** PROGRAM/DATA MEMORY *****

Addresses	Assignment
000000-0157776	[RAM] Dynamic Memory - 16 Bit Systems
000000-0757776	[RAM] Dynamic Memory - 18 Bit Systems
000000-17757776	[RAM] Dynamic Memory - 22 Bit Systems

***** DEVICE WINDOWS (Model 1) *****

Addresses	Assignment
*60000-*67776	[Cache] E-Systems A/N Cache Window
*60000-*63776	[Cache] MRV11-C PROM Window #1
*64000-*67776	[Cache] MRV11-C PROM Window #2
	Note: A/N Cache and PROM may not be mapped in at the same time.

***** DEVICE WINDOWS (Model 1 Full Capacity) *****

Addresses	Assignment
400000-417776	[Cache] E-Systems A/N Cache Window
760000-763776	[Cache] MRV11-C PROM Window #1
764000-767776	[Cache] MRV11-C PROM Window #2

***** CONTROL/STATUS REGISTERS *****

Addresses	Assignment
*70000-*70776	[CSR] Scanoptik DQ-11/23 Trace Memory
*71000-*71006	[CSR] Scanoptik DQ-11/23 Control
*71010-*71076	[CSR] (Reserved)
*71100-*71106	[CSR] E-Systems Graphics Control Processor #1
*71110-*71116	[CSR] E-Systems Graphics Control Processor #2
*71120-*71126	[CSR] E-Sys. Graphics Ctrl. Proc. #3 (Reserved)
*71130-*71136	[CSR] E-Sys. Graphics Ctrl. Proc. #4 (Reserved)
*71140-*71146	[CSR] E-Sys. Graphics Ctrl. Proc. #5 (Reserved)
*71150-*71156	[CSR] E-Sys. Graphics Ctrl. Proc. #6 (Reserved)
*71160-*71166	[CSR] E-Sys. Graphics Ctrl. Proc. #7 (Reserved)
*71170-*71176	[CSR] E-Sys. Graphics Ctrl. Proc. #8 (Reserved)
*71200-*71316	[CSR] Peritek DMA-Q PROM and CSR #1
*71320-*71376	[CSR] (Reserved)
*71400-*71516	[CSR] Peritek DMA-Q PROM and CSR #2
*71520-*71576	[CSR] (Reserved)
*71600-*71716	[CSR] Peritek DMA-Q PROM and CSR #3
*71720-*71766	[CSR] (Reserved)
*71770-*71776	[CSR] Digital Pathways TCU-50D
*72000	[CSR] E-Systems OTF Processor #1
*72002	[CSR] E-Systems OTF Processor #2
*72004	[CSR] E-Systems OTF Processor #3
*72006	[CSR] E-Systems OTF Processor #4
*72010	[CSR] E-Systems OTF Processor #5
*72012	[CSR] E-Systems OTF Processor #6 (Reserved)
*72014	[CSR] E-Systems OTF Processor #7 (Reserved)
*72016	[CSR] E-Systems OTF Processor #8 (Reserved)
*72020-*72076	[CSR] (Reserved)
*72100	[CSR] MSV11-L #1
*72102	[CSR] MSV11-L #2
*72104	[CSR] MSV11-L #3
*72106	[CSR] MSV11-L #4
*72110	[CSR] MSV11-L #5
*72112	[CSR] MSV11-L #6
*72114	[CSR] MSV11-L #7
*72116	[CSR] MSV11-L #8

Addresses	Assignment
*72120-*72136	[CSR] (Reserved)
*72140-*72156	[CSR] DRV11-J
*72160-*72176	[CSR] FP11 Floating Point
*72200-*72276	[CSR] Memory Management (Reserved)
*72300-*72316	[CSR] Memory Management Kernel Page Descripter Registers
*72320-*72336	[CSR] Memory Management (Reserved)
*72340-*72356	[CSR] Memory Management Kernel Page Address Registers
*72360-*72376	[CSR] Memory Management (Reserved)
*72400-*72406	[CSR] (Reserved)
*72410-*72416	[CSR] DRV11-B DMA Interface
*72420-*72426	[CSR] DRV11-B DMA Interface (MADTS)
*72430-*72514	[CSR] (Reserved)
*72516	[CSR] Memory Management Unit SR3
*72520-*72536	[CSR] TM11 Tape (EMULEX TC01)
*72540-*72542	[CSR] KWV11-P Programmable Clock
*72544-*72546	[CSR] (Reserved)
*72550-*72776	[CSR] (Reserved)
*73000-*73776	[CACHE] MRV11-C Bootstrap
*74000-*74176	[CSR] MADTS DMA-Q
*74200-*74376	[CSR] (Reserved)
*74400-*74406	[CSR] RLV12 Disc Controller #1
*74410-*74436	[CSR] (Reserved)
*74440-*74446	[CSR] RLV12 Disc Controller #2
*74450-*74776	[CSR] (Reserved)
*75000-*75002	[CSR] Keyboard Input - Position 1
*75004-*75006	[CSR] (Reserved)
*75010-*75012	[CSR] Keyboard Input - Position 2

Addresses	Assignment
*75014-*75016	[CSR] (Reserved)
*75020-*75022	[CSR] Keyboard Input - Position 3
*75024-*75026	[CSR] (Reserved)
*75030-*75032	[CSR] Keyboard Input - Position 4
*75034-*75036	[CSR] (Reserved)
*75040-*75042	[CSR] Keyboard Input - Position 5
*75044-*75046	[CSR] (Reserved)
*75050-*75052	[CSR] Keyboard Input - Position 6
*75054-*75056	[CSR] (Reserved)
*75060-*75062	[CSR] Keyboard Input - Position 7
*75064-*75066	[CSR] (Reserved)
*75070-*75072	[CSR] Keyboard Input - Position 8
*75074-*75076	[CSR] (Reserved)
*75100-*75102	[CSR] Keyboard Input - Position 9
*75104-*75106	[CSR] (Reserved)
*75110-*75112	[CSR] Keyboard Input - Position 10
*75114-*75116	[CSR] (Reserved)
*75120-*75122	[CSR] Keyboard Input - Position 11
*75124-*75126	[CSR] (Reserved)
*75130-*75132	[CSR] Keyboard Input - Position 12
*75134-*75136	[CSR] (Reserved)
*75140-*75142	[CSR] Keyboard Input - Position 13
*75144-*75146	[CSR] (Reserved)
*75150-*75152	[CSR] Keyboard Input - Position 14
*75154-*75156	[CSR] (Reserved)
*75160-*75162	[CSR] Keyboard Input - Position 15
*75164-*75166	[CSR] (Reserved)
*75170-*75172	[CSR] Keyboard Input - Position 16
*75174-*75176	[CSR] (Reserved)
*75200-*75776	[CSR] (Reserved)
*76000-*76006	[CSR] DZV11 Multiplexer #1
*76010-*76016	[CSR] DZV11 Multiplexer #2
*76020-*76476	[CSR] (Reserved)
*76500-*76502	[CSR] 8S Channel #1 Input - Reserved
*76504-*76506	[CSR] 8S Channel #1 Output - Reserved
*76510-*76512	[CSR] 8S Channel #2 Input - Reserved
*76514-*76516	[CSR] 8S Channel #2 Output - Reserved
*76520-*76522	[CSR] 8S Channel #3 Input - Reserved
*76524-*76526	[CSR] 8S Channel #3 Output - Reserved
*76530-*76532	[CSR] 8S Channel #4 Input - Reserved

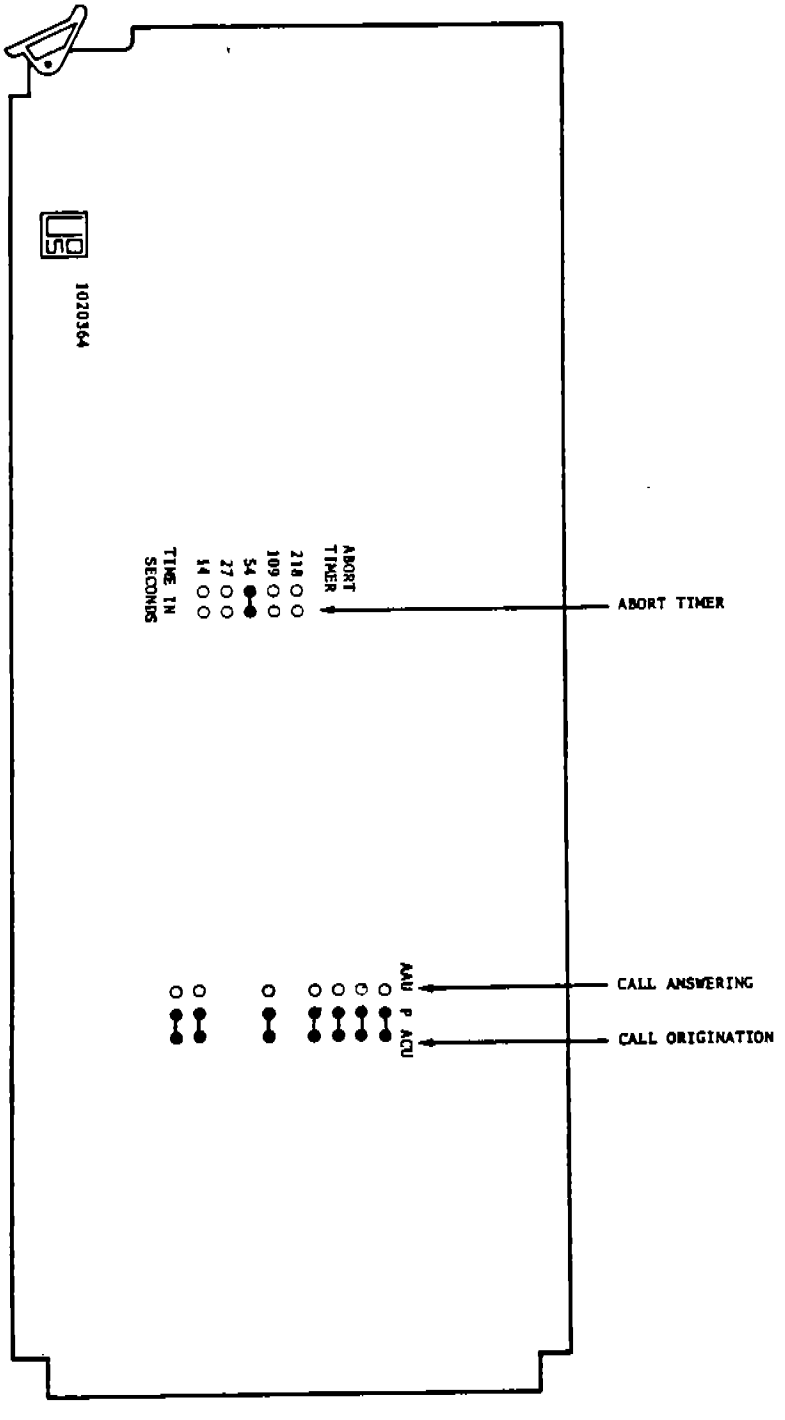
Addresses	Assignment
*76534-*76536	[CSR] 8S Channel #4 Output - Reserved
*76540-*76542	[CSR] 8S Channel #5 Input - TSX-NET
*76544-*76546	[CSR] 8S Channel #5 Output - TSX-NET
*76550-*76552	[CSR] 8S Channel #6 Input - Line Printer
*76554-*76556	[CSR] 8S Channel #6 Output - Line Printer
*76560-*76562	[CSR] 8S Channel #7 Input - Prog. Workstation
*76564-*76566	[CSR] 8S Channel #7 Output - Prog. Workstation
*76570-*76572	[CSR] 8S Channel #8 Input - Reserved (Non-console)
*76574-*76576	[CSR] 8S Channel #8 Output - Reserved (Non-console)
*76600	[CSR] E-Systems Mux #1
*76602	[CSR] E-Systems Mux #2
*76604	[CSR] E-Systems Mux #3 (Reserved)
*76606	[CSR] E-Systems Mux #4 (Reserved)
*76610-*76676	[CSR] (Reserved)
*76700-*76736	[CSR] RM02 Disk (EMULEX SC01)
*76740-*76746	[CSR] (Unassigned)
*76750-*76776	[CSR] (Reserved)
*77000-*77002	[CSR] MRV11-C #1
*77004-*77006	[CSR] MRV11-C #2 (Reserved)
*77010-*77012	[CSR] MRV11-C #3 (Reserved)
*77014-*77016	[CSR] MRV11-C #4 (Reserved)
*77020-*77166	[CSR] (Reserved)
*77170-*77176	[CSR] RXV11 Floppy Disc
*77200-*77276	[CSR] (Reserved)
*77300-*77316	[CSR] Floating Point Operations (Reserved)
*77320-*77512	[CSR] (Reserved)
*77514-*77516	[CSR] LPV11 - Line Printer
*77520-*77526	[CSR] (Unassigned)
*77530-*77544	[CSR] (Reserved)

Addresses	Assignment
*77546	[CSR] KPV11-B Line Time Clock
*77550-*77556	[CSR] (Reserved)
*77560-*77562	[CSR] 8S Console Input
*77564-*77566	[CSR] 8S Console Output
*77570	[CSR] Console Switch Panel (Reserved)
*77572	[CSR] Memory Management Unit SR0
*77574	[CSR] Memory Management Unit SR1
*77576	[CSR] Memory Management Unit SR2
*77600-*77616	[CSR] Memory Management Unit Page Description Registers
*77620-*77636	[CSR] Memory Management Unit (Reserved)
*77640-*77656	[CSR] Memory Management Unit Page Address Registers
*77660-*77676	[CSR] Memory Management Unit (Reserved)
*77700-*77774	[CSR] (Reserved)
*77776	[CSR] Processor Status Word

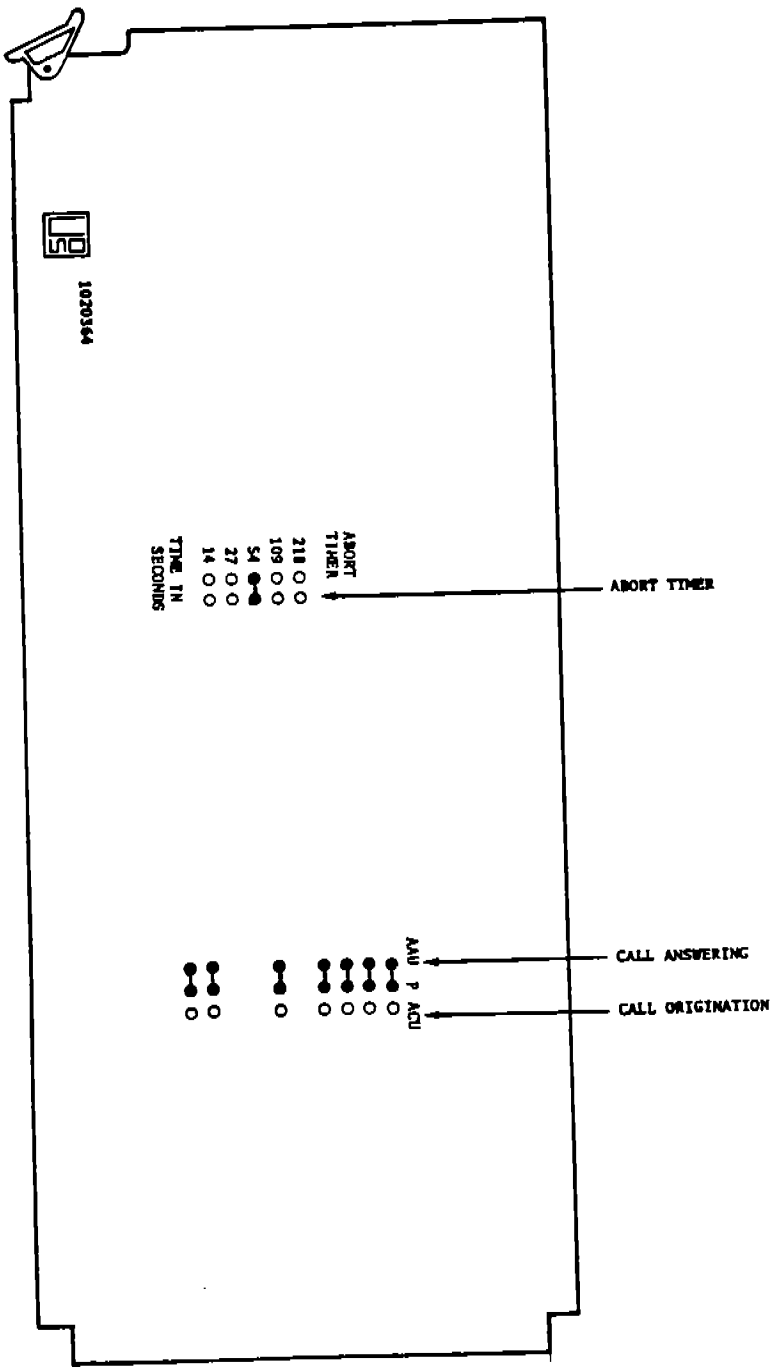
MODEM CODING SPECIFICATIONS

E-AO	Card	P/N	1020364
E-208A	Card	P/N	2082278
E-9600	Card	P/N	2092284
MSD		P/N	2005064
RM8E-9600FP CARD		P/N	2092842

E-AO Card P/N 51020364
JUMPER CONFIGURATION-FSDPS

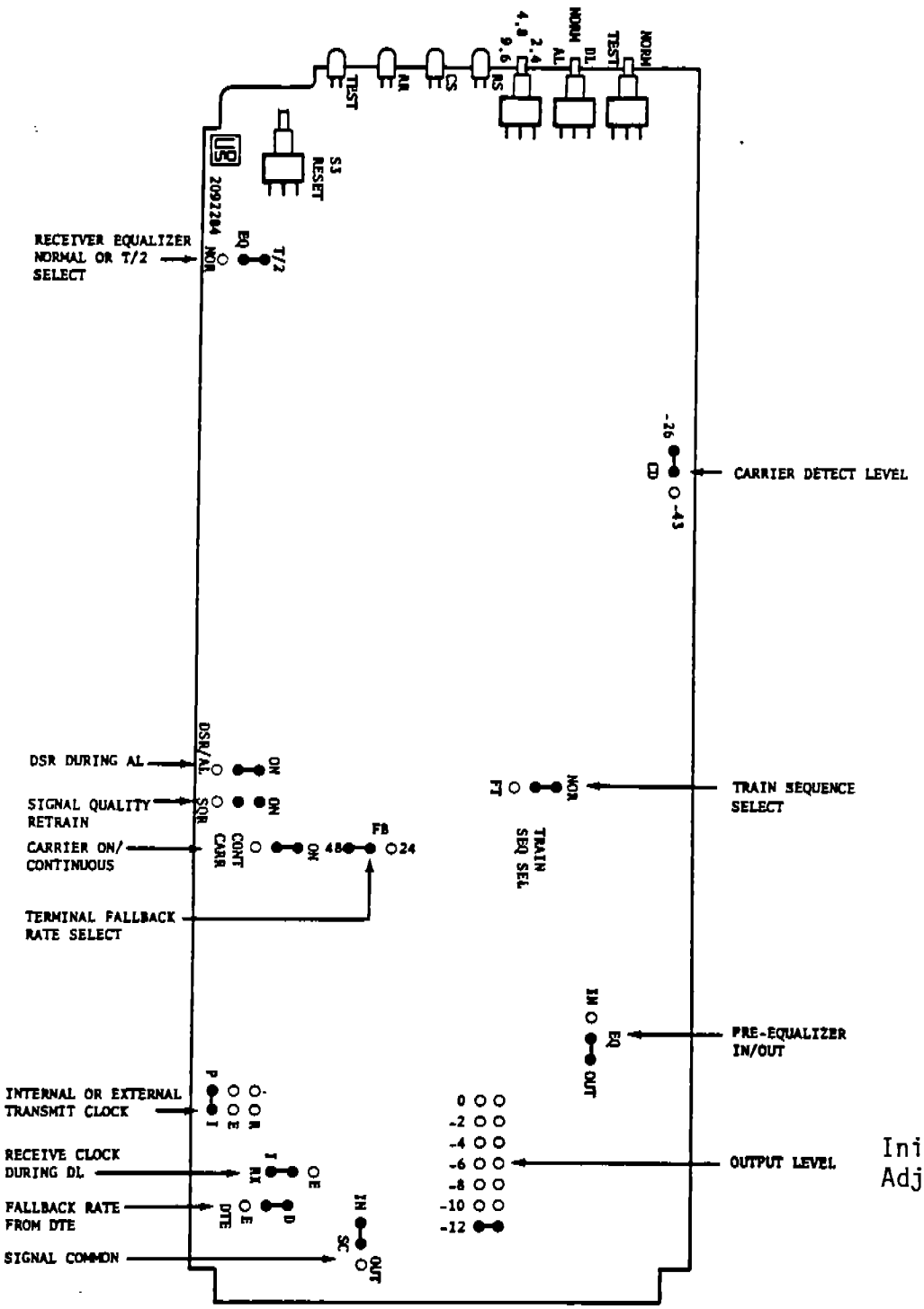


E-AO CARD P/N 51020364
JUMPER CONFIGURATION - AFSS



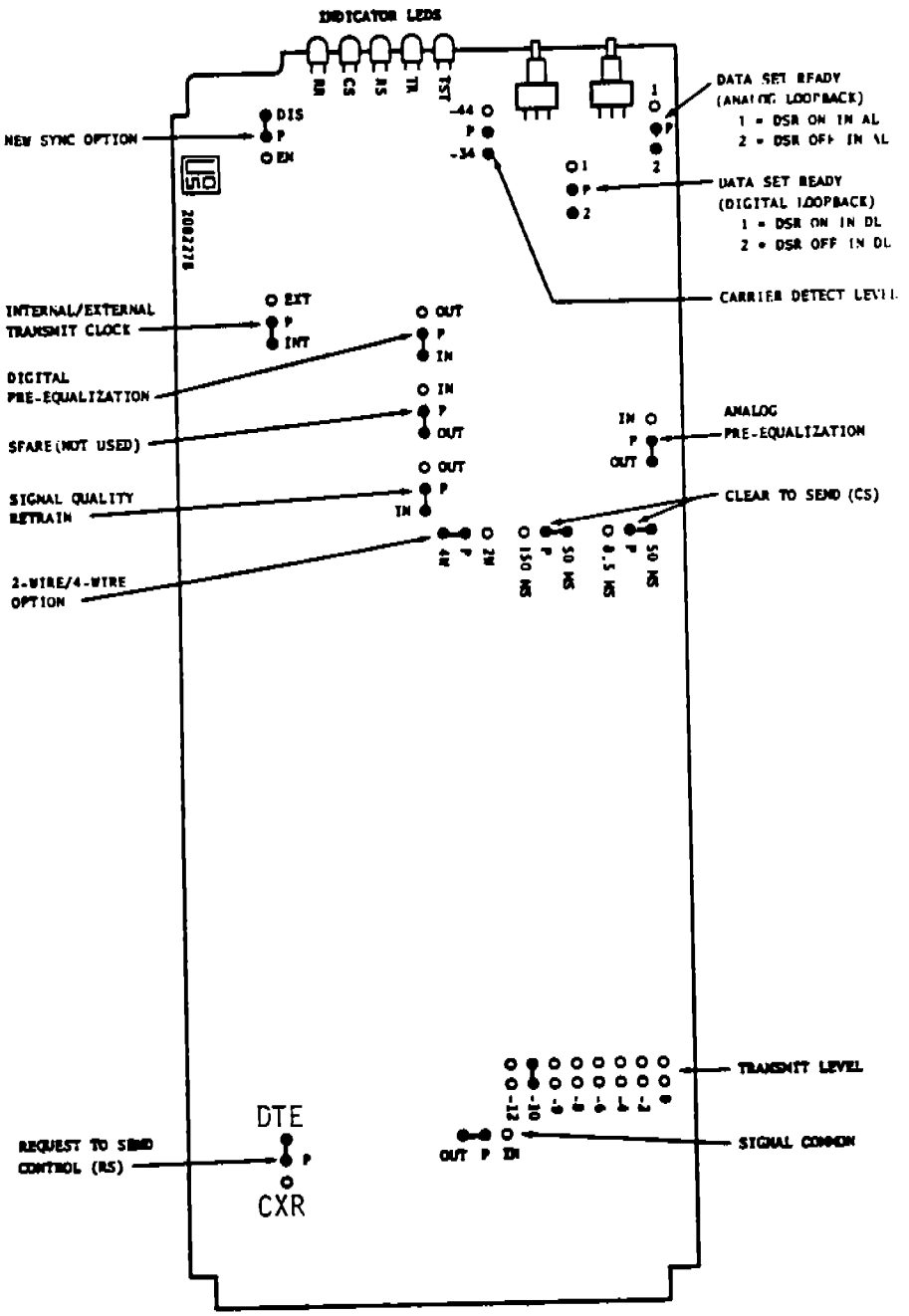
E-9600 Card P/N 52092284

JUMPER CONFIGURATION

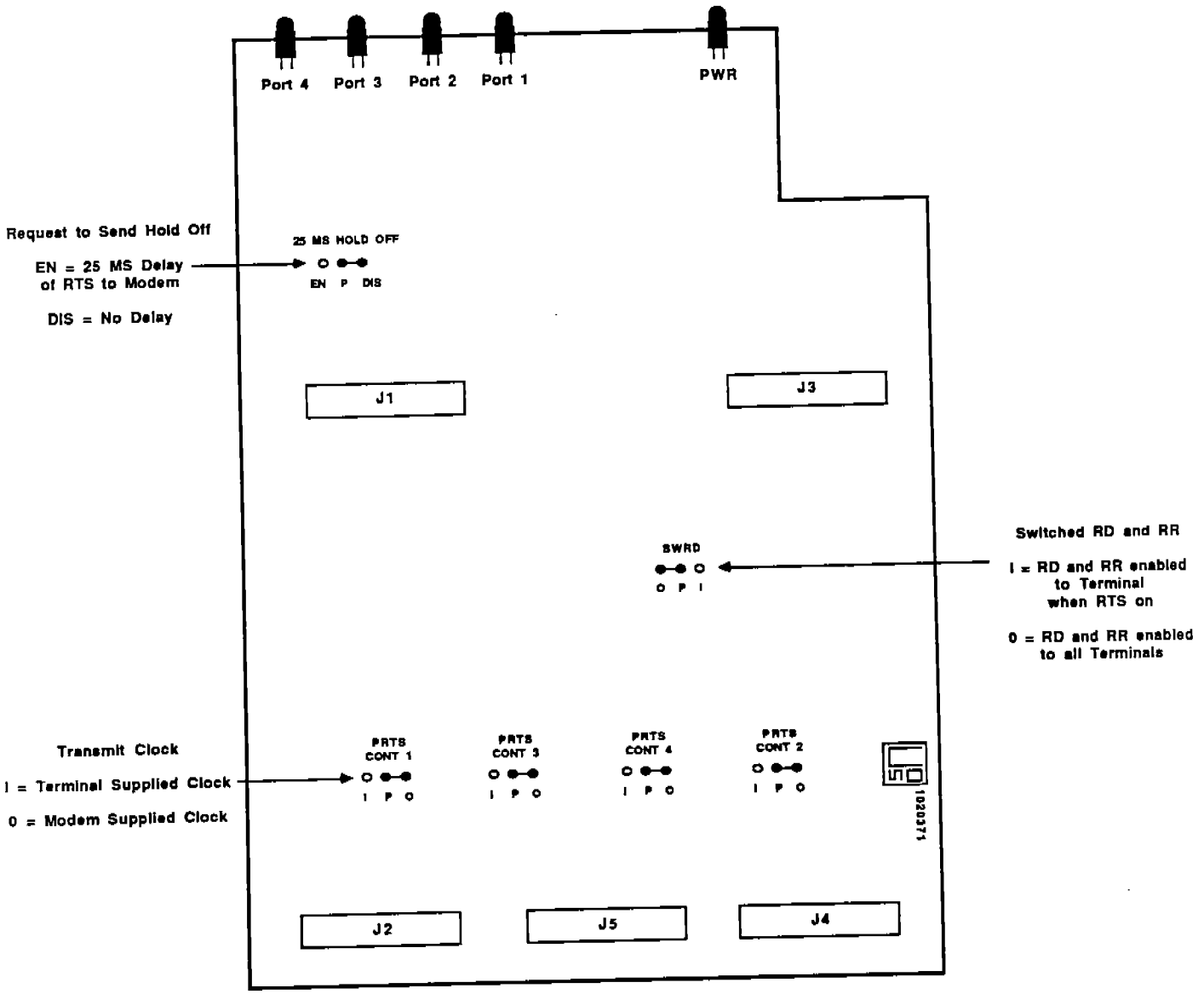


Initial Configuration
Adjust as Necessary

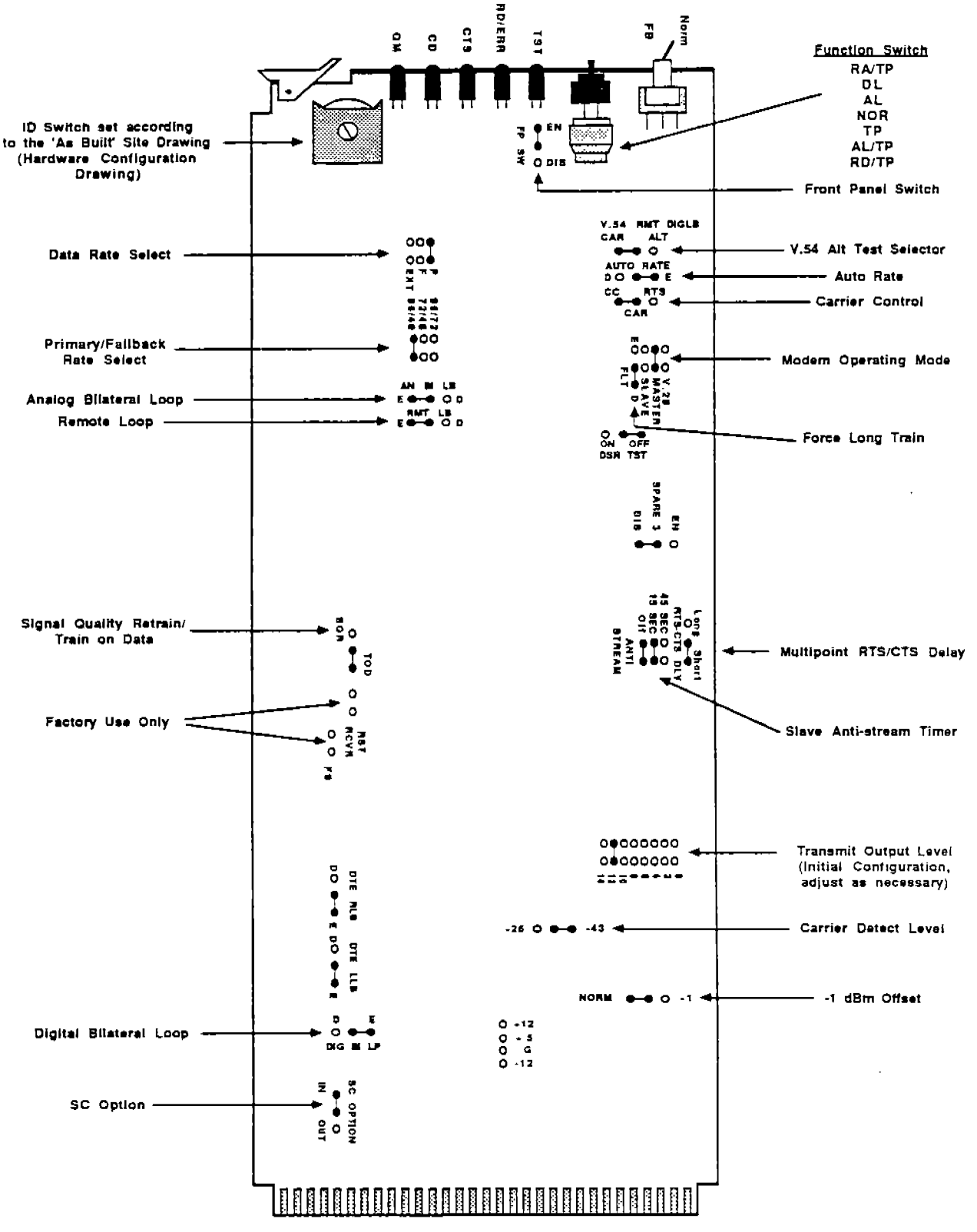
E-208A Card P/N 52082278
JUMPER CONFIGURATION



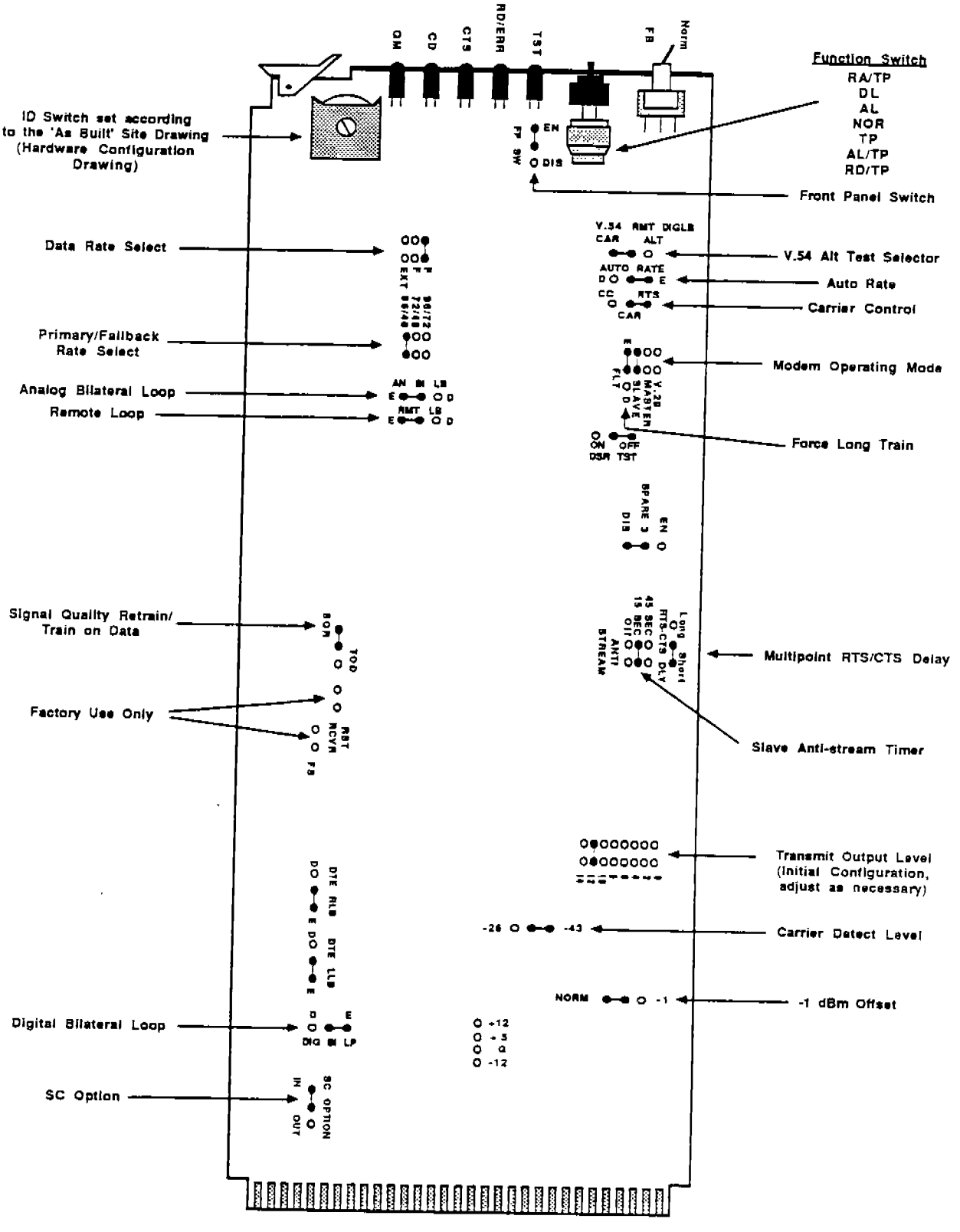
MSD - P/N 52005064
Jumper Configuration



RM8E-9600FP Card - P/N 52092842
Jumper Configuration - Master



RM8E-9600FP Card - P/N 52092842
Jumper Configuration - Slave



CONFIGURATION SPECIFICATIONS

P300 LINE PRINTER

406-02171

INTRODUCTION

Both the Logic A Printed Circuit Board Assembly (PCBA) and the Logic B PCBA have 14-pin DIP platform(s) used to connect jumpers selecting different printer functions.

The RS232 interface on the Data Communications Board provides a switch-controlled self-test feature. In the self-test mode, the interface causes the Printer to print a full-width all-characters pattern to verify correct operation.

To remove the logic PCBAs, swing open the card cage (secured by a magnetic latch at the right-hand end of the cage) through the rear of the Printer. The PCAs are removed using ejector levers built onto the cards and card cage. Access through the rear of the Printer is obtained by releasing two retaining screws and swinging the back panel downward.

The self-test switch on the Data Communications card can be reached without removing the PCBA.

The following pages describe the configuration of the RS232 interface on the Data Communication board and the nominal status of the jumpers on the Logic A and B PCBAs. Figure 1 shows the locations and identification of jumpers on the RS-232 interface. Figures 2-6 shows the location of the jumper platforms on the Logic A and Logic B PCBA.

CONFIGURATION SPECIFICATION P300 LINE PRINTER
JUMPER CONFIGURATION FOR RS-232 BOARD

HYBRID CURRENT LOOP DISABLE - Installed

CURRENT LOOP ENABLE - Removed

DSR - Removed

ACK/NACK PROG. RECD.
CHARACTER - Removed

BIT 8
P1 to GND - Installed
DATA to GND - Installed

CURRENT LOOP OUT
A (both places) - Installed

REQ TO SEND

		AFSS	FSDPS
IONL	-	Installed	Removed
BSY	-	Removed	Removed
NSBY	-	Removed	Installed

DTR
BSY - Installed

DATA TRANSMIT
TOB - Installed

REVERSE CHANNEL
NBSY - Installed

BAUD RATE
9.6K - Installed

CURRENT LOOP OUT		
	TOB	- Installed
2K BUFF		- Removed
ODD PARITY		
	PAR ENAB	- Installed
	128	- Installed
	512	- Installed
BAFL		
	HYS	- Installed
	DIS PAR ERR	- Removed
2K BUF		- Removed
1024 BAFL		- Removed
ON-ACK		
		8 Installed
		1 Removed
		7 Installed
		2 Installed
		6 Installed
		3 Installed
		5 Removed
		4 Installed
OFF-NACK		
		8 Installed
		1 Removed
		7 Installed
		2 Removed
		6 Installed
		3 Installed
		5 Removed
		4 Installed

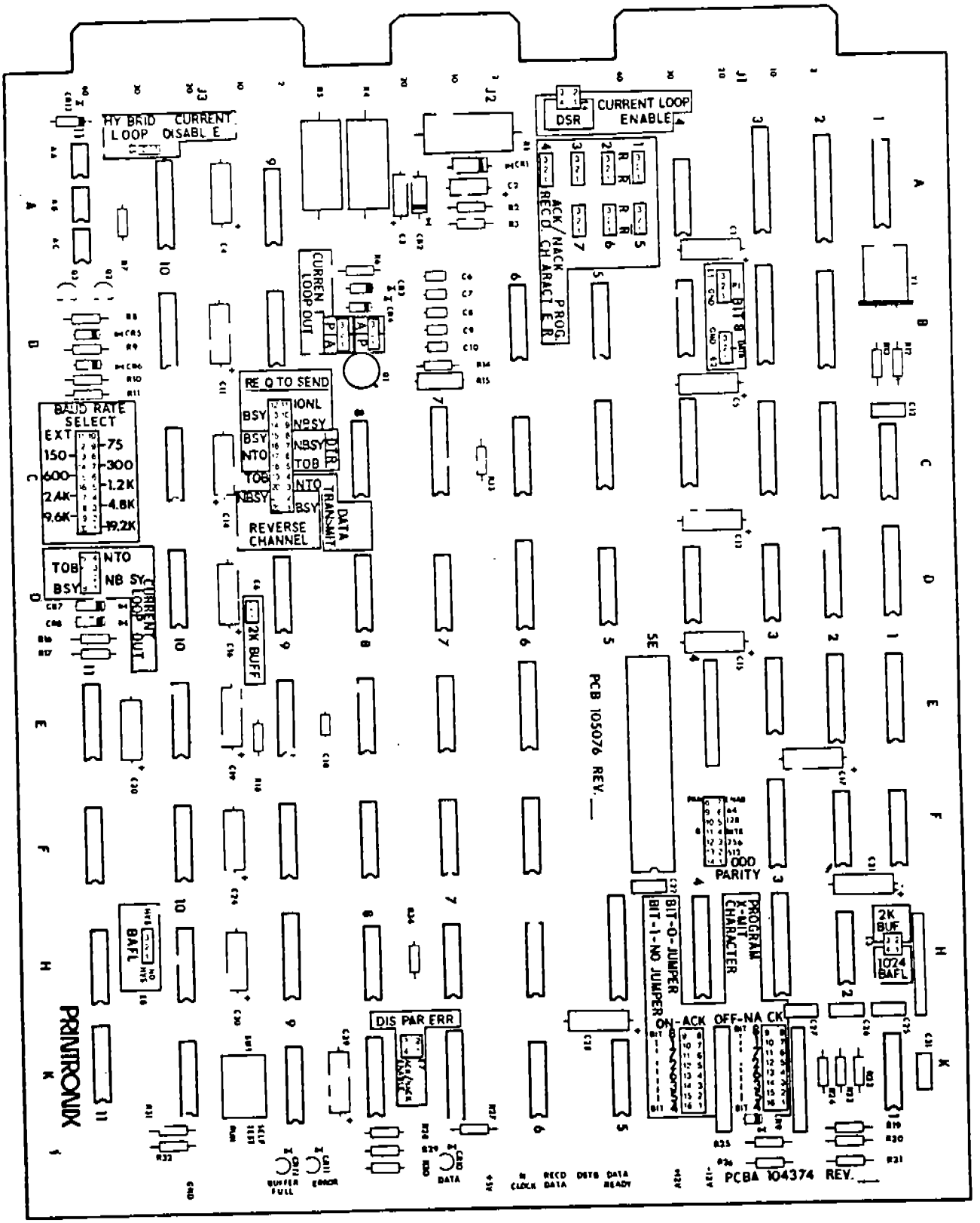


Figure 1. LOCATION DRAWING OF RS-232 INTERFACE

LOGIC A PRINTED CIRCUIT BOARD ASSEMBLY - A1
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
Auto Line Feed	W1	8K	1-14	Omit
Line Feed With Carriage Return	W2	8K	2-13	Omit
Underline	W3	8K	3-12	Omit
Data Line 8	W4	8K	4-11	Connect
VFU Control (P1)	W5	8K	5-10	Connect: P1 Line Not Used
Upper-Case Enable	W6	8K	6-9	Connect: Lower-Case PROM Removed (IC's F1 and F2)
Polarity Select	W7	8K	7-8	Omit: High-True Interface

LOGIC B PRINTED CIRCUIT BOARD ASSEMBLY - B4
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
Skip-over perforation	W1	8K	1-14	Omit
	W2	8K	2-13	Omit
	W3	8K	3-12	Connect: Sets skip-over distance
Plotting Speed	W4	8K	4-11	Omit: Disable double speed plotting at lower densities
(Not assigned)	W5	8K	5-10	Omit
Paper motion detector	W6	8K	6-9	Connect: Factory Installed
VFU Disable	W7	8K	7-8	Omit: Enables all VFU functions
6LPI/8LPI	W9	10A	2-13	Connect
	W10	10A	3-12	Omit
	W13	10A	6-9	Connect
	W14	10A	7-8	Omit: Enables 8LPI
Paper Out (12)	W11	10A	4-11	Connect
Skip-over Perforation	W12	10A	5-10	Connect
Location 11A	W15	11A	A-B	Omit: 8LPI/6LPI
8LPI (10LPI) only				Software Selected
Paper-out Delay	W27	11K	6-9	Omit
Override	W28	11K	7-8	Connect: Enable printing of last two inches of last form.

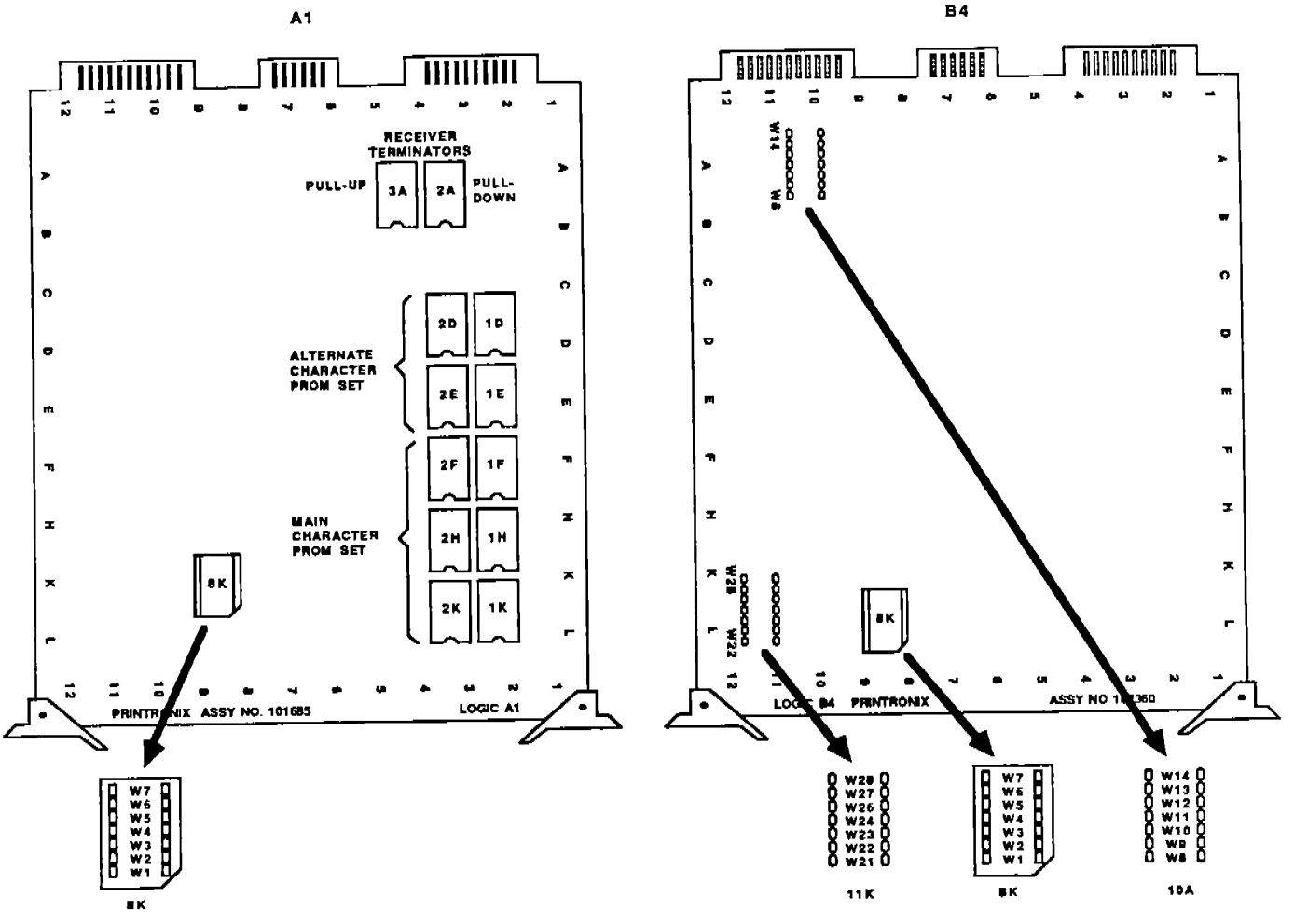


FIGURE 2
LOGIC PCBAs A1, B4

LOGIC A PRINTED CIRCUIT BOARD ASSEMBLY - A2
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
Auto Line Feed	W1	8K	1-14	Omit
Line Feed With Carriage Return	W2	8K	2-13	Omit
Underline	W3	8K	3-12	Omit
Data Line 8	W4	8K	4-11	Connect
VFU Control (P1)	W5	8K	5-10	Connect: P1 Line Not Used
Upper-Case Enable	W6	8K	6-9	Connect: Lower-Case PROM Removed (IC's F1 and F2)
Polarity Select	W7	8K	7-8	Omit: High-True Interface
Half Dot Disable	W9	9K	2-13	Omit
P300	W14	9K	7-8	Omit

LOGIC B PRINTED CIRCUIT BOARD ASSEMBLY - B5
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
Skip-over perforation	W1	8K	1-14	Omit
	W2	8K	2-13	Omit
	W3	8K	3-12	Connect: Sets skip-over distance
Plotting Speed	W4	8K	4-11	Omit: Disable double speed plotting at lower densities
(Not assigned)	W5	8K	5-10	Omit
Paper motion detector	W6	8K	6-9	Connect: Factory Installed
VFU Disable	W7	8K	7-8	Omit: Enables all VFU functions
6LPI/8LPI	W8	9K	1-14	Omit
6LPI/8LPI	W9	9K	2-13	Omit
Move 1 Line	W12	9K	5-10	Omit
P300	W13	9K	6-9	Connect
Paper-out Delay Override	F1 to F2			Omit: Enable printing of last two inches of last form.

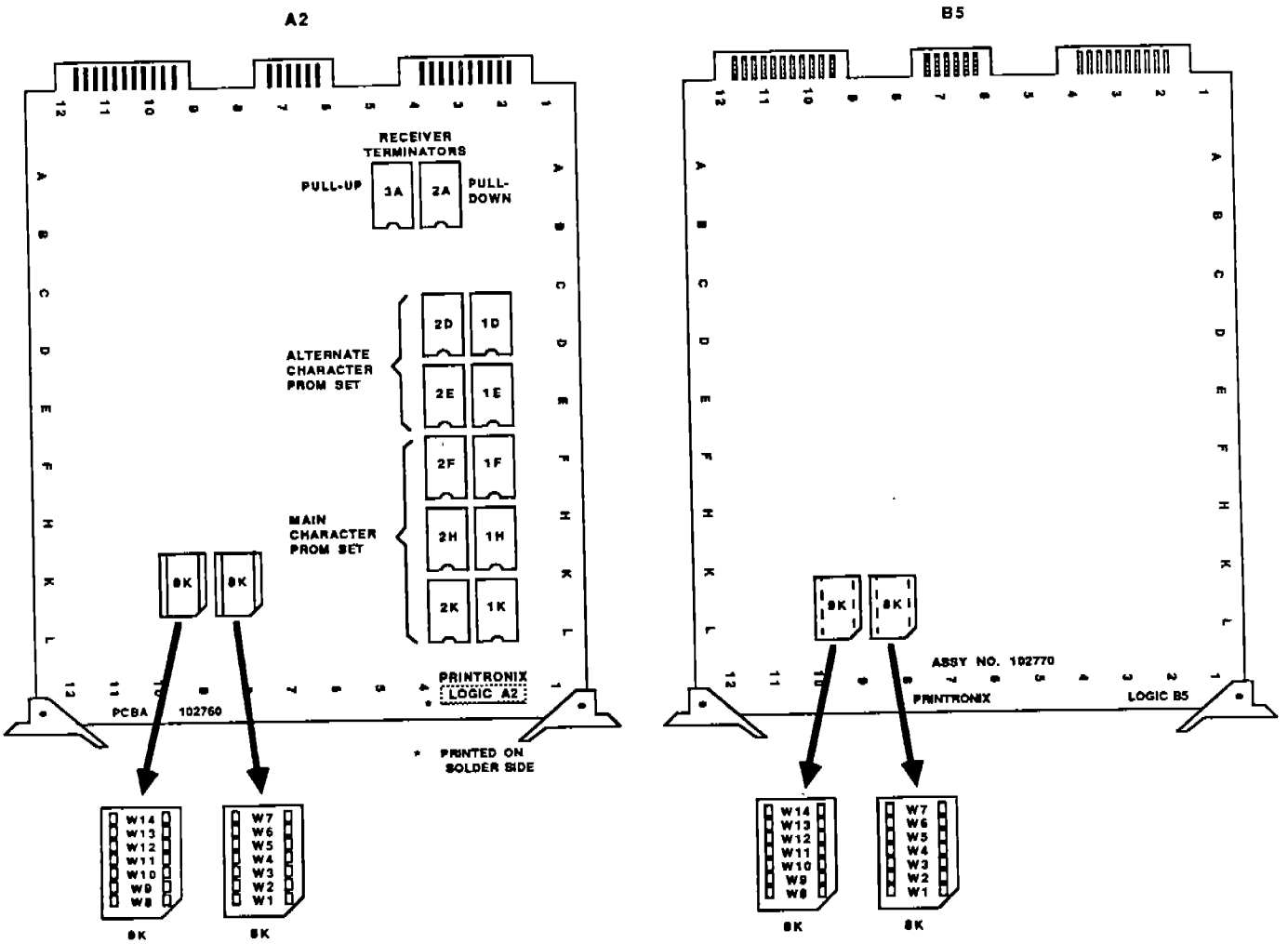


FIGURE 3
LOGIC PCBAs A2, B5

LOGIC A PRINTED CIRCUIT BOARD ASSEMBLY - A4
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
P600--Enable	W1	8K	1-14	Connect: P600
Data Strobe Polarity	W2	8K	2-13	Omit
Underline	W3	8K	3-12	Omit
Data line 8	W4	8K	4-11	Connect
VFU Control (P1)	W5	8K	5-10	Connect: P1 Line Not Used
Upper-Case Enable	W6	8K	6-9	Connect: Lower-Case PROM Removed (IC's F1 and F2)
Polarity Select	W7	8K	7-8	Omit: High-True Interface
N/A	W8	9K	1-14	
Half Dot Disable	W9	9K	2-13	Omit
N/A	W10	9K	3-12	
P300	W11	9K	4-11	Connect
Auto Line Feed	W12	9K	5-10	Omit
Line Feed with Carriage Return	W13	9K	6-9	Omit
P300	W14	9K	7-8	Omit

LOGIC B PRINTED CIRCUIT BOARD ASSEMBLY - B7
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
Skip-over Perforation	W1	8K	1-14	Omit
	W2	8K	2-13	Omit
	W3	8K	3-12	Connect: Sets skip-over distance
Plotting Speed	W4	8K	4-11	Omit: Disable double speed plotting at lower densities
P300	W5	8K	5-10	Omit
Paper motion detector	W6	8K	6-9	Connect: Factory Installed
VFU Disable	W7	8K	7-8	Omit: Enables all VFU functions
6LPI/8LPI	W8	9K	1-14	Omit
6LPI/8LPI	W9	9K	2-13	Omit
P300	W11	9K	4-11	Connect
Move 1 Line	W12	9K	5-10	Omit
P300	W13	9K	6-9	Connect
P300	W14	9K	7-8	Connect
Paper-out Delay Override	F1 and F2			Omit: Enable printing of last two inches of last form.

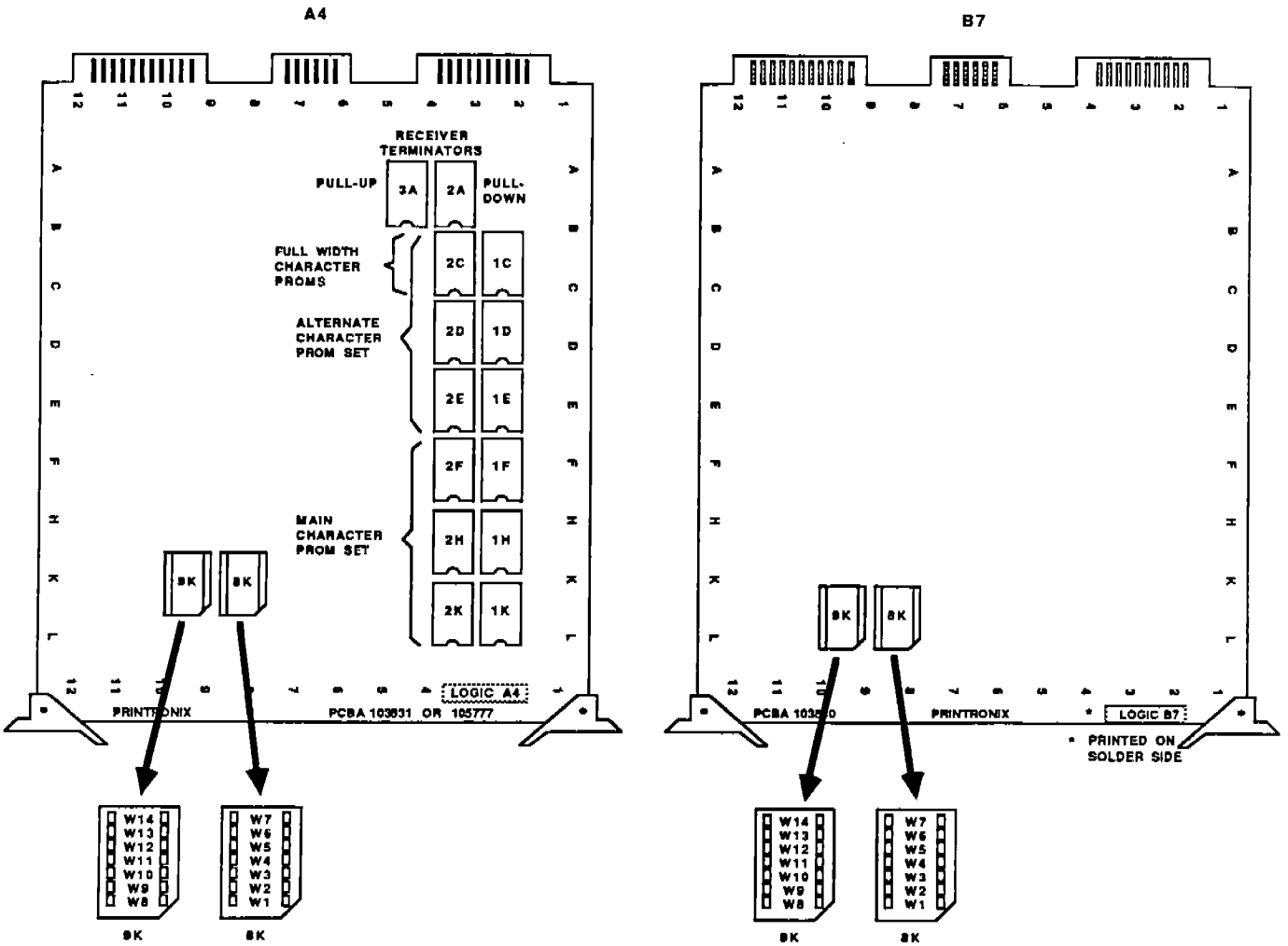


FIGURE 4
LOGIC PCBAs A4, B7

LOGIC A PRINTED CIRCUIT BOARD ASSEMBLY - A6
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
P600--Enable	W1	8K	1-14	Omit
Data Strobe Polarity	W2	8K	2-13	Omit
Underline	W3	8K	3-12	Omit
Data line 8	W4	8K	4-11	Connect
VFU Control (P1)	W5	8K	5-10	Connect: P1 Line Not Used
Upper-Case Enable	W6	8K	6-9	Connect: Lower-Case PROM Removed (IC's F1 and F2)
Polarity Select	W7	8K	7-8	Omit: High-True Interface
N/A	W8	9K	1-14	
Half Dot Disable	W9	9K	2-13	Omit
7-8 Dot Rows	W10	9K	3-12	Omit
P300	W11	9K	4-11	Connect
Auto Line Feed	W12	9K	5-10	Omit
Line Feed with Carriage Return	W13	9K	6-9	Omit
P300	W14	9K	7-8	Omit
Main Socket	W15	7A	1-14	Omit
Alt Socket	W16	7A	2-13	Omit

LOGIC B PRINTED CIRCUIT BOARD ASSEMBLY - B9
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
Skip-over Perforation	W1	8K	1-14	Omit
	W2	8K	2-13	Omit
	W3	8K	3-12	Connect: Sets skip-over distance
Plotting Speed	W4	8K	4-11	Omit: Disable double speed plotting at lower densities
P300	W5	8K	5-10	Omit
Paper motion detector	W6	8K	6-9	Connect: Factory Installed
VFU Disable	W7	8K	7-8	Omit: Enables all VFU functions
6LPI/8LPI	W8	9K	1-14	Omit
6LPI/8LPI	W9	9K	2-13	Omit
P300	W11	9K	4-11	Connect
Move 1 Line	W12	9K	5-10	Omit
P300	W13	9K	6-9	Connect
P300	W14	9K	7-8	Connect
Paper-out Delay Override	E13 to E14			Connect: Enable printing of last two inches of last form.

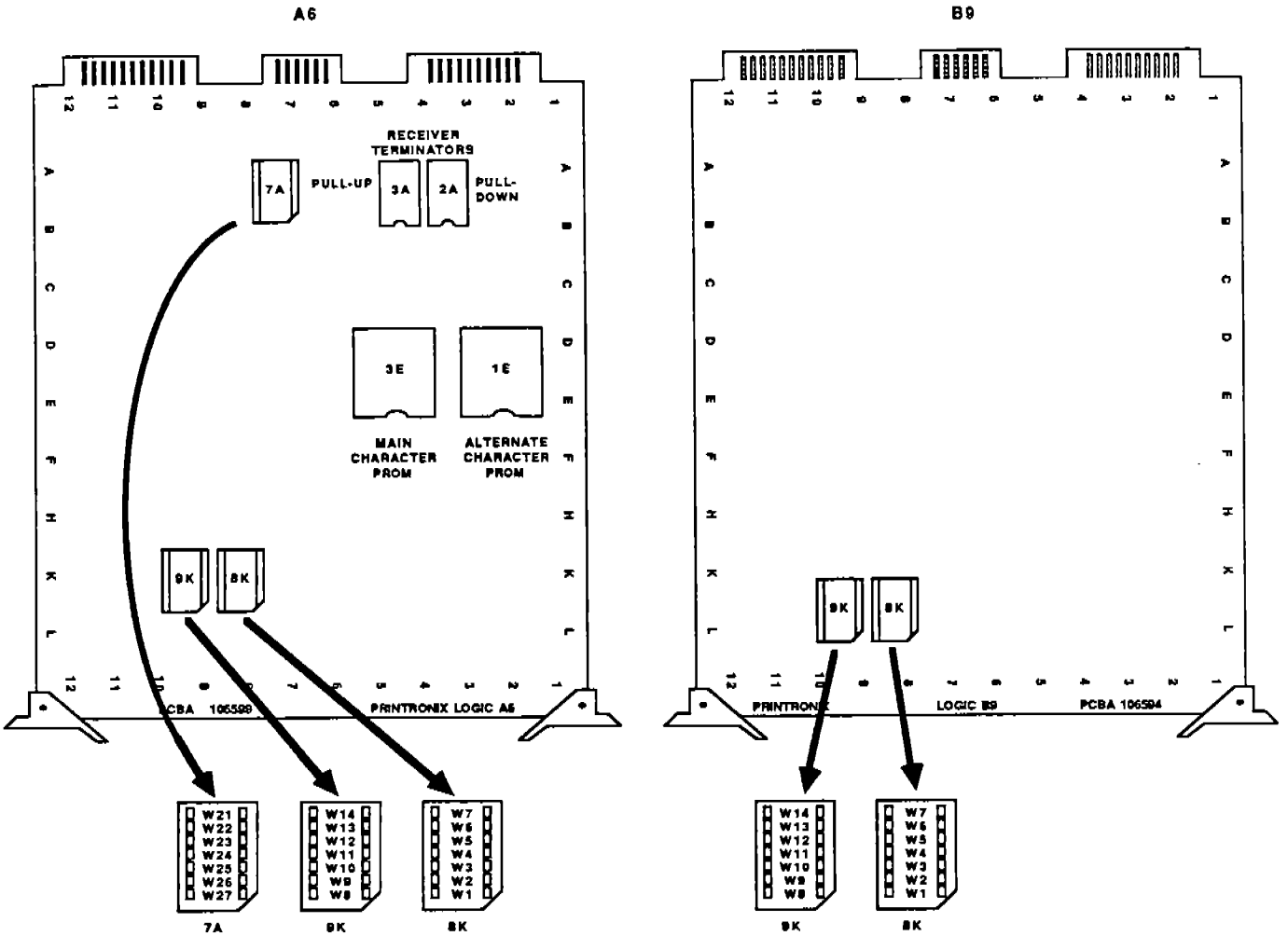


FIGURE 5
LOGIC PCBAs A6, B9

LOGIC B PRINTED CIRCUIT BOARD ASSEMBLY - A9
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
P600--Enable	W1	9A	1-14	Connect: P600
Data Strobe Polarity	W2	9A	2-13	Omit
Underline	W3	9A	3-12	Omit
Data line 8	W4	9A	4-11	Connect
VFU Control (P1)	W5	9A	5-10	Connect: P1 Line Not Used
Upper-Case Enable	W6	9A	6-9	Connect: Lower-Case PROM Removed (IC's F1 and F2)
Polarity Select	W7	9A	7-8	Omit: High-True Interface
N/A	W8	12F	1-14	
Half Dot Disable	W9	12F	2-13	Omit
7-8 Dot Rows	W10	12F	3-12	Omit
P300	W11	12F	4-11	Connect
Auto Line Feed	W12	12F	5-10	Omit
Line Feed with Carriage Return	W13	12F	6-9	Omit
P300	W14	12F	7-8	Omit
Main Socket	W15	1H	1-14	Omit
Alt Socket	W16	1H	2-13	Omit
Normal Print	W17	1H	3-12	Omit
Normal Print	W18	1H	4-11	Omit
Alt. Comp Print	W19	1H	5-10	Omit
132 Enable Jumper	W21	1H	7-8	Omit

LOGIC B PRINTED CIRCUIT BOARD ASSEMBLY - B10
P300 LINE PRINTER

FUNCTION	JUMPER	LOCATION	PINS	EXPLANATION
Skip-over Perforation	W1	12C	1-14	Omit
	W2	12C	2-13	Omit
	W3	12C	3-12	Connect: Sets skip-over distance
Plotting Speed	W4	12C	4-11	Omit: Disable double speed plotting at lower densities
P300	W5	12C	5-10	Omit
Paper motion detector	W6	12C	6-9	Connect: Factory Installed
VFU Disable	W7	12C	7-8	Omit: Enables all VFU functions
6LPI/8LPI	W8	4H	1-14	Omit
6LPI/8LPI	W9	4H	2-13	Omit
P300	W11	4H	4-11	Connect
Move 1 Line	W12	4H	5-10	Omit
P300	W13	4H	6-9	Connect
P300	W14	4H	7-8	Connect
Paper-out Delay Override	E13 to E14			Connect: Enable printing of last two inches of last form.

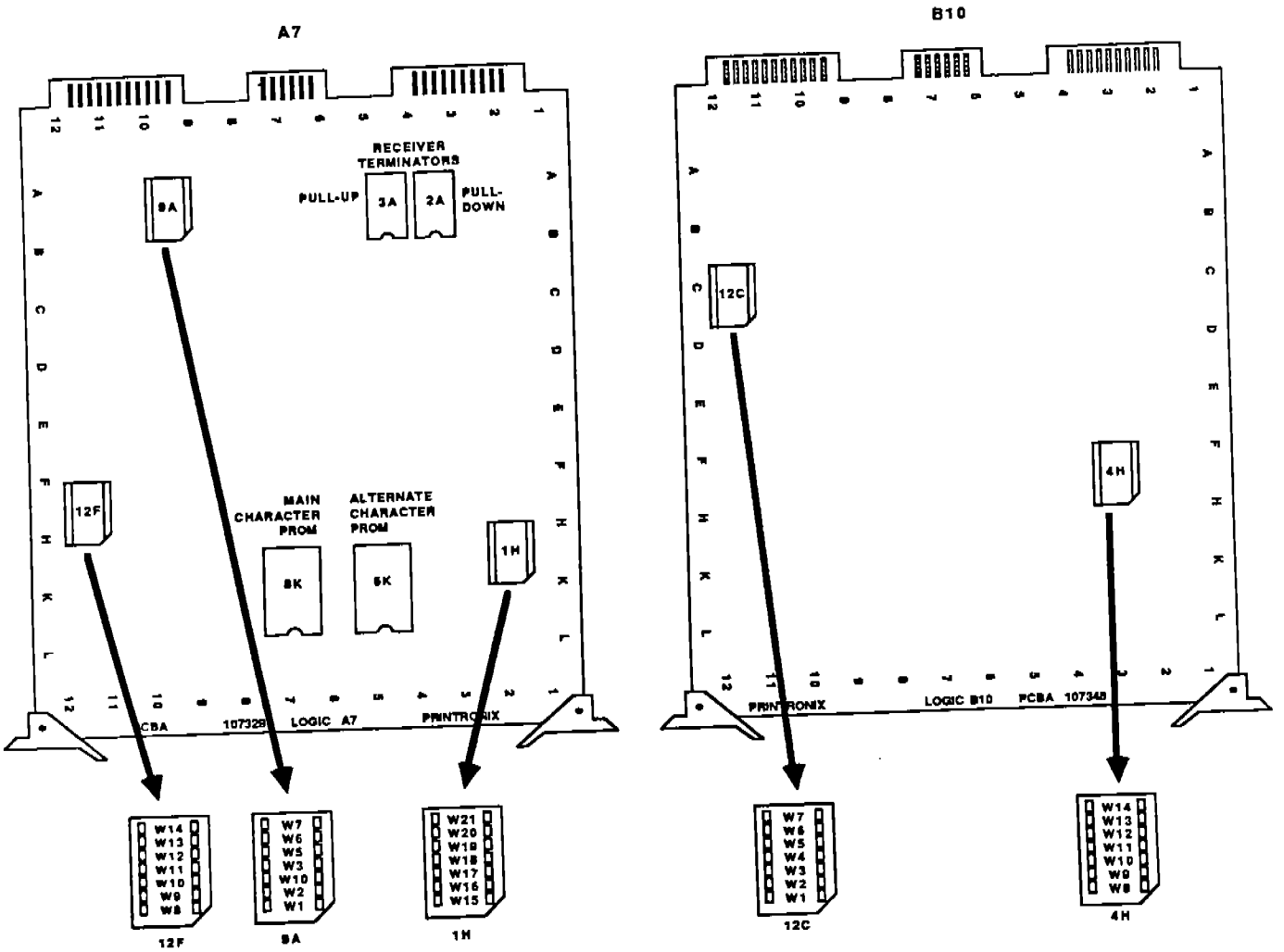


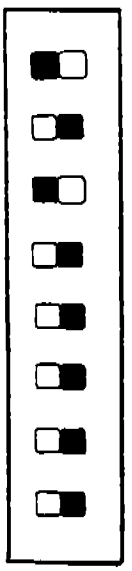
FIGURE 6
LOGIC PCBAs A7, B10

CONFIGURATION SPECIFICATION

I/O CHARACTER PRINTER

DEC LA34-AA

SWITCH SETTINGS



F202-144

1 - PARITY = ENABLED

2 - ODD/EVEN = EVEN

3 - X/ON-X/OFF = ENABLED

4 - ANSI NL = DISABLED

5 - AUTO LF = DISABLED

6 - L ECHO = DISABLED

7 - PAPER OUT PAPER LO

8 - PAPER OUT B PAPER OUT A

NOTE: SWITCH IS ACCESSED THROUGH OPENING UNDER PRINT HEAD.

CONFIGURATION SPECIFICATION

DISK DRIVE

AMPEX DM9300TDQ

CONFIGURATION SPECIFICATION
AMPEX DISK DRIVE DM9300TDQ
DUAL PORT OPERATION

NOTE: This circuit card assembly and the DATA I/O connectors are factory configured. Use this for validation only.

JUMPER CONFIGURATION

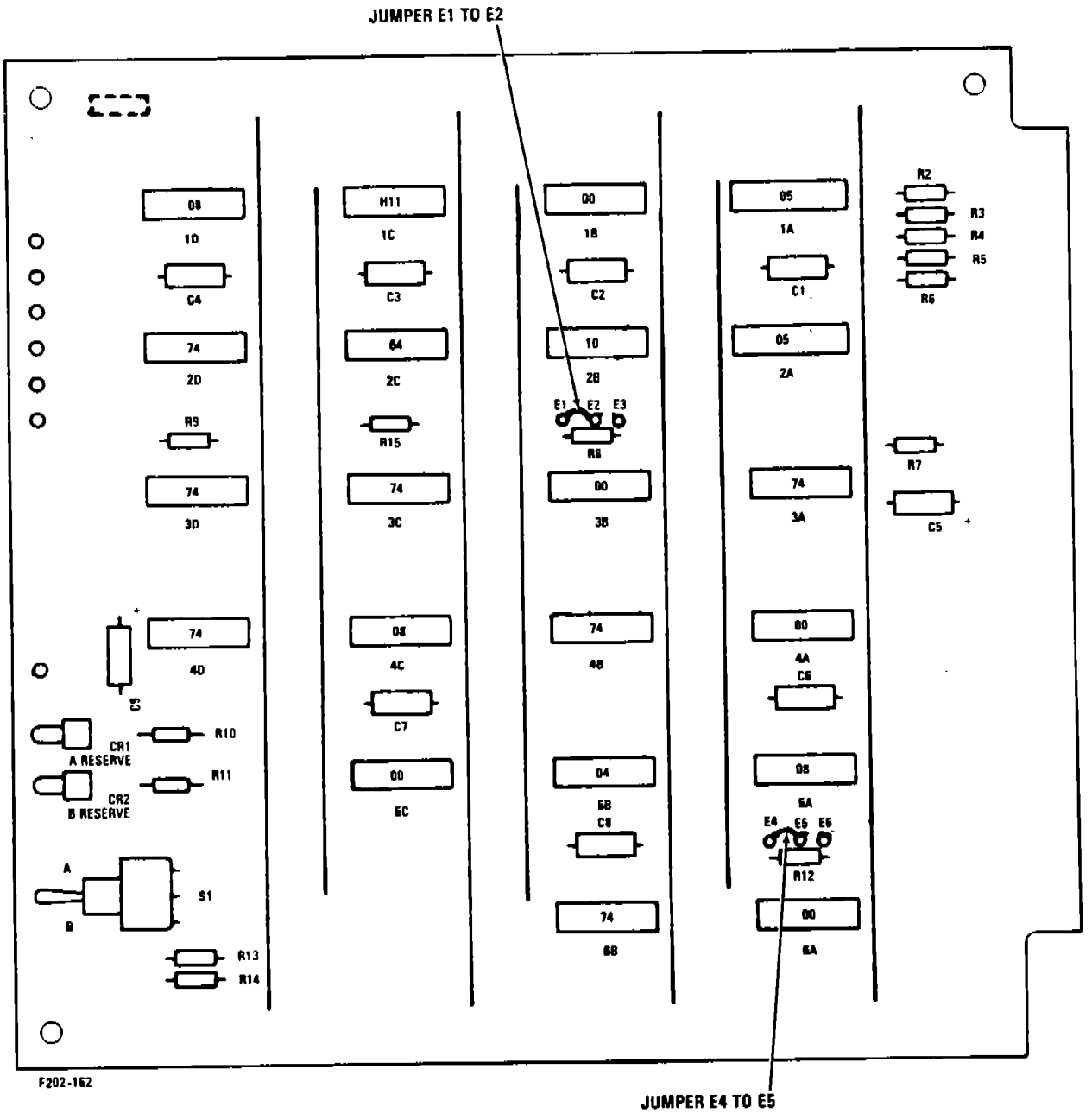
Port Control Circuit Card B12

E2 to E3 - Remove
E5 to E6 - Remove
E1 to E2 - Install
E4 to E5 - Install

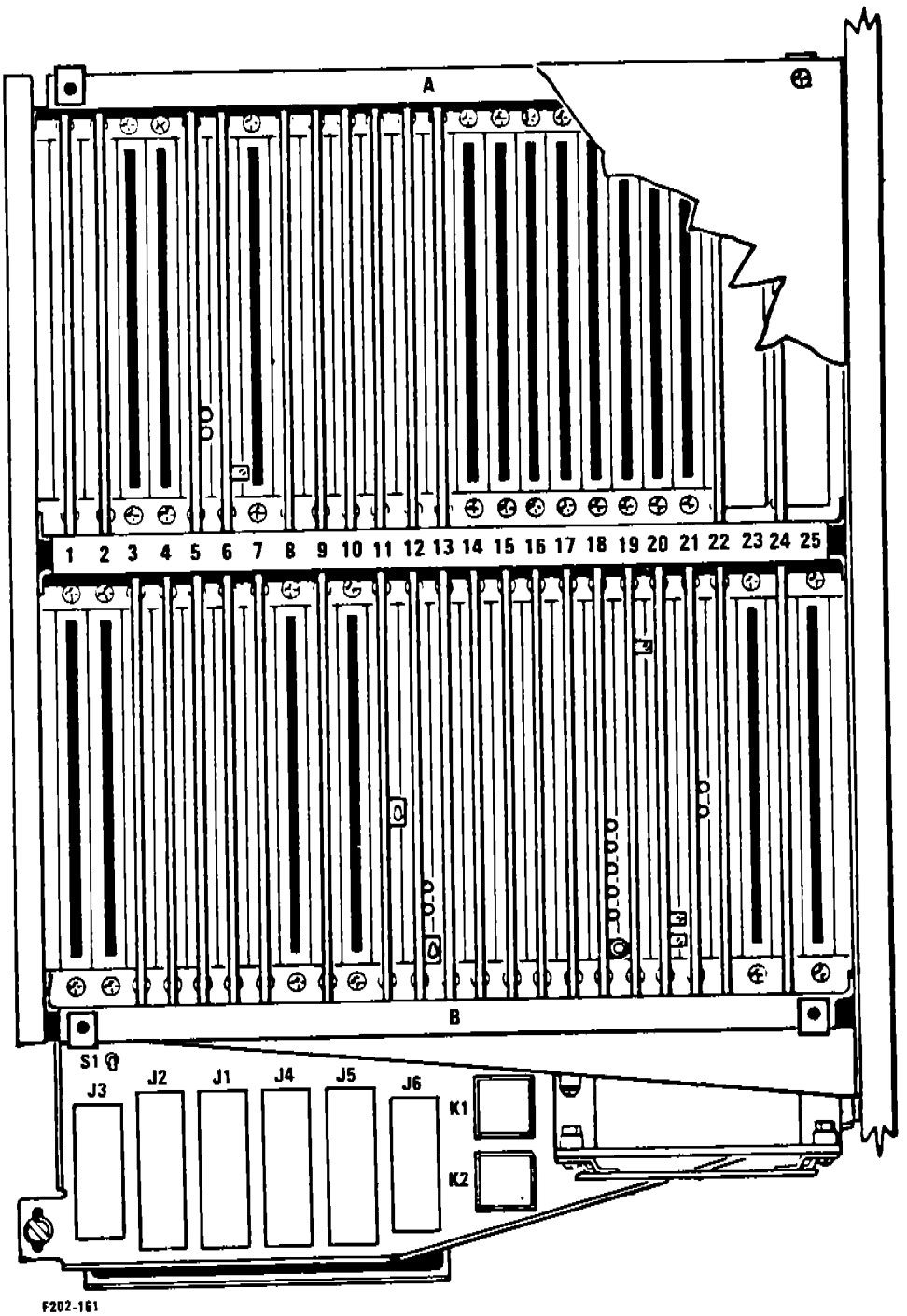
Data I/O Connectors

J3 pin G to ground - Install
J6 pin G to ground - Install

JUMPER CONFIGURATION
PORT CONTROL CARD B12



CARD CAGE AND DATA I/O CONNECTORS
DM9300TDQ



CONFIGURATION SPECIFICATION

LETTER WRITER

DEC LA100-CA

GENERAL

Letterwriter 100 terminals have many operator-selectable features (SET-UP features) that allow you to configure the terminal to meet specific applications. These features allow the terminal to handle different forms or provide computer or communication system compatibility.

This Configuration Specification defines the SET-UP for FSAS Model 1 Full Capacity.

SET-UP

The operator-selectable features can be changed only while the terminal is in SET-UP. Five steps usually are required to change or select a SET-UP feature.

1. Enter SET-UP
2. Print a status message to check feature settings
3. Change a feature such as tabs, baud rate, etc.
4. Store the feature if desired
5. Exit SET-UP

Note: Storing a feature saves it for future use. Refer to the Feature Memories section in this chapter for more detail.

The terminal can enter SET-UP while on-line or local. However, to prevent data loss while the terminal is on-line, enter SET-UP only while the computer is not transmitting characters.

When changing more than one SET-UP feature, it is not necessary to enter and exit SET-UP each time. Also, if you press a key that has no function in SET-UP when changing a SET-UP feature, the terminal prints a question mark (?) and a bell tone rings.

The Letterwriter 100 terminal does not use two communication switches (Figure 1) for feature selection. They must be set to the left position to allow selection through the keyboard.

ENTER SET-UP

	Procedure	Indication/Comment
Perform the following procedure to enter SET-UP.	Press and hold CTRL down. Then press SET-UP and release both keys.	SET-UP indicator flashes, indicating terminal is in SET-UP.

Now you can change any SET-UP feature.

CAUTION

Always use a small blade screwdriver, ballpoint pen, or equivalent to change a switch selectable feature. Never use a lead pencil.

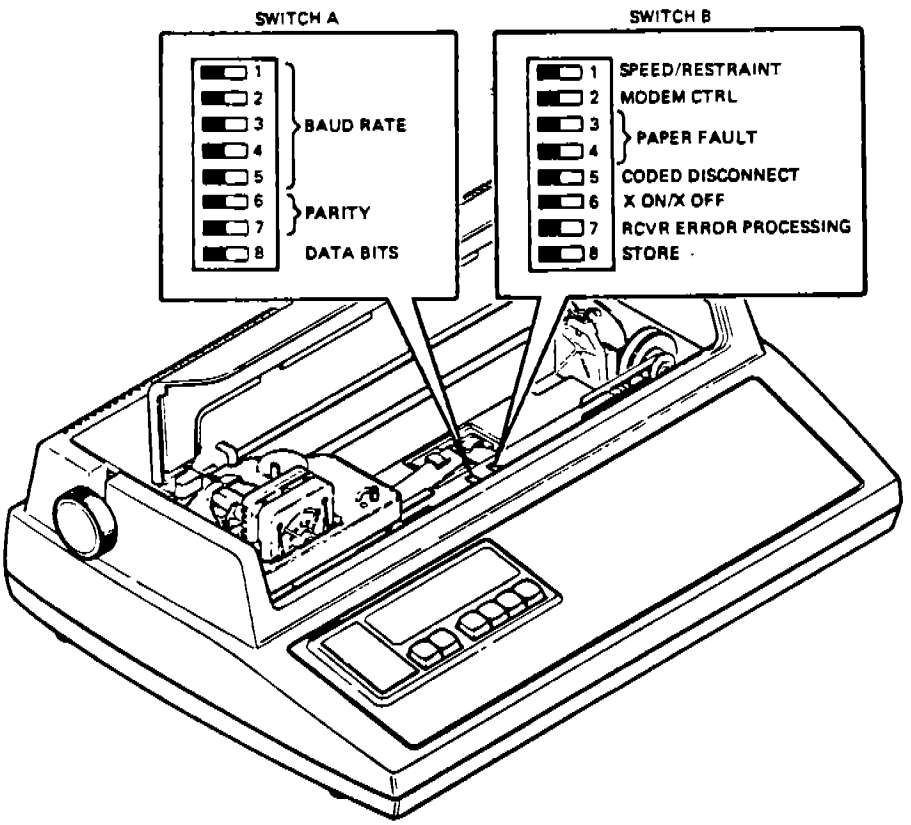


Figure 1 Communication Switches

RECALL DEFAULT SETTINGS

The Letterwriter 100 has default settings stored in non-volatile memory. Prior to changing the SET-UP the default settings should be stored in the operating memory to provide a known baseline (See Table I).

	Procedure	Indication/Comment
Perform the following procedure to recall the default settings.	I Return	Resets the features in operating memory to default memory settings.

PARITY AND DATA BITS

The parity and data bits procedure selects two separate but related features, data bits per character and parity. The data bits per character can be set to 7 or 8 data bits per character. Parity selects the type of parity bit that the terminal generates for transmitted and received characters. (Also see Receiver Error Processing).

	Procedure	Indication/Comment
Perform the following procedure to change the parity or data bit feature.	Press P RETURN	To select: Prints selections and current setting.
	P = B RETURN	Even parity, 7 data bits
Perform the following procedure to set the baud rate.	Press S RETURN	To select: Prints available selections and current setting.
	S = G RETURN	300 Baud

USER PERMANENT MEMORY

User permanent memory stores operator-selected features. The computer cannot change the features stored in user permanent memory. You can change the features in user permanent memory by changing the feature and performing a store while in SET-UP. You can enter the features from user permanent memory into operating memory by performing a recall. When power to the terminal is turned on, the features in user permanent memory are entered automatically into the operating memory.

Note: Retaining information in the permanent memories requires no power or batteries.

The following paragraph describes the store procedure.

STORE

Enters the operating memory features into user permanent memory. Storing features can be performed from the keyboard only. The computer cannot store features.

	Procedure	Indication/Comment
Perform the following procedure to store the features into user permanent memory.	While pressing SHIFT press (9	Stores features in operating memory in user permanent memory. SET-UP indicator stays on for approximately 9 seconds. When SET-UP indicator starts to flash again, store is complete.
	Press SET-UP to exit SET-UP	SET-UP indicator stops flashing.

For additional information, refer to the "Letterwriter 100 Operator Guide", Chapter 3.

TABLE I
FEATURE DEFAULT VALUES

Feature	Default Value
Last character view	Automatic last character view
Keyclick	Off
Horizontal pitch	10 characters per inch
Left margin	Column 1 (first printable column)
Right margin	Column 132
Horizontal tabs	One tab stop every 8 columns
Vertical pitch	6 lines per inch
Form length	11 inches
Top margin	At 0 inch
Bottom margin	At 11th inch
Vertical tab stops	Tab stops set every line
Parity and data bits	Space parity/7 data bits
Receiver error processing	Check for receiver error (print substitute character)
Baud rate	1200 baud
Modem control	No modem control/restraint mode
Paper fault	No action
Coded Disconnect	Off
Local echo	Off
Auto-XON/XOFF	On
Answerback	None
Auto-answerback	Off
End of line control	On
Printer new line	No new line
Printer character sets	U.S. ASCII
BREAK key	On
Alternate keypad	Numeric
Auto-linefeed	Off
Keyboard layout	U.S. ASCII