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TI 6490.37

INSTRUCTION BOOK
(EQUIPMENT)

MODEL 1 FULL CAPACITY FLIGHT SERVICE DATA PROCESSING SUBSYSTEM FA-10017

WITH

TYPE FA-10017/1 FSDPS COMMUNICATIONS SWITCHING RACK
TYPE FA-10017/2 FSDPS COMMUNICATIONS EQUIPMENT RACK
TYPE FA-10017/3 FSDPS COTC PROCESSOR RACK

MODEL 1 FULL CAPACITY AUTOMATED FLIGHT SERVICE STATION FA-10018

WITH

TYPE FA-10018/1 AFSS COMMUNICATIONS EQUIPMENT RACK
TYPE FA-10018/2 AFSS COMMUNICATIONS PROCESSOR RACK
TYPE FA-10018/3 AFSS POSITION PROCESSOR RACK

MODEL 1 FULL CAPACITY AVIATION WEATHER PROCESSOR FA-10020

CONTROLLED DOCUMENT

WITH

TYPE FA-10020/1 COMMUNICATIONS EQUIPMENT RACK
TYPE FA-10020/2 COMMUNICATIONS PROCESSOR RACK
TYPE FA-10020/3 POSITION PROCESSOR RACK

CONTRACT DTFA01-81-C 10039

CONTRACTOR

E-SYSTEMS, INC.
GARLAND DIVISION
P.O. BOX 660023
DALLAS, TEXAS 75266-0023

416-32141

MADE FOR

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION

29 MAY 1989

LIST OF EFFECTIVE PAGES

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

Dates of issue for original and changed pages are:
Original...0... 27 February 1989

TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 642 CONSISTING OF THE FOLLOWING:

Page No.	Change No.	Page No.	Change No.
Title	0	5-1 to 5-2	0
ii to xxxii	0	6-1 to 6-2	0
1-1 to 1-100	0	7-1 to 7-44	0
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4-1 to 4-2	0	10-1 to 10-142	0
		11-1 to 11-2	0

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VALIDATION PERFORMANCE

TITLE OF DOCUMENT:	
EQUIPMENT MANUAL, MODEL I FULL CAPACITY FLIGHT SERVICE AUTOMATION SYSTEM	
CONTRACTOR: E-SYSTEMS, GARLAND DIVISION	SUBCONTRACTOR:
APPLICABLE CONTRACT AND PURCHASE ORDER NUMBERS: DTFA01-81-C-10039	

SECTION NUMBER	PARAGRAPH AND SUBPARAGRAPH NUMBERS (WHEN APPLICABLE, LIST INCLUSIVE PARAGRAPHS, E.G., 4-21 THRU 4.21.6)	DATE OF VALIDATION COMPLETION	CHECK BELOW IF NOT VALIDATED	AUTHORITY

VALIDATING OFFICER

SIGNATURE OF VALIDATING OFFICER

VALIDATING OFFICER'S TITLE

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SAFETY NOTICE

The attention of operating and maintenance personnel is directed to FAA Instruction 6000.15 "Maintenance of Airway Facilities" for instructions on the subject of safety precautions to be observed, and to FAA Order 3900.0 "Accident Prevention Handbook for Airway Facility Personnel." Personnel must observe the safety regulations at all times. Maintenance personnel shall become familiar with the technique for resuscitation.

INTERLOCKS

This equipment contains interlocks for your protection. To ensure safety, always remove power from the equipment prior to opening access panels or doors. Do not depend on the interlocks or door switches when working with the equipment. Do not short-circuit or tamper with any access gate, door, or other safety interlock switch. When it is absolutely mandatory that an interlock be bypassed in order to trace a fault or correct a malfunction, authorized maintenance personnel may perform the bypass for the specific test to be made. Immediately after completing the test, the interlock shall be restored to working condition.

KEEP AWAY FROM LIVE CIRCUITS

Operating and maintenance personnel must at all times observe all safety regulations. Do not change plug-in components or make adjustments inside equipment with high voltage supply on. Under certain conditions, dangerous potentials may exist in circuits with power controls in the off position.

RESUSCITATION

Maintenance personnel should familiarize themselves with the technique for resuscitation found in the manual of first aid instructions.

EXPLANATION OF SHADED AREAS

WHITE AREAS - Indicates external circuit connections.

LEVEL 1 GREY SHADE AREAS - Indicates composite functional groups

LEVEL 2 GREY SHADE AREAS - Indicates functional groups

FUNCTIONAL INDEX

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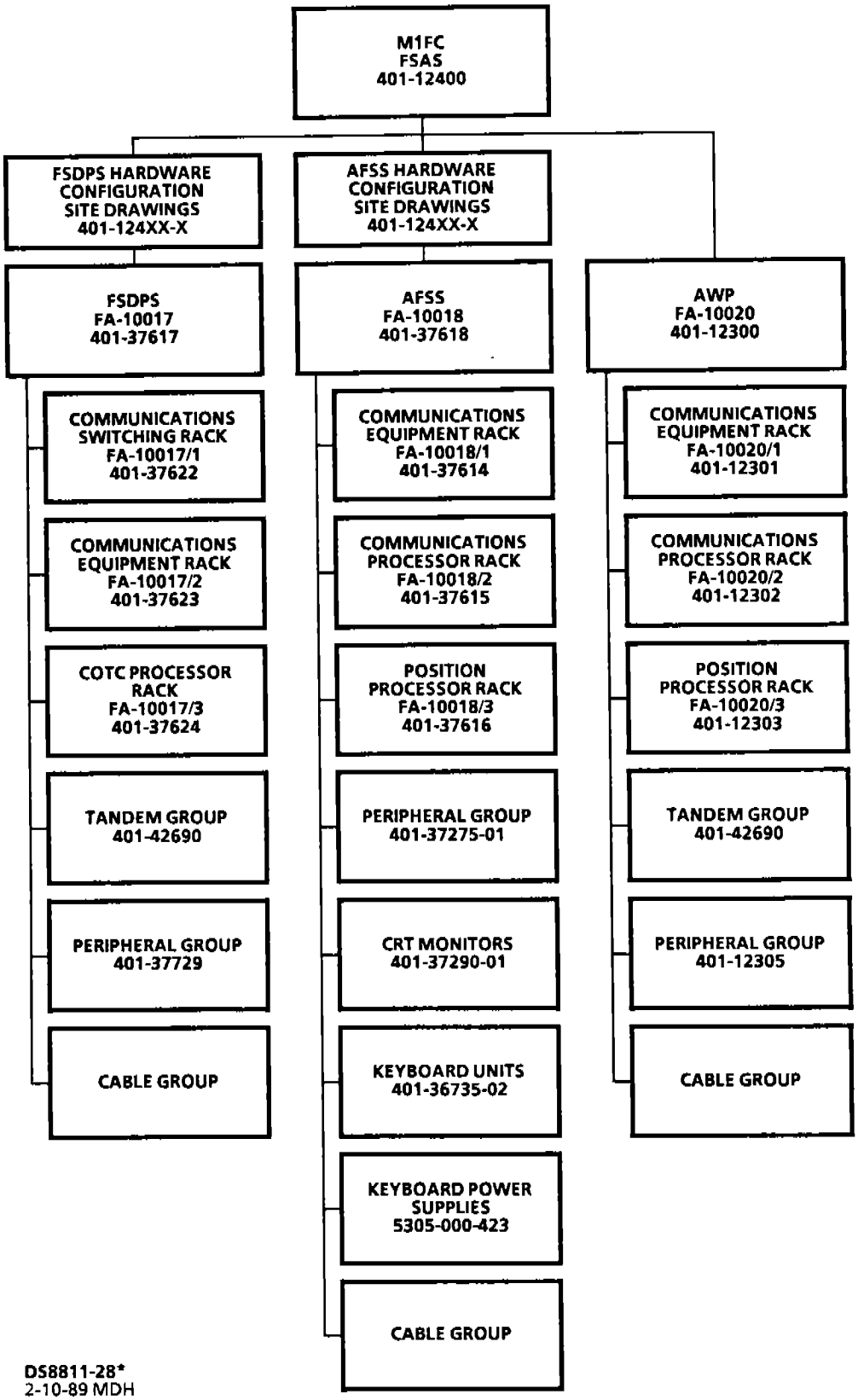

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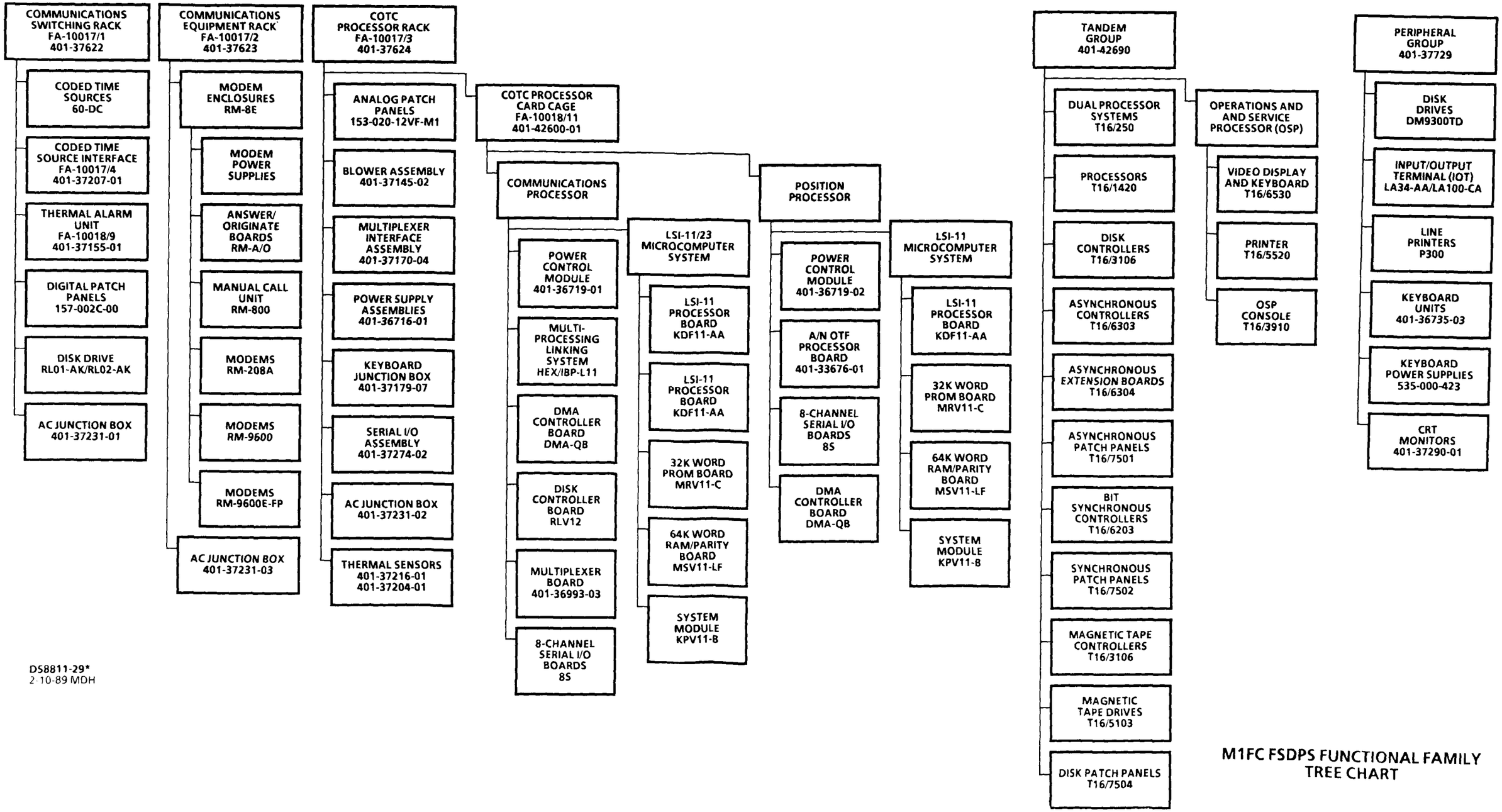
M1FC FSAS FUNCTIONAL FAMILY TREE CHART

PRELIMINARY MANUSCRIPT NOTES

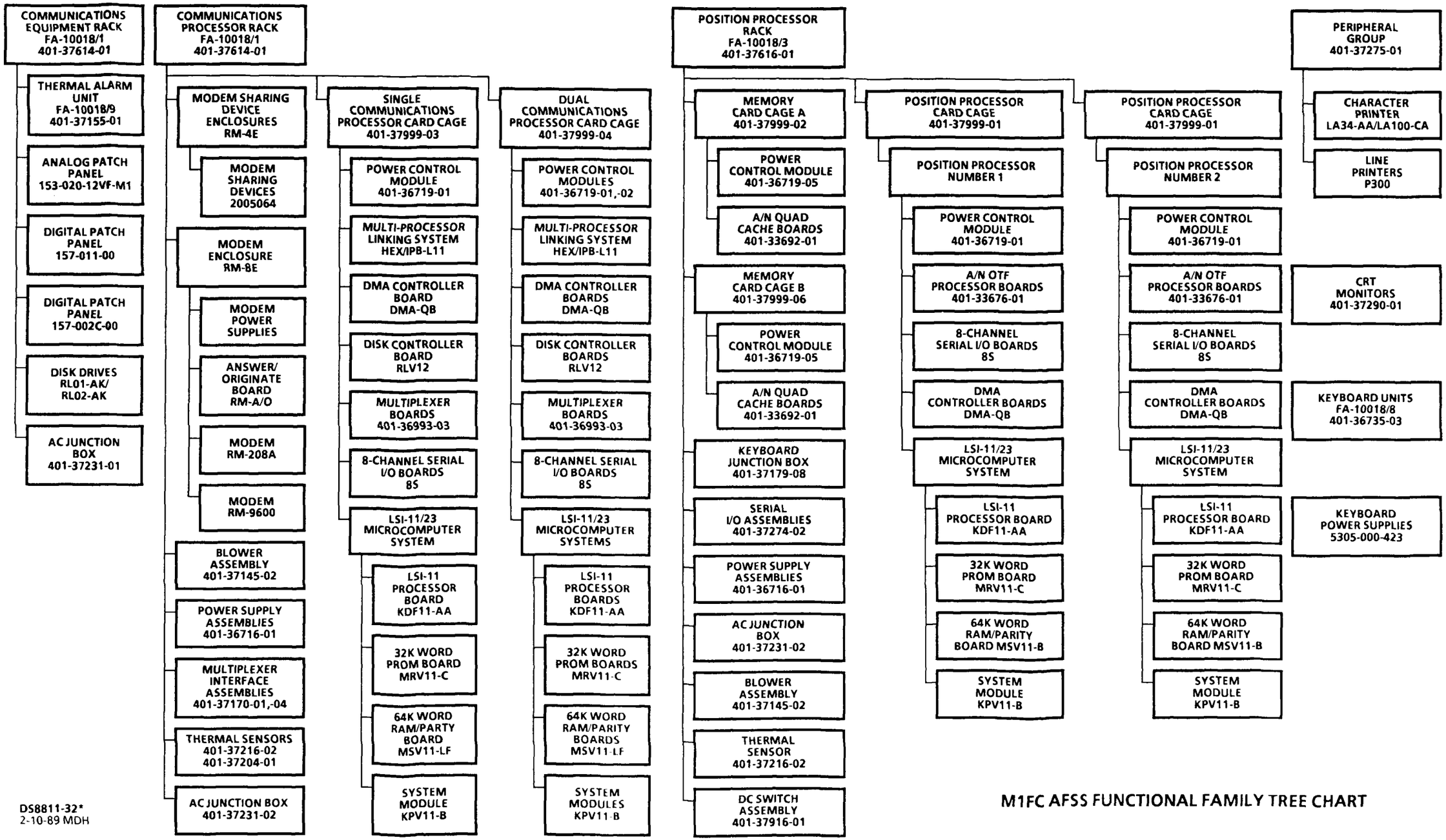
This preliminary manuscript is submitted to review with the following deviations from the quality and format requirements of FAA-D-2494/2a specification (preparation for reproducible copy):

1. Keyed text and shaded blocked schematic diagrams are provided on one side of page only, instead of on facing pages.

2. Fold out diagrams in this manuscript do not have the required blank apron.



M1FC FSDPS FUNCTIONAL FAMILY TREE CHART



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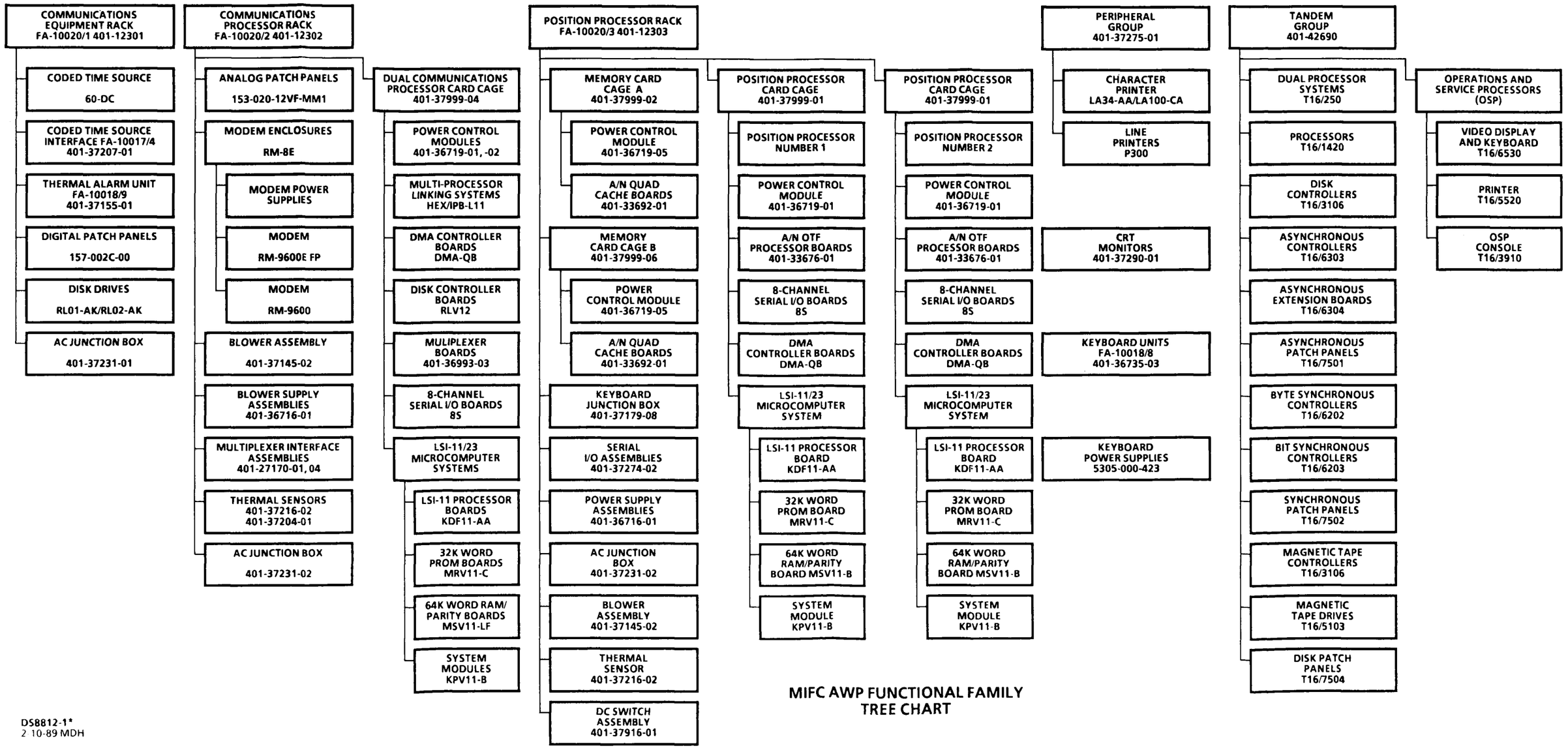
M1FC AFSS FUNCTIONAL FAMILY TREE CHART



MIFC AWP FUNCTIONAL FAMILY TREE CHART

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SECTION 1

GENERAL INFORMATION AND REQUIREMENTS

1.1 INTRODUCTION. - The Model 1 Full Capacity (M1FC) Flight Service Automation System (FSAS) Equipment Manual provides detailed information concerning the description of equipment contained in the M1FC FSAS system, how the equipment operates, and what is required to isolate and correct equipment failures within the system.

NOTE

The FAA type numbers that appear on equipment name plates are not item identifying in all cases. One FAA type number may represent more than one configuration of an equipment or subsystem. Therefore, the FAA type numbers should not be used to identify a specific configuration. For complete identification of specific configurations, use the part number that appears on the E-Systems nameplate and refer to the parts list in this manual.

Section 1 of this manual describes and identifies the principal characteristics of the equipment. Section 2 provides a technical description of the equipment consisting of theory of operation, intermediate logic diagrams, blocked schematic diagrams, and keyed text. An index of logic circuits is provided in this section. Section 3 provides necessary operating instructions. Section 4 provides standards and tolerances for the equipment. Section 5 provides periodic maintenance procedures. Section 6 provides maintenance procedures for the equipment. Section 7 provides corrective maintenance procedures required to diagnose faults, troubleshoot, repair, and overhaul repairable equipment. Section 8 provides a parts list for all equipment used in the system. Section 9 refers to the System Instruction Book, TI 6490.36, for installation, integration, and checkout procedures. Section 10 provides troubleshooting support data for the equipment. Printed wiring board illustrations, cable diagrams, and wiring diagrams are provided in this section. Section 11 provides a reference of computer software documentation applicable to this system.

1.2 DESCRIPTION. - The M1FC FSAS system consists of a central

computing complex referred to as the Flight Service Data Processing Subsystem (FSDPS), distributed Automated Flight Service Stations (AFSSs), and an Aviation Weather Processor (AWP). The FSDPS provides the collection and dissemination of information related to flight safety to the AFSSs. The FSDPS maintains an external interface to Service B and internal interfaces to the AWPs and AFSSs.

The AFSSs maintain/control the specialists' terminals and provide for the transfer of information between the AFSS and its controlling FSDPS. The AFSSs receive information from the specialist via keyboard, send this information to the FSDPS, receive responses from the FSDPS, and display this information to the specialist via CRT or printer.

The AWP provides for the collection and maintenance of all weather and global flight safety information in the M1FC FSAS. The AWP maintains external interfaces to WMSC and Service B and internal interfaces to terminal equipment at the AWP, to all FSDPSs, and to the other AWP.

The equipment used in the FSDPS is contained in the following groups:

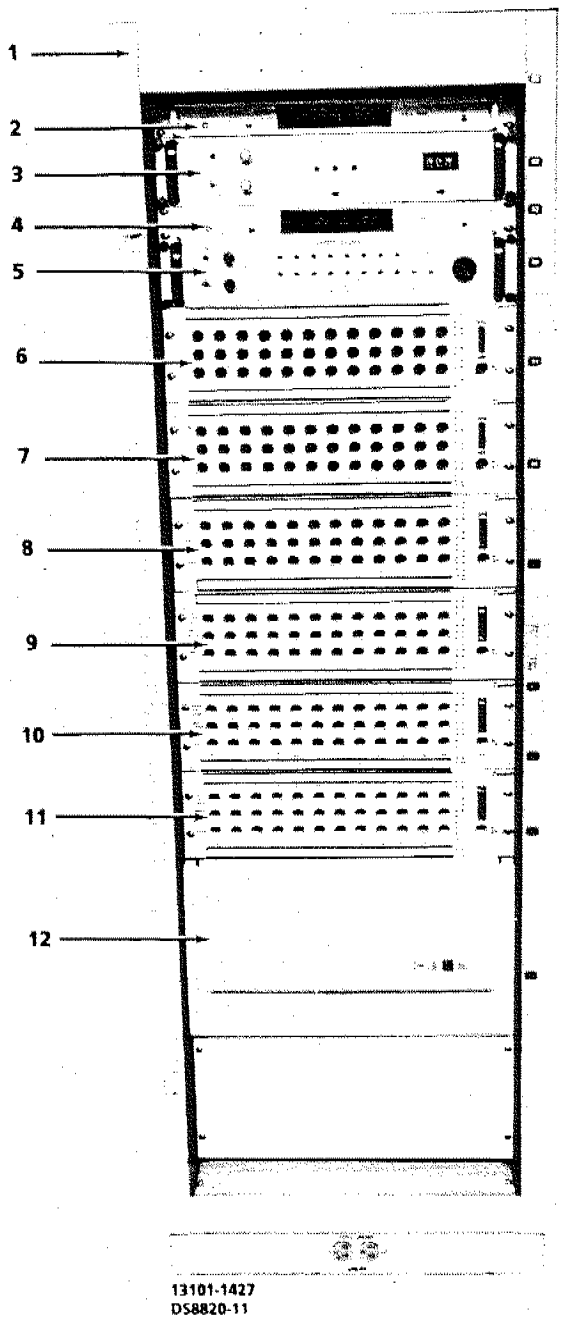
1. Communications Switching Rack, 401-37622
2. Communications Equipment Rack, 401-37623
3. COTC Processor Rack, 401-37624
4. Tandem Group, 401-42690
5. Peripheral Group, 401-37729
6. Communications Cable Group (part number varies among sites).

The FSDPS rack-mounted equipment is shown in figure 1-1 and the remaining equipment is shown in the manuals listed in table 1-4. The individual equipment provided within each group is listed in table 1-1.

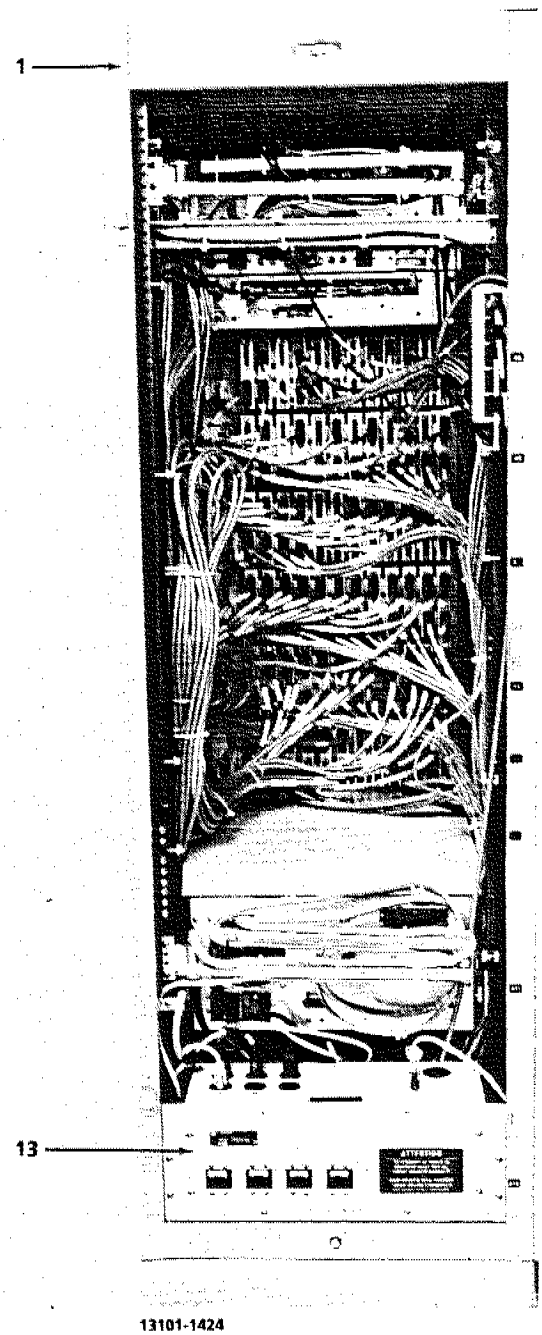
The equipment used in each AFSS is contained in the following groups:

1. Communications Equipment Rack, 401-37614
2. Communications Processor Rack, 401-37615
3. Position Processor Rack, 401-37616
4. Peripheral Group, 401-37275
5. Keyboard Units, 401-36735
6. Keyboard Power Supplies, 401-36707
7. CRT Monitors, 401-37290
8. Cable Group (part number varies among sites).

The AFSS rack-mounted equipment is shown in figure 1-2 and the remaining equipment is shown in the manuals listed in table 1-4. The individual equipment provided within each group is listed in table 1-2.



FRONT VIEW



REAR VIEW

Figure 1-1. M1FC FSDPS Rack-Mounted Equipment (Sheet 1 of 4) (Communications Switching Rack)

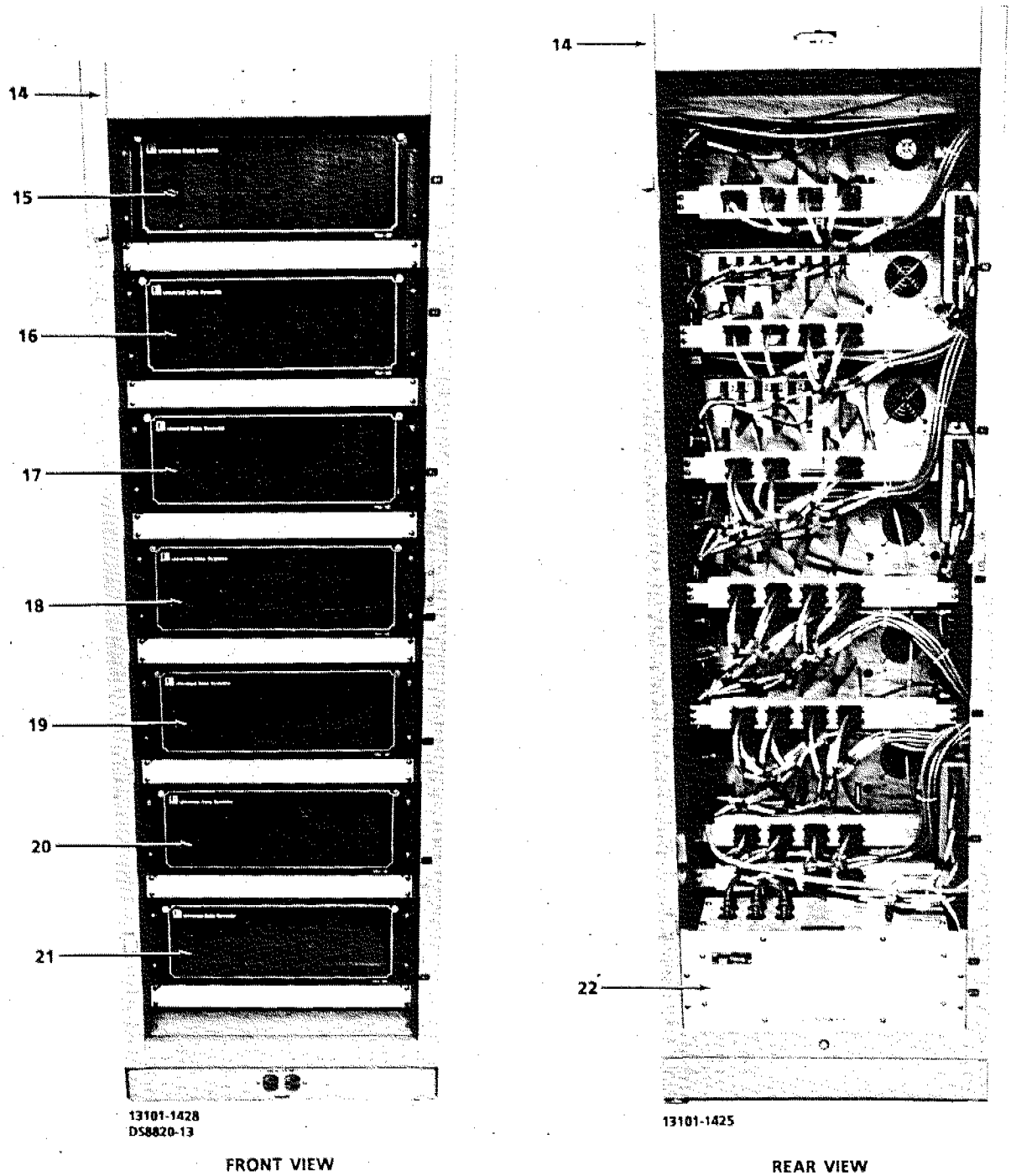


Figure 1-1. M1FC FSDPS Rack-Mounted Equipment (Sheet 2 of 4) (Communications Equipment Rack)

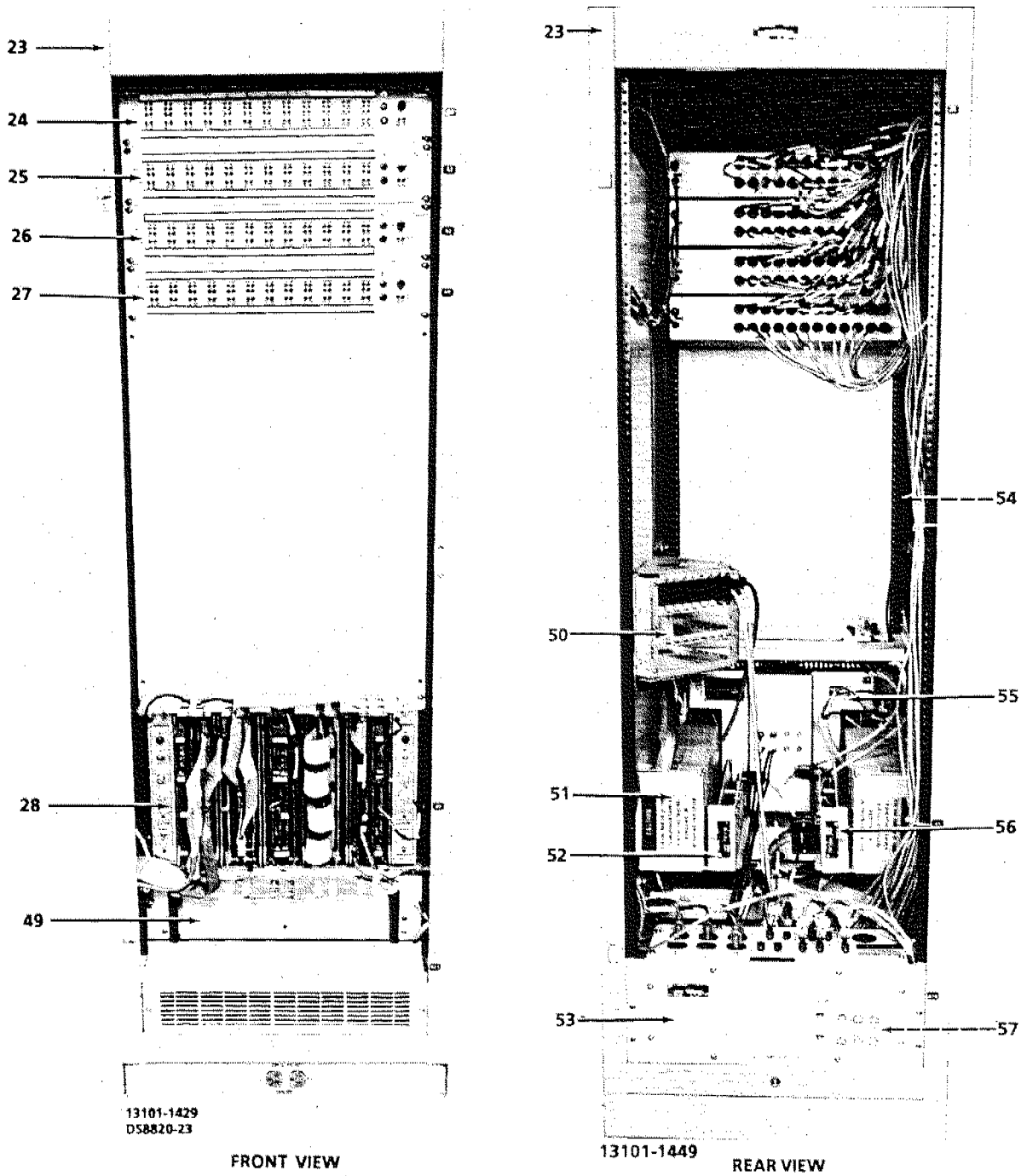


Figure 1-1. M1FC FSDPS Rack-Mounted Equipment (Sheet 3 of 4) (COTC Processor Rack)

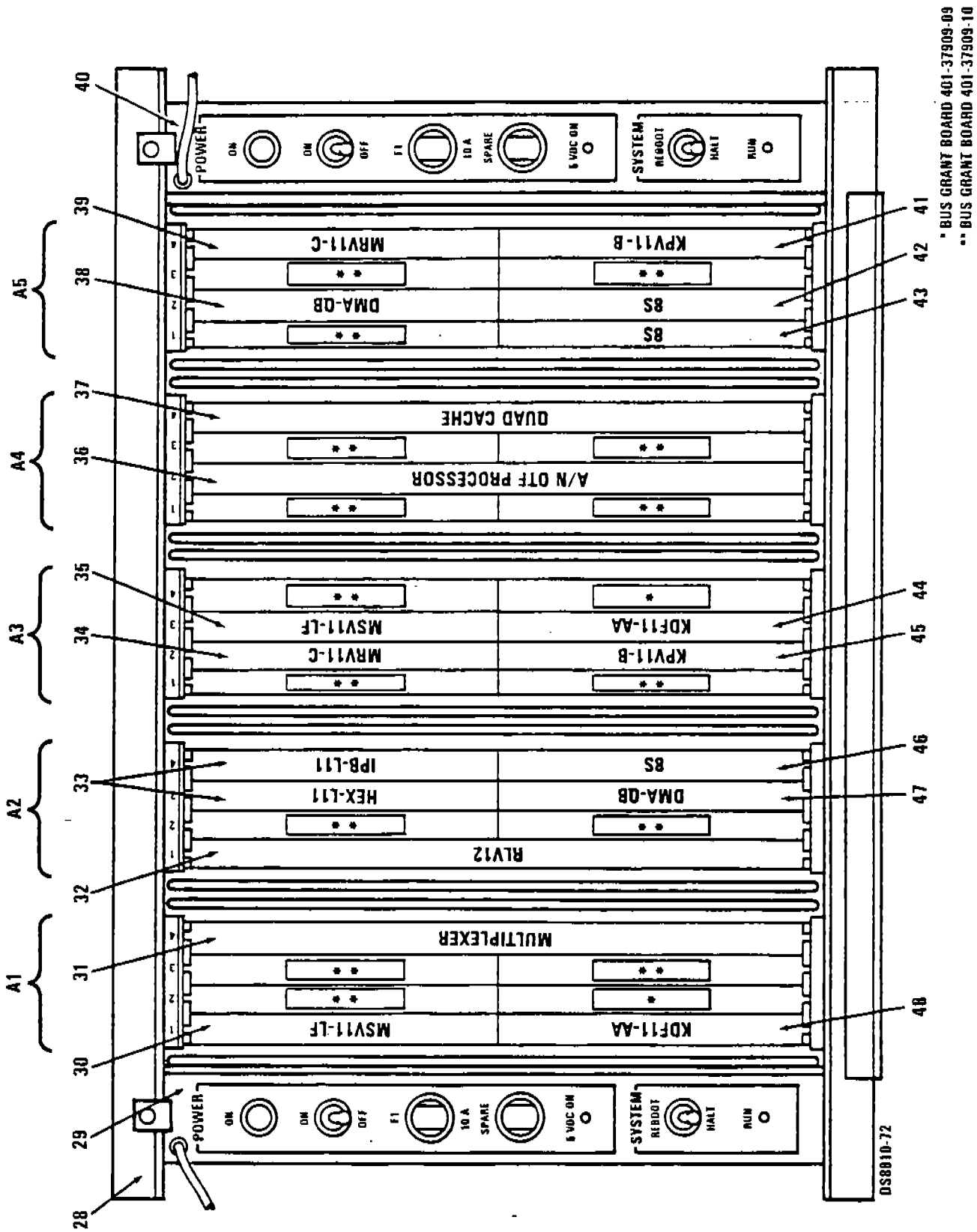


Figure 1-1. M1FC FSDPS Rack-Mounted Equipment (Sheet 4 of 4)
(COTC Processor Card Cage)

Table 1-1. FSDPS Equipment

Item No. (Fig. 1-1)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
1	Communications Switching Rack	Unit 1	401-37622-04	E-Systems
2	Coded Time Source	1A1	60-DC	True Time
3	Coded Time Source Interface	1A2	401-37207-01	E-Systems
4	Coded Time Source	1A3	60-DC	True Time
5	Thermal Alarm Unit	1A4	401-37155-01	E-Systems
6	Digital Patch Panel	1A5	157-002C-00	Dynatech
7	Digital Patch Panel	1A6	157-002C-00	Dynatech
8	Digital Patch Panel	1A7	157-002C-00	Dynatech
9	Digital Patch Panel	1A8	157-002C-00	Dynatech
10	Digital Patch Panel	1A9	157-002C-00	Dynatech
11	Digital Patch Panel	1A10	157-002C-00	Dynatech
12	Disk Drive	1A11	RL01-AK/RL02-AK	Digital Equipment
13	Circuit Breaker AC Junction Box	1A16	401-37231-01	E-Systems
14	Communications Equipment Rack	Unit 2	401-37623-05	E-Systems
15	Modem Enclosure	2A1	RM-8E	Universal Data Systems
	Modem Power Supplies (2)			Universal Data Systems
*	Answer/Originate Board (4)		RM-A/O	Universal Data Systems
*	Manual Call Unit		RM-800	Universal Data Systems
*	Modem (4)		RM-208A	Universal Data Systems
16	Modem Enclosure	2A2	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem (4)		RM-9600	Universal Data Systems
*	Modem (4)		RM-9600E FP	Universal Data Systems
17	Modem Enclosure	2A3	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem (5)		RM-9600	Universal Data Systems
*	Modem		RM-9600E FP	Universal Data Systems
18	Modem Enclosure	2A4	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem		RM-9600	Universal Data Systems
19	Modem Enclosure	2A5	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem (8)		RM-9600	Universal Data Systems

* Equipment is shown in manuals listed in table 1-4.

Table 1-1. FSDPS Equipment (Continued)

Item No. (Fig. 1-1)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
20	Modem Enclosure	2A6	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem (8)		RM-9600	Universal Data Systems
21	Modem Enclosure	2A7	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	RM-9600 Modem (4)		RM-9600	Universal Data Systems
22	Plain AC Junction Box	2A16	401-37231-03	E-Systems
23	COTC Processor Rack	Unit 3	401-37624-03	E-Systems
24	Analog Patch Panel	3A1	153-020-12VF-M1	Dynatech
25	Analog Patch Panel	3A2	153-020-12VF-M1	Dynatech
26	Analog Patch Panel	3A3	153-020-12VF-M1	Dynatech
27	Analog Patch Panel	3A4	153-020-12VF-M1	Dynatech
28	COTC Processor Card Cage	3A5	401-42600-01	E-Systems
29	Power Control Module		401-36719-01	E-Systems
30	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
31	Multiplexer		401-36993-03	E-Systems
32	Disk Controller Circuit Card		RLV12	Digital Equipment
33	Multi-Processor Linking System		HEX/IPB-L11	Peritek
34	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
35	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
36	A/N OTF Processor Circuit Card		401-33676-01	E-Systems
37	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
38	DMA Controller		DMA-QB	Peritek
39	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
40	Power Control Module		401-36719-02	E-Systems
41	System Module		KPV11-B	Digital Equipment
42	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
43	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
44	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment
45	System Module		KPV11-B	Digital Equipment
46	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
47	DMA Controller		DMA-QB	Peritek
48	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment

* Equipment is shown in manuals listed in table 1-4.

Table 1-1. FSDPS Equipment (Continued)

Item No. (Fig. 1-1)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
49	Blower Assembly	3A17	401-37145-02	E-Systems
50	Keyboard Junction Box	3A10	401-37179-07	E-Systems
51	Power Supply Assembly	3PS5	401-36716-01	E-Systems
52	Serial I/O Assembly	3A9	401-37274-02	E-Systems
53	Fan AC Junction Box	3A16	401-37231-02	E-Systems
54	Thermal Sensor	3A18	401-37216-02	E-Systems
55	Power Supply Assembly	3PS6	401-36716-01	E-Systems
56	Multiplexer Interface Assembly	3A6	401-37170-04	E-Systems
57	Thermal Sensor	3A19	401-37204-01	E-Systems
	Tandem Group		401-42690-01	E-Systems
*	Processor		T16/1420	Tandem
*	Disk Controller		T16/3106	Tandem
*	Asynchronous Controller		T16/6303	Tandem
*	Asynchronous Extension Board		T16/6304	Tandem
*	Asynchronous Patch Panel		T16/7501	Tandem
*	Bit Synchronous Controller		T16/6203	Tandem
*	Synchronous Patch Panel		T16/7502	Tandem
*	Magnetic Tape Controller		T16/3106	Tandem
*	Magnetic Tape Drive		T16/5103	Tandem
*	Disk Patch Panel		T16/7504	Tandem
*	Operations and Service Processor (OSP)			Tandem
*	Video Display and Keyboard		T16/6530	Tandem
*	OSP Console		T16/3910	Tandem
*	Printer		T16/5520	Tandem
	Peripheral Group		401-37729-01	E-Systems
*	Input/Output Terminal (IOT)		LA34/LA100	Digital Equipment
*	Line Printers (2)		P300	Printronix
*	Keyboard Units (2)		401-36735-03	E-Systems
*	Keyboard Power Supplies (2)		5305-000-423	Ault
*	CRT Monitors (2)		401-37290-01	Ball Brothers/E-Systems
*	Disk Drives (6)		DM9300TD	Ampex

* Equipment is shown in manuals listed in table 1-4.

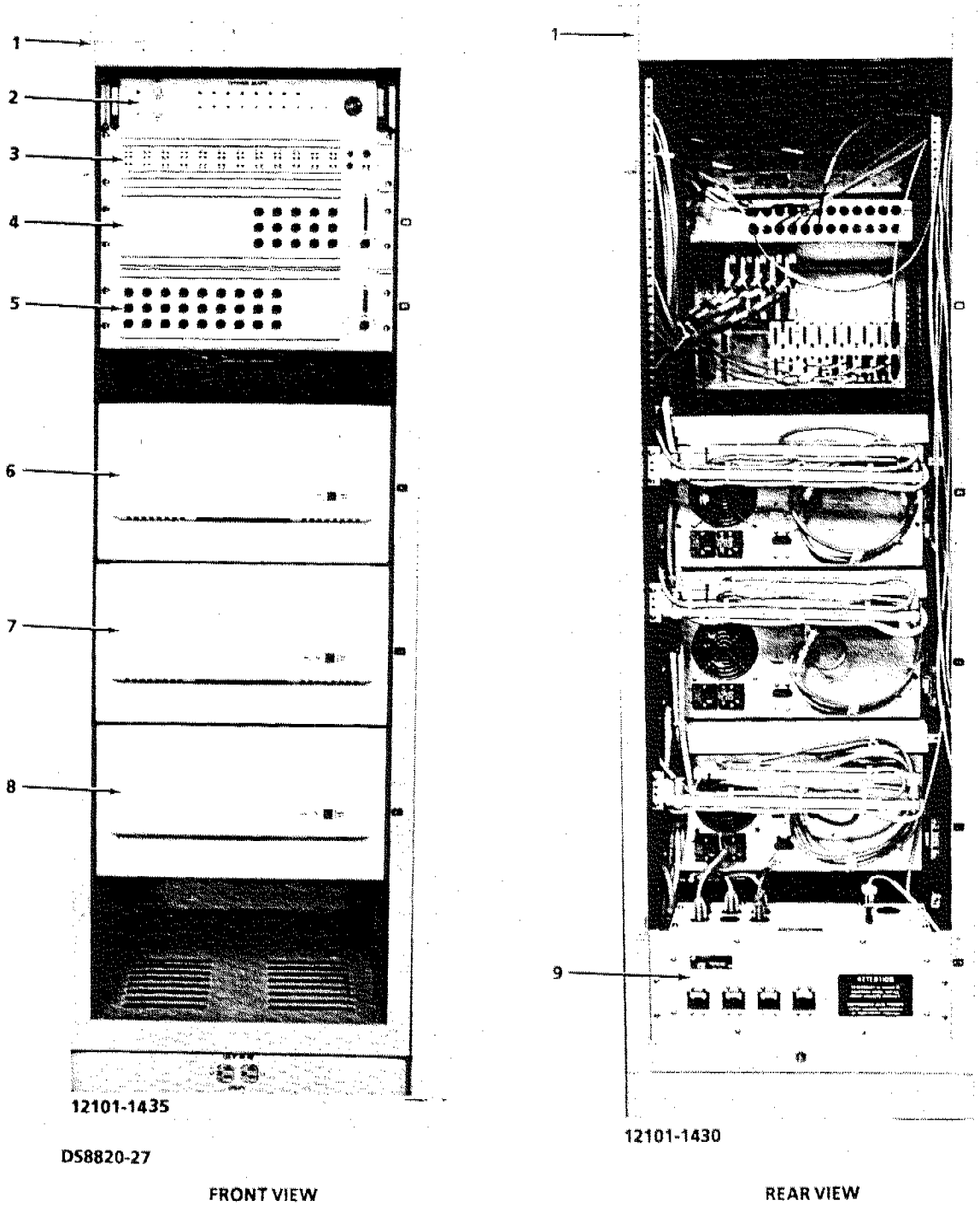
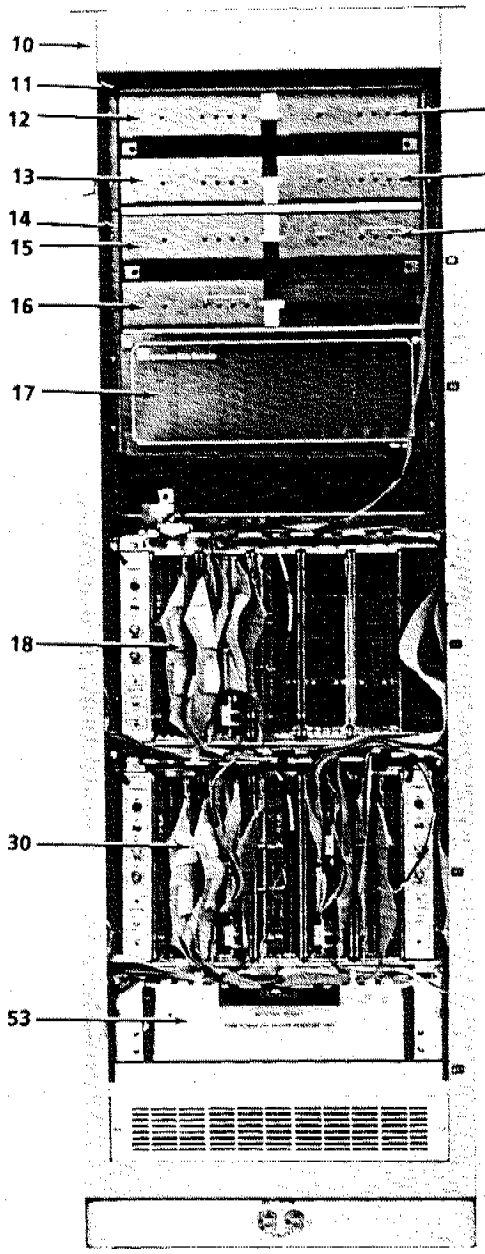
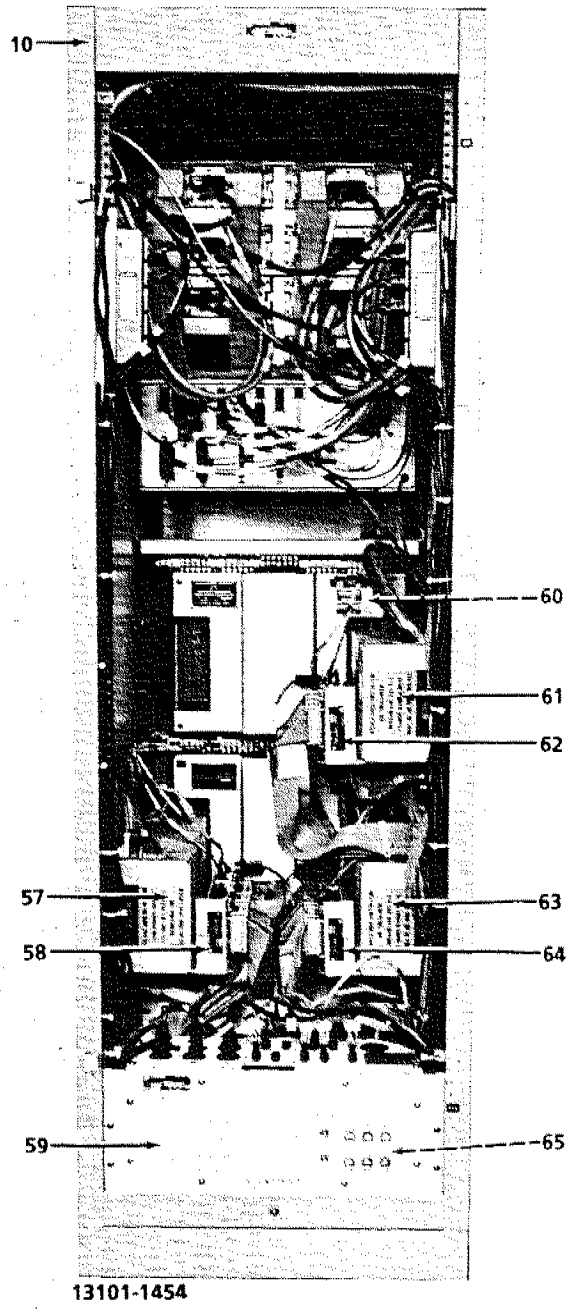


Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 1 of 8) (Communications Equipment Rack)



FRONT VIEW



REAR VIEW

Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 2 of 8)
(Communications Processor Rack)

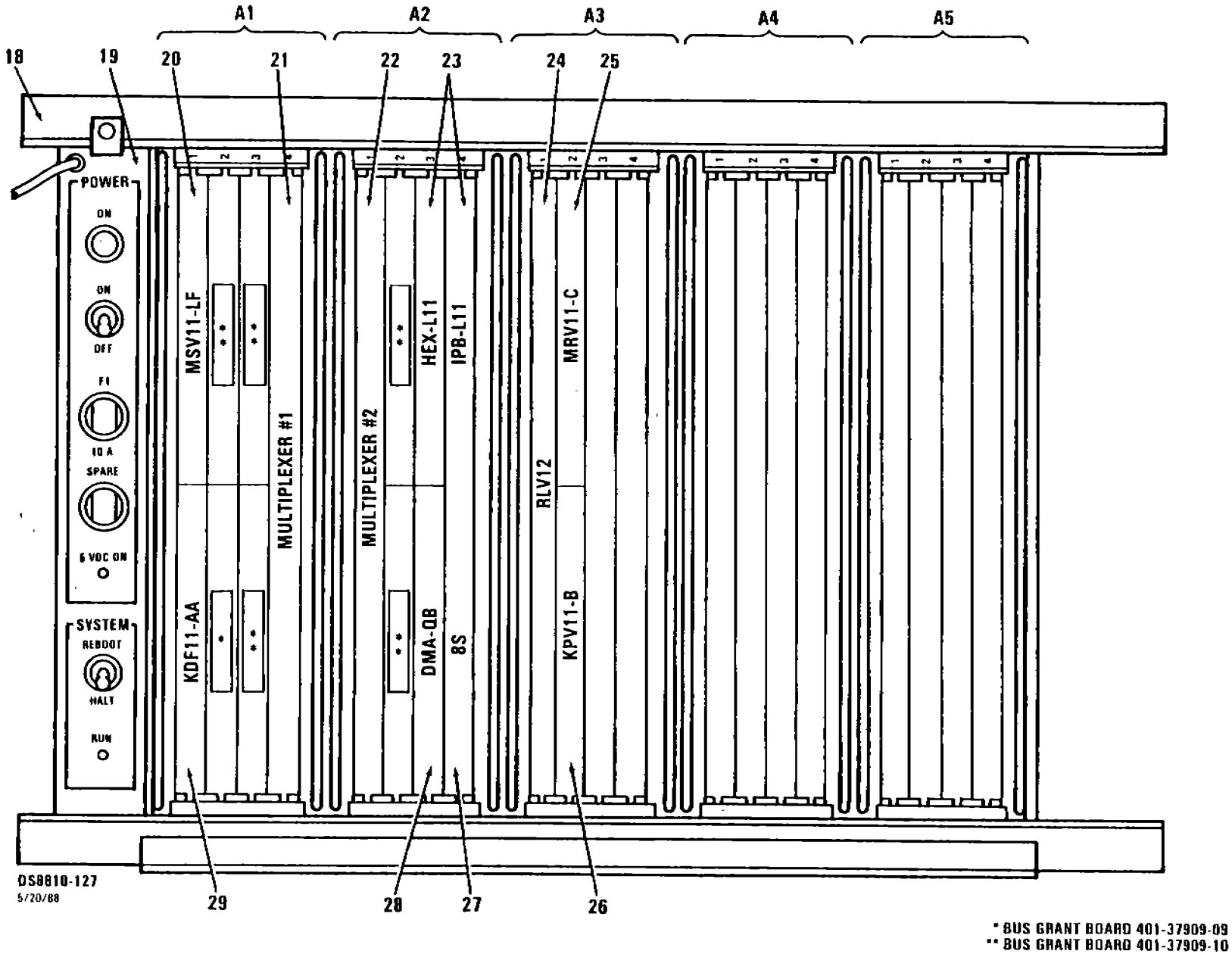


Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 3 of 8)
(Single Communications Processor Card Cage)

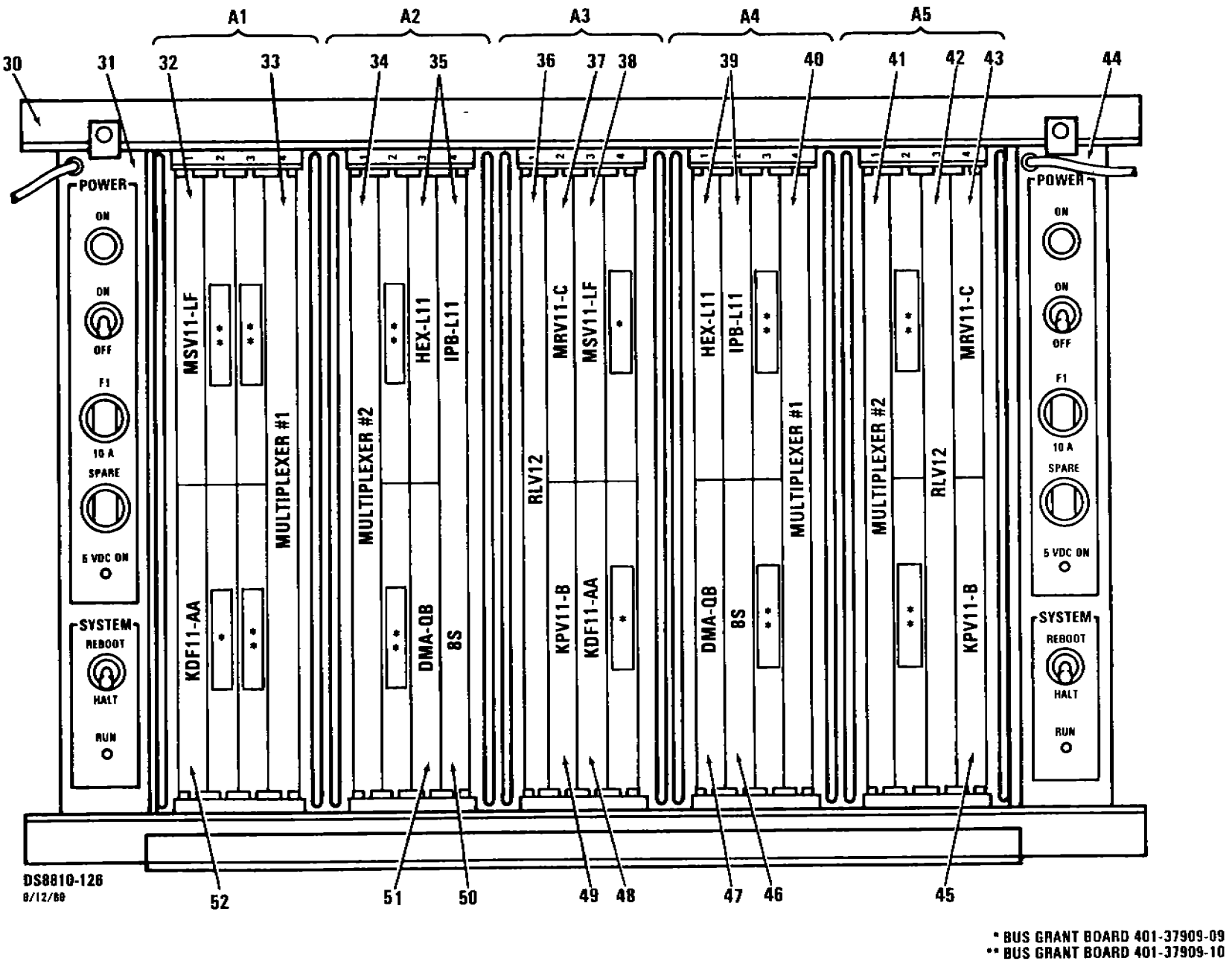
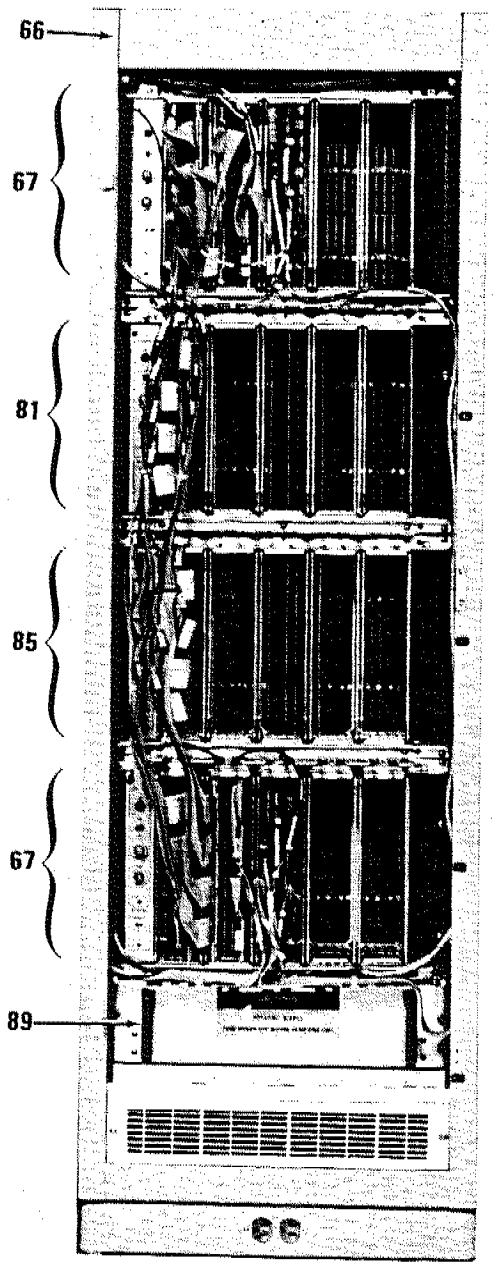
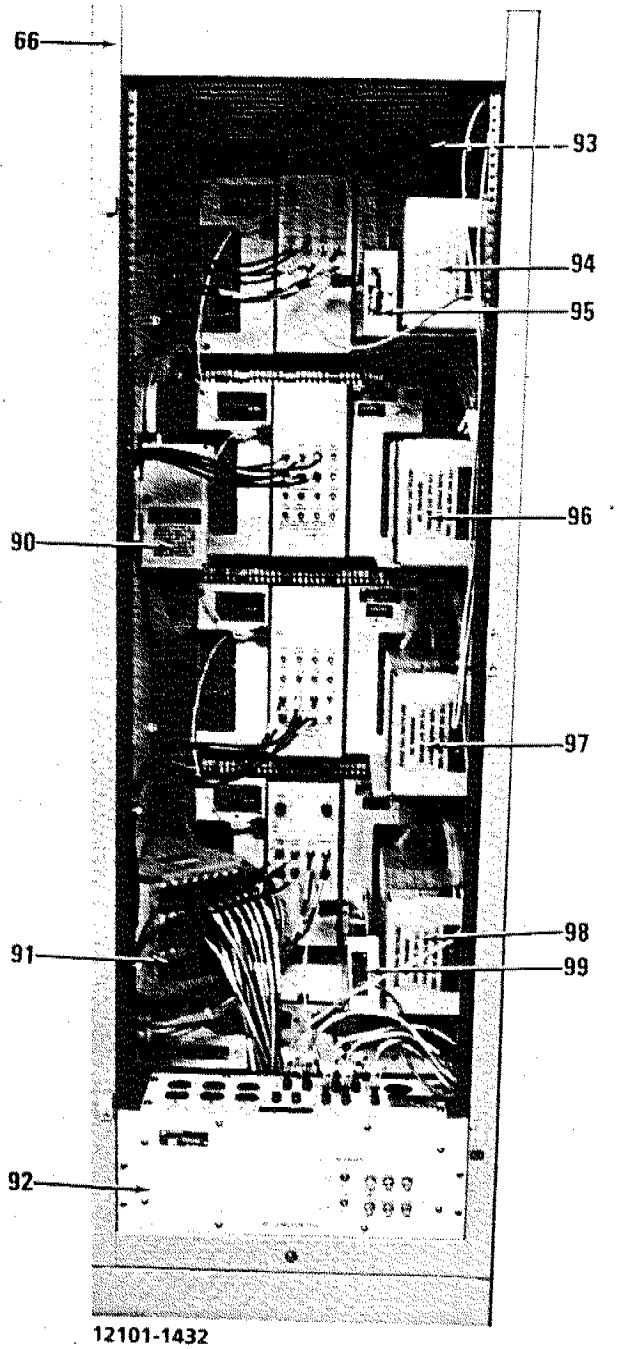


Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 4 of 8)
(Dual Communications Processor Card Cage)



12101-1433
DS8820-29

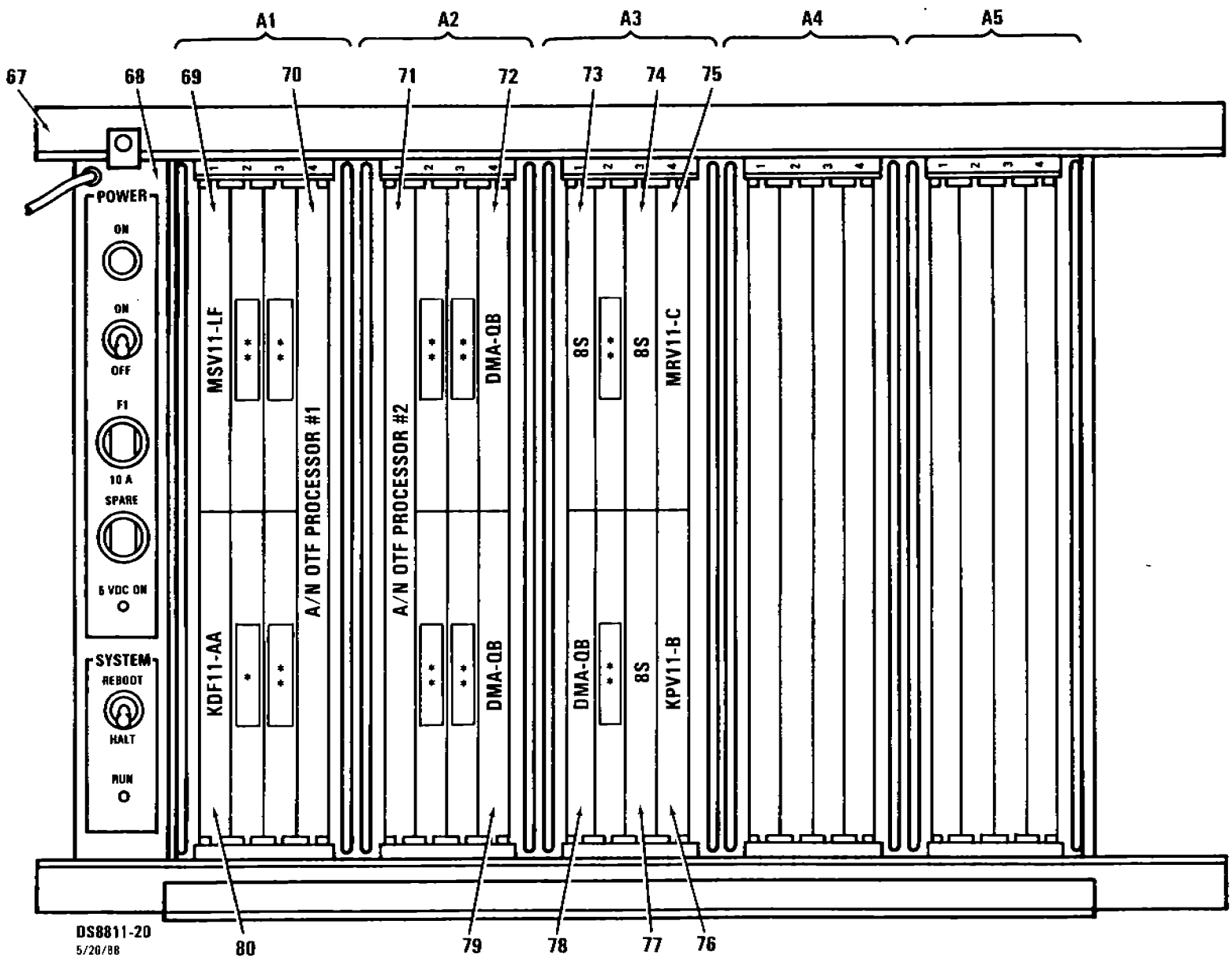
FRONT VIEW



12101-1432

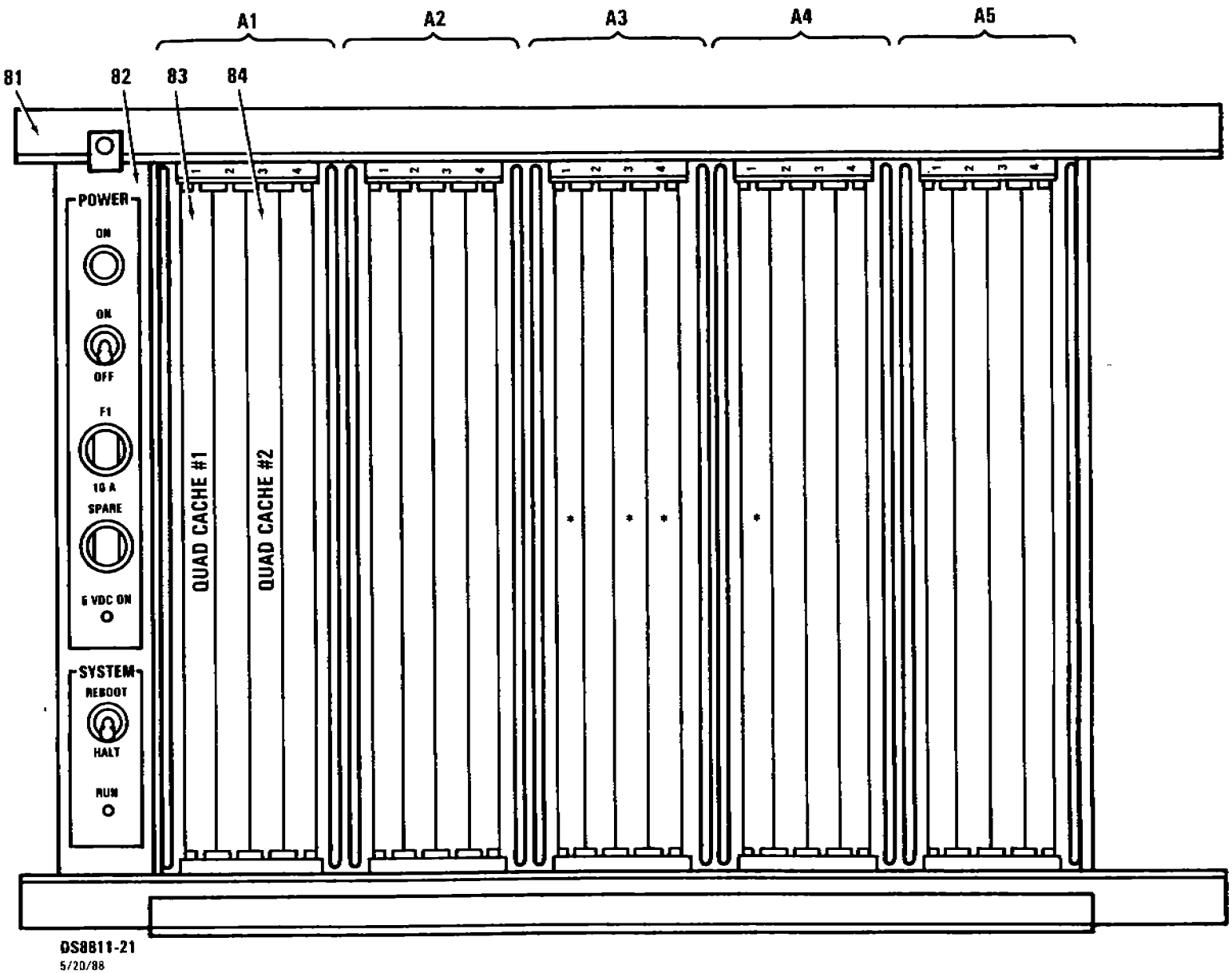
REAR VIEW

Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 5 of 8) (Position Processor Rack)



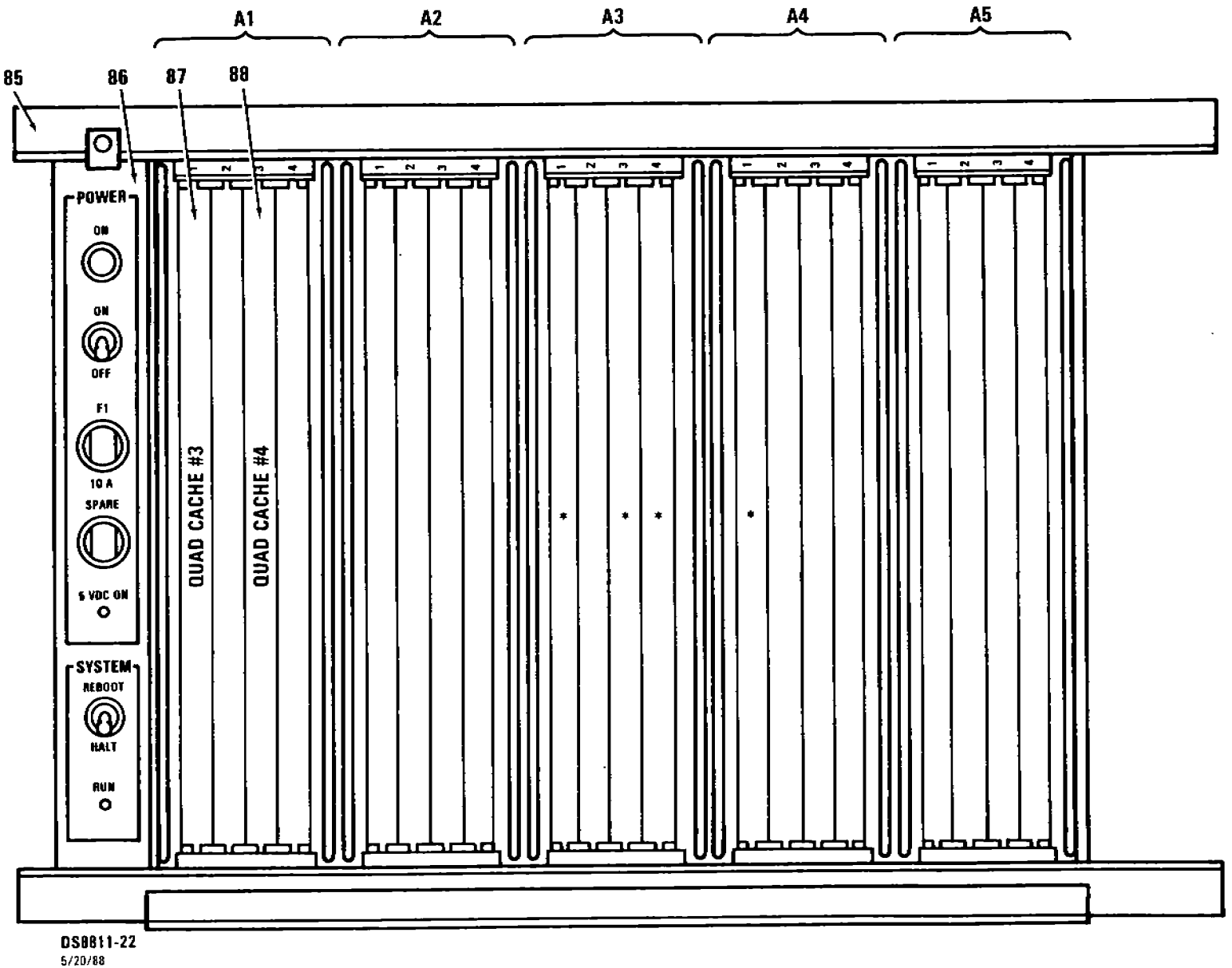
* BUS GRANT BOARD 401-37909-09
** BUS GRANT BOARD 401-37909-10

Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 6 of 8)
(Position Processor Card Cage)



*GRAPHICS VIDEO JUMPER 401-37925-01

Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 7 of 8)
(Memory "A" Card Cage)



* GRAPHICS VIDEO JUMPER 401-37925-01

Figure 1-2. M1FC AFSS Rack-Mounted Equipment (Sheet 8 of 8)
(Memory "B" Card Cage)

Table 1-2. AFSS Equipment

Item No. (Fig. 1-2)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
1	Communications Equipment Rack	Unit 1	401-37614-01	E-Systems
2	Thermal Alarm Unit	1A1	401-37155-01	E-Systems
3	Analog Patch Panel	1A2	153-020-12VF-M1	Dynatech
4	Digital Patch Panel	1A3	157-011-00	Dynatech
5	Digital Patch Panel	1A4	157-002C-00	Dynatech
6	Disk Drive	1A5	RL01-AK/RL02-AK	Digital Equipment
7	Disk Drive	1A6	RL01-AK/RL02-AK	Digital Equipment
8	Disk Drive	1A7	RL01-AK/RL02-AK	Digital Equipment
9	Circuit Breaker AC Junction Box	1A16	401-37231-01	E-Systems
10	Communications Processor Rack	Unit 2	401-37615-01	E-Systems
11	Modem Sharing Device Enclosure	2A1	2005061	Universal Data Systems
12	Modem Sharing Device	2A1A1	2005064	Universal Data Systems
13	Modem Sharing Device	2A1A3	2005064	Universal Data Systems
14	Modem Sharing Device Enclosure	2A2	2005061	Universal Data Systems
15	Modem Sharing Device	2A2A1	2005064	Universal Data Systems
16	Modem Sharing Device	2A2A2	2005064	Universal Data Systems
17	Modem Enclosure	2A3	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Answer/Originate Board		RM-A/O	Universal Data Systems
*	Modem		RM-208A	Universal Data Systems
*	Modem		RM-9600	Universal Data Systems
18	Single Comm Processor Card Cage	2A5	401-37999-03	E-Systems
19	Power Control Module	2A5A6	401-36719-01	E-Systems
20	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
21	Multiplexer		401-36993-03	E-Systems
22	Multiplexer		401-36993-03	E-Systems
23	Multi-processor Linking System		HEX/IPB-L11	Peritek
24	Disk Controller Circuit Card		RLV12	Digital Equipment
25	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
26	System Module		KPV11-B	Digital Equipment
27	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
28	DMA Controller		DMA-QB	Peritek
29	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment

* Equipment is shown in manuals listed in table 1-4.

Table 1-2. AFSS Equipment (Continued)

Item No. (Fig. 1-2)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
30	Dual Comm Processor Card Cage	2A4	401-37999-04	E-Systems
31	Power Control Module	2A4A6	401-36719-01	E-Systems
32	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
33	Multiplexer		401-36993-03	E-Systems
34	Multiplexer		401-36993-03	E-Systems
35	Multi-Processor Linking System		HEX/IPB-L11	Peritek
36	Disk Controller Circuit Card		RLV12	Digital Equipment
37	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
38	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
39	Multi-Processor Linking System		HEX/IPB-L11	Peritek
40	Multiplexer		401-36993-03	E-Systems
41	Multiplexer		401-36993-03	E-Systems
42	Disk Controller Circuit Card		RLV12	Digital Equipment
43	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
44	Power Control Module	2A4A7	401-36719-02	E-Systems
45	System Module		KPV11-B	Digital Equipment
46	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
47	DMA Controller		DMA-QB	Peritek
48	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment
49	System Module		KPV11-B	Digital Equipment
50	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
51	DMA Controller		DMA-QB	Peritek
52	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment
53	Blower Assembly	2A17	401-37145-02	E-Systems
54	Modem Sharing Device	2A1A2	2005064	Universal Data Systems
55	Modem Sharing Device	2A1A4	2005064	Universal Data Systems
56	Modem Sharing Device	2A2A2	2005064	Universal Data Systems
57	Power Supply Assembly	2PS6	401-36716-01	E-Systems
58	Multiplexer Interface Assembly	2A7	401-37170-01	E-Systems
59	Fan AC Junction Box	2A16	401-37231-02	E-Systems
60	Thermal Sensor	2A18	401-37216-02	E-Systems
61	Power Supply Assembly	2PS3	401-36716-01	E-Systems
62	Multiplexer Interface Assembly	2A8	401-37170-04	E-Systems
63	Power Supply Assembly	2PS5	401-36716-01	E-Systems
64	Multiplexer Interface Assembly	2A6	401-37170-04	E-Systems
65	Thermal Sensor	2A19	401-37204-01	E-Systems

Table 1-2. AFSS Equipment (Continued)

Item No. (Fig. 1-2)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
66	Position Processor Rack	Units 3/4/5	401-37616-01	E-Systems
67	Position Processor Card Cage	3A1	401-37999-01	E-Systems
68	Power Control Module	3A1A6	401-36719-01	E-Systems
69	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
70	A/N OTF Processor Circuit Card		401-33676-01	E-Systems
71	A/N OTF Processor Circuit Card		401-33676-01	E-Systems
72	DMA Controller Circuit Card		DMA-QB	Peritek
73	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
74	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
75	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
76	System Module		KPV11-B	Digital Equipment
77	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
78	DMA Controller Circuit Card		DMA-QB	Peritek
79	DMA Controller Circuit Card		DMA-QB	Peritek
80	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment
81	Memory Card Cage "A"	3A2	401-37999-02	E-Systems
82	Power Control Module	3A2A6	401-36719-05	E-Systems
83	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
84	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
85	Memory Card Cage"B"	3A3	401-37999-06	E-Systems
86	Power Control Module	3A3A6	401-36719-05	E-Systems
87	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
88	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
89	Blower Assembly	A17	401-37145-02	E-Systems
90	DC Power Switch Assembly	S1	401-37916-01	E-Systems
91	Keyboard Junction Box	A10	401-37179-08	E-Systems
92	Fan AC Junction Box	A16	401-37231-02	E-Systems
93	Thermal Sensor	A18	401-37216-02	E-Systems
94	Power Supply Assembly	PS7	401-36716-01	E-Systems
95	Serial I/O Assembly	A8	401-37274-02	E-Systems
96	Power Supply Assembly	PS1	401-36716-01	E-Systems
97	Power Supply Assembly	PS3	401-36716-01	E-Systems
98	Power Supply Assembly	PS5	401-36716-01	E-Systems
99	Serial I/O Assembly	A9	401-37274-02	E-Systems

Table 1-2. AFSS Equipment (Continued)

Item No. (Fig. 1-2)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
*	Peripheral Group		401-37275-01	E-Systems
*	Input/Output Terminal (IOT)		LA34/LA100	Digital Equipment
*	Line Printer		P300	Printronix
*	CRT Monitor		401-37290-01	Ball Brothers/E-Systems
*	Keyboard Unit		401-36735-03	E-Systems
*	Keyboard Power Supply		5305-000-423	Ault

* Equipment is shown in manuals listed in table 1-4

The equipment used in the AWP is contained in the following groups:

1. Communications Equipment Rack, 401-12301
2. Communications Processor Rack, 401-12302
3. Position Processor Rack, 401-12303
4. Tandem Group, 401-42690
5. Peripheral Group, 401-12305
6. Keyboard Units, 401-36735
7. Keyboard Power Supplies, 401-36707
8. CRT Monitors, 401-37290
9. Cable Group

The AWP rack-mounted equipment is shown in figure 1-3 and the remaining equipment is shown in the manuals listed in table 1-4. The individual equipment provided within each group is listed in table 1-3.
The relationship of the equipment used in the FSDPS, AFSS, and AWP is shown in figures 1-4, 1-5, and 1-6, respectively.

1.2.1 Flight Service Data Processing Subsystem (FSDPS). - The M1FC FSDPS consists of processing equipment, communications equipment, and maintenance equipment. The processing equipment includes the Tandem CPUs and all I/O controllers and peripheral equipment connected to the Tandem CPUs. The communications equipment consists of patch panels and modems necessary to complete the communication links to Service B, AWP, and the AFSSs. The maintenance equipment consists of Tandem diagnostic hardware, including the Operations and Service Processor (OSP) and the Processor Maintenance Interface (PMI), the Diagnostic Test Set (MADTS), and all special tools required to repair the equipment.

The Computer Operator Terminal Console (COTC) is used to control the M1FC FSAS computer system operation and to accomplish confidence checking, certification, and maintenance.

1.2.1.1 Communications Switching Rack. - There are four different configurations for the communications switching rack. The E-Systems part number for these four configurations are 401-37622-01, -02, -03, and -04. The maximum configured Communications Switching Rack, 401-37622-04, is shown in figure 1-1. This rack is used in the FSDPS to house the following equipment:

1. Coded Time Source, 60 DC
2. Coded Time Source Interface, 401-37207-01
3. Thermal Alarm Unit, 401-37155-01
4. Digital Patch Panel, 157-002C-00
5. Disk Drive, RL01-AK/RL02-AK
6. Circuit Breaker AC Junction Box, 401-37231-01

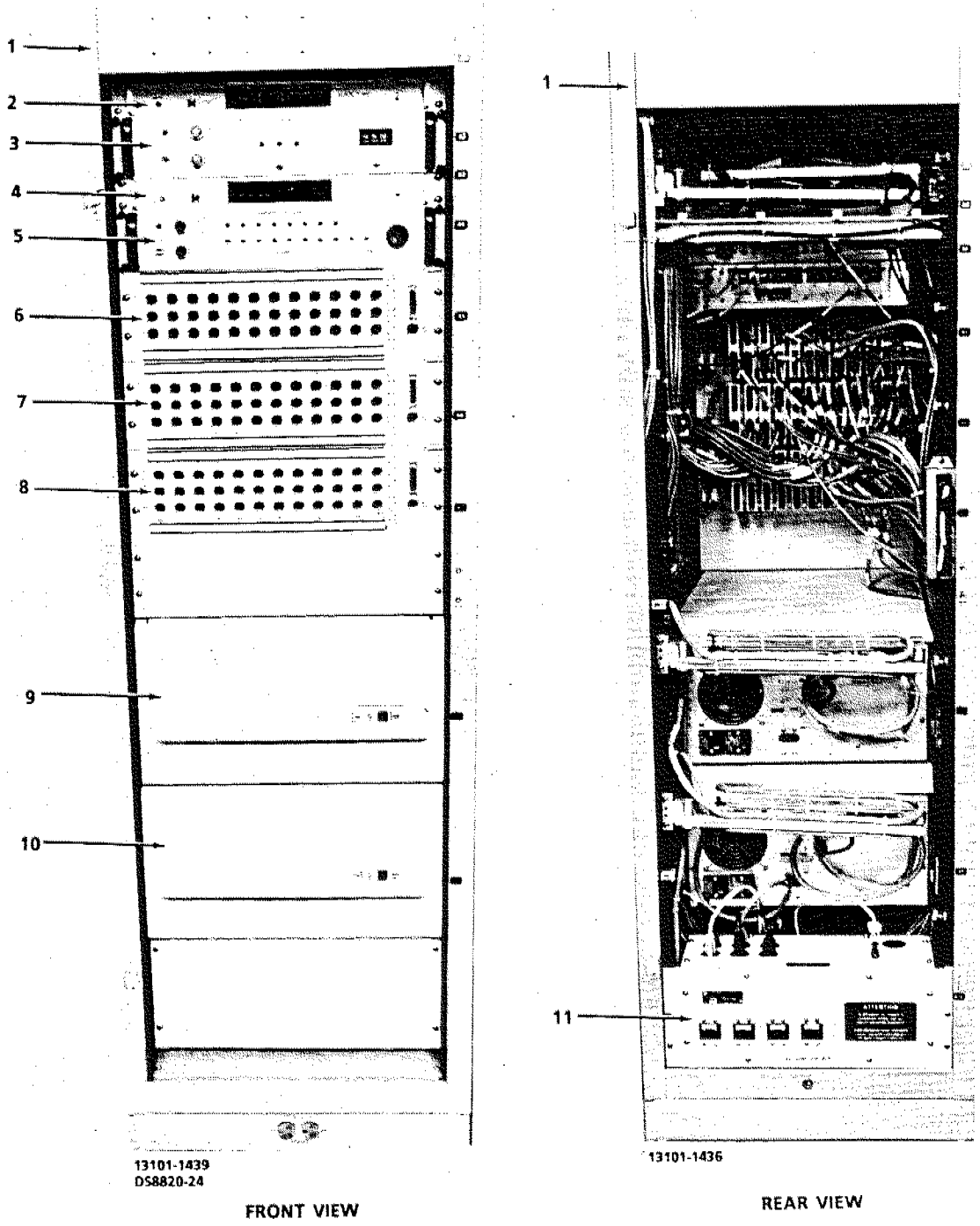
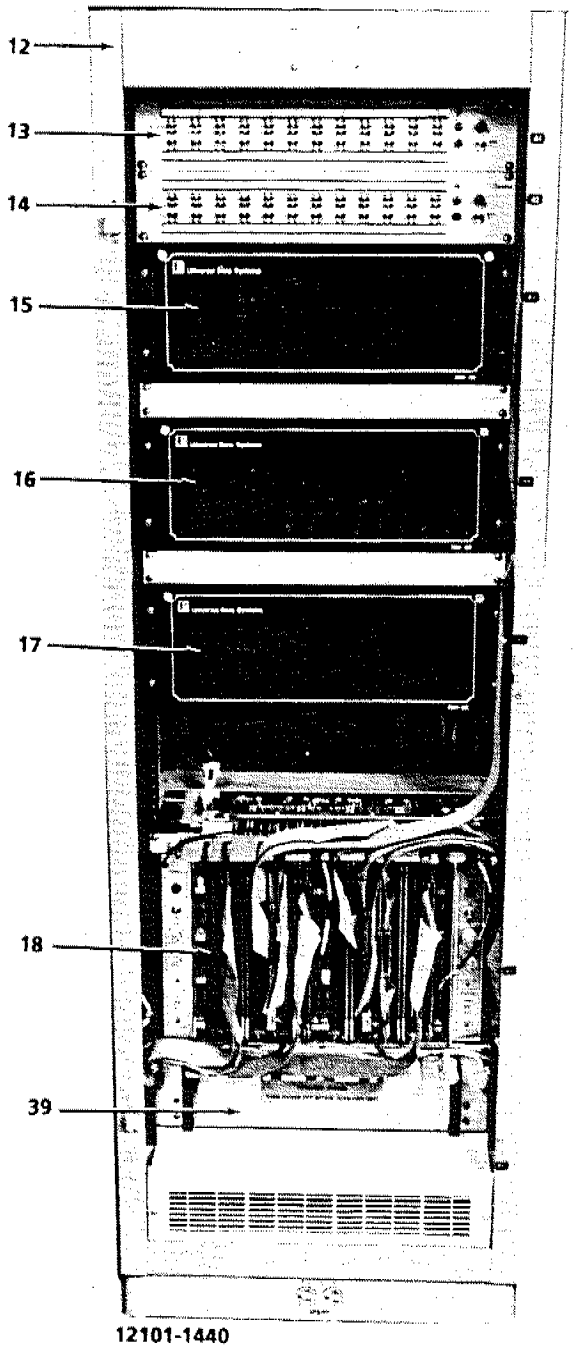


Figure 1-3. M1FC AWP Rack-Mounted Equipment (Sheet 1 of 7)
(Communications Equipment Rack)



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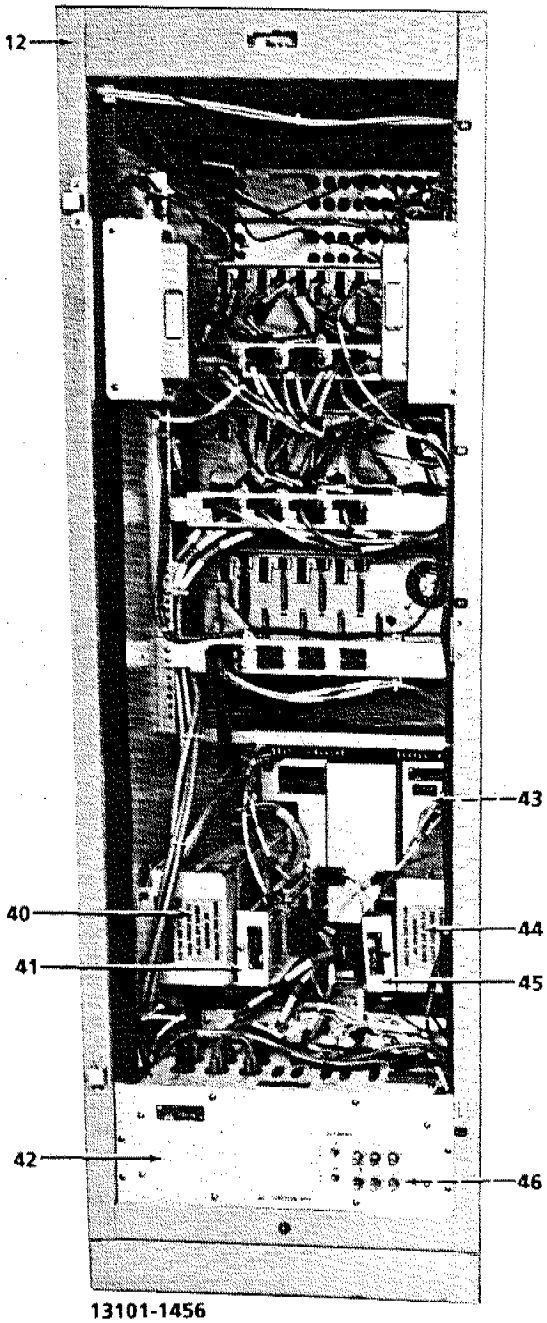
FRONT VIEW



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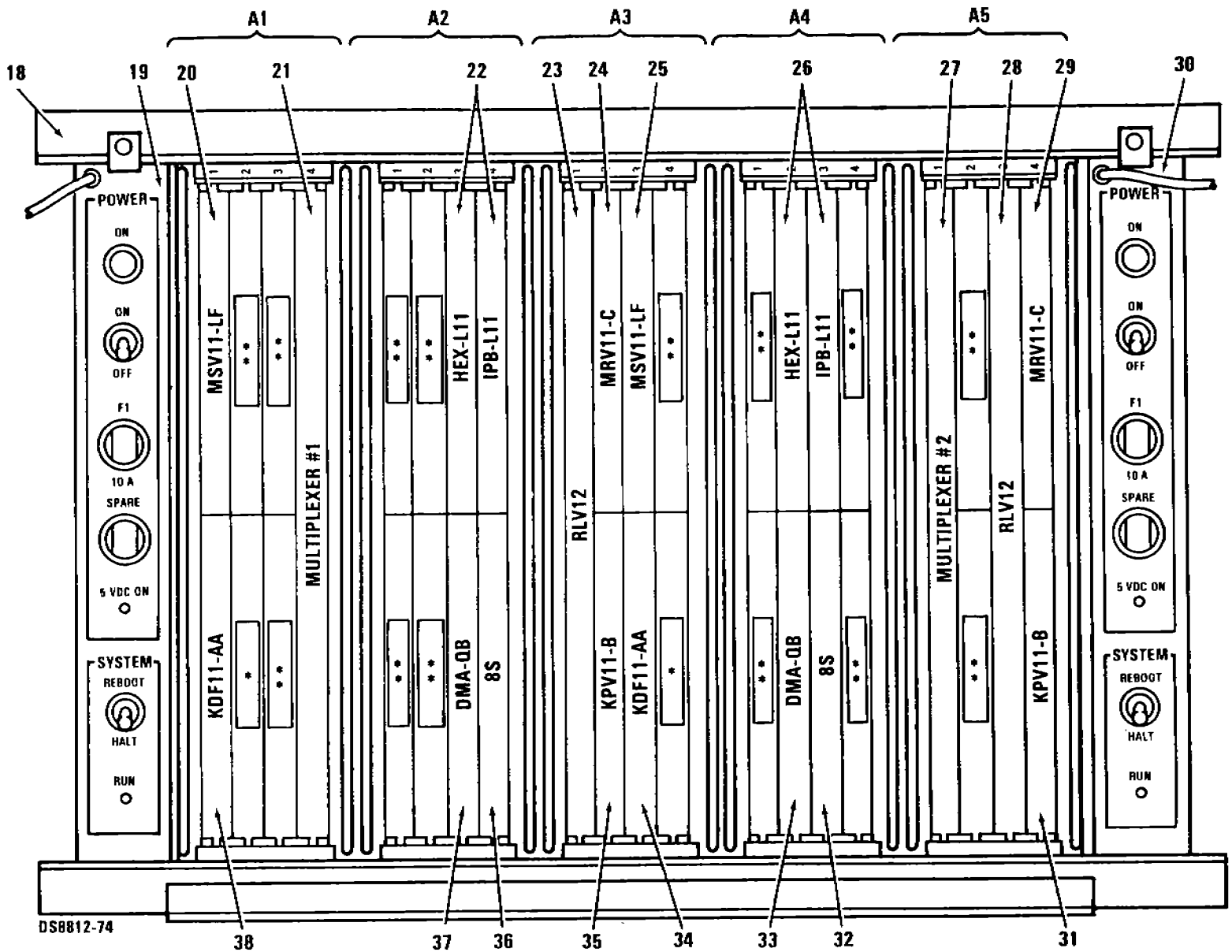
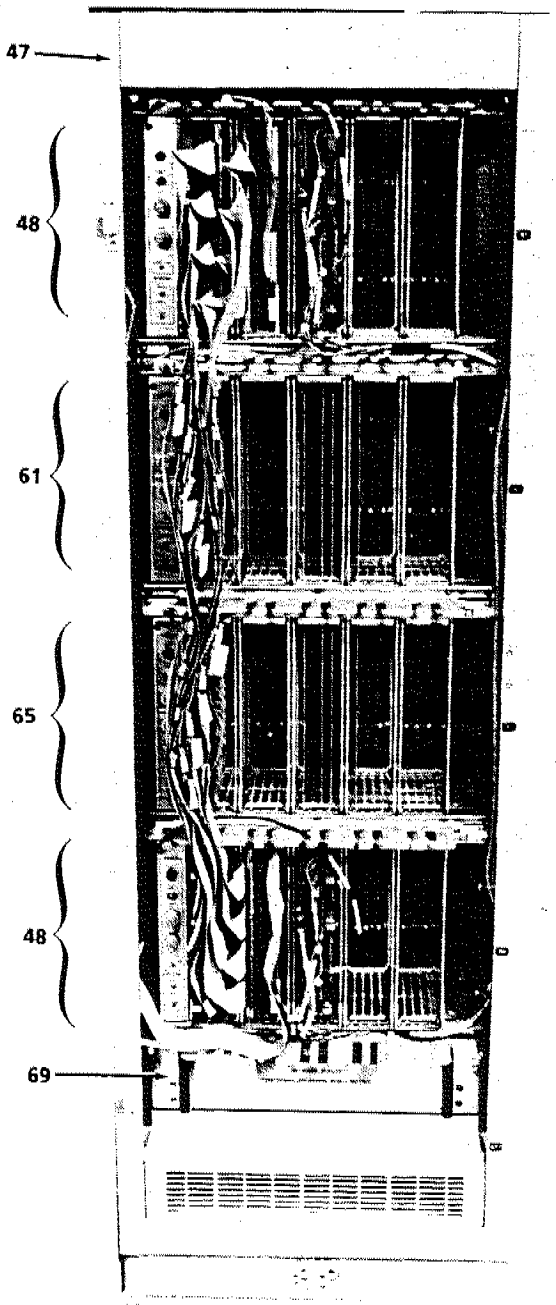
REAR VIEW

Figure 1-3. M1FC AWP Rack-Mounted Equipment (Sheet 2 of 7)
(Communications Processor Rack)



* BUS GRANT BOARD 401-37909-09
** BUS GRANT BOARD 401-37909-10

Figure 1-3. M1FC AWP Rack-Mounted Equipment (Sheet 3 of 7)
(Dual Communications Processor Card Cage)



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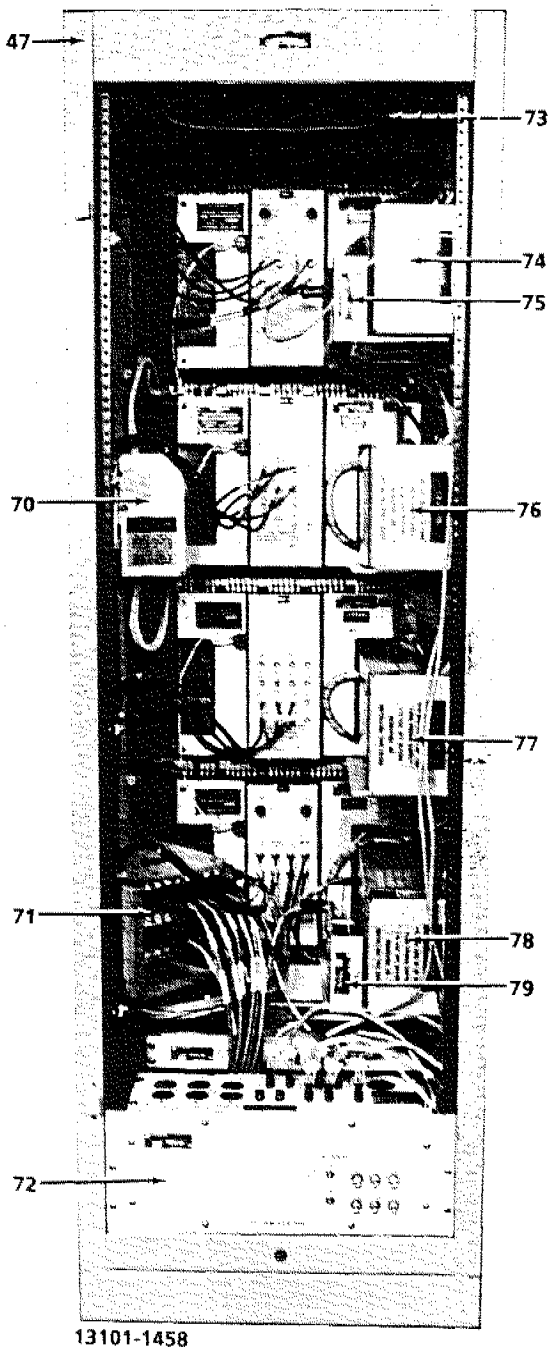
FRONT VIEW



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REAR VIEW

Figure 1-3. M1FC AWP Rack-Mounted Equipment (Sheet 4 of 7)
(Position Processor Rack)

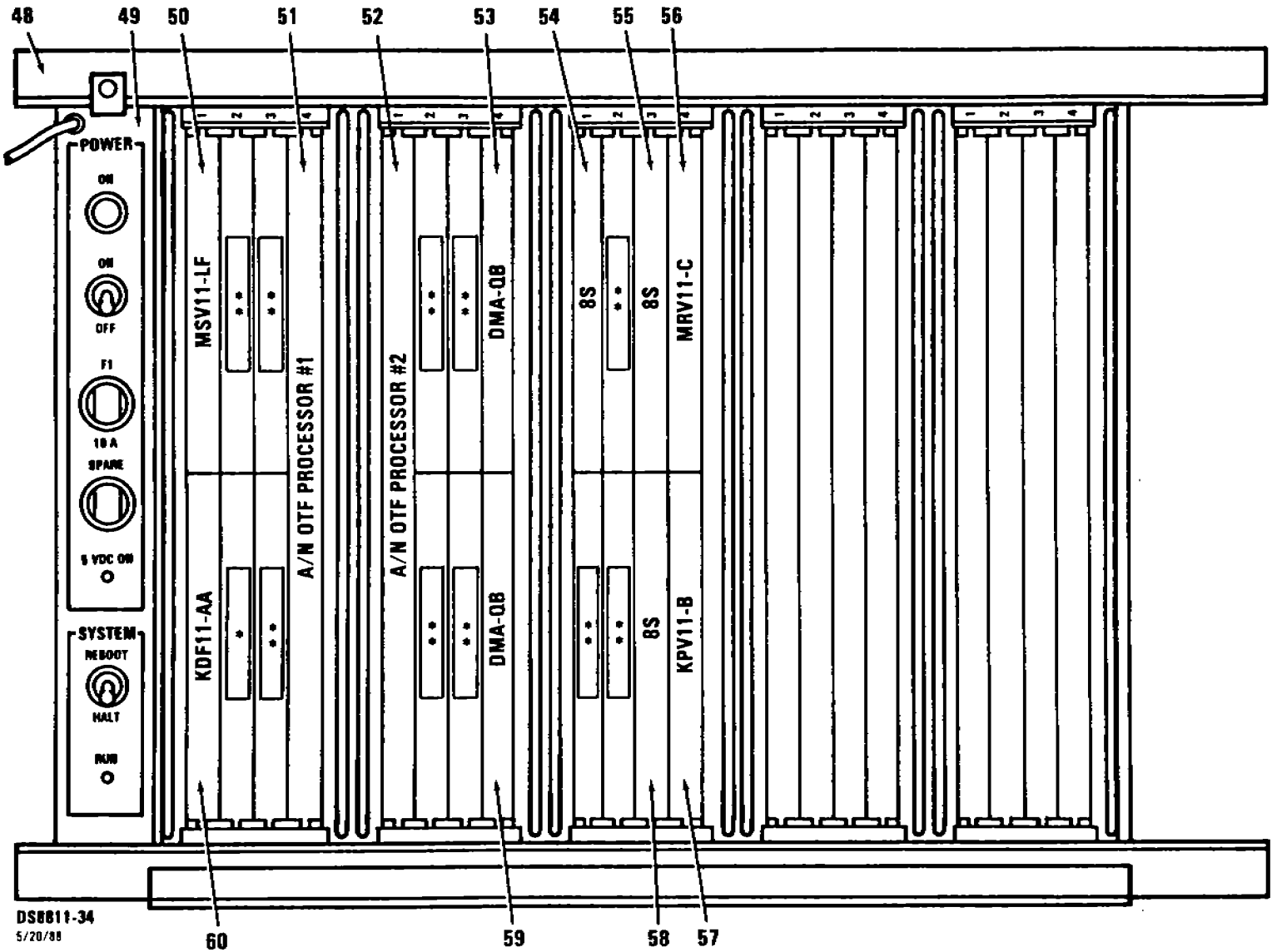
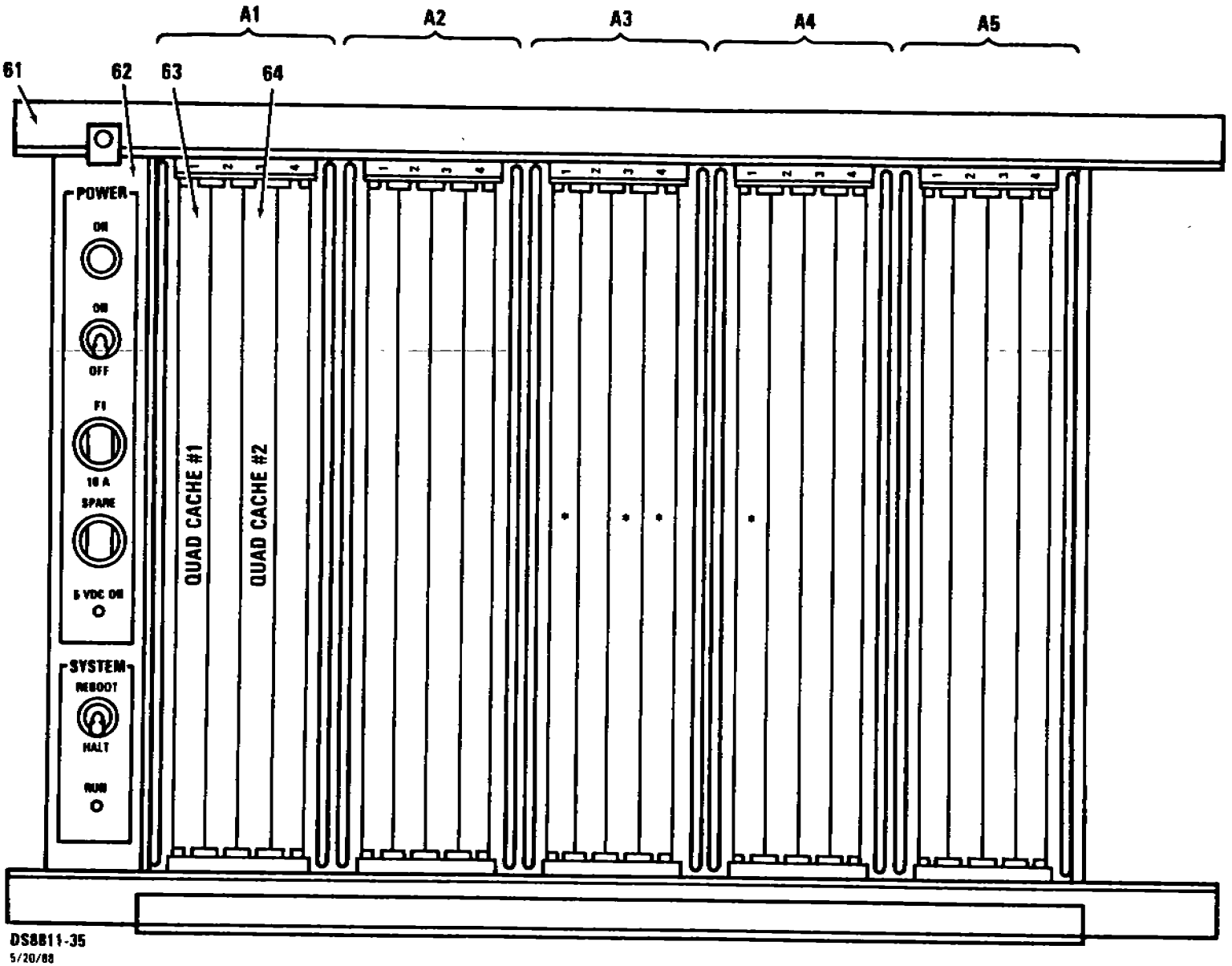


Figure 1-3. M1FC AWP Rack-Mounted Equipment (Sheet 5 of 7)
(Position Processor Card Cage)



* GRAPHICS VIDEO JUMPER 401-37925-01

Figure 1-3. M1FC AWP Rack-Mounted Equipment (Sheet 6 of 7)
(Memory Card Cage "A")

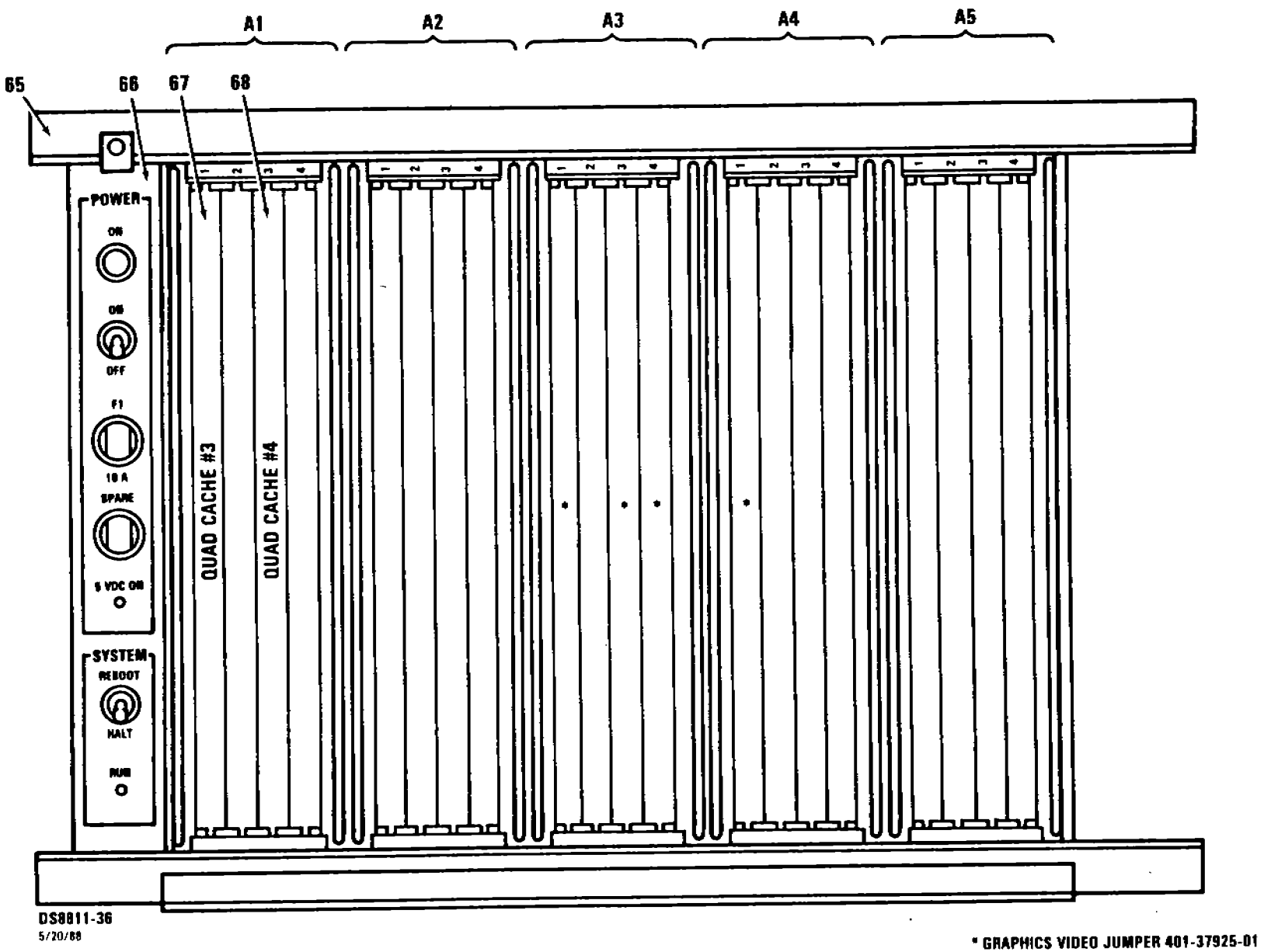


Figure 1-3. M1FC AWP Rack-Mounted Equipment (Sheet 7 of 7)
(Memory Card Cage "B")

Table 1-3. AWP Equipment

Item No. Fig. 1-3)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
1	AWP Communications Equipment Rack	UNIT 1	401-12301-01	E-Systems
2	Coded Time Source	1A1	60-DC	True Time
3	Coded Time Source Interface	1A2	401-37207-01	E-Systems
4	Coded Time Source	1A3	60-DC	True Time
5	Thermal Alarm Unit	1A4	401-37155-01	E-Systems
6	Digital Patch Panel	1A5	157-002C-00	Dynatech
7	Digital Patch Panel	1A6	157-002C-00	Dynatech
8	Digital Patch Panel	1A7	157-002C-00	Dynatech
9	Disk Drive	1A8	RL01-AK/RL02-AK	Digital Equipment
10	Disk Drive	1A9	RL01-AK/RL02-AK	Digital Equipment
11	Circuit Breaker AC Junction Box	1A16	401-37231-01	E-Systems
12	AWP Communications Processor Rack	UNIT 2	401-12302-01	E-Systems
13	Analog Patch Panel	2A1	153-020-12VF-M1	Dynatech
14	Analog Patch Panel	2A2	153-020-12VF-M1	Dynatech
15	Modem Enclosure	2A3	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem (8)		RM-9600E FP	Universal Data Systems
16	Modem Enclosure	2A4	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem (8)		RM-9600	Universal Data Systems
17	Modem Enclosure	2A5	RM-8E	Universal Data Systems
*	Modem Power Supplies (2)			Universal Data Systems
*	Modem		RM-9600	Universal Data Systems
*	Modem		RM-9600E FP	Universal Data Systems
18	Dual Comm Processor Card Cage	2A6	401-37999-04	E-Systems
19	Power Control Module	2A6A6	401-36719-01	E-Systems
20	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
21	Multiplexer		401-36993-03	E-Systems
22	Multi-Processor Linking System		HEX/IPB-L11	Peritek
23	Disk Controller Circuit Card		RLV12	Digital Equipment
24	32K Word PROM Circuit Card		MRV11-C	Digital Equipment

* Equipment is shown in manuals listed in table 1-4.

Table 1-3. AWP Equipment (Continued)

Item No. (Fig. 1-3)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
25	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
26	Multi-Processor Linking System		HEX/IPB-L11	Peritek
27	Multiplexer		401-36993-03	E-Systems
28	Disk Controller Circuit Card		RLV12	Digital Equipment
29	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
30	Power Control Module	2A6A7	401-36719-02	E-Systems
31	System Module		KPV11-B	Digital Equipment
32	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
33	DMA Controller		DMA-QB	Peritek
34	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment
35	System Module		KPV11-B	Digital Equipment
36	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
37	DMA Controller		DMA-QB	Peritek
38	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment
39	Blower Assembly	2A17	401-37145-02	E-Systems
40	Power Supply Assembly	2PS6	401-36716-01	E-Systems
41	Multiplexer Interface Assembly	2A8	401-37170-01	E-Systems
42	Fan AC Junction Box	2A16	401-37231-02	E-Systems
43	Thermal Sensor	2A18	401-37216-02	E-Systems
44	Power Supply Assembly	2PS3	401-36716-01	E-Systems
45	Multiplexer Interface Assembly	2A7	401-37170-04	E-Systems
46	Thermal Sensor	2A19	401-37204-01	E-Systems
47	AWP Position Processor Rack	UNIT 3	401-12303-01	E-Systems
48	Position Processor Card Cage	3A1	401-37999-01	E-Systems
49	Power Control Module	3A1A6	401-36719-01	E-Systems
50	64K Word RAM/Parity Circuit Card		MSV11-LF	Digital Equipment
51	A/N OTF Processor Circuit Card		401-33676-01	E-Systems
52	A/N OTF Processor Circuit Card		401-33676-01	E-Systems
53	DMA Controller Circuit Card		DMA-QB	Peritek
54	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
55	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
56	32K Word PROM Circuit Card		MRV11-C	Digital Equipment
57	System Module		KPV11-B	Digital Equipment

* Equipment is shown in manuals listed in table 1-4.

Table 1-3. AWP Equipment (Continued)

Item No. (Fig. 1-3)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
58	Eight-Channel Serial I/O Circuit Card		8S	Technical Magic
59	DMA Controller Circuit Card		DMA-QB	Peritek
60	LSI-11 Processor Circuit Card		KDF11-AA	Digital Equipment
61	Memory Card Cage "A"	3A2	401-37999-02	E-Systems
62	Power Control Module	3A2A6	401-36719-05	E-Systems
63	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
64	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
65	Memory Card Cage"B"	3A3	401-37999-06	E-Systems
66	Power Control Module	3A3A6	401-36719-05	E-Systems
67	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
68	A/N Quad Cache Memory Circuit Card		401-33692-01	E-Systems
69	Blower Assembly	3A17	401-37145-02	E-Systems
70	DC Power Switch Assembly	3S1	401-37916-01	E-Systems
71	Keyboard Junction Box	3A10	401-37179-01	E-Systems
72	Fan AC Junction box	3A16	401-37231-02	E-Systems
73	Thermal Sensor	3A18	401-37216-02	E-Systems
74	Power Supply Assembly	3PS7	401-36716-01	E-Systems
75	Serial I/O Assembly	3A8	401-37274-02	E-Systems
76	Power Supply Assembly	3PS1	401-36716-01	E-Systems
77	Power Supply Assembly	3PS3	401-36716-01	E-Systems
78	Power Supply Assembly	3PS5	401-36716-01	E-Systems
79	Serial I/O Assembly	3A9	401-37274-02	E-Systems
	Tandem Group		401-42690-04	E-Systems
*	Processor		T16/1420	Tandem
*	Disk Controller		T16/3106	Tandem
*	Asynchronous Controller		T16/6303	Tandem
*	Asynchronous Extension Board		T16/6304	Tandem
*	Asynchronous Patch Panel		T16/7501	Tandem
*	Byte Synchronous Controller		T16/6202	Tandem
*	Bit Synchronous Controller		T16/6203	Tandem
*	Synchronous Patch Panel		T16/7502	Tandem

* Equipment is shown in manuals listed in table 1-4.

Table 1-3. AWP Equipment (Continued)

Item No. (Fig. 1-3)	Nomenclature	Reference Designator	Part/Model Number	Manufacturer
*	Magnetic Tape Controller		T16/3106	Tandem
*	Magnetic Tape Drive		T16/5103	Tandem
*	Disk Patch Panel		T16/7504	Tandem
*	Operations and Service Processor (OSP)		T16/3910	Tandem
*	Video Display and Keyboard		T16/6530	Tandem
*	Printer		T16/5520	Tandem
*	Data Modem		T212A	Tandem
	Peripheral Group		401-12305-01	E-Systems
*	Input/Output Terminal (IOT)		LA34/LA100	Digital Equipment
*	Line Printers (2)		P300	Printronix
*	Keyboard Units (12)		401-36735-03	E-Systems
*	Keyboard Power Supplies (12)		5305-000-423	Ault
*	CRT Monitors (12)		401-37290-01	Ball Brothers/E-Systems
*	Disk Drives (8)		DM9300TD	Ampex

* Equipment is shown in manuals listed in table 1-4.

The following paragraphs describe the equipment located in the Communications Switching Rack. The relationship of the equipment used in the rack is shown in figure 1-4.

1.2.1.1.1 Coded Time Source. - The Coded Time Source, 60-DC, provides an accurate digital output of the time of day and Julian date. Two of these units are provided in the communications switching rack with both outputs applied to the coded time source interface. Consult the manual listed in table 1-4 for a detailed description of the coded time source.

1.2.1.1.2 Coded Time Source Interface. - The Coded Time Source Interface, 401-37207-01, is shown in figure 1-7. It is used within the FSDPS to provide accurate time and date information in a format compatible with the Tandem group.

1.2.1.1.3 Thermal Alarm Unit. - The Thermal Alarm Unit, 401-37155-01, is shown in figure 1-8. This unit visually and audibly monitors overheating conditions within equipment racks containing thermal sensors. The thermal alarm unit contained in the communications switching rack monitors the thermal sensors located in the COTC processor rack.

1.2.1.1.4 Digital Patch Panel. - The Digital Patch Panel, 157-002C-00, patches digital signals coming to and from modem equipment. Six digital patch panels are provided in the maximum configured communications switching rack. Consult the manual specified in table 1-4 for a detailed description of the digital patch panel.

1.2.1.1.5 Disk Drive. - The Disk Drive can be either an RL01-AK or an RL02-AK. The RL01-AK Disk Drive provides 5.2 MB (megabytes) of disk memory compatible with the LSI-11/23 Microcomputer System, while the RL02-AK Disk Drive provides 10.4 MB of disk memory. This disk drive provides disk storage for the COTC processor. Consult the manual specified in table 1-4 for a detailed description of the disk drive.

1.2.1.1.6 Circuit Breaker AC Junction Box. - The Circuit Breaker AC Junction Box, 401-37231-01, is shown in figure 1-9. This junction box is connected to primary AC power and has the capability to connect or disconnect AC power to or from the following equipment in the FSDPS:

1. Communications Switching Rack, 401-37622
2. Communications Equipment Rack, 401-37623
3. COTC Processor Rack, 401-37624
4. Utility Outlets on above three racks.

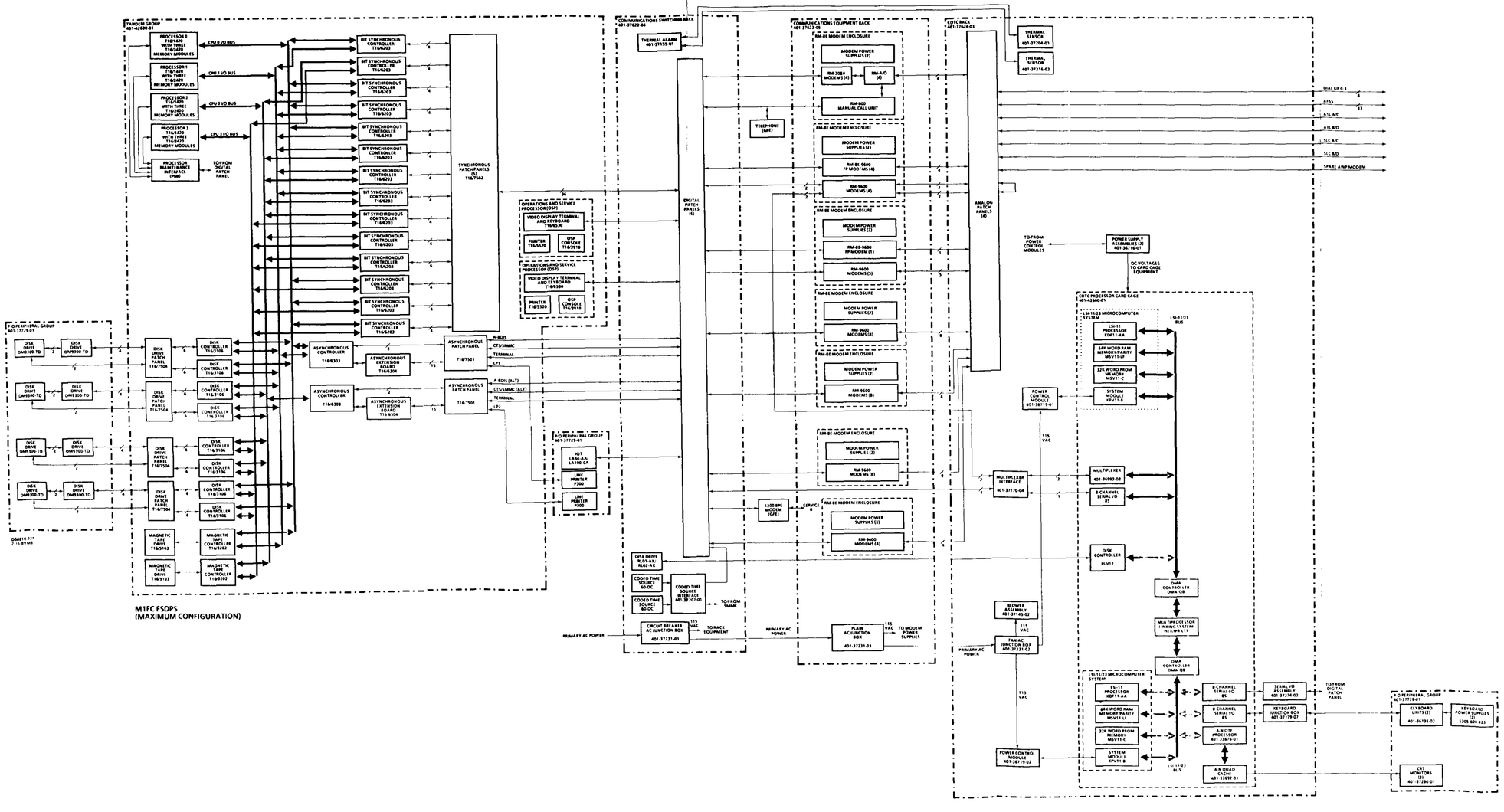


Figure 1-4. M1FC FSDPS Relationship of Equipment

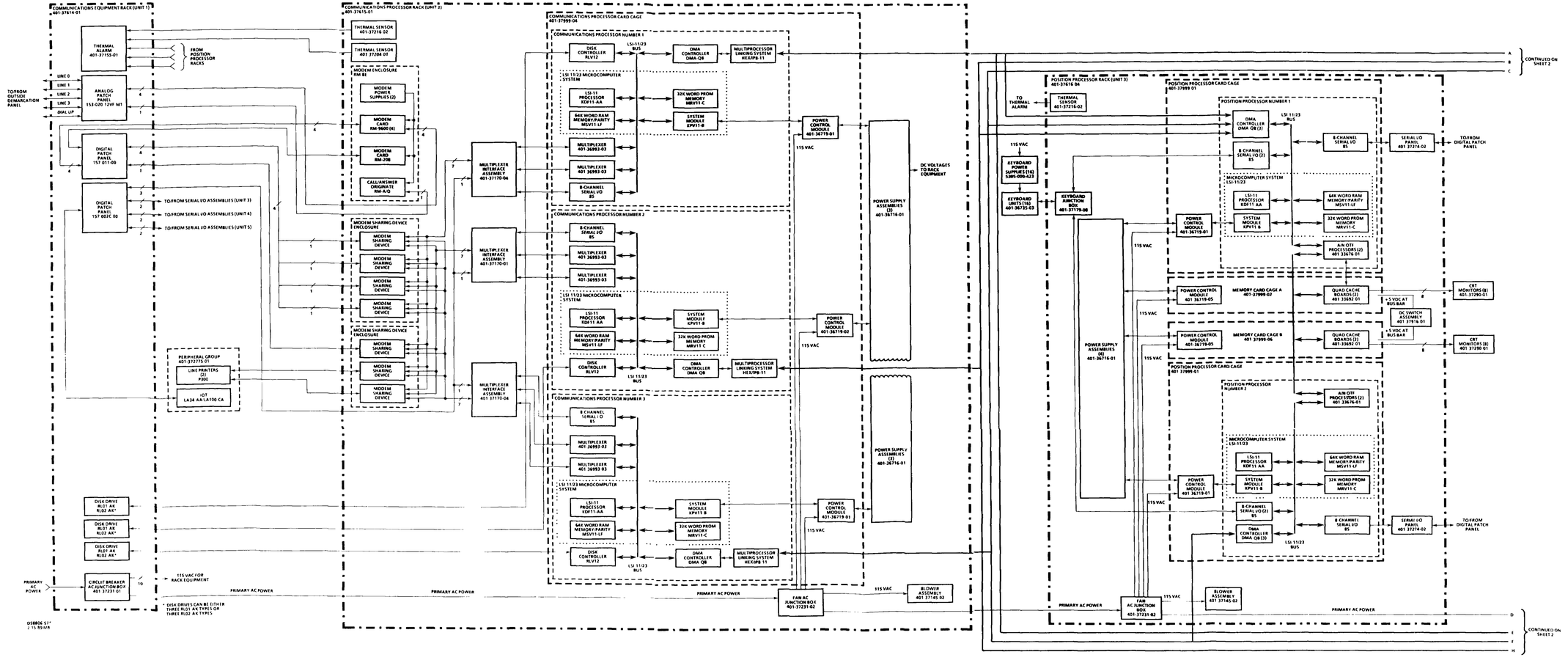


Figure 1-5. M1FC AFSS Relationship of Equipment (Sheet 1 of 2)

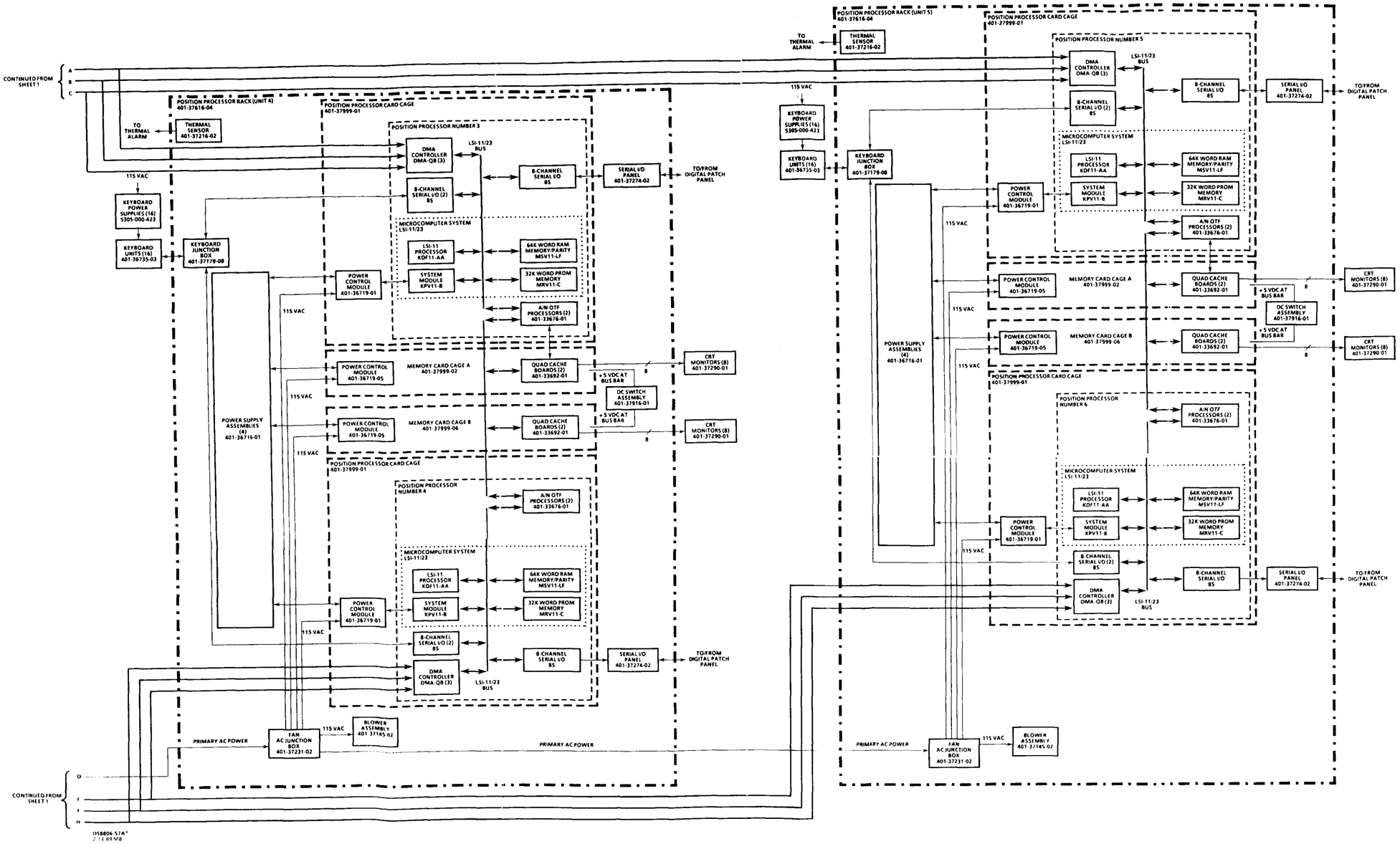


Figure 1-5. M1FC AFSS Relationship of Equipment (Sheet 2 of 2)

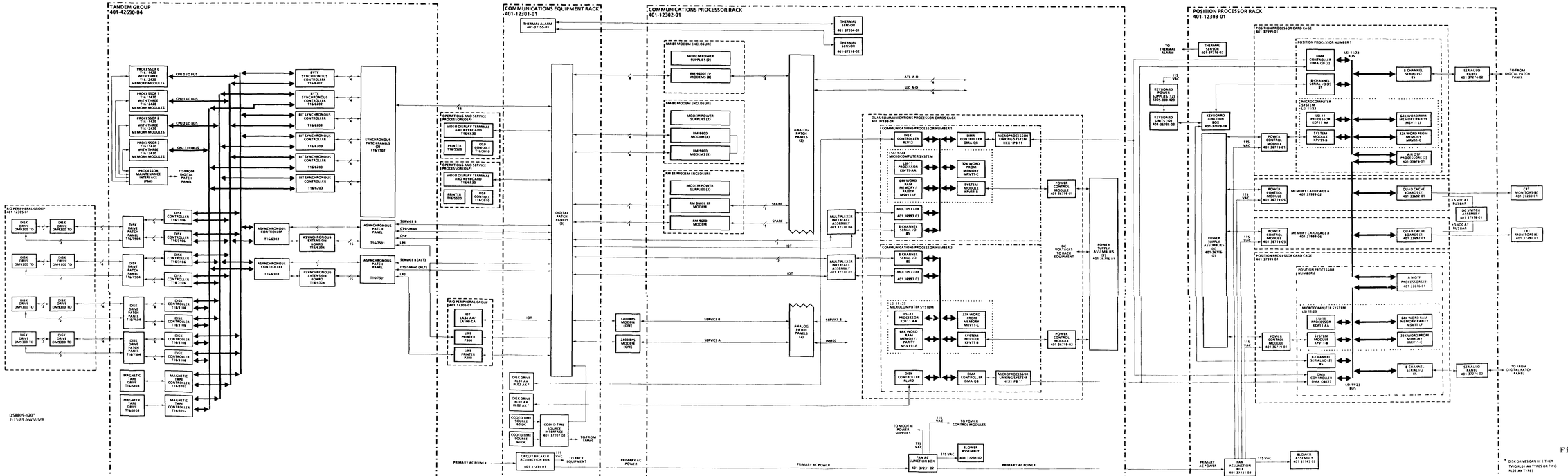


Figure 1-6. M1FC AWP Relationship of Equipment

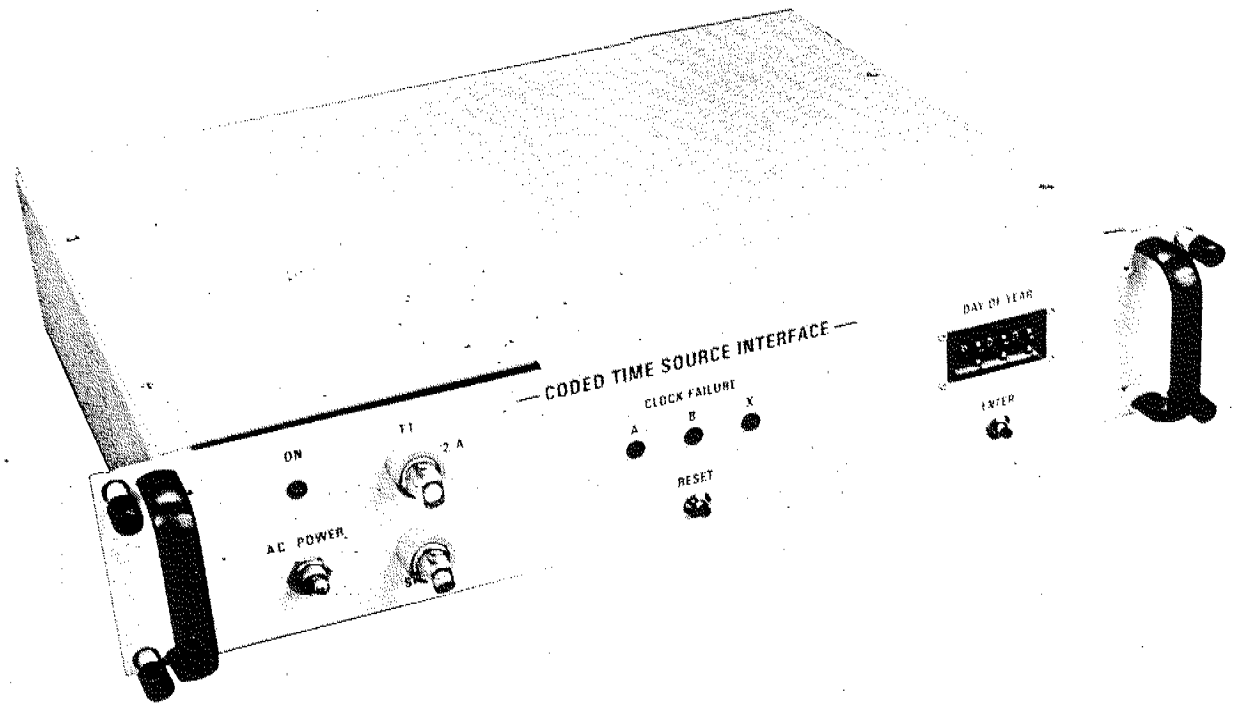


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Figure 1-7. Coded Time Source Interface, 401-37207-01

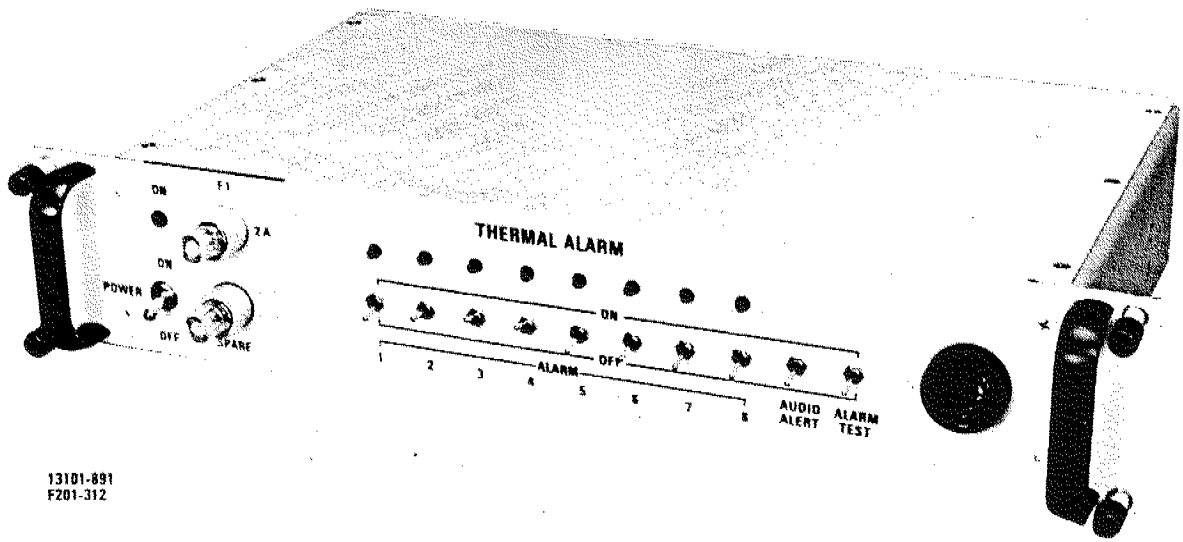

Figure 1-8. Thermal Alarm Unit, 401-37155-01

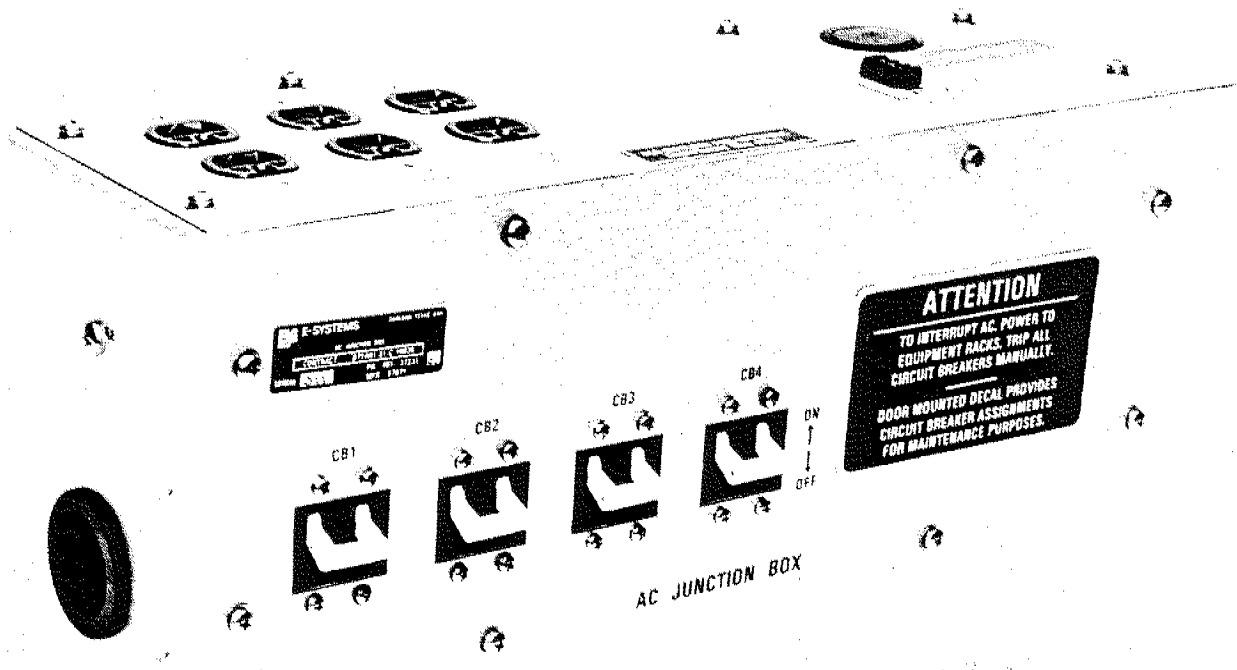

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Figure 1-9. Circuit Breaker AC Junction Box, 401-37231-01

1.2.1.2 Communications Equipment Rack. - There are five different configurations for the communications equipment rack. The E-Systems part numbers for these five configurations are 401-37623-01, -02, -03, -04, and -05. The maximum configured Communications Equipment Rack, 401-37623-05, is shown in figure 1-1. This rack is used in the FSDPS to house the following equipment:

1. Modem Enclosure, RM-8E
2. Modem Power Supplies
3. Answer/Originate Boards, RM-A/O
4. Manual Call Unit, RM-800
5. Modem, RM-208A
6. Modem, RM-9600
7. Modem, RM-9600E FP
8. Plain AC Junction Box, 401-37231-03

The following modem equipment is required for each configuration of the Communications Equipment Rack:

Equipment Rack Configuration	208 Modem	9600 Modem	RM-8E PWR. SUP.	MCU	E-A/O	9600E FP Modem
401-37623-01	1	9	6	1	1	5
401-37623-02	2-3	13-17	8	1	2-3	5
401-37623-03	4	21-25	10	1	4	5
401-37623-04	4	29-33	12	1	4	5
401-37623-05	4	37	14	1	4	5

The communications equipment rack is used in the FSDPS to house a maximum of seven RM-8E Modem Enclosures and a Plain AC Junction Box, 401-37231-03. The relationship of the equipment used in the 401-37623-05 rack is shown in figure 1-4.

1.2.1.2.1 RM-8E Modem Enclosure. - The RM-8E Modem Enclosures are used in the communications equipment rack to house the modem related equipment used in the FSDPS. This modem related equipment consists of the following modules:

1. RM-9600 Modem
2. Modem Power Supplies
3. RM-208 Modem
4. RM-800 Manual Call Unit
5. RM-A/O Answer/Originate Card
6. RM-9600E FP Modem

Consult the manual listed in table 1-4 for a detailed description of the RM-8E Modem Enclosure. Figure 1-10 provides a slot location diagram of the RM-8E Modem Enclosure.

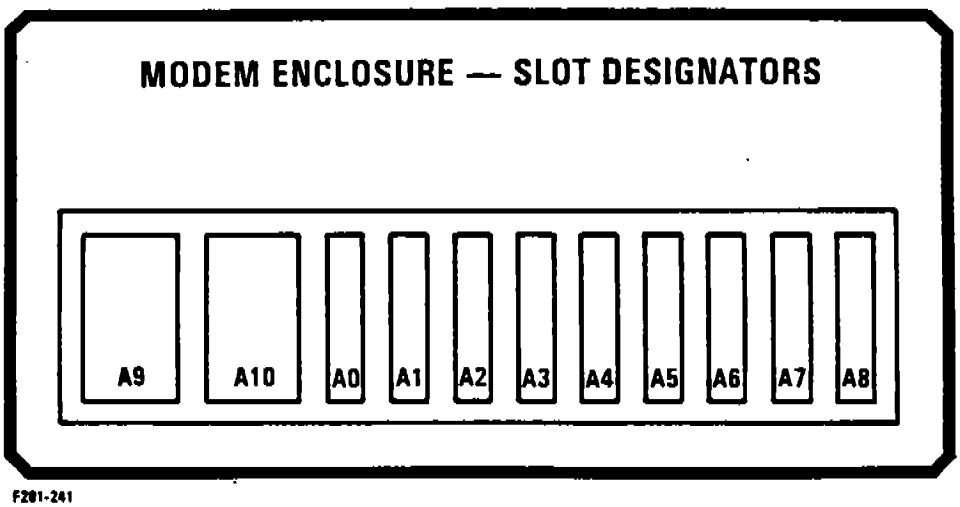


Figure 1-10. RM-8E Modem Enclosure Slot Locations

1.2.1.2.1.1 RM-9600 Modem. - The RM-9600 Modem provides 9600 bits per second (bps) conversion of digital to analog or analog to digital signals over four-wire leased telephone lines. Consult the manual listed in table 1-4 for a detailed description of the RM-9600 Modem.

1.2.1.2.1.2 Modem Power Supplies. - Two modem power supplies are provided in each RM-8E Modem Enclosure. The power supplies act redundantly to power all modules within the enclosure. Consult the manual specified in table 1-4 for a detailed description of the modem power supplies.

1.2.1.2.1.3 RM-208 Modem. - The RM-208 Modem provides 4800 bits per second conversion of digital to analog or analog to digital signals. The modem can be used with either four-wire leased telephone lines or a dial-up network. Consult the manual listed in table 1-4 for a detailed description of the RM-208 Modem.

1.2.1.2.1.4 RM-800 Manual Call Unit. - The RM-800 Manual Call Unit is used in conjunction with the RM-208 Modem to allow call-out on manual call using a dial-up network. Consult the manual listed in table 1-4 for a detailed description of the manual call unit.

1.2.1.2.1.5 RM-A/O Answer/Originate Card. - The Answer/Originate Card is used in conjunction with the RM-208 Modem to convert the modem from a four-wire private line modem to a four-wire dial modem. Consult the manual listed in table 1-4 for a detailed description of the RM-A/O Answer/Originate Card.

1.2.1.2.1.6 RM-9600E FP Modem. - The RM-9600E FP (fast poll) Modem is a fast training 9600 bit per second modem designed for use in multi-drop networks. It is used in the M1FC FSAS to provide communications channels between the AWP and FSDPS.

1.2.1.2.2 Plain AC Junction Box. - The Plain AC Junction Box, 401-37231-03, is shown in figure 1-11. Primary AC power is input to this junction box from the circuit breaker AC junction box in the communications switching rack. This junction box supplies 115 VAC to the modem power supplies used in the communications equipment rack.

1.2.1.3 COTC Processor Rack. - There are three different configurations for the COTC processor rack. The E-Systems part numbers for these three configurations are 401-37624-01, -02, and

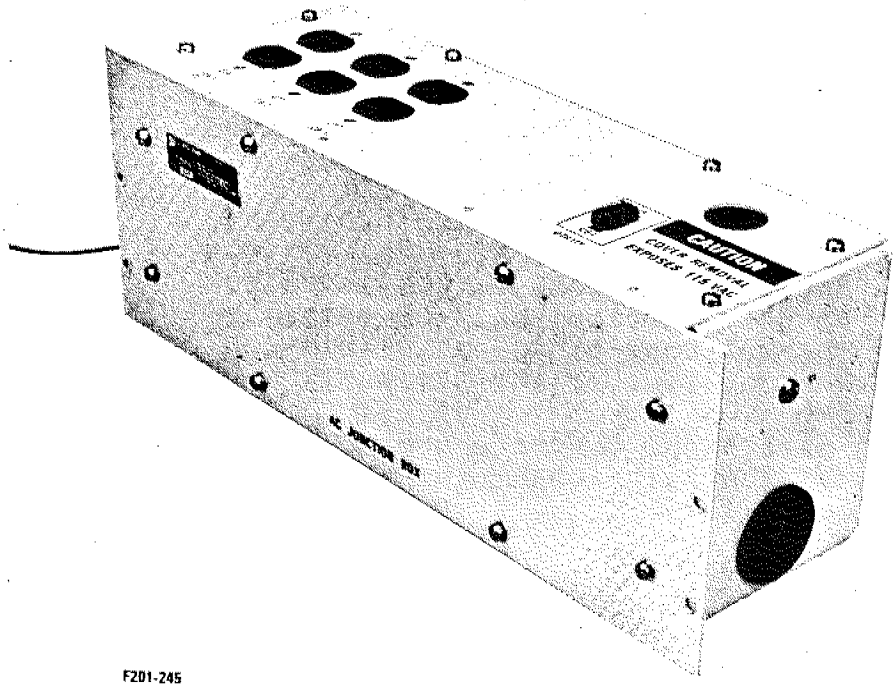


Figure 1-11. Plain AC Junction Box, 401-37231-03

-03. The maximum configured COTC Processor Rack, 401-37623-03, is shown in figure 1-1. This rack is used in the FSDPS to house the following equipment:

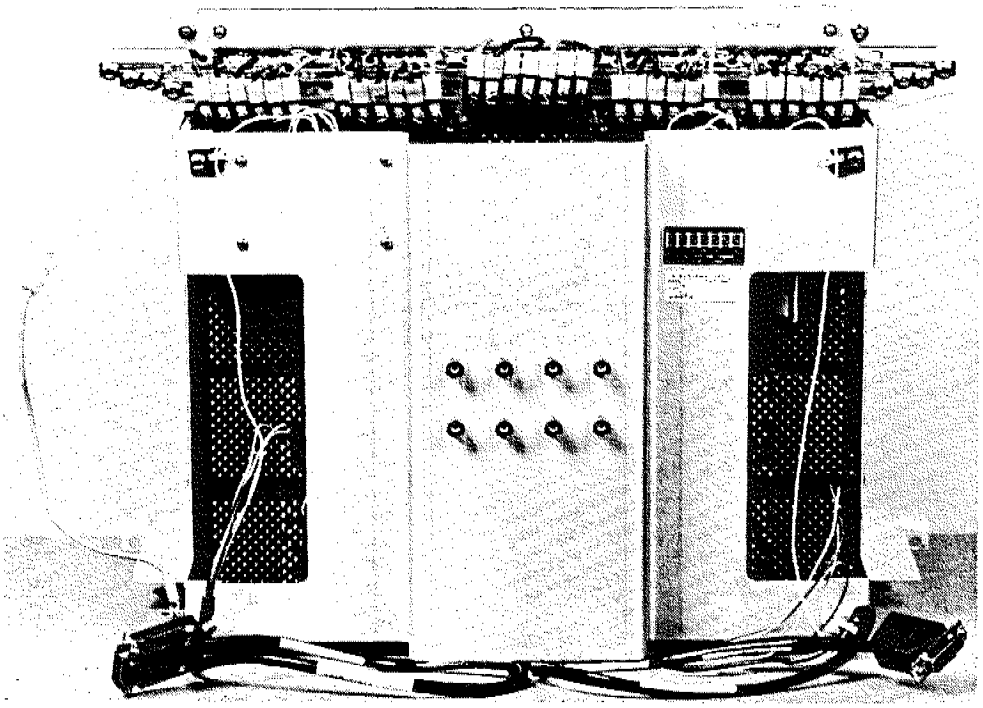
1. Analog Patch Panels, 153-020-12VF-M1
2. COTC Processor Card Cage, 401-42600-01
3. Position Processor Card Cage, 401-37999-01
4. Power Control Modules, 401-36719-01, -02
5. Multi-Processor Linking Systems, HEX/IPB-L11
6. DMA Controller Circuit Cards, DMA-QB
7. Disk Controller Circuit Card, RLV12
8. Multiplexer Circuit Card, 401-36993-03
9. Eight-Channel Serial I/O Circuit Cards, 8S
10. LSI-11 Processor Circuit Cards, KDF11-AA
11. 32K Word PROM Circuit Cards, MRV11-C
12. 64K Word RAM/Parity Circuit Cards, MSV11-LF
13. System Modules, KPV11-B
14. A/N OTF Processor Circuit Card, 401-33676-01
15. A/N Quad Cache Memory Circuit Card, 401-33692-01
16. Blower Assembly, 401-37145-02
17. DC Power Switch Assembly, 401-37916-01
18. Power Supply Assemblies, 401-36716-01
19. Keyboard Junction Box, 401-37179-07
20. Serial I/O Assembly, 401-37274-02
21. Fan AC Junction Box, 401-37231-02
22. Thermal Sensor, 401-37204-01
23. Thermal Sensor, 401-37216-02

The following paragraphs describe the equipment located in the COTC processor rack. The relationship of the equipment used in the rack is shown in figure 1-4.

1.2.1.3.1 Analog Patch Panel. - The Analog Patch Panel, 153-020-12VF-M1, patches analog signals coming to and from modem equipment. Four analog patch panels are provided in the maximum configured COTC processor rack. Consult the manual specified in table 1-4 for a detailed description of the analog patch panel.

1.2.1.3.2 COTC Processor Card Cage. - The COTC Processor Card Cage, 401-42600-01 is shown in figure 1-12. This card cage is used to house the circuit cards which make up a position processor and communications processor.

1.2.1.3.3 Power Control Module. - Three types of power control modules are used in the MIFC FSAS System (figure 1-13). One Power Control Module, 401-36719-01, is used in the first slot (from left to right) of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-02, is used in the last slot of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-05, is used in the



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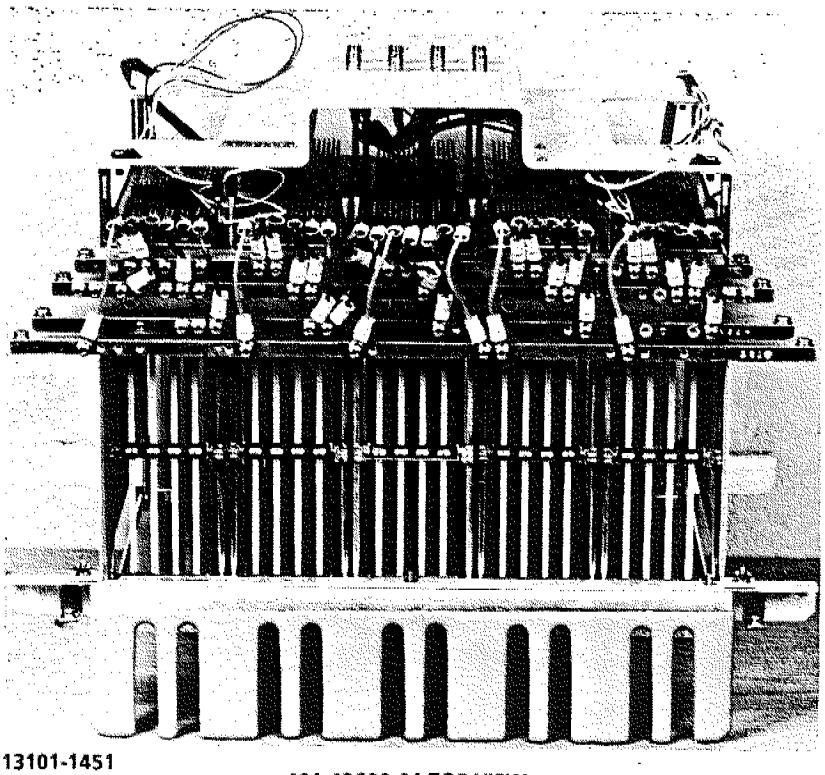
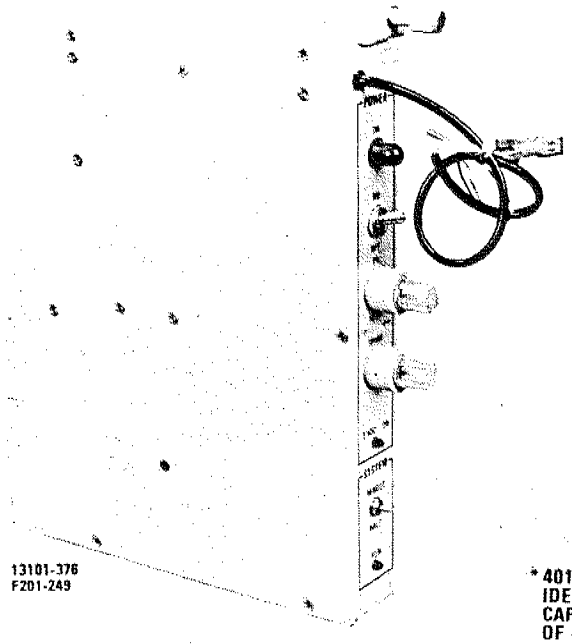
401-42600-01 REAR VIEW



13101-1451

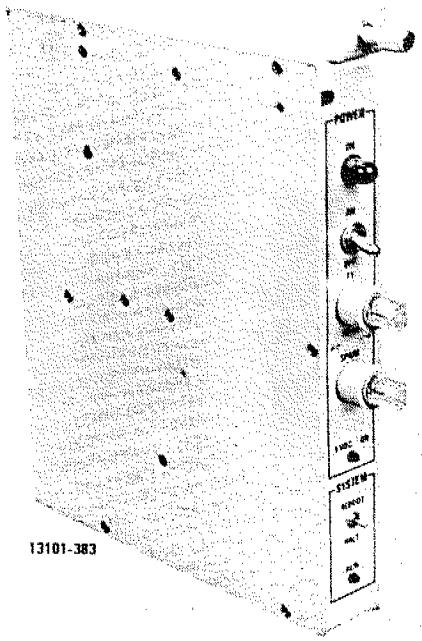
401-42600-01 TOP VIEW

Figure 1-12. COTC Processor Card Cage, 401-42600-01



*401-36719-01 AND -02 ARE ELECTRICALLY IDENTICAL. -01 MOUNTS ON LEFT SIDE OF CARD CAGE, -02 MOUNTS ON RIGHT SIDE OF CARD CAGE.

401-36719-01, -02 *



401-36719-05

Figure 1-13. Power Control Module, 401-36719-01, -02, and -05

first slot of card cages which do not contain KPV11-B System Module Circuit Cards.

The main function of the Power Control Module is to provide control and fusing for the 115 VAC between the AC junction box and power supply assemblies. The 401-36719-01 and -02 Power Control Modules contain additional wiring and connectors for interface with the KPV11-B Circuit Cards.

The COTC processor rack contains two power control modules: one of the 401-36719-01 type, and one of the 401-46719-02 type.

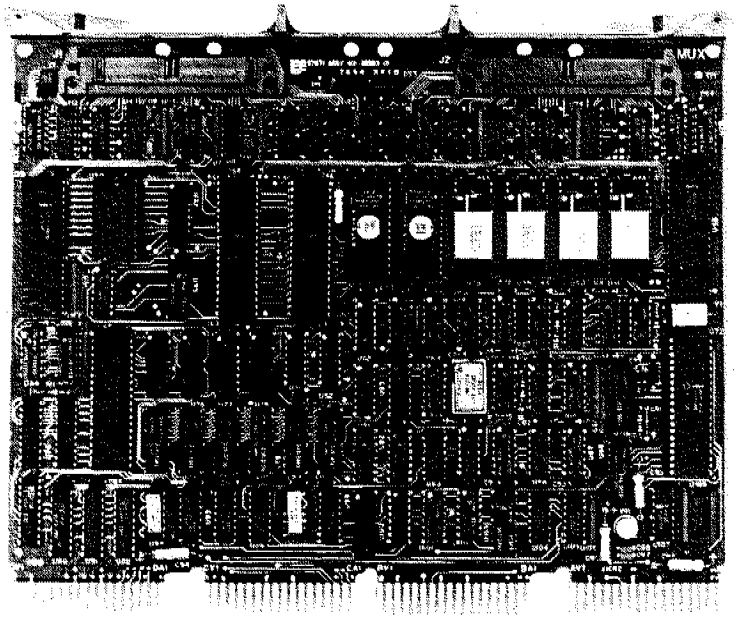
1.2.1.3.4 Multi-Processor Linking System. - The Multi-Processor Linking System, HEX/IPB-L11, contains two connected circuit cards. This system establishes six high speed communication ports between the DMA Controller Circuit Card (DMA-QB) of a communications processor and the DMA-QB Circuit Card of a position processor. One multi-processor linking system is provided in the COTC processor rack. Consult the manual listed in table 1-4 for a detailed description of the multi-processor linking system.

1.2.1.3.5 DMA Controller Circuit Card. - The DMA Controller Circuit Card, DMA-QB, provides a DMA (Direct Memory Access) interface between the LSI-11/23 bus of a position processor and the LSI-11/23 bus of a communications processor using the interprocessor bus.

Two DMA controller circuit cards are provided in the COTC processor rack. One controller is located in the position processor and the other controller is located in the communications processor. Consult the manual listed in table 1-4 for a detailed description of the DMA controller circuit card.

1.2.1.3.6 Disk Controller Circuit Card. - The Disk Controller Circuit Card, RLV12, is used to interface the RL01-AK or RL02-AK Disk Drive with the LSI-11/23 bus of a communications processor. One RLV12 circuit card is located in the COTC processor rack. This circuit card is used to interface the RL01-AK/RL02-AK Disk Drive in the communications switching rack with the communications processor's LSI-11/23 bus in the COTC processor rack. Consult the manual listed in table 1-4 for a detailed description of the RLV12 Disk Controller Circuit Card.

1.2.1.3.7 Multiplexer Circuit Card. - The Multiplexer Circuit Card, 401-36993-03, is shown in figure 1-14. This card provides a four-channel serial interface, RS449, between a communications processor's LSI-11/23 bus and external peripherals. The multiplexer circuit card located in the COTC processor rack is used to interface the communications processor's LSI-11/23 bus with the Tandem group and peripheral group of the FSDPS.



F201-250

Figure 1-14. Multiplexer Circuit Card, 401-36993-03

1.2.1.3.8 Eight-Channel Serial I/O Circuit Card. - The Eight-Channel Serial I/O Circuit Card, 8S, provides eight channels for serial input or output of data to/from the LSI-11/23 bus. The COTC processor rack contains three 8S circuit cards. One 8S circuit card is located in the communications processor and is used to interface the communications processor with peripheral equipment in the FSDPS. Two 8S circuit cards are located in the position processor. One 8S circuit card is used to interface the position processor with peripheral equipment in the FSDPS. The other 8S circuit card is used to interface two keyboards with the position processor.

1.2.1.3.9 LSI-11 Processor Circuit Card. - The LSI-11 Processor Circuit Card, KDF11-AA, performs the CPU (Central Processing Unit) function for the LSI-11/23 Microcomputer System. Two LSI-11 processor circuit cards are provided in the COTC processor rack. One processor provides the CPU function for the communications processor, and the other processor provides the CPU function for the position processor. Consult the manual listed in table 1-4 for a detailed description of the KDF11-AA circuit card.

1.2.1.3.10 32K Word PROM Circuit Card. - The 32K Word PROM Circuit Card, MRV11-C, contains 32K of PROM (Programmable Read Only Memory) in 16, 24-pin sockets. Two 32K Word PROM Circuit Cards are provided in the COTC processor rack. One of the cards provides the PROM for the communications processor and the other card provides the PROM for the position processor. Consult the manual listed in table 1-4 for a detailed description of the MRV11-C Circuit Card.

1.2.1.3.11 64K Word RAM/Parity Circuit Card. - The 64K Word RAM/Parity Circuit Card, MSV11-LF, contains 64K, 16-bit words of MOS (Metal Oxide Semiconductor) RAM (Random Access Memory) and generates and detects byte parity for each word. Two 64K word RAM/parity cards are provided in the COTC processor rack. One of the cards is used in the communications processor, and the other card is used in the position processor. Consult the manual listed in table 1-4 for a detailed description of the MSV11-LF Circuit Card.

1.2.1.3.12 System Module Circuit Card . - The System Module Circuit Card , KPV11-B, alerts the LSI-11/23 bus when a power failure occurs and restarts the LSI-11/23 Microcomputer System when power is restored. Two of these cards are provided in the COTC processor rack. One card is used in the communications processor and the other card is used in the position processor. Consult the manual listed in table 1-4 for a detailed description of the KPV11-B Circuit Card.

1.2.1.3.13 Alphanumeric (A/N) Quad Cache Memory Circuit Card. - The A/N Quad Cache Memory Circuit Card, 401-33692-01, is shown in figure 1-15. This circuit card provides alphanumeric memory for up to four CRT monitors. One A/N quad cache circuit card is used in the COTC processor rack to provide alphanumeric memory for two CRT monitors used in the FSDPS.

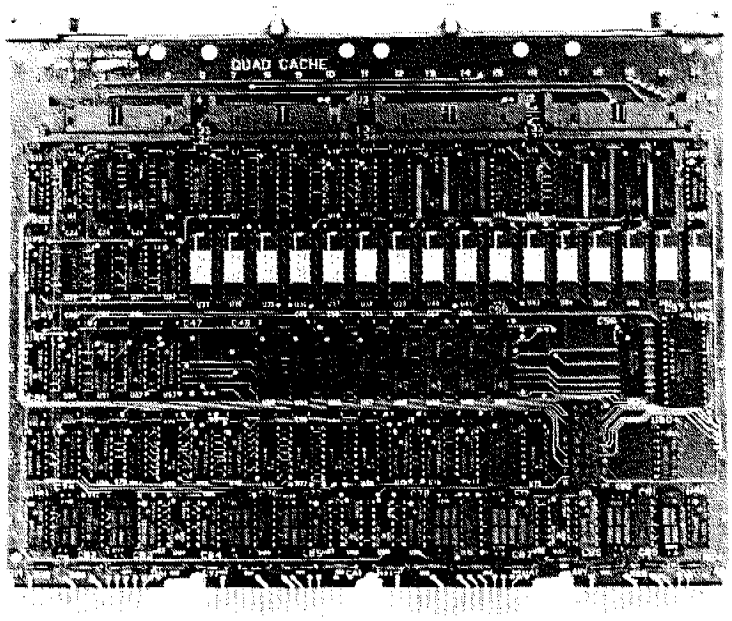
1.2.1.3.14 Alphanumeric (A/N) On-The-Fly (OTF) Processor Circuit Card. - The A/N OTF Processor Circuit Card, 401-33676-01, is shown in figure 1-16. This circuit card processes and controls alphanumeric data to and from the A/N quad cache. It acts as an interface between the A/N quad cache and the LSI-11/23 bus. One A/N OTF processor circuit card is provided in the COTC processor rack to interface the A/N quad cache with the LSI-11/23 bus in the position processor.

1.2.1.3.15 Blower Assembly. - The Blower Assembly, 401-37145-02, is shown in figure 1-17. This assembly uses fans to provide air circulation inside the COTC processor rack. The blower assembly is powered by 115 VAC from the fan AC junction box.

1.2.1.3.16 Multiplexer Interface Assembly. - The Multiplexer Interface Assembly, 401-37170-01 and -04, is shown in figure 1-18. This assembly provides eight RS-449 compatible connectors which interface the Multiplexer Circuit Card, 401-36993-03, with desired equipment such as digital patch panels and modems. Two circuit cards are provided in the multiplexer interface assembly to provide appropriate signal levels for the RS-449 interface. Four RS-232C compatible connectors are provided on the multiplexer interface assembly to provide an interface between an 8S Circuit Board and devices such as line printers and character printers.

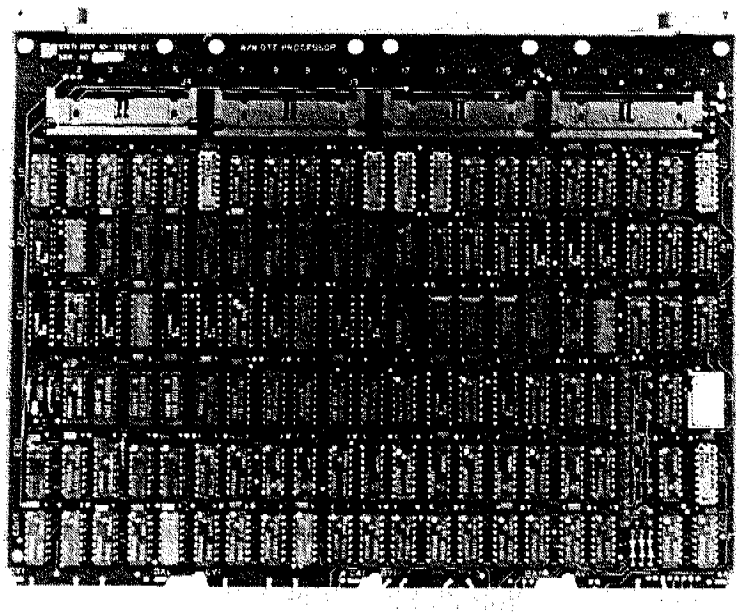
One type of Multiplexer Interface Assembly, 401-37170-01, is used when the assembly is mounted in the right side of a cabinet. The other type of Multiplexer Interface Assembly, 401-37170-04, is used when the assembly is mounted in the left side of a cabinet. Both types are electrically identical. One Multiplexer Interface Assembly, 401-37170-04, is used in the COTC processor rack.

1.2.1.3.17 Power Supply Assembly. - The Power Supply Assembly, 401-36716-01, is shown in figure 1-19. The power supply assembly provides +5VDC, +12VDC, -12VDC, and signal ground for use by rack equipment. The COTC processor rack contains two power supply assemblies. Consult the manual listed in table 1-4 for a detailed description of the power supply assembly.



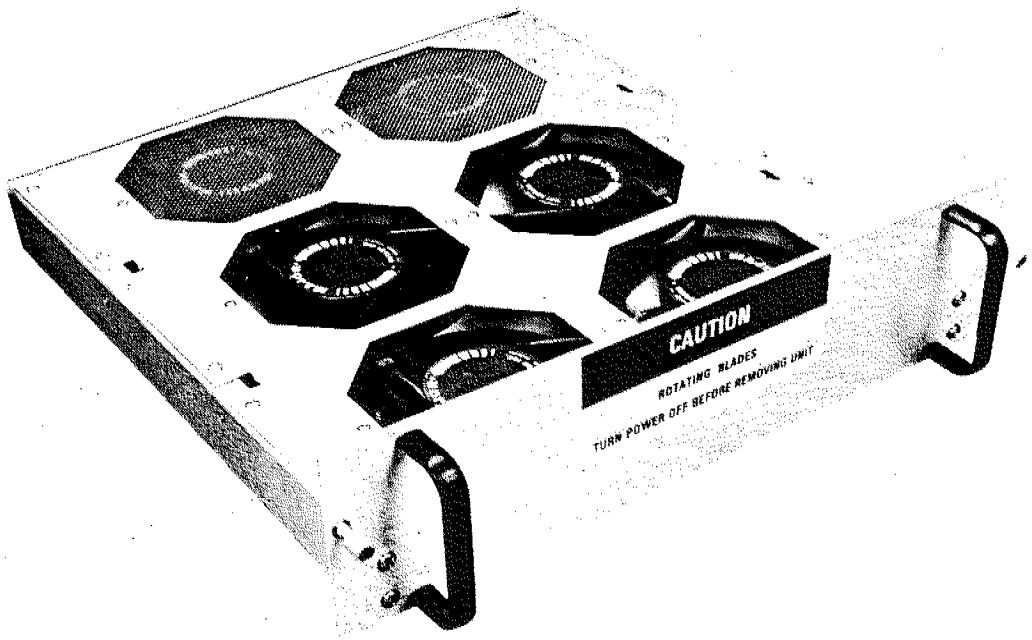
F201-251

Figure 1-15. A/N Quad Cache Memory Circuit Card, 401-33692-01



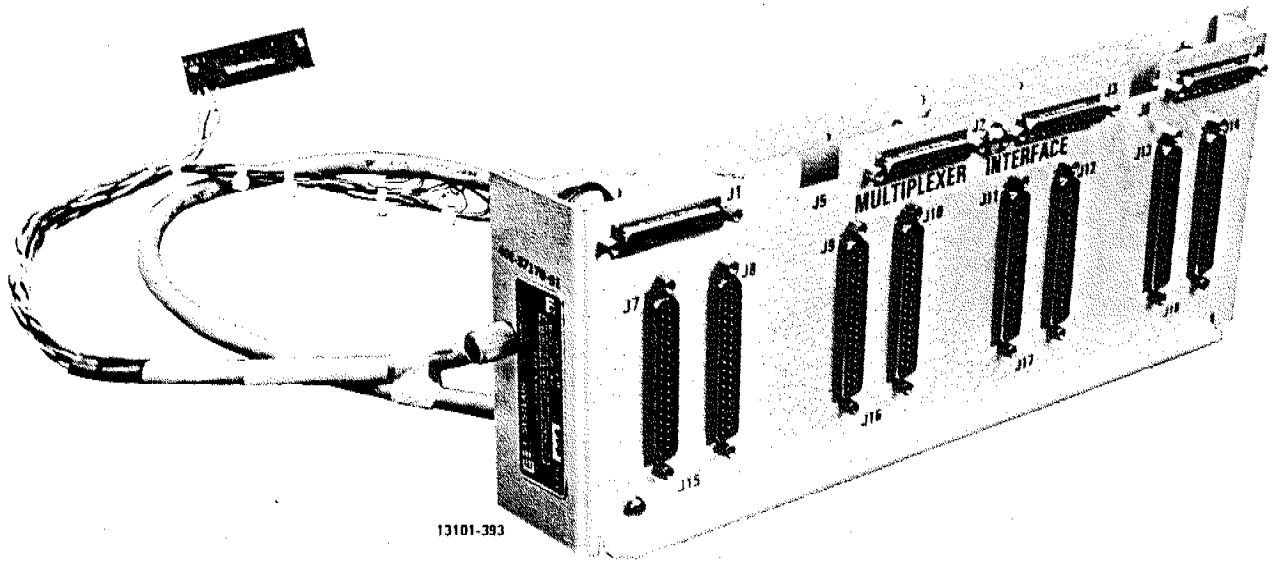
F201-252

Figure 1-16. A/N OTF Processor Circuit Card, 401-33676-01

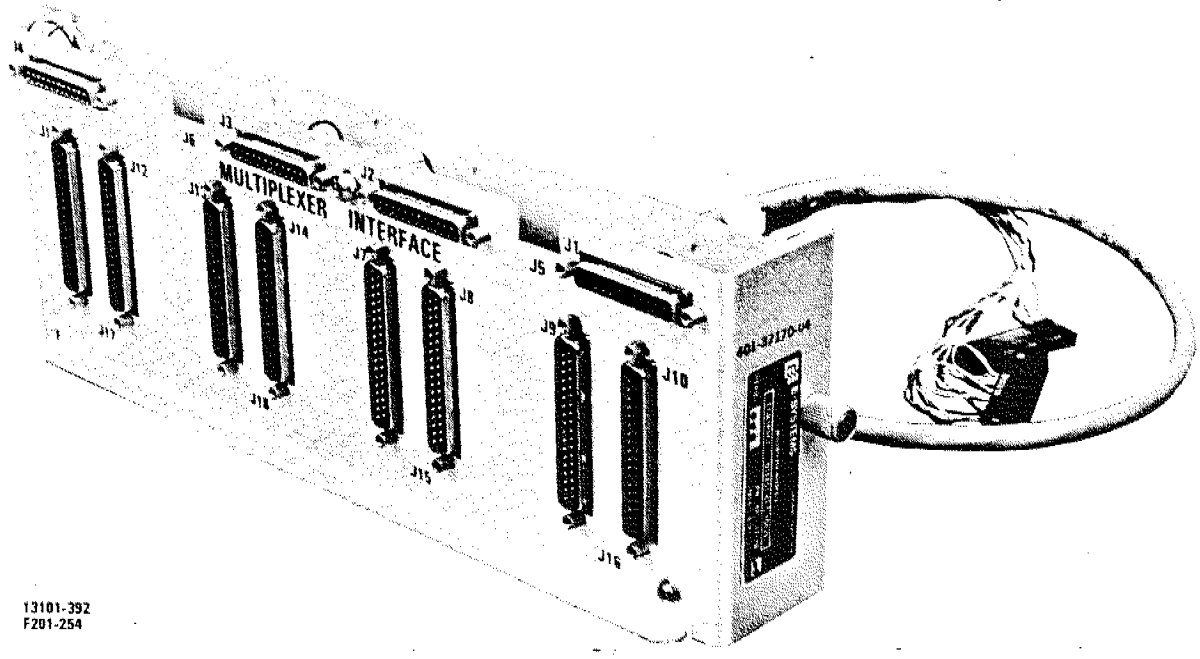


F201-253

Figure 1-17. Blower Assembly, 401-37145-02

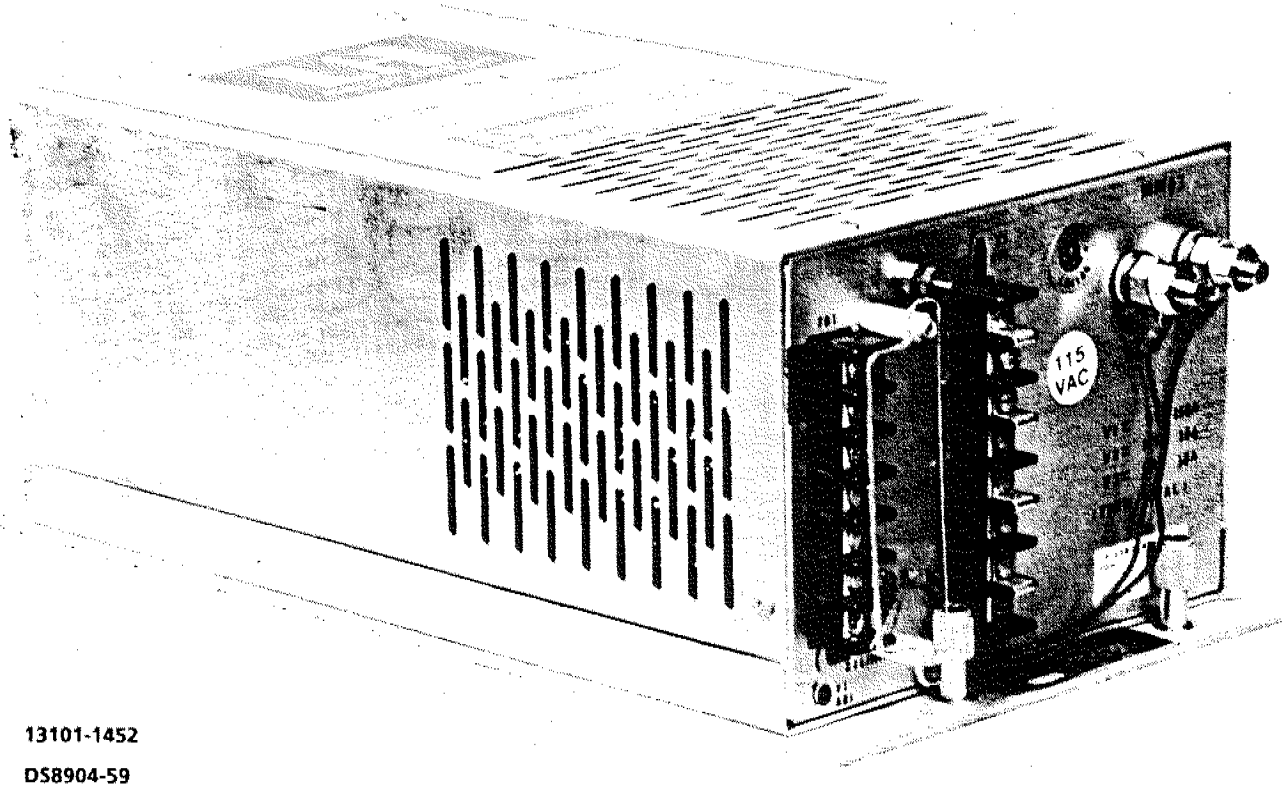


401-37170-01



401-37170-04

Figure 1-18. Multiplexer Interface Assembly, 401-37170-01 and -04



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DS8904-59

Figure 1-19. Power Supply Assembly, 401-36716-01

1.2.1.3.18 Keyboard Junction Box. - The Keyboard Junction Box, 401-37179-07 and -08, is shown in figure 1-20. This unit is used as an interface between keyboard units and eight-channel serial I/O circuit cards. One type of Keyboard Junction Box, 401-37179-07, can interface a maximum of eight keyboard units and two eight-channel serial I/O circuit cards. The other type of Keyboard Junction Box, 401-37179-08, can interface a maximum of 16 keyboard units and four eight-channel serial I/O circuit cards. One Keyboard Junction Box, 401-37179-07, is used in the COTC processor rack.

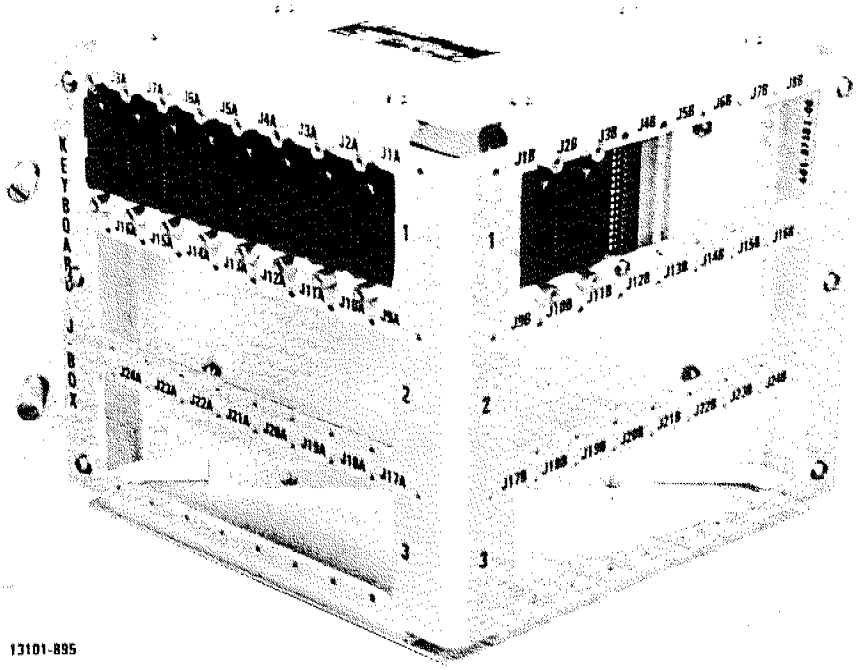
1.2.1.3.19 Serial I/O Assembly. - The Serial I/O Assembly, 401-37274-01, is shown in figure 1-21. The serial I/O assembly is provided for connections between digital patch panels and an eight-channel serial I/O circuit card. The COTC processor rack contains one serial I/O assembly which connects an eight-channel serial I/O circuit card in the position processor to a digital patch panel.

1.2.1.3.20 Fan AC Junction Box. - The AC junction box in the COTC processor rack is the Fan AC Junction Box, 401-37231-02, shown in figure 1-22. This junction box receives primary AC power from the Plain AC junction box in the communications equipment rack and distributes 115 VAC to two power control modules and the blower assembly in the COTC processor rack.

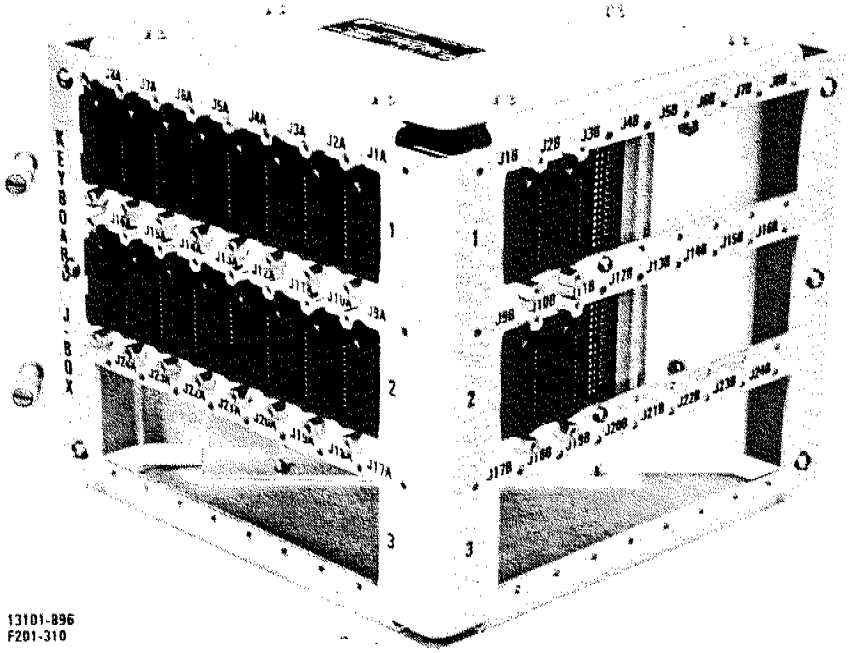
1.2.1.3.21 Thermal Sensors. - The Thermal Sensors, 401-37216-02 and 401-37204-01, are shown in figure 1-23. The thermal sensor provides temperature dependent resistance to a 2 VDC voltage sent from the Thermal Alarm Unit, 401-37155-01. The voltage is then returned to comparator circuits in the thermal alarm unit. One type of Thermal Sensor, 401-37216-02, is designed to be mounted in the upper section of an equipment cabinet. The other type of Thermal Sensor, 401-37204-01, is designed to be mounted in the lower section of an equipment cabinet. The COTC processor rack contains two Thermal Sensors, 401-37216-02 and 401-37204-01, whose outputs are connected to the thermal alarm unit located in the communications switching rack.

1.2.1.4 Tandem Group. - The Tandem Group, 401-42690-01, consists of the following equipment in the M1FC FSDPS:

1. Processors, T16/1420
2. Disk Controllers, T16/3106
3. Asynchronous Controllers, T16/6303
4. Asynchronous Extension Boards, T16/6304
5. Asynchronous Patch Panels, T16/7501
6. Bit Synchronous Controllers, T16/6203



401-37179-07 ASSEMBLY



401-37179-08 ASSEMBLY

Figure 1-20. Keyboard Junction Box, 401-37179-07 and -08

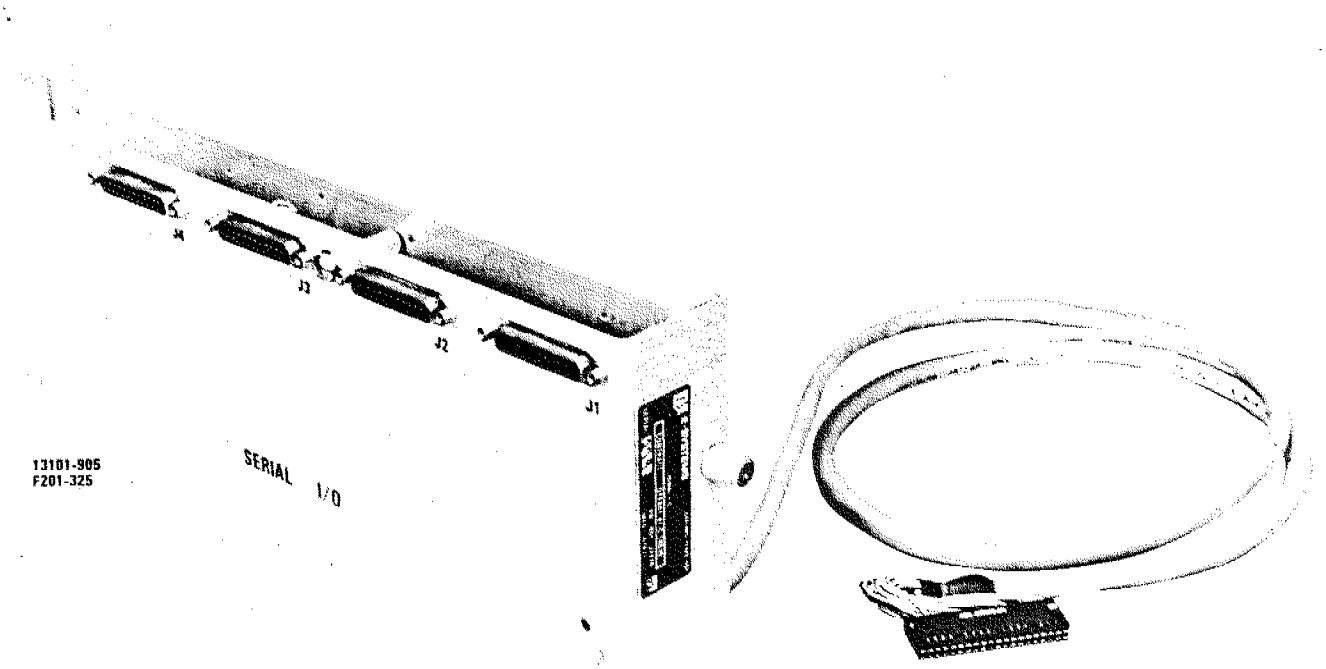
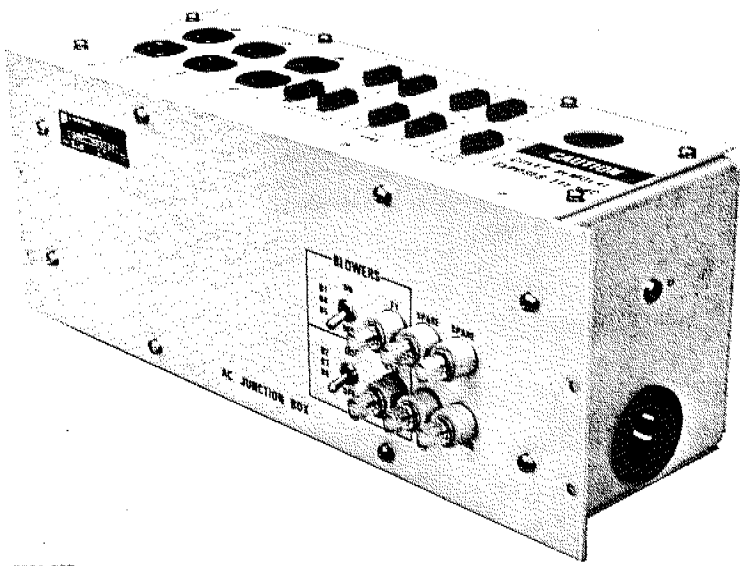
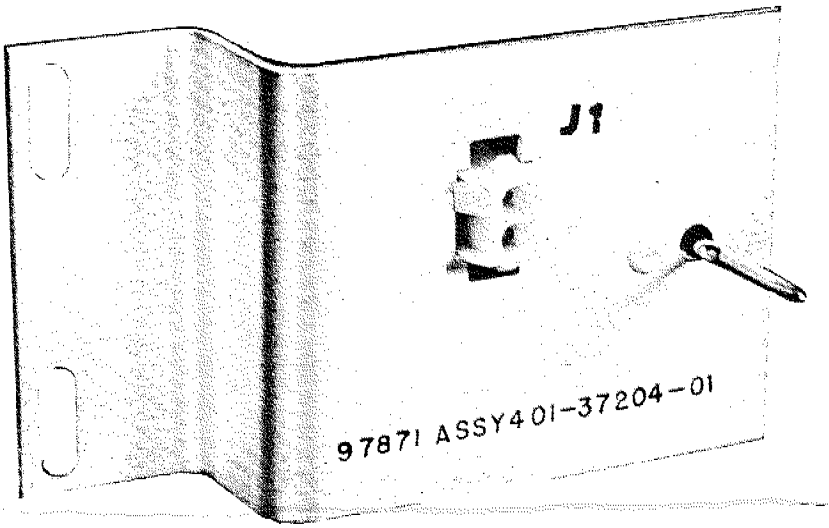


Figure 1-21. Serial I/O Assembly, 401-37274-02



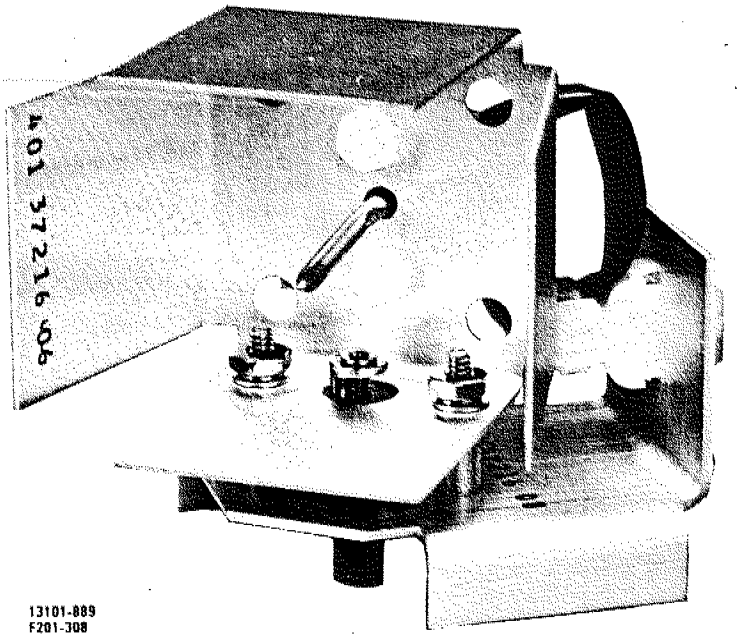
F201-257

Figure 1-22. Fan AC Junction Box, 401-37231-02



13101-886

401-37204-01 ASSEMBLY



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F201-308

401-37216-02 ASSEMBLY

Figure 1-23. Thermal Sensor, 401-37204-01 and 401-37216-02

7. Synchronous Patch Panels, T16/7502
8. Magnetic Tape Controllers, T16/3106
9. Magnetic Tape Drives, T16/5103
10. Disk Drive Patch Panels, T16/7504
11. Operations and Service Processor (OSP) Consoles, T16/3910
12. Video Displays and Keyboards, T16/6530
13. Printers, T16/5520

Consult the manuals listed in table 1-4 for a detailed description of the Tandem group equipment.

1.2.1.5 Peripheral Group. - The Peripheral Group, 401-37729-01, consists of the following equipment in the FSDPS:

1. Input/Output Terminal (IOT), LA34-AA/LA100-CA
2. Line Printers, P300
3. Keyboard Units, 401-36735-03
4. Keyboard Power Supplies, 5305-000-423
5. CRT Monitors, 401-37290-01
6. Disk Drives, DM9300TD

The following paragraphs describe the equipment located in the peripheral group of the FSDPS. The relationship of the equipment is shown in figure 1-4.

1.2.1.5.1 Input/Output Terminal (IOT). - The Input/Output Terminal (IOT), LA34-AA or LA100-CA, provides a hard copy output device for use by the Tandem Group via the Digital Patch Panel. One of these units is provided in the peripheral group of the FSDPS. Consult the manual listed in table 1-4 for a detailed description of the IOT.

1.2.1.5.2 Line Printer. - The Line Printer, P300, provides a hard copy output device for use by the Tandem group via the digital patch panel. Two of these units are provided in the peripheral group of the FSDPS. Consult the manual listed in table 1-4 for a detailed description of the line printer.

1.2.1.5.3 Keyboard Unit. - The Keyboard Unit, 401-36735-03, is shown in figure 1-24. The keyboard unit is an input device for the position processor via the keyboard junction box. This unit is a Maxiswitch Keyboard, 2160069, which has circuit board modifications performed by E-Systems. Two keyboard units are provided in the peripheral group of the FSDPS. Consult the manual listed in table 1-4 for a detailed description of the keyboard unit.

1.2.1.5.4 Keyboard Power Supply. - The Keyboard Power Supply, 5305-000-423, provides +5VDC for use by the keyboard unit. This power supply plugs directly into an AC power outlet. Two of these supplies are provided in the peripheral group of the FSDPS. Consult

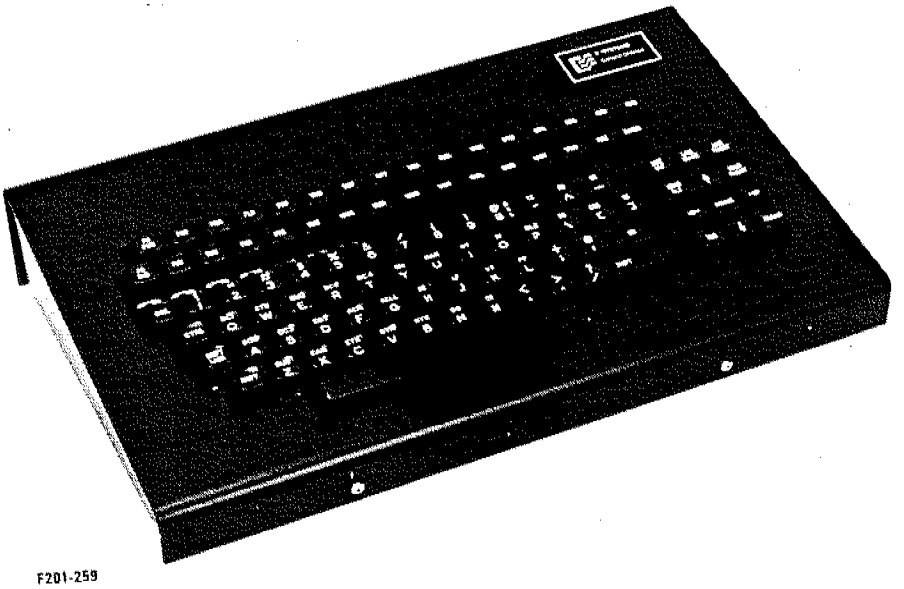


Figure 1-24. Keyboard Unit, 401-36735-03

the manual listed in table 1-4 for a detailed description of the keyboard power supply.

1.2.1.5.5 CRT Monitor. - The CRT Monitor, 401-37290-01, provides an output display device for the position processor via the A/N quad cache memory circuit card. Two CRT monitors are provided in the peripheral group of the FSDPS. Consult the manual listed in table 1-4 for a detailed description of the CRT monitor.

1.2.1.5.6 Disk Drive. - The Disk Drive, DM9300TD, provides disk storage for up to 300-million eight-bit bytes for use by the Tandem group. Six of these disk drives are provided in the peripheral group of the FSDPS. Consult the manual listed in table 1-4 for a detailed description of the DM9300TD Disk Drive.

1.2.1.6 Communications Cable Group. - The communications cable group varies depending on the particular FSDPS site configuration. Wiring diagrams for the different configurations and schematic diagrams of cables are provided in section 10 of this manual.

1.2.2 Automated Flight Service Station (AFSS). - An AFSS is used in the MIFC FSAS System to receive information concerning flight safety from an FSDPS via CRT Monitors and also to send flight related data to an FSDPS via keyboard units. The following paragraphs describe the equipment provided in an AFSS.

1.2.2.1 Communications Equipment Rack. - The Communications Equipment Rack, 401-36709-01, and equipment located within the rack are shown in figure 1-2. This rack is used in the AFSS to house the following equipment:

1. Thermal Alarm Unit, 401-37155-01
2. Analog Patch Panel, 153-020-12VF-M1
3. Digital Patch Panel, 157-011-00
4. Digital Patch Panel, 157-002C-00
5. Disk Drives, RL01-AK/RL02-AK
6. Circuit Breaker AC Junction Box, 401-37231-01

The following paragraphs describe the equipment located in the communications equipment rack. The relationship of the equipment used in the rack is shown in figure 1-5.

1.2.2.1.1 Thermal Alarm Unit. - The Thermal Alarm Unit, 401-37155-01, is shown in figure 1-8. This unit visually and audibly monitors overheating conditions within equipment racks containing thermal sensors. The thermal alarm unit contained in the

communications equipment rack monitors the thermal sensors located in the communications processor rack and position processor rack(s) in the AFSS.

1.2.2.1.2 Analog Patch Panel. - The Analog Patch Panel, 153-020-12VF-M1, patches analog signals coming to and from modem equipment in the AFSS. Consult the manual listed in table 1-4 for a detailed description of the analog patch panel.

1.2.2.1.3 Digital Patch Panel. - The Digital Patch Panel, 157-011-00, provides a means of patching digital signals to and from modem equipment in the Communications Processor Rack. The 157-011-00 Digital Patch Panel contains six 24 circuit jacks and six 32 circuit jacks. The 157-002C-00 Digital Patch Panel contains twelve 24 circuit jacks. Consult the manual listed in table 1-4 for a detailed description of the two types of digital patch panels.

1.2.2.1.4 Disk Drive. - The RL01-AK Disk Drive provides 5.2 MB (megabytes) of disk memory compatible with the LSI-11/23 Microcomputer System. The RL02-AK Disk Drive provides 10.4 MB of disk memory. Three of these Disk Drives (all either RL01-AK or RL02-AK, but not mixed) are provided in the communications equipment rack. One disk drive provides disk storage for communications processor no. 1, the second disk drive provides storage for communications processor no. 2, and the third disk drive provides storage for communications processor no. 3 in a redundant manner. Consult the manual listed in table 1-4 for a detailed description of the RL01-AK/RL02-AK Disk Drive.

1.2.2.1.5 Circuit Breaker AC Junction Box. - The Circuit Breaker AC Junction Box, 401-37231-01, is shown in figure 1-9. This junction box is connected to primary AC power and has the capability to connect or disconnect AC power to or from the following:

1. Communications Equipment Rack, 401-37614
2. Communications Processor Rack, 401-37615
3. Position Processor Rack(s), 401-37616
4. Utility outlets on above three racks

1.2.2.2 Communications Processor Rack. - The Communications Processor Rack, 401-37615-01, and equipment located within the rack are shown in figure 1-2. This rack is used in the AFSS to house the following equipment:

1. Modem Sharing Device Enclosures, 2005061
2. Modem Sharing Devices, 2005064
3. Modem Enclosure, RM-8E
4. Modem Power Supplies

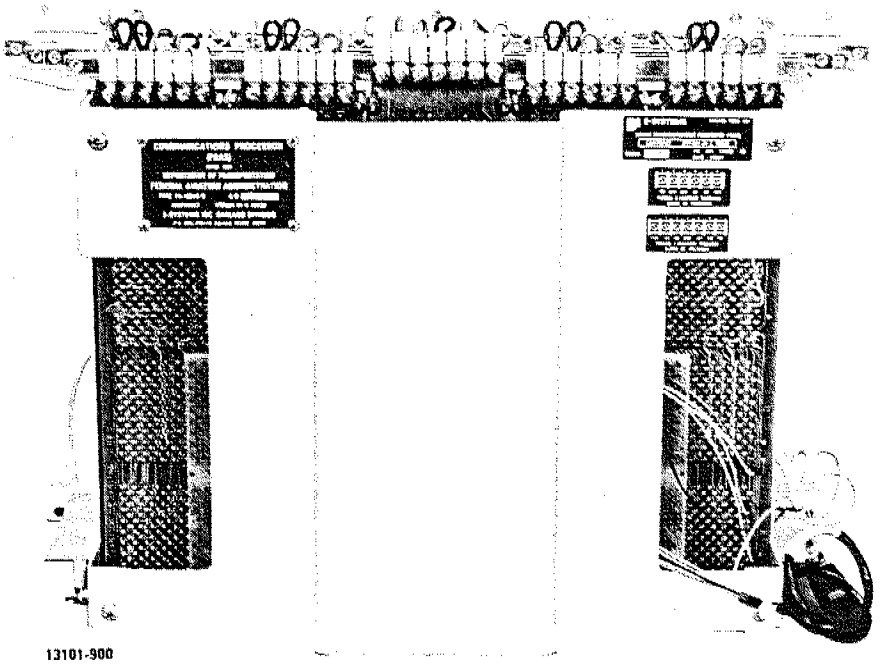
5. Answer/Originate Board, RM-A/O
6. Modem, RM-208A
7. Modem, RM-9600
8. Single Communications Processor Card Cage, 401-37999-03
9. Dual Communication Processor Card Cage, 401-37999-04
10. Power Control Modules, 401-36719-01, -02
11. Multi-Processor Linking Systems HEX/IPB-L11
12. DMA Controller Circuit Cards, DMA-QB
13. Disk Controller Circuit Cards, RLV12
14. Multiplexer Circuit Cards, 401-36993-03
15. System Module Circuit Cards, KPV11-B
16. LSI-11 Processor Circuit Cards, KDF11-AA
17. 32K Word PROM Circuit Cards, MRV11-C
18. 64K Word RAM/Parity Cards, MSV11-LF
19. Eight-Channel Serial I/O Circuit Cards, 8S
20. Blower Assembly, 401-37145-02
21. Power Supply Assemblies, 401-36716-01
22. Multiplexer Interface Assemblies, 401-37170-01, -04
23. Thermal Sensor, 401-37216-02
24. Thermal Sensor, 401-37204-01
25. Fan AC Junction Box, 401-37231-02

The following paragraphs describe the equipment located in the communications processor rack. The relationship of the equipment used in the rack is shown in figure 1-5.

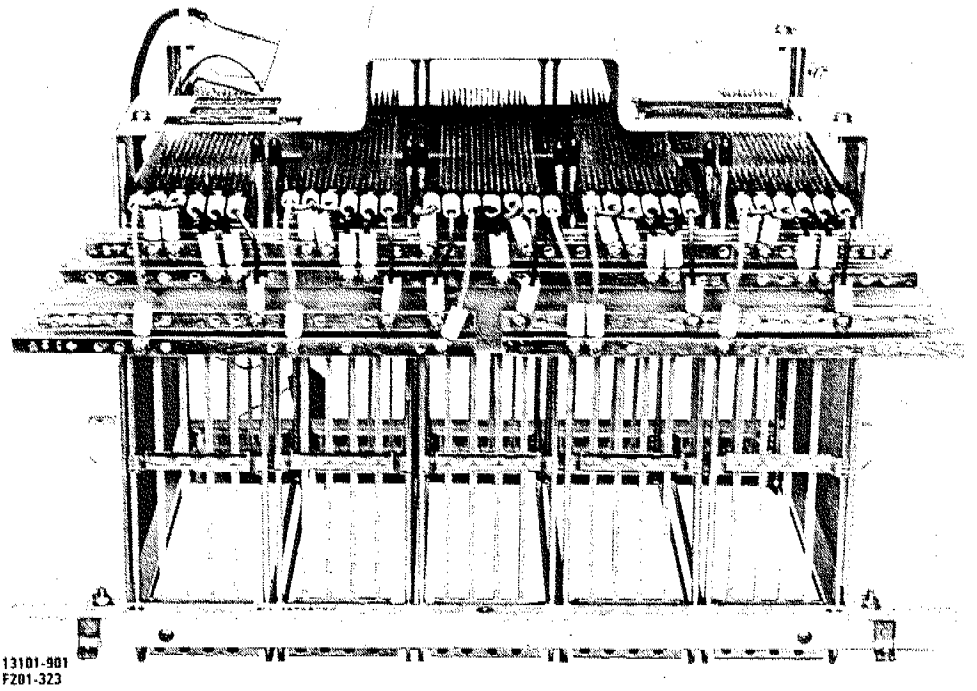
1.2.2.2.1 Modem Sharing Device Enclosures. - The Modem Sharing Device Enclosure, 2005061, has the capability of housing a maximum of four Modem Sharing Devices, 2005064. The communications processor rack contains two modem sharing device enclosures. Consult the manual listed in table 1-4 for a detailed description of the modem sharing device enclosure.

1.2.2.2.2 Modem Sharing Devices. - The Modem Sharing Device, 2005064, contains the necessary logic and buffers to connect a single I/O port (modem or printer) with each of the three communications processors in the AFSS. The communications processor rack contains seven modem sharing devices. Consult the manual listed in table 1-4 for a detailed description of the modem sharing devices.

1.2.2.2.3 Communications Processor Card Cages. - Two types of communications processor card cages are used in the M1FC FSAS (figure 1-25). The Single Communications Processor Card Cage, 401-37999-03, is used to contain the circuit cards which comprise a single communications processor. The Dual Communications Processor Card Cage, 401-37999-04, is used to contain the circuit cards which comprise two communications processors. The communications processor rack contains one single communications processor card cage and one dual communications processor card cage.

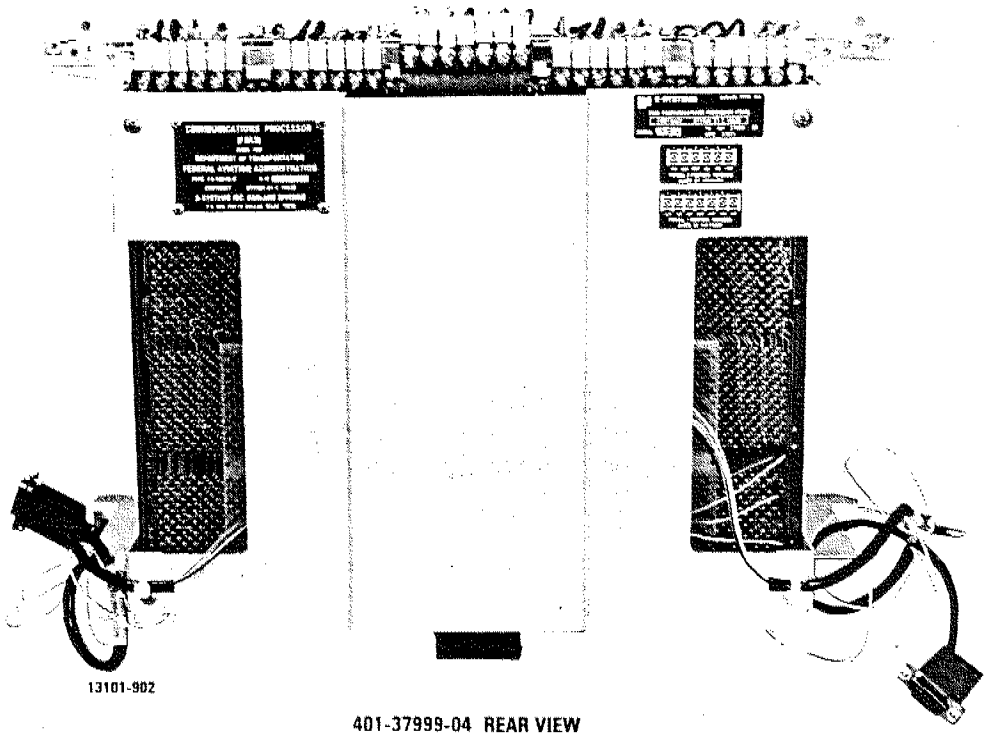


401-37999-03 REAR VIEW

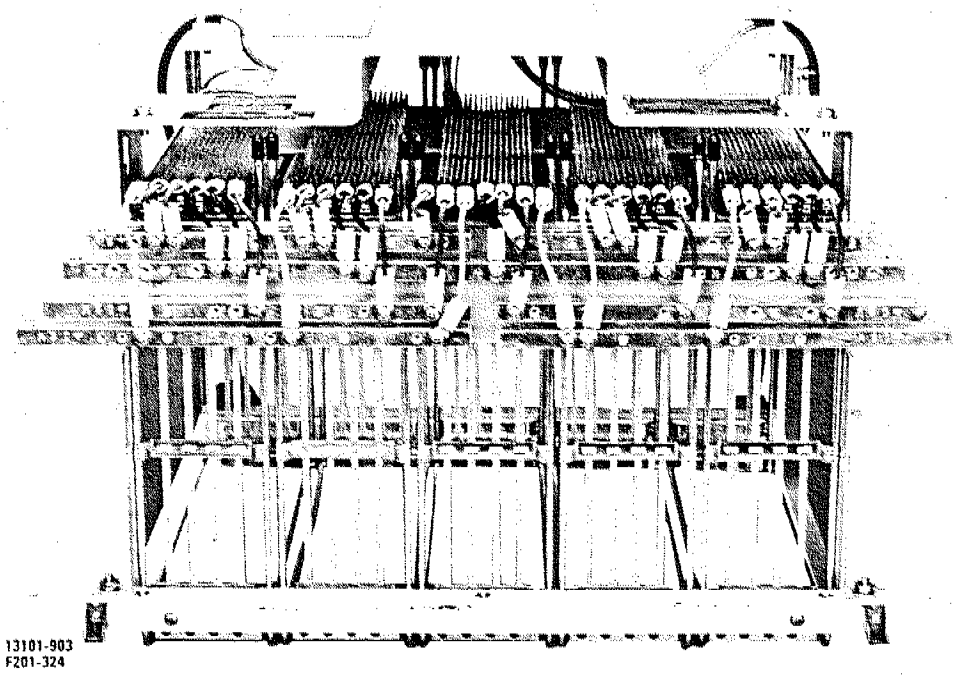


401-37999-03 TOP VIEW

Figure 1-25. Communications Processor Card Cage, 401-37999-03 and -04 (Sheet 1 of 2)



401-37999-04 REAR VIEW



401-37999-04 TOP VIEW

Figure 1-25. Communications Processor Card Cage, 401-37999-03 and -04 (Sheet 2 of 2)

1.2.2.2.4 Power Control Modules. - Three types of power control modules are used in the MIFC FSAS System (figure 1-13). One Power Control Module, 401-36719-01, is used in the first slot (left to right) of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-02, is used in the last slot of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-05, is used in the first slot of card cages which do not contain KPV11-B System Module Circuit Cards.

The main function of the Power Control Module is to provide control and fusing for the 115 VAC between the AC junction box and power supply assemblies. The 401-36719-01 and -02 types are provided with additional wiring and connectors for interface with the KPV11-B Circuit Cards.

The communications processor rack contains three power control modules: two of the 401-36719-01 type and one of the 401-36719-02 type.

1.2.2.2.5 Multi-Processor Linking System. - The Multi-Processor Linking System, HEX/IPB-11, contains two connected circuit cards. These cards establish six high speed communication ports between the DMA Controller Circuit Card (DMA-QB) of a communications processor and the DMA-QB Circuit Card of a position processor. Three multi-processor linking systems are provided in the communications processor rack. One is used to interface the DMA-QB Circuit Card in communications processor no. 1 with the DMA-QB Circuit Card in position processor no. 1; the other two are used to interface the DMA-QB Circuit Cards in communications processors No. 2 and 3 with the DMA-QB Circuit Cards in position processors no. 2 and 3 in a redundant manner. Consult the manual listed in table 1-4 for a detailed description of the multi-processor linking system.

1.2.2.2.6 DMA Controller Circuit Card. - The DMA Controller Circuit Card, DMA-QB, provides a DMA (Direct Memory Access) interface between the LSI-11/23 bus of a position processor and the LSI-11/23 bus of a communications processor using the interprocessor bus. Three DMA controller circuit cards are provided in the communications processor rack. One card is used in communications processor no. 1, one card is used in communications processor no. 2, and the other card is used in communications processor no. 3 in a redundant manner. Consult the manual listed in table 1-4 for a detailed description of the DMA-QB circuit card.

1.2.2.2.7 Disk Controller Circuit Card. - The Disk Controller Circuit Card, RLV12, is used to interface the RL01-AK/RL02-AK Disk Drive with the LSI-11/23 bus of a communications processor. Three disk controller circuit cards are used in the communications

processor rack. One card is used in communications processor no. 1, one card is used in communications processor no. 2, and one card is used in communications processor no. 3. Consult the manual listed in table 1-4 for a detailed description of the RLV12 circuit card.

1.2.2.2.8 Multiplexer Circuit Card. - The Multiplexer Circuit Card, 401-36993-03, is shown in figure 1-14. This circuit card provides a four-channel serial interface (RS449) between a Communications Processor's LSI-11/23 bus and external peripherals. Six multiplexer circuit cards are provided in the communications processor rack. Two of the multiplexer circuit cards are used to interface the LSI-11/23 bus in communications processor no. 1 with FSDPS peripheral equipment. Two other multiplexer circuit cards are used to interface the LSI-11/23 bus in communications processor no. 2 with FSDPS peripheral equipment. The final two multiplexer circuit cards are used to interface the LSI-11/23 bus in communications processor no. 3 with FSDPS peripheral equipment.

1.2.2.2.9 System Module Circuit Card. - The System Module Circuit Card, KPV11-B, alerts the LSI-11/23 bus when a power failure occurs and restarts the LSI-11/23 Microcomputer System when power is restored. Three of these cards are provided in the communications processor rack. One card is used in communications processor no. 1, one card is used in communications processor no. 2, and one card is used in communications processor no. 3. Consult the manual listed in table 1-4 for a detailed description of the KPV11-B circuit card.

1.2.2.2.10 LSI-11 Processor Circuit Card. - The LSI-11 Processor Circuit Card, KDF11-AA, performs the CPU (Central Processing Unit) function for the LSI-11/23 Microcomputer System. Three LSI-11 Processor Circuit Cards are provided in the communications processor rack. One processor provides the CPU function for communications processor no. 1, one processor provides the CPU function for communications processor no. 2, and one processor provides the CPU function for communications processor no. 3. Consult the manual listed in table 1-4 for a detailed description of the KDF11-AA circuit card.

1.2.2.2.11 32K Word PROM Circuit Card. - The 32K Word PROM Circuit Card, MRV11-C, contains 32K of PROM (Programmable Read Only Memory) in 16, 24-pin sockets. Three 32K word PROM circuit cards are provided in the communications processor rack. One of the cards provides the PROM for communications processor no. 1, one card provides the PROM for communications processor no. 2, and one card provides the PROM for communications processor no. 3. Consult the manual listed in table 1-4 for a detailed description of the MRV11-C circuit card.

1.2.2.2.12 64K Word RAM/Parity Circuit Card. - The 64K Word RAM/Parity Circuit Card, MSV11-LF, contains 64K, 16-bit words of MOS (Metal Oxide Semiconductor) RAM (Random Access Memory) and generates and detects byte parity for each word. Three 64K word RAM/parity circuit cards are provided in the communications processor rack. One of the cards is used in communications processor no. 1, one card is used in communications processor no. 2, and one card is used in communications processor no. 3. Consult the manual listed in table 1-4 for a detailed description of the MSV11-LF circuit card.

1.2.2.2.13 Eight-Channel Serial I/O Circuit Card. - The Eight-Channel Serial I/O Circuit Card, 8S, provides eight channels for serial input or output of data to/from the LSI-11/23 bus. Three of these cards are provided in the communications processor rack. One card is used to interface communications processor no. 1 with peripheral equipment in the FSDPS, one card is used to interface communications processor no. 2 with peripheral equipment in the FSDPS, and one card is used to interface communications processor no. 3 with peripheral equipment in the FSDPS. Consult the manual listed in table 1-4 for a detailed description of the 8S circuit card.

1.2.2.2.14 Blower Assembly. - The Blower Assembly, 401-37145-02, is shown in figure 1-17. This assembly uses fans to provide air circulation inside the communications processor rack. The blower assembly is powered by 115 VAC from the fan AC junction box.

1.2.2.2.15 Power Supply Assemblies. - The Power Supply Assembly, 401-36716-01, is shown in figure 1-19. The Power Supply Assembly provides +5VDC, +12VDC, -12VDC, and signal ground for use by rack equipment. The communications processor rack contains three power supply assemblies. Consult the manual listed in table 1-4 for a detailed description of the power supply assembly.

1.2.2.2.16 Multiplexer Interface Assembly. - The Multiplexer Interface Assembly, 401-37170-01 and -04, is shown in figure 1-18. This assembly provides an RS-449 interface for the multiplexer. Two types of multiplexer interface assemblies are used in the M1FC FSAS. One type of Multiplexer Interface Assembly, 401-37170-01, is used when the assembly is mounted in the right side of a cabinet. The other type of Multiplexer Interface Assembly, 401-37170-04, is used when the assembly is mounted in the left side of a cabinet. Both types are electrically identical. Three multiplexer interface assemblies are used in the communication processor rack. The communication processor no. 1 uses the 401-37170-04 assembly, communications processor no. 2 uses the 401-37170-01 assembly, and communications processor no. 3 uses the 401-37170-04 assembly.

1.2.2.2.17 Thermal Sensors. - The Thermal Sensors, 401-37216-02 and 401-37204-01, are shown in figure 1-23. The Thermal Sensor provides temperature dependent resistance to a 2 VDC voltage sent from the Thermal Alarm Unit, 401-37155-01. The voltage is then returned to comparator circuits in the thermal alarm unit. One type of Thermal Sensor, 401-37216-02, is designed to be mounted in the upper section of an equipment cabinet. The other type of Thermal Sensor, 401-37204-01, is designed to be mounted in the lower section of an equipment cabinet. The communications processor rack contains two Thermal Sensors, 401-37216-02 and 401-37204-01, whose outputs are connected to the thermal alarm unit located in the communications equipment rack.

1.2.2.2.18 Fan AC Junction Box. - The Fan AC Junction Box, 401-37231-02, is shown in figure 1-22. This junction box receives primary AC power from the plain AC junction box in the communications equipment rack. The fan AC junction box distributes 115 VAC to three power control modules and the blower assembly in the communications processor rack.

1.2.2.3 Position Processor Rack. - There are four different configurations for the position processor rack. The E-Systems part number for these four configurations are 401-37616-01, -02, -03, and -04. The maximum configured Position Processor Rack, 401-37616-04, is shown in figure 1-2. The number of positions supported by each configuration of position processor rack is as follows:

Rack Configuration	Number of Positions
401-37616-01	1-4
401-37616-02	5-8
401-37616-03	9-12
401-37616-04	13-16

The Position Processor Rack, 401-37616-04, and equipment located within the rack are shown in figure 1-2. This rack is used in the AFSS to house the following equipment:

1. Position Processor Card Cages, 401-37999-01
2. Memory Card Cage "A", 401-37999-02
3. Memory Card Cage "B", 401-37999-06
4. Power Control Modules, 401-36719-01, -05
5. 32K Word PROM Circuit Cards, MRV11-C
6. 64K Word RAM/Parity Circuit Cards, MSV11-LF
7. A/N OTF Processor Circuit Cards, 401-33676-01
8. Eight-Channel Serial I/O Circuit Cards, 8S
9. LSI-11 Processor Circuit Cards, KDF11-AA
10. DMA Controller Circuit Cards, DMA-QB
11. System Module Circuit Cards, KPV11-B
12. Thermal Sensor, 401-37216-02

13. A/N Quad Cache Memory Circuit Cards, 401-33692-01
14. Blower Assembly, 401-37145-02
15. DC Power Switch Assembly, 401-37916-01
16. Power Supply Assemblies, 401-36716-01
17. Keyboard Junction Box, 401-37179-08
18. Serial I/O Assemblies, 401-37274-02
19. Fan AC Junction Box, 401-37231-02

The following paragraphs describe the equipment located in the position processor rack. The relationship of the equipment used in the rack is shown in figure 1-5.

1.2.2.3.1 Position Processor Card Cage. - The Position Processor Card Cage, 401-37999-01, is shown in figure 1-26. This card cage is used to house the circuit cards which make up a position processor. Two of these card cages are used in the position processor rack.

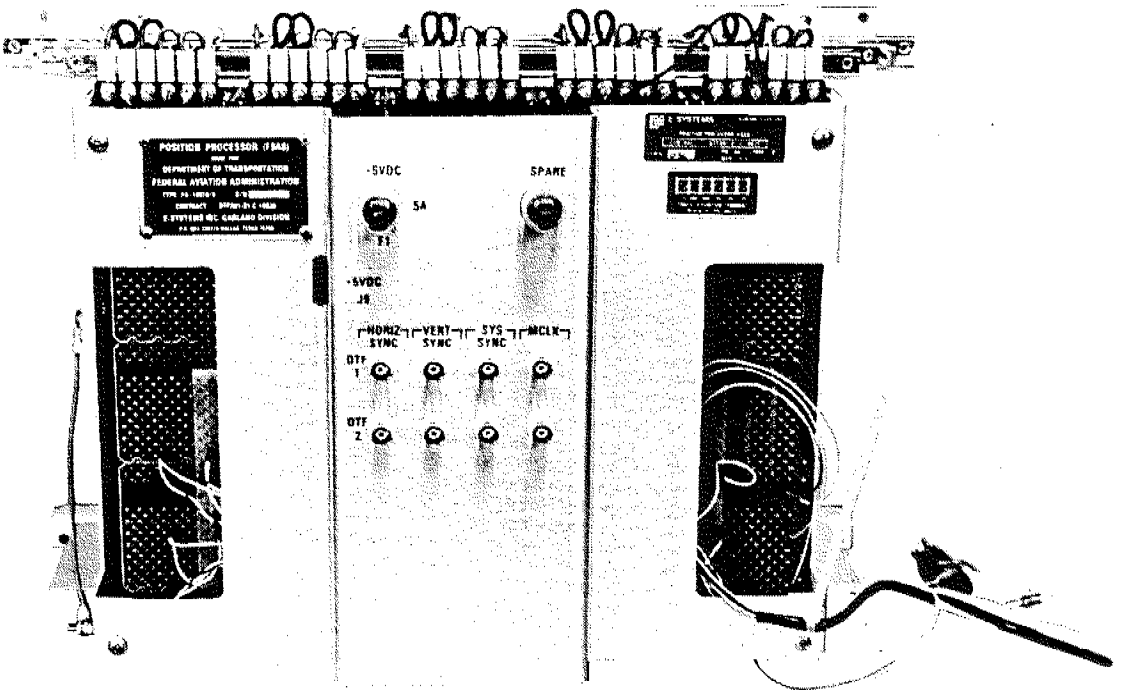
1.2.2.3.2. Memory Card Cage "A". - Memory Card Cage "A", 401-37999-02, is shown in figure 1-27. This card cage is used to house a maximum of two alphanumeric quad cache memory circuit cards and a power control module.

1.2.2.3.3 Memory Card Cage "B". Memory Card Cage "B", 401-37999-06, is shown in figure 1-28. This card cage is used to house a maximum of two alphanumeric quad cache memory circuit cards and a power control module. It provides a redundant power supply voltage of +5 VDC to memory card cage "A".

1.2.2.3.4 Power Control Module. - Three types of power control modules are used in the MIFC FSAS (figure 1-13). One Power Control Module, 401-36719-01, is used in the first slot (left to right) of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-02, is used in the last slot of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-05, is used in the first slot of card cages which do not contain KPV11-B System Module Circuit Cards. The 401-36719-01 and -02 types are provided with additional wiring and connectors for interface with the KPV11-B Circuit Cards.

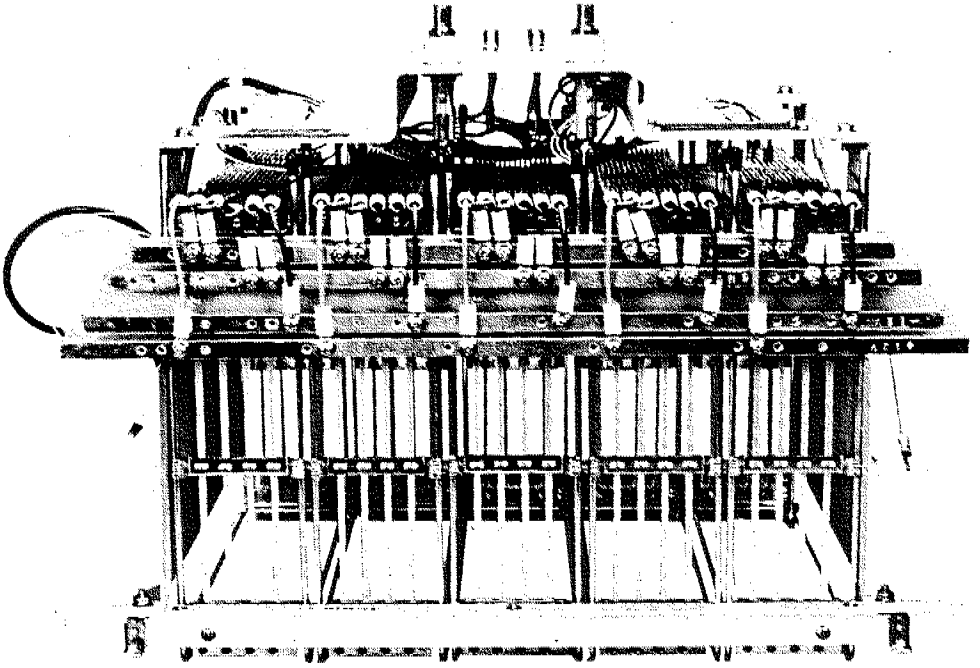
The main function of the power control module in the position processor rack is to provide control and fusing for the 115 VAC between the fan AC junction box and power supply assemblies. The position processor rack contains four power control modules; two of the 401-36719-01 type and two of the 401-36719-05 type.

1.2.2.3.5 32K Word PROM Circuit Card. - The 32K Word PROM Circuit Card, MRV11-C, contains 32K words of PROM (Programmable Read Only Memory) in 16, 24-pin sockets. Two 32K word PROM circuit cards are



REAR VIEW

13101-878



TOP VIEW

13101-879
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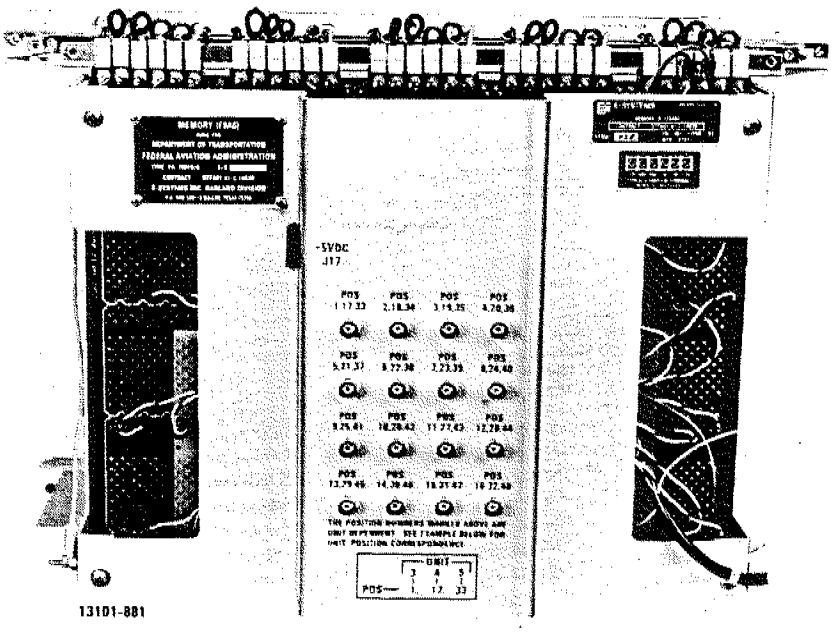
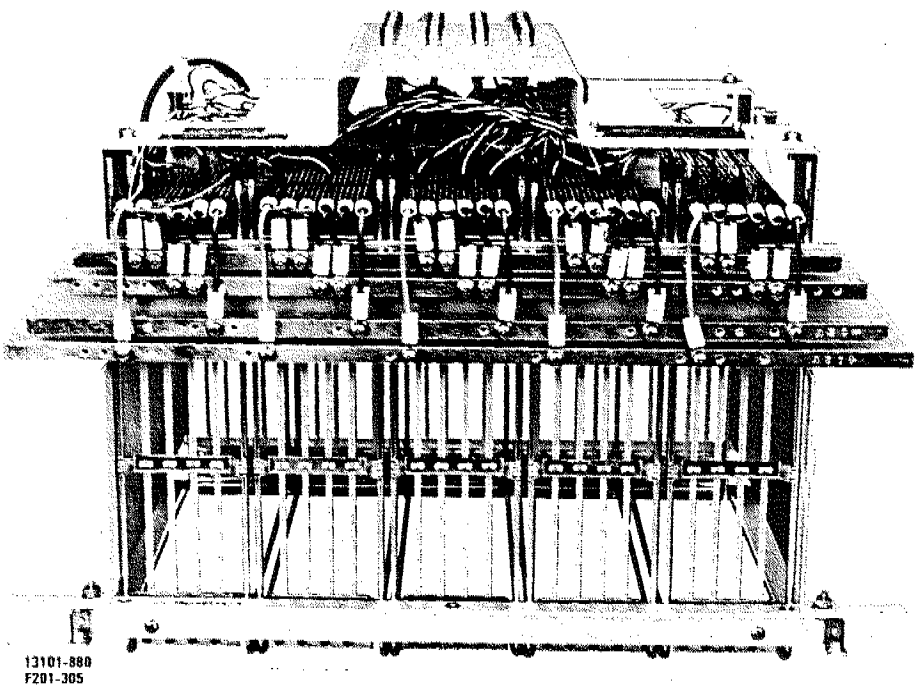
Figure 1-26. Position Processor Card Cage, 401-37999-01

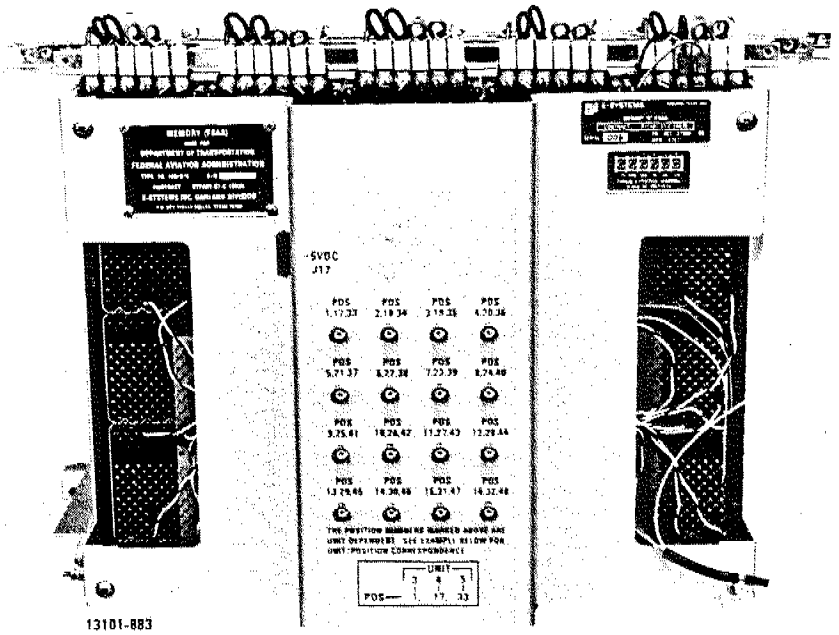


REAR VIEW

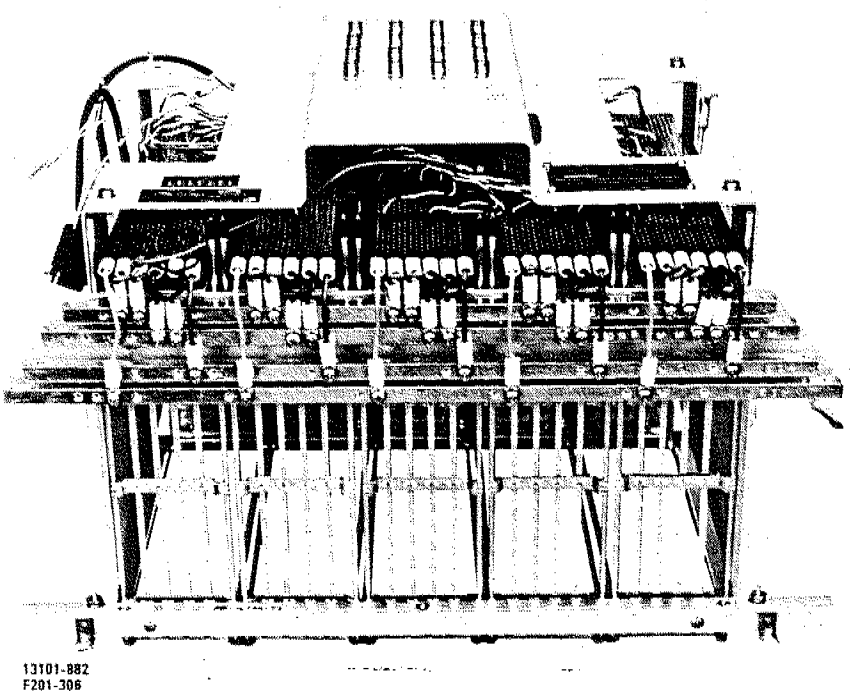


TOP VIEW

Figure 1-27. Memory Card Cage "A", 401-37999-02



REAR VIEW



TOP VIEW

Figure 1-28. Memory Card Cage "B", 401-37999-06

provided in the position processor rack. One of the cards provides the PROM for position processor no. 1, and the other card provides the PROM for position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the MRV11-C circuit card.

1.2.2.3.6 64K Word RAM/Parity Circuit Card. - The 64K Word RAM/Parity Circuit Card, MSV11-LF, contains 64K, 16-bit words of MOS (Metal Oxide Semiconductor) RAM (Random Access Memory). It generates and detects byte parity for each word. Two 64K word RAM/parity circuit cards are provided in the position processor rack. One of the cards is used in position processor no. 1 and the other card is used in position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the MSV11-LF circuit card.

1.2.2.3.7 Alphanumeric (A/N) On-The-Fly (OTF) Processor Circuit Card. - The A/N OTF Processor Circuit Card, 401-33676-01, is shown in figure 1-16. This card processes and controls alphanumeric data to and from the A/N quad cache memory circuit card. It acts as an interface between the A/N quad cache memory circuit card and the LSI-11/23 bus. A maximum of four A/N OTF processor circuit cards can be used in the position processor rack (two in position processor no. 1 and two in position processor no. 2).

1.2.2.3.8 Eight-Channel Serial I/O Circuit Card. - The Eight-Channel Serial I/O Circuit Card, 8S, provides eight channels for serial input or output of data to/from the LSI-11/23 bus. A maximum of six, 8S cards are used in the position processor rack (three in position processor no. 2 and three in position processor no. 2). Consult the manual listed in table 1-4 for a detailed description of the 8S circuit card.

1.2.2.3.9 LSI-11 Processor Circuit Card. - The LSI-11 Processor Circuit Card, KDF11-AA, performs the CPU (Central Processing Unit) function for the LSI-11/23 Microcomputer System. Two LSI-11 Processor Circuit Cards are provided in the position processor rack. One processor provides the CPU function for position processor no. 1 and the other processor provides the CPU function for position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the KDF11-AA circuit card.

1.2.2.3.10 DMA Controller Circuit Card. - The DMA Controller Circuit Card, DMA-QB, provides a DMA (Direct Memory Access) interface between the LSI-11/23 bus of a position processor and the LSI-11/23 bus of a communications processor using the interprocessor bus. Six of these cards are provided in the position processor rack. Three cards are used in position processor no. 1 and the other three cards are used in position processor no. 2 in a

redundant manner. Consult the manual listed in table 1-4 for a detailed description of the DMA-QB circuit card.

1.2.2.3.11 System Module Circuit Card. - The System Module Circuit Card, KPV11-B, alerts the LSI-11/23 bus when a power failure occurs and restarts the LSI-11/23 Microcomputer System when power is restored. Two of these cards are provided in the position processor rack. One card is used in position processor no. 1, and the other card is used in position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the KPV11-B circuit card.

1.2.2.3.12 Thermal Sensor. - The Thermal Sensor, 401-37216-02, is shown in figure 1-23. The sensor provides temperature dependent resistance to a 2 VDC voltage sent from the Thermal Alarm Unit, 401-37155. The voltage is then returned to comparator circuits in the thermal alarm unit. The position processor rack contains one Thermal Sensor, 401-37216-02, whose output is connected to the thermal alarm unit in the communications equipment rack.

1.2.2.3.13 Alphanumeric (A/N) Quad Cache Memory Circuit Card. - The A/N quad cache memory circuit card, 401-33692-01, is shown in figure 1-15. This circuit card provides memory for up to four CRT Monitors. A maximum of four of these cards can be used in the position processor rack.

1.2.2.3.14 Blower Assembly. - The Blower Assembly, 401-37145-02, is shown in figure 1-17. This assembly uses fans to provide air circulation inside the position processor rack. The blower assembly is powered by 115 VAC from the fan AC junction box.

1.2.2.3.15 DC Power Switch Assembly. - The DC Power Switch Assembly, 401-37916-01, is shown in figure 1-29. The DC power switch assembly is used in the position processor rack to provide redundant power from one memory card cage to another. It also allows maintenance to be performed on one memory card cage while the other memory card cage is still being powered.

1.2.2.3.16 Power Supply Assembly. - The Power Supply Assembly, 401-36716-01, is shown in figure 1-19. The power supply assembly provides +5VDC, +12VDC, -12VDC, and signal ground for use by rack equipment. The position processor rack contains four power supply assemblies. Consult the manual listed in table 1-4 for a detailed description of the power supply assembly.

1.2.2.3.17 Keyboard Junction Box. - The Keyboard Junction Box, 401-37179-08, is shown in figure 1-20. This unit is used as an

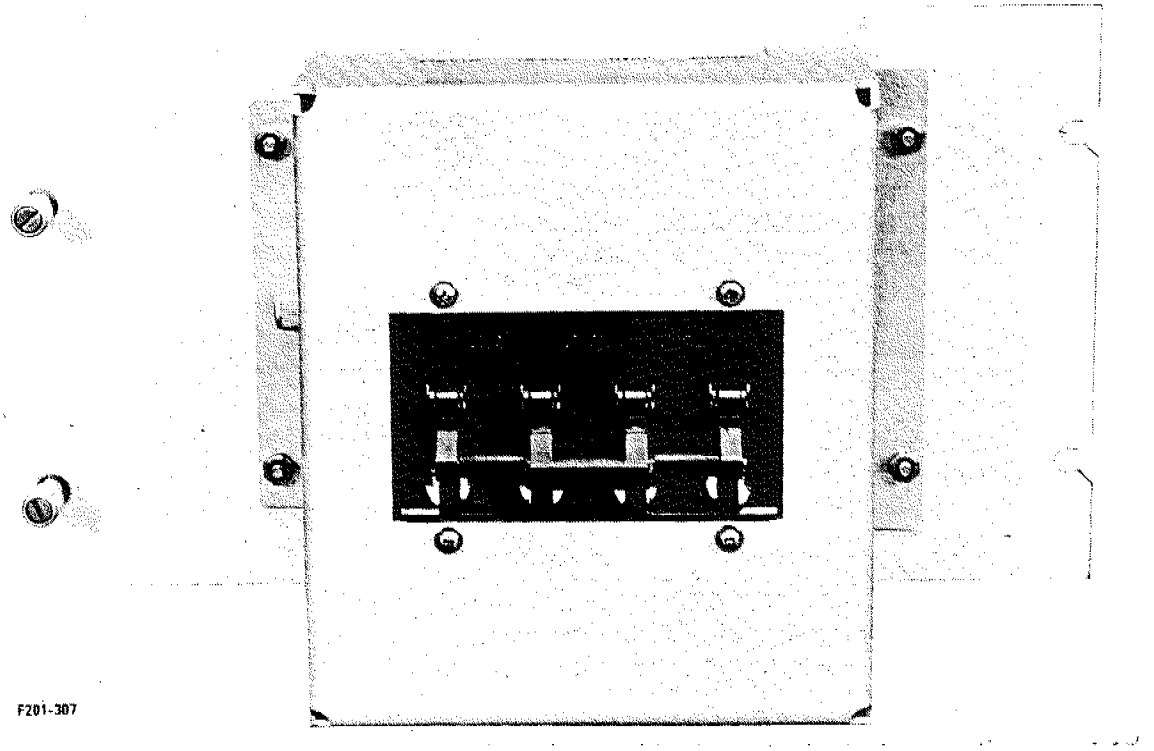


Figure 1-29. DC Power Switch Assembly, 401-37916-01

interface between keyboard units and eight-channel serial I/O circuit cards. The position processor rack contains one keyboard junction box which interfaces a maximum of 16 keyboard units with two eight-channel serial I/O circuit cards.

1.2.2.3.18 Serial I/O Assembly. - The Serial I/O Assembly, 401-37274-02, is shown in figure 1-21. This assembly is provided for connections between digital patch panels and an eight-channel serial I/O circuit card. The position processor rack contains two serial I/O assemblies; one used by position processor no. 1 and the other used by position processor no. 2.

1.2.2.3.19 Fan AC Junction Box. - The Fan AC Junction Box, 401-37231-02, is shown in figure 1-22. This junction box receives primary AC power from the fan AC junction box in the communications processor rack. It then distributes 115 VAC to four power control modules and the blower assembly in the position processor rack.

1.2.2.4 Peripheral Group. - The Peripheral Group, 401-37275-01, contains the following equipment in the AFSS:

1. Input/Output Terminal (IOT), LA34-AA or LA100-CA
2. Line Printers, P300.

The following paragraphs describe the equipment located in the peripheral group of the AFSS. The relationship of the equipment used in the AFSS peripheral group is shown in figure 1-5.

1.2.2.4.1 Input/Output Terminal (IOT). - The Input/Output Terminal (IOT), LA34-AA/LA100-CA provides a hard copy output device for use by the AFSS via the digital patch panel. Consult the manual listed in table 1-4 for a detailed description of the LA34-AA and LA100-CA IOTs.

1.2.2.4.2 Line Printer. - The Line Printer, P300, provides a hard copy output device for use by the AFSS via the digital patch panel. Two of these printers are provided in the AFSS peripheral group. Consult the manual listed in table 1-4 for a detailed description of the P300 Line Printer.

1.2.2.5 Keyboard Units. - The Keyboard Unit, 401-36735-03, is shown in figure 1-24. The keyboard unit is an input device for the position processor via the keyboard junction box. This unit is a Maxiswitch Keyboard, 2160069, which has circuit board modifications performed by E-Systems. A maximum of 16 keyboard units can be used to provide input to either position processor no. 1 or position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the keyboard unit.

1.2.2.6 Keyboard Power Supplies. - The Keyboard Power Supply, 5305-000-423, provides +5 VDC for use by the keyboard unit. This power supply plugs directly into an AC power outlet. Consult the manual listed in table 1-4 for a detailed description of the keyboard power supply.

1.2.2.7 CRT Monitors. - The CRT Monitor, 401-37290-01, provides an output display device for the position processor via the A/N quad cache memory circuit card. A maximum of 16 monitors can be connected to a position processor. Consult the manual listed in table 1-4 for a detailed description of the CRT monitor.

1.2.2.8 Cable Group. - The cable group for the AFSS varies depending on the particular AFSS site configuration. Wiring diagrams for the different configurations and schematic diagrams of cables are provided in section 10 of this manual.

1.2.3 Aviation Weather Processor (AWP). - The AWP collects and maintains all weather and flight safety information in the M1FC FSAS. The following paragraphs describe the equipment provided in the AWP.

1.2.3.1 Communications Equipment Rack. - The Communications Equipment Rack, 401-12301-01, and equipment located within the rack is shown in figure 1-3. This rack is used in the AWP to house the following equipment:

1. Coded Time Sources, 60DC
2. Coded Time Source Interface, 401-37207-01
3. Thermal Alarm Unit, 401-37155-01
4. Digital Patch Panels, 157-002C-00
5. Disk Drives, RL01-AK/RL02-AK
6. Circuit Breaker AC Junction Box, 401-37231-01

The following paragraphs describe the equipment located in the communications equipment rack. The relationship of the equipment used in the rack is shown in figure 1-6.

1.2.3.1.1 Coded Time Source. - The Coded Time Source, 60-DC, provides an accurate digital output of the time of day and Julian date. Two of these units are provided in the AWP communications equipment rack with both outputs applied to the coded time source interface. Consult the manual listed in table 1-4 for a detailed description of the coded time source.

1.2.3.1.2 Coded Time Source Interface. - The Coded Time Source Interface, 401-37207-01, is shown in figure 1-7. It is used within the AWP to provide accurate time and date information in a format compatible with the Tandem group.

1.2.3.1.3 Thermal Alarm Unit. - The Thermal Alarm Unit, 401-37155-01, is shown in figure 1-8. This unit visually and audibly monitors overheating conditions within equipment racks containing thermal sensors. The thermal alarm unit contained in the AWP communications equipment rack monitors the thermal sensors located in the AWP communications processor rack and the AWP position processor rack.

1.2.3.1.4 Digital Patch Panels. - The Digital Patch Panel, 157-002C-00, patches digital signals coming to and from modem equipment. Three digital patch panels are provided in the AWP communications equipment rack. Consult the manual specified in table 1-4 for a detailed description of the digital patch panel.

1.2.3.1.5 Disk Drives. -The two disk drives can be either RL01-AK or RL02-AK Disk Drives (but not mixed types). The RL01-AK Disk Drive provides 5.2 MB (megabytes) of disk memory compatible with the LSI-11/23 Microcomputer System, while the RL02-AK Disk Drive provides 10.4 MB of disk memory. The two disk drives in the AWP communications equipment rack provide disk storage for communications processor no. 1 and communications processor no. 2. Consult the manual specified in table 1-4 for a detailed description of the disk drive.

1.2.3.1.6 Circuit Breaker AC Junction Box. - The Circuit Breaker AC Junction Box, 401-37231-01, is shown in figure 1-9. This junction box is connected to primary AC power and has the capability to connect or disconnect AC power to or from the following equipment in the AWP:

1. Communications Equipment Rack, 401-12301-01
2. Communications Processor Rack, 401-12302-01
3. Position Processor Rack, 401-12303-01
4. Utility outlets on above three racks.

1.2.3.2 Communications Processor Rack. - The Communications Processor Rack, 401-12302-01, and equipment located within the rack are shown in figure 1-3. This rack is used in the AWP to house the following equipment:

1. Analog Patch Panels, 153-020-12VF-M1
2. Modem Enclosures, RM-8E

3. Modem Power Supplies
4. Modems, RM-9600E FP
5. Modems, RM-9600
6. Dual Communication Processor Card Cage, 401-37999-04
7. Power Control Modules, 401-36719-01, -02
8. 64K Word RAM/Parity Circuit Cards, MSV11-LF
9. Multiplexer Circuit Cards, 401-36993-03
10. Multi-Processor Linking Systems, HEX/IPB-L11
11. Disk Controller Circuit Cards, RLV12
12. 32K Word PROM Circuit Cards, MRV11-C
13. System Modules, KPV11-B
14. Eight-Channel Serial I/O Circuit Cards, 8S
15. DMA Controller Circuit Cards, DMA-QB
16. LSI-11 Processor Circuit Cards, KDF11-AA
17. Blower Assembly, 401-37145-02
18. Power Supply Assemblies, 401-36716-01
19. Multiplexer Interface Assemblies, 401-37170-01
20. Fan AC Junction Box, 401-37231-02
21. Thermal Sensor, 401-37216-02
22. Thermal Sensor, 401-37204-01

The following paragraphs describe the equipment located in the communications processor rack. The relationship of the equipment used in the rack is shown in figure 1-6.

1.2.3.2.1 Analog Patch Panels. - The Analog Patch Panel, 153-020-12VF-M1, patches analog signals coming to and from modem equipment. Two analog patch panels are provided in the AWP communications processor rack Consult the manual specified in table 1-4 for a detailed description of the analog patch panel.

1.2.3.2.2 RM-8E Modem Enclosure. - Three RM-8E Modem Enclosures are used in the AWP communications processor rack to house the modem related equipment used in the AWP. This modem related equipment consists of the following modules:

1. Modem Power Supplies
2. RM-9600 Modem
3. RM-9600E FP Modem

Consult the manual listed in table 1-4 for a detailed description of the RM-8E Modem Enclosure. Figure 1-28 provides a slot location diagram of the RM-8E Modem Enclosure.

1.2.3.2.2.1 Modem Power Supplies. - Two modem power supplies are provided in each RM-8E Modem Enclosure. The power supplies act redundantly to power all modules within the enclosure. Consult the manual specified in table 1-4 for a detailed description of the modem power supplies.

1.2.3.2.2.2 RM-9600 Modem. - The RM-9600 Modem provides 9600 bits per second (bps) conversion of digital to analog or analog to digital signals over four-wire leased telephone lines. Consult the manual listed in table 1-4 for a detailed description of the RM-9600 Modem.

1.2.3.2.2.3 RM-9600E FP Modem. - The RM-9600E FP (fast poll) Modem is a fast training 9600 bit per second modem designed for use in multi-drop networks. It is used in the M1FC FSAS to provide communications channels between the AWP and FSDPS.

1.2.3.2.3 Dual Communications Processor Card Cage. - The Dual Communications Processor Card Cage, 401-37999-04, (figure 1-25) is used to house the circuit cards and power control modules which comprise two communications processors.

1.2.3.2.4 Power Control Module. - Three types of power control modules are used in the M1FC FSAS System (figure 1-13). One Power Control Module, 401-36719-01, is used in the first slot (from left to right) of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-02, is used in the last slot of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-05, is used in the first slot of card cages which do not contain KPV11-B System Module Circuit Cards.

The main function of the power control modules is to provide control and fusing for the 115 VAC between the AC junction box and power supply assemblies. The 401-36719-01 and -02 Power Control Modules contain additional wiring and connectors for interface with the KPV11-B Circuit Cards.

The AWP communications processor rack contains two Power Control Modules: one of the 401-36719-01 type, and one of the 401-46719-02 type.

1.2.3.2.5 64K Word RAM/Parity Circuit Card. - The 64K Word RAM/Parity Circuit Card, MSV11-LF, contains 64K, 16-bit words of MOS (Metal Oxide Semiconductor) RAM (Random Access Memory) and generates and detects byte parity for each word. Two 64K word RAM/parity circuit cards are provided in the AWP communications processor rack. One of the cards is used in communications processor no. 1, and the other card is used in communications processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the MSV11-LF circuit card.

1.2.3.2.6 Multiplexer Circuit Card. - The Multiplexer Circuit Card, 401-36993-03, is shown in figure 1-14. This circuit card provides a four-channel serial interface (RS449) between a communications processor's LSI-11/23 bus and external peripherals. Two multiplexer circuit cards are provided in the AWP communications processor rack.

1.2.3.2.7 Multi-Processor Linking System. - The Multi-Processor Linking System, HEX/IPB-11, contains two connected circuit cards. These cards establish six high speed communication ports between the DMA Controller Circuit Card (DMA-QB) of a communications processor and the DMA-QB Circuit Card of a position processor. Two multi-processor linking systems are provided in the AWP communications processor rack. One is used to interface the DMA-QB Circuit Card in communications processor no. 1 with the DMA-QB Circuit Card in position processor no. 1, and the other is used to interface the DMA-QB Circuit Cards in communications processors no. 2 with the DMA-QB Circuit Cards in position processors no. 2 in a redundant manner. Consult the manual listed in table 1-4 for a detailed description of the multi-processor linking system.

1.2.3.2.8 Disk Controller Circuit Card. - The Disk Controller Circuit Card, RLV12, is used to interface the RL01-AK/RL02-AK Disk Drive with the LSI-11/23 bus of a communications processor. Two disk controller circuit cards are used in the AWP communications processor rack. One card is used in communications processor no. 1, and the other card is used in communications processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the RLV12 circuit card.

1.2.3.2.9 32K Word PROM Circuit Card. - The 32K Word PROM Circuit Card, MRV11-C, contains 32K of PROM (Programmable Read Only Memory) in 16, 24-pin sockets. Two 32K word PROM circuit cards are provided in the AWP communications processor rack. One of the cards provides the PROM for communications processor no. 1, and the other card provides the PROM for Communications Processor No. 2. Consult the manual listed in table 1-4 for a detailed description of the MRV11-C circuit card.

1.2.3.2.10 System Module Circuit Card. - The System Module Circuit Card, KPV11-B, alerts the LSI-11/23 bus when a power failure occurs and restarts the LSI-11/23 Microcomputer System when power is restored. Two of these cards are provided in the AWP communications processor rack. One card is used in communications processor no. 1, and the other card is used in communications processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the KPV11-B circuit card.

1.2.3.2.11 Eight-Channel Serial I/O Circuit Card. - The Eight-Channel Serial I/O Circuit Card, 8S, provides eight channels for serial input or output of data to/from the LSI-11/23 bus. Two of these cards are provided in the AWP communications processor rack. One card is used to interface communications processor no. 1 with peripheral equipment, and the other card is used to interface communications processor no. 2 with peripheral equipment. Consult the manual listed in table 1-4 for a detailed description of the 8S circuit card.

1.2.3.2.12 DMA Controller Circuit Card. - The DMA Controller Circuit Card, DMA-QB, provides a DMA (Direct Memory Access) interface between the LSI-11/23 bus of a position processor and the LSI-11/23 bus of a communications processor using the interprocessor bus. Two DMA controller circuit cards are provided in the communications processor rack. One card is used in communications processor no. 1, and the other card is used in communications processor no. 2 in a redundant manner. Consult the manual listed in table 1-4 for a detailed description of the DMA-QB circuit card.

1.2.3.2.13 LSI-11 Processor Circuit Card. - The LSI-11 Processor Circuit Card, KDF11-AA, performs the CPU (Central Processing Unit) function for the LSI-11/23 Microcomputer System. Two LSI-11 Processor Circuit Cards are provided in the communications processor rack. One processor provides the CPU function for communications processor no. 1, and the other processor provides the CPU function for communications processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the KDF11-AA circuit card.

1.2.3.2.14 Blower Assembly. - The Blower Assembly, 401-37145-02, is shown in figure 1-16. This assembly uses fans to provide air circulation inside the AWP communications processor rack. The blower assembly is powered by 115 VAC from the fan AC junction box.

1.2.3.2.15 Power Supply Assemblies. - The Power Supply Assembly, 401-36716-01, is shown in figure 1-19. The power supply assembly provides +5VDC, +12VDC, -12VDC, and signal ground for use by rack equipment. The AWP communications processor rack contains two power supply assemblies. Consult the manual listed in table 1-4 for a detailed description of the power supply assembly.

1.2.3.2.16 Multiplexer Interface Assemblies. - The Multiplexer Interface Assembly, 401-37170-01 and -04, is shown in figure 1-18. This assembly provides an RS-449 interface for the multiplexer. Two types of multiplexer interface assemblies are used in the M1FC FSAS. One type of Multiplexer Interface Assembly, 401-37170-01, is used when the assembly is mounted in the right side of a cabinet.

The other type of Multiplexer Interface Assembly, 401-37170-04, is used when the assembly is mounted in the left side of a cabinet. Both types are electrically identical.

Two multiplexer interface assemblies are used in the AWP communications processor rack. The communications processor no. 1 uses the 401-37170-04 Multiplexer Interface Assembly, and communications processor no. 2 uses the 401-37170-01 Multiplexer Interface Assembly.

1.2.3.2.17 Thermal Sensors. - The Thermal Sensors, 401-37216-02 and 401-37204-01, are shown in figure 1-23. The thermal sensor provides temperature dependent resistance to a 2 VDC voltage sent from the Thermal Alarm Unit, 401-37155-01. The voltage is then returned to comparator circuits in the thermal alarm unit. One type of Thermal Sensor, 401-37216-02, is designed to be mounted in the upper section of an equipment cabinet. The other type of Thermal Sensor, 401-37204-01, is designed to be mounted in the lower section of an equipment cabinet. The AWP communications processor rack contains two Thermal Sensors, 401-37216-02 and 401-37204-01, whose outputs are connected to the thermal alarm unit located in the AWP communications equipment rack.

1.2.3.2.18 Fan AC Junction Box. - The Fan AC Junction Box, 401-37231-02, is shown in figure 1-22. This junction box receives primary AC power from the plain AC junction box in the AWP communications equipment rack. The fan AC junction box distributes 115 VAC to two power control modules and the blower assembly in the AWP communications processor rack.

1.2.3.3 Position Processor Rack. - The AWP Position Processor Rack, 401-12303-01, and equipment located within the rack are shown in figure 1-3. This rack is used in the AWP to house the following equipment:

1. Position Processor Card Cages, 401-37999-01
2. Memory Card Cage "A", 401-37999-02
3. Memory Card Cage "B", 401-37999-06
4. Power Control Modules, 401-36719-01, -05
5. 32K Word PROM Circuit Cards, MRV11-C
6. 64K Word RAM/Parity Circuit Cards, MSV11-LF
7. A/N OTF Processor Circuit Cards, 401-33676-01
8. Eight-Channel Serial I/O Circuit Cards, 8S
9. LSI-11 Processor Circuit Cards, KDF11-AA
10. DMA Controller Circuit Cards, DMA-QB
11. System Module Circuit Cards, KPV11-B
12. Thermal Sensor, 401-37216-02
13. A/N Quad Cache Memory Circuit Cards, 401-33692-01
14. Blower Assembly, 401-37145-02
15. DC Power Switch Assembly, 401-37916-01

16. Power Supply Assemblies, 401-36716-01
17. Keyboard Junction Box, 401-37179-08
18. Serial I/O Assemblies, 401-37274-02
19. Fan AC Junction Box, 401-37231-02

The following paragraphs describe the equipment located in the AWP position processor rack. The relationship of the equipment used in the rack is shown in figure 1-6.

1.2.3.3.1 Position Processor Card Cage. - The Position Processor Card Cage, 401-37999-01, is shown in figure 1-26. This card cage is used to house the circuit cards which make up a position processor. Two of these card cages are used in the AWP position processor rack.

1.2.3.3.2. Memory Card Cage "A". - Memory Card Cage "A", 401-37999-02, is shown in figure 1-27. This card cage is used to house two alphanumeric quad cache memory circuit cards and a power control module.

1.2.3.3.3 Memory Card Cage "B". Memory Card Cage "B", 401-37999-06, is shown in figure 1-28. This card cage is used to house two alphanumeric quad cache memory circuit cards and a power control module. It provides a redundant power supply voltage of +5 VDC to memory card cage "A".

1.2.3.3.4 Power Control Module. - Three types of power control modules are used in the MIFC FSAS (figure 1-13). One Power Control Module, 401-36719-01, is used in the first slot (left to right) of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-02, is used in the last slot of card cages containing KPV11-B System Module Circuit Cards. Another Power Control Module, 401-36719-05, is used in the first slot of card cages which do not contain KPV11-B System Module Circuit Cards. The 401-36719-01 and -02 types are provided with additional wiring and connectors for interface with the KPV11-B Circuit Cards.

The main function of the power control module in the AWP position processor rack is to provide control and fusing for the 115 VAC between the fan AC junction box and power supply assemblies. The AWP position processor rack contains four power control modules; two of the 401-36719-01 type and two of the 401-36719-05 type.

1.2.3.3.5 32K Word PROM Circuit Card. - The 32K Word PROM Circuit Card, MRV11-C, contains 32K words of PROM (Programmable Read Only Memory) in 16, 24-pin sockets. Two 32K word PROM circuit cards are provided in the AWP position processor rack. One of the cards provides the PROM for position processor no. 1, and the other card provides the PROM for position processor no. 2. Consult the manual

listed in table 1-4 for a detailed description of the MRV11-C circuit card.

1.2.3.3.6 64K Word RAM/Parity Circuit Card. - The 64K Word RAM/Parity Circuit Card, MSV11-LF, contains 64K, 16-bit words of MOS (Metal Oxide Semiconductor) RAM (Random Access Memory). It generates and detects byte parity for each word. Two 64K word RAM/parity circuit cards are provided in the AWP position processor rack. One of the cards is used in position processor no. 1 and the other card is used in position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the MSV11-LF circuit card.

1.2.3.3.7 Alphanumeric (A/N) On-The-Fly (OTF) Processor Circuit Card. - The A/N OTF Processor Circuit Card, 401-33676-01, is shown in figure 1-16. This card processes and controls alphanumeric data to and from the A/N quad cache memory circuit card. It acts as an interface between the A/N quad cache memory circuit card and the LSI-11/23 bus. Four A/N OTF processor circuit cards are used in the AWP position processor rack (two in position processor no. 1 and two in position processor no. 2).

1.2.3.3.8 Eight-Channel Serial I/O Circuit Card. - The Eight-Channel Serial I/O Circuit Card, 8S, provides eight channels for serial input or output of data to/from the LSI-11/23 bus. Four 8S cards are used in the AWP position processor rack (two in position processor no. 1 and two in position processor no. 2). Consult the manual listed in table 1-4 for a detailed description of the 8S circuit card.

1.2.3.3.9 LSI-11 Processor Circuit Card. - The LSI-11 Processor Circuit Card, KDF11-AA, performs the CPU (Central Processing Unit) function for the LSI-11/23 Microcomputer System. Two LSI-11 processor circuit cards are provided in the AWP position processor rack. One processor provides the CPU function for position processor no. 1 and the other processor provides the CPU function for position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the KDF11-AA circuit card.

1.2.3.3.10 DMA Controller Circuit Card. - The DMA Controller Circuit Card, DMA-QB, provides a DMA (Direct Memory Access) interface between the LSI-11/23 bus of a position processor and the LSI-11/23 bus of a communications processor using the interprocessor bus. Four of these cards are provided in the AWP position processor rack. Two cards are used in position processor no. 1 and the other two cards are used in position processor no. 2 in a redundant manner. Consult the manual listed in table 1-4 for a detailed description of the DMA-QB circuit card.

1.2.3.3.11 System Module Circuit Card. - The System Module Circuit Card, KPV11-B, alerts the LSI-11/23 bus when a power failure occurs and restarts the LSI-11/23 Microcomputer System when power is restored. Two of these cards are provided in the AWP position processor rack. One card is used in position processor no. 1, and the other card is used in position processor no. 2. Consult the manual listed in table 1-4 for a detailed description of the KPV11-B circuit card.

1.2.2.3.12 Thermal Sensor. - The Thermal Sensor, 401-37216-02, is shown in figure 1-23. The sensor provides temperature dependent resistance to a 2 VDC voltage sent from the thermal alarm unit, 401-37155. The voltage is then returned to comparator circuits in the thermal alarm unit. The AWP position processor rack contains one Thermal Sensor, 401-37216-02, whose output is connected to the thermal alarm unit in the AWP communications equipment rack.

1.2.3.3.13 Alphanumeric (A/N) Quad Cache Memory Circuit Card. - The A/N Quad Cache Memory Circuit Card, 401-33692-01, is shown in figure 1-15. This circuit card provides memory for up to four CRT monitors. Four of these cards are used in the AWP position processor rack.

1.2.3.3.14 Blower Assembly. - The Blower Assembly, 401-37145-02, is shown in figure 1-17. This assembly uses fans to provide air circulation inside the AWP position processor rack. The blower assembly is powered by 115 VAC from the fan AC junction box.

1.2.3.3.15 DC Power Switch Assembly. - The DC Power Switch Assembly, 401-37916-01, is shown in figure 1-29. The DC power switch assembly is used in the AWP position processor rack to provide redundant power from one memory card cage to another. It also allows maintenance to be performed on one memory card cage while the other memory card cage is still being powered.

1.2.3.3.16 Power Supply Assembly. - The Power Supply Assembly, 401-36716-01, is shown in figure 1-19. The power supply assembly provides +5VDC, +12VDC, -12VDC, and signal ground for use by rack equipment. The AWP position processor rack contains four power supply assemblies. Consult the manual listed in table 1-4 for a detailed description of the power supply assembly.

1.2.3.3.17 Keyboard Junction Box. - The Keyboard Junction Box, 401-37179-08, is shown in figure 1-20. This unit is used as an interface between keyboard units and eight-channel serial I/O circuit cards. The AWP position processor rack contains one

keyboard junction box which interfaces 12 keyboard units with two eight-channel serial I/O circuit cards.

1.2.3.3.18 Serial I/O Assembly. - The Serial I/O Assembly, 401-37274-02, is shown in figure 1-21. This assembly is provided for connections between digital patch panels and an eight-channel serial I/O circuit card. The AWP position processor rack contains two serial I/O assemblies; one used by position processor no. 1 and the other used by position processor no. 2.

1.2.3.3.19 Fan AC Junction Box. - The Fan AC Junction Box, 401-37231-02, is shown in figure 1-22. This junction box receives primary AC power from the fan AC junction box in the AWP communications processor rack. It then distributes 115 VAC to four power control modules and the blower assembly in the AWP position processor rack.

1.2.3.4 Peripheral Group. - The Peripheral Group, 401-12305-01, contains the following equipment in the AWP:

1. Input/Output Terminal (IOT), LA34-AA or LA100-CA
2. Line Printers, P300.

1.2.3.5 Keyboard Units. - The Keyboard Unit, 401-36735-03, is shown in figure 1-24. The Keyboard Unit is an input device for the position processor via the keyboard junction box. This unit is a Maxiswitch Keyboard, 2160069, which has circuit board modifications performed by E-Systems. Twelve keyboards are used in the AWP. Consult the manual listed in table 1-4 for a detailed description of the keyboard unit.

1.2.3.6 Keyboard Power Supplies. - The Keyboard Power Supply, 5305-000-423, provides +5 VDC for use by the keyboard unit. This power supply plugs directly into an AC power outlet. Twelve keyboard power supplies are used in the AWP. Consult the manual listed in table 1-4 for a detailed description of the keyboard power supply.

1.2.3.7 CRT Monitors. - The CRT Monitor, 401-37290-01, provides an output display device for the position processor via the A/N quad cache memory circuit card. The CRT monitor is a Ball TTL-150 Monitor which has been modified by E-Systems. Twelve CRT monitors are used in the AWP. Consult the manual listed in table 1-4 for a detailed description of the CRT monitor.

1.3 EQUIPMENT SPECIFICATION DATA. - Table 1-5 provides equipment specification data for equipment used in both FSDPS and AFSS.

Specifications for related equipment can be found in the manuals listed in table 1-4.

1.4 EQUIPMENT REQUIRED BUT NOT SUPPLIED. - Consult M1FC FSAS System Instruction Book, TI 6490.36, for a listing of equipment required but not supplied.

Table 1-4. Related Equipment Manuals

EQUIPMENT	MANUFACTURER	DOCUMENTATION
Analog Patch Panel, 153-020-12VF-M1	Dynatech	Analog and Digital Patch Panels Instruction Book, TI 6490.14
Input/Output Terminal, LA34-AA	Digital Equipment	LA34 Terminal Instruction Book, TI 6490.6
Input/Output Terminal, LA100-CA	Digital Equipment	LA100 Terminal Instruction Book TI 6490.39
Power Supply Assembly, 401-36716-01	LH Research	MM43 Regulated Power Supply Instruction Book, TI 6490.18
Coded Time Source, 60-DC	True Time Instruments	Model 60-DC Coded Time Source Instruction Book, TI 6490.17
CRT Monitor, TTL-150	Ball Brothers/ E-Systems	TTL 150 Display Monitor Instruction Book, TI 6490.15
Digital Patch Panel, 157-011-00 and 157-002C-00	Dynatech	Analog and Digital Patch Panels Instruction Book, TI 6490.14
Disk Controller Circuit Card, RLV12	Digital Equipment	RL01/RL02 Disk Drive, Controller RLV12 Disk Instruction Book, TI 6490.7 Rev. A
Disk Drive, DM9300TD	Ampex	DM9300TD Disk Drive Instruction Book, TI 6490.12
Disk Drive, RL01/RL02	Digital Equipment	RL01/RL02 Disk Drive, RLV12 Disk Controller Instruction Book, TI 6490.7 Rev. A
DMA Controller Circuit Card, DMA-QB	Peritek	DMA-QB, DMA Controller, and HEX-IPB Instruction Book, TI 6490.8
Eight-Channel Serial I/O Circuit Card, 8S	Technical Magic	8S Eight Channel Serial Interface Instruction Book, TI 6490.9

Table 1-4. Related Equipment Manuals
(Continued)

EQUIPMENT	MANUFACTURER	DOCUMENTATION
Keyboard Power Supply, 5305-000-423	Ault	Keyboard Unit, P/N 401-36735, Instruction Book, TI 6490.16
Keyboard Unit, 401-36735-03	Maxiswitch/ E-Systems	Keyboard Unit, P/N 401-36735, Instruction Book, TI 6490.16
Line Printer, P300	Printronix	P300 Line Printer Instruction Book, TI 6490.13
LSI-11 Processor Circuit Card, KDF11-AA	Digital Equipment	LSI-11/23 Processor and MRV11-C Memory Instruction Book, TI 6490.4
Maintenance and Diagnostic Test Set (MADTS)	E-Systems	MADTS Instruction Book, TI 6490.3 Rev. A
Modem Enclosure, RM-8E Modem, RM-9600 Modem Power Supply Manual Call Unit, RM-800 Answer/Originate Board, RM-A/O Modem, RM-208A Modem, RM-9600E FP	Universal Data Systems	RM-8E Multiple Modem System Instruction Book, TI 6490.38
Modem Sharing Device Enclosure, 2005061, and Modem Sharing Device, 2005064	Universal Data Systems	Modem Sharing Device Instruction Book, TI 6490.40
M1FC FSAS System	E-Systems	M1FC Flight Service Automation System Instruction Book, TI 6490.36
Multi-Processor Linking System, HEX/IPB-11	Peritek	DMA-QB, DMA Controller, and HEX-IPB Instruction Book, TI 6490.8
M200 Matrix Printer	Data products	M200 Matrix Printer Instruction Book, TI 6490.20

Table 1-4. Related Equipment Manuals
(Continued)

EQUIPMENT	MANUFACTURER	DOCUMENTATION
System Module Circuit Card, KPV11-B	Digital Equipment	DRV11-B DMA Interface, H9270Backplane, KPV11-B Power-Fail/Line-Time Clock Terminator Instruction Book, TI 6490.5
Tandem Equipment	Tandem	Technical Communications Library - TANDEM Instruction Book, Volume 1, TI 6490.19
Tandem Equipment	Tandem	Non Stop II Maintenance Instruction Book-Second Level, Volume 2, TI 6490.19 Non Stop II Maintenance Instruction Book - Third Level, Volume 3, TI 6490.19 Non Stop II Maintenance Instruction Book - Fifth Level, Volume 4, TI 6490.19
Tape Drive, Model 9000	Kennedy	Model 9000 Tape Drive Instruction Book, TI 6490.13
32K PROM Circuit Card, MRV11-AA	Digital Equipment	LSI-11/23 Processor and MRV11-C Memory Instruction Book, TI 6490.4
64K RAM/Parity Circuit Card, MSV11-LF	Digital Equipment	LSI-11/23 Processor and MRV11-C Memory Instruction Book, TI 6490.4

Table 1-5. Equipment Specification Data

NAMEPLATE DATA EQUIPMENT TYPE/MODEL	MANUFACTURER	FAA NO.	FUNCTIONAL CHARACTERISTICS	EXTERNAL POWER REQUIREMENTS	RATED OUTPUT
Coded Time Source Interface, 401-37207-01	E-Systems	FA-10017/4	Average Power Dissipation: 30 Watts	120 Vac at .60 Amperes	
Multiplexer Circuit Card, 401-36993-03	E-Systems	Part of FA-10018/6	Average Power Dissipation: 22 Watts; Number of Channels: 4; Channel Type: RS-449; Maximum Aggregate Data Rate: 50.4 K bits/second Maximum Channel Data Rate: 9600 bits/second	+5 Vdc at 4.25 Amperes; -12 Vdc at 0.1 Amperes	
A/N OTF Processor Circuit Card, 401-33676-01	E-Systems	Part of FA-10018/5	Average Power Dissipation: 28 Watts; Maximum Aggregate Data Rate: 1M word	+5 Vdc at 5.3 Amperes	
A/N Quad Cache Circuit Card, 401-33692-01	E-Systems	Part of FA-10018/5	Average Power Dissipation: 28.12 Watts; Number of Channels: 4; Channel Type: Video; Bit Rate: 16.34 MHz; Input Data Rate: 1 MHz, 16 bit Words (1,000,000 words/second)	+5 Vdc at 5.6 Amperes	

Table 1-5. Equipment Specification Data (Continued)

NAMEPLATE DATA			FUNCTIONAL CHARACTERISTICS	EXTERNAL POWER REQUIREMENTS	RATED OUTPUT
EQUIPMENT TYPE/MODEL	MANUFACTURER	FAA NO.			
Thermal Alarm Unit, 401-37155-01	E-Systems	FA-10018/9	Average Power Dissipation: 20 Watts	120 Vac at .25 Amperes	
Power Control Module, 401-36719	E-Systems		Average Power Dissipation: Dependent upon associated power supplies	120 Vac at 5 Amperes (max.) 5 Vdc at 50 Milliamperes	120 Vac

SECTION 2

TECHNICAL DESCRIPTION

2.1 THEORY OF OPERATION. - The following paragraphs describe the theory of operation for all equipment used in the M1FC FSAS System. The Flight Service Data Processing Subsystem (FSDPS), the Automated Flight Service Station (AFSS), and the Automated Weather Processor (AWP) are the three basic units of the M1FC FSAS system and will be discussed separately.

2.1.1 Flight Service Data Processing Subsystem (FSDPS). - The FSDPS consists of the following groups of equipment:

1. Communications Switching Rack, 401-37622
2. Communications Equipment Rack, 401-37623
3. COTC Processor Rack, 401-37624
4. Tandem Group, 401-42690
5. Peripheral Group, 401-37729
6. Communications Cable Group (part number varies among sites).

Figure 2-1 provides a block diagram showing the individual equipment contained in each group of the FSDPS and their relationship.

2.1.1.1 Communications Switching Rack. - The following paragraphs provide the theory of operation for the equipment provided in the communications switching rack.

2.1.1.1.1 Coded Time Source Interface. - The Coded Time Source (CTS) Interface, 401-37202-01, performs the following functions in the FSDPS:

1) accepts parallel data from two coded time source units; compares the data from the two units, and serializes the data for input to a Tandem asynchronous port, and

2. provides relay contact closures for the SMMC (Model D).

An intermediate logic diagram for the CTS interface is provided in figure 2-2. Each block on the intermediate logic diagram contains a circuit identifier code in the upper left-hand corner and a circled keyed text reference number in the upper right-hand corner of the block. These identifier codes and keyed text reference numbers refer to the blocked schematic diagrams provided in figure 2-3.

The CTS interface provides a time/days counter to keep track of the correct hours, minutes, and seconds of time, as well as the correct day of the year.

A clock/switch multiplexer accepts time data from a selected coded time source. The multiplexer outputs the time and day data to the time/days counter for initial setup and to a time/days multiplexer.

The output of the time/days counter and the input from a coded time source (either J2 or J3) are compared by the clock/counter comparator to ensure that the time is accurate. If the time of the counter and coded time source are different, the clock/counter failure detector will cause one of the following lamps to be lit on the front panel:

FAILURE A - J2 Clock is not accurate
FAILURE B - J3 Clock is not accurate
FAILURE X - Total failure (cause cannot be determined)

The remainder of the circuitry on this board is concerned with sending time and date data to Tandem asynchronous ports in serialized form and receiving format instructions from the ports. These circuits are discussed in detail in the blocked schematic diagrams and keyed text given in figure 2-3.

2.1.1.1.2 Coded Time Source - Consult the manual listed in table 1-4 for the theory of operation of the Coded Time Source, 60-DC.

2.1.1.1.3 Thermal Alarm Unit - The Thermal Alarm Unit, 401-37155-01, consists of a Thermal Alarm Unit I/O Circuit Card, 401-37209, and a Thermal Alarm Unit Control Circuit Card, 401-37208. These two circuit cards combine to provide a means of detecting overheating conditions which may occur during operation of rack mounted equipment.

The thermal alarm unit I/O circuit card is connected via cables to thermal sensors in equipment racks containing a blower assembly. The thermal alarm unit I/O circuit card compares the ambient temperature with exhaust temperatures and outputs an alarm signal to the thermal alarm unit control circuit card in the event of a 12° C deviation in temperature. The thermal alarm unit control circuit card provides a visual and audible alarm indication.

Figure 2-4 provides an intermediate logic diagram of the thermal alarm unit. Each block on the intermediate logic diagram contains a circuit identifier code in the upper left-hand corner and a circled keyed text reference number in the upper right-hand corner of the block. These identifier codes and keyed text reference numbers refer to the blocked schematic diagram shown in figure 2-5.

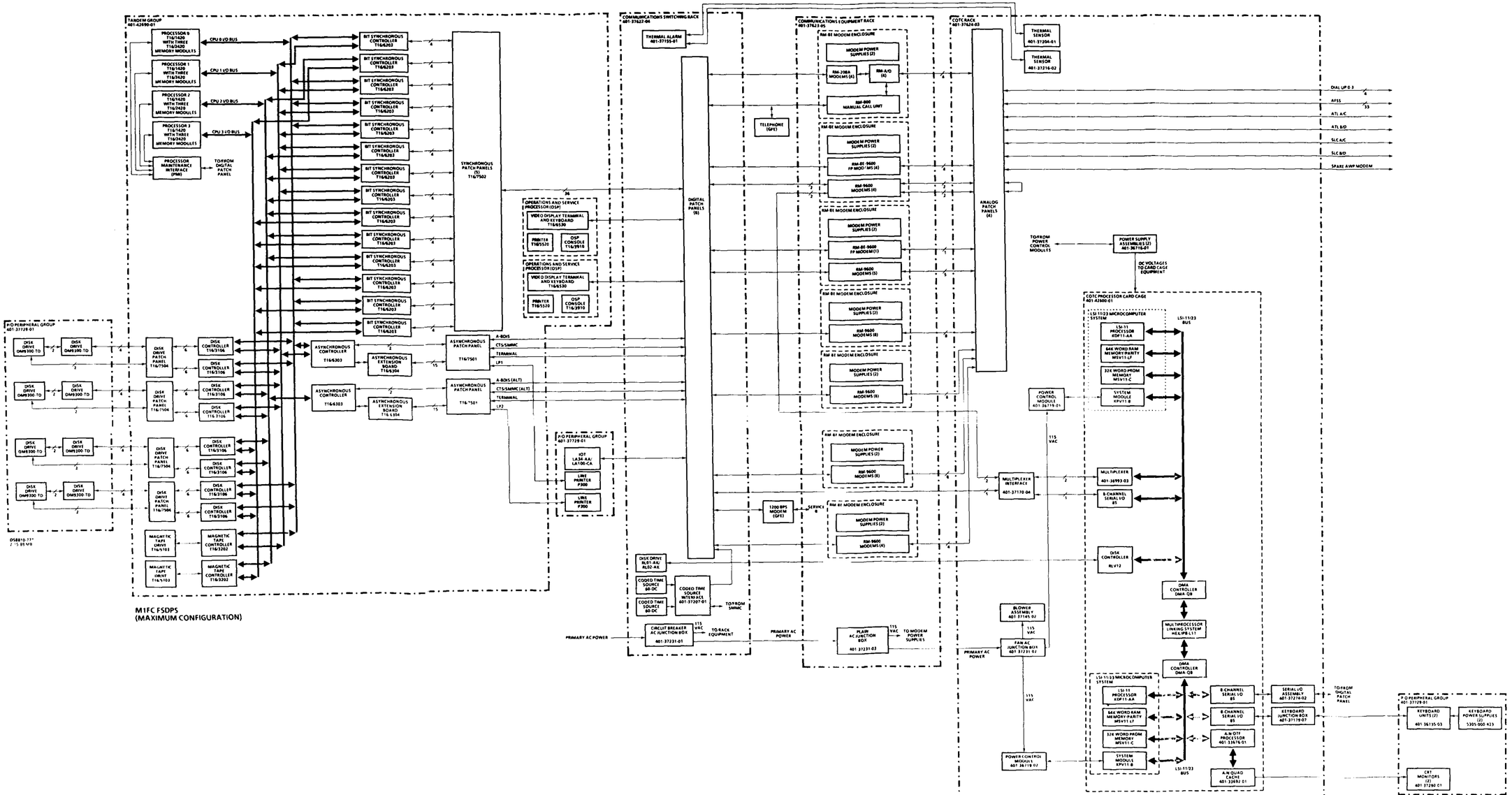


Figure 2-1. FSDPS Block Diagram

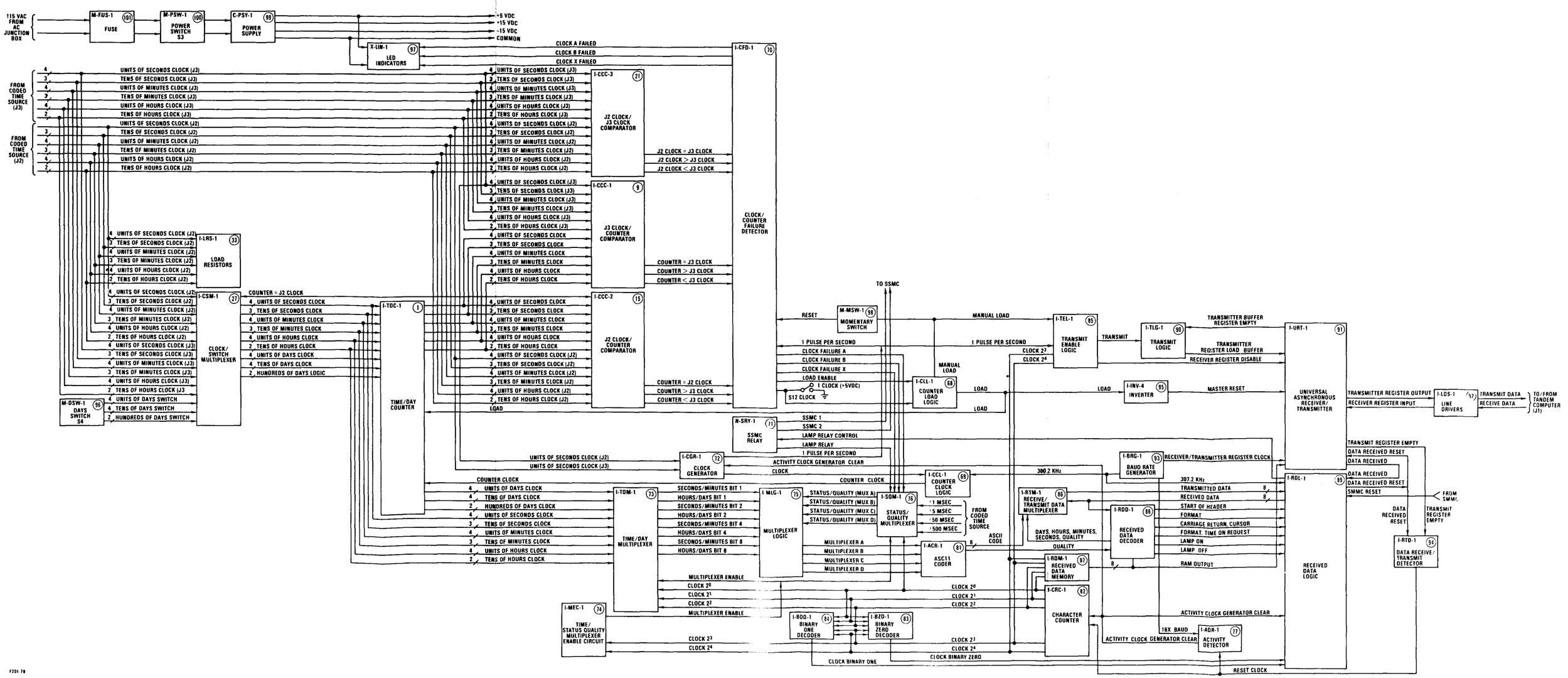


FIGURE 2-15 CODED TIME SOURCE INTERFACE INTERMEDIATE LOGIC DIAGRAM.

Figure 2-2. CTS Interface Intermediate Logic Diagram

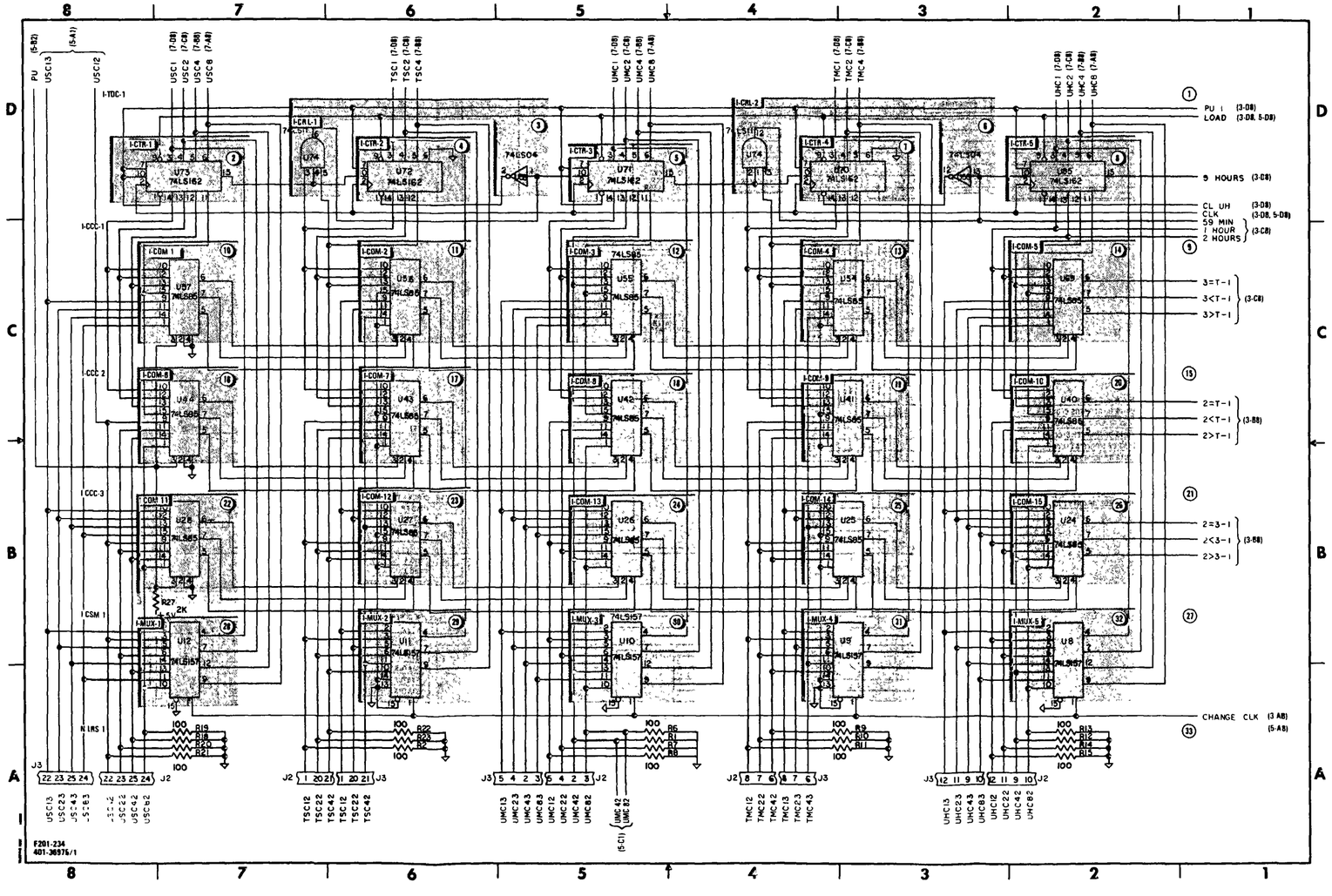


Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 1 of 13)

① **(I-TDC-1) TIME/DAY COUNTER:**

PROVIDES CORRECT COUNT OF TIME (SECONDS, MINUTES, AND HOURS) AND DAY OF YEAR IN BINARY FORMAT. LOAD INPUT ALLOWS COUNTER TO BE INITIALIZED WITH CORRECT TIME AND DAY OF YEAR FROM CODED TIME SOURCE AT FSDPS (FLIGHT SERVICE DATA PROCESSING SYSTEM). I-TDC-1 COUNT IS ADVANCED EACH TIME UNITS OF SECONDS INPUT FROM J2 CLOCK OR J3 CLOCK CHANGES STATE. J2 AND J3 CLOCKS ARE BOTH CODED TIME SOURCE UNITS AT FSDPS. THE CLOCKS CAN BE AS MUCH AS 12 MSEC APART AND ADVANCE COUNTER WITH NO ERROR. IF OVER THIS AMOUNT, LAGGING CLOCK LAMP WILL INDICATE A FAILURE ALONG WITH THE FAILURE X LAMP.

② **(I-CTR-1) COUNTER:**

COUNTS 4-BIT BINARY DECIMAL UNITS OF SECONDS TIME AND OUTPUTS BINARY TIME TO U44, I-CCC-2 (J2 CLOCK/COUNTER COMPARATOR) AND U57, I-COM-1 (J3 CLOCK/COUNTER COMPARATOR).

③ **(I-CRL-1) COUNTER RESET LOGIC:**

NAND GATE U74 PROVIDES LOGIC HIGH OUTPUT LEVEL TO CLEAR COUNTER U72 AND ENABLE U71 (I-CTR-3) WHEN BINARY 5 (0101) IS OUTPUT BY U72 AND CARRY OUTPUT SIGNAL IS OUTPUT FROM U73. U71 ADVANCES ON NEXT CLOCK PULSE. INVERTER U58 INVERTS HIGH LEVEL OUTPUT FROM U74 TO LOW LEVEL IN ORDER TO ENABLE LOW LOGIC CLEAR OF COUNTER U72 ON NEXT CLOCK PULSE.

④ **(I-CTR-2) COUNTER:**

COUNTS 3-BIT BINARY DECIMAL TENS OF SECONDS (1_, 2_, 3_, 4_ , 5_) TIME AND OUTPUTS BINARY TIME TO U43, I-CCC-2 (J2 CLOCK/COUNTER COMPARATOR) AND U56, I-COM-2 (J3 CLOCK/COUNTER COMPARATOR).

⑤ **(I-CTR-3) COUNTER:**

COUNTS 4-BIT BINARY DECIMAL UNITS OF MINUTES (0, 1, . . ., 9) TIME AND OUTPUTS BINARY TIME TO U42, I-CCC-2 (J2 CLOCK/COUNTER COMPARATOR) AND U55, I-COM-3 (J3 CLOCK/COUNTER COMPARATOR).

⑥ **(I-CRL-2) COUNTER RESET LOGIC:**

NAND GATE U74 PROVIDES LOGIC HIGH OUTPUT LEVEL TO CLEAR COUNTER U70, ENABLE I-CTR-5 (U85), AND PROVIDES 59 MIN INPUT TO I-CSL-3 WHEN BINARY 5 (0101) IS OUTPUT BY U70 AND CARRY OUTPUT SIGNAL IS OUTPUT FROM U71. U85 ADVANCES COUNT ON NEXT CLOCK PULSE. INVERTER U58 INVERTS HIGH LEVEL OUTPUT FROM U74 TO LOW LEVEL IN ORDER TO ENABLE LOW LOGIC CLEAR OF COUNTER U70 ON NEXT CLOCK PULSE.

⑦ **(I-CTR-4) COUNTER:**

COUNTS 3-BIT BINARY DECIMAL TENS OF MINUTES (0, 1, . . ., 5) TIME AND OUTPUTS BINARY TIME TO U41, I-CCC-2 (J2 CLOCK/COUNTER COMPARATOR).

⑧ **(I-CTR-5) COUNTER:**

COUNTS 4-BIT BINARY DECIMAL UNITS OF HOURS (0, 1, . . ., 9) TIME AND OUTPUTS BINARY TIME TO U40, I-CCC-2 (J2 CLOCK/COUNTER COMPARATOR) AND U69, I-COM-5 (J3 CLOCK/COUNTER COMPARATOR).

⑨ **(I-CCC-1) J3 CLOCK/COUNTER COMPARATOR:**

COMPARES J3 CLOCK SIGNALS AND COUNTER SIGNALS TO SEE IF THEY AGREE. OUTPUT SIGNALS FROM THIS COMPARATOR CIRCUIT ARE APPLIED TO CLOCK FAILURE DETECTOR (I-CFD-1). ONE OF THE FOLLOWING SIGNALS ARE OUTPUT FROM THIS COMPARATOR CIRCUIT:

1. COUNTER = J3 CLOCK
2. COUNTER > J3 CLOCK
3. COUNTER < J3 CLOCK

SHEETS 3 AND 5 OF THIS FIGURE CONTAIN ADDITIONAL CIRCUITRY FOR THIS COMPARATOR CIRCUIT.

⑩ **(I-COM-1) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF SECONDS TIME FROM I-CTR-1 (COUNTER) AND J3 CLOCK.

⑪ **(I-COM-2) COMPARATOR:**

COMPARES BINARY DECIMAL TENS OF SECONDS TIME FROM I-CTR-2 (COUNTER) AND J3 CLOCK.

⑫ **(I-COM-3) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF MINUTES TIME FROM I-CTR-3 (COUNTER) AND J3 CLOCK.

⑬ **(I-COM-4) COMPARATOR:**

COMPARES BINARY DECIMAL TENS OF MINUTES TIME FROM I-CTR-4 (COUNTER) AND J3 CLOCK.

⑭ **(I-COM-5) COMPARATOR:**

COMPARES BINARY UNITS OF HOURS TIME FROM I-CTR-5 (COUNTER) AND J3 CLOCK.

⑮ **(I-CCC-2) J2 CLOCK/COUNTER COMPARATOR:**

COMPARES J2 CLOCK SIGNALS AND COUNTER SIGNALS TO SEE IF THEY AGREE. OUTPUT SIGNALS FROM THIS COMPARATOR CIRCUIT ARE APPLIED TO CLOCK FAILURE DETECTOR (I-CFD-1). ONE OF THE FOLLOWING SIGNALS ARE OUTPUT FROM THIS COMPARATOR CIRCUIT:

1. COUNTER = J2 CLOCK
2. COUNTER > J2 CLOCK
3. COUNTER < J2 CLOCK

SHEETS 3 AND 5 OF THIS FIGURE CONTAIN ADDITIONAL CIRCUITRY FOR THIS COMPARATOR CIRCUIT.

⑯ **(I-COM-6) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF SECONDS TIME FROM I-CTR-1 (COUNTER) AND J2 CLOCK.

⑰ **(I-COM-7) COMPARATOR:**

COMPARES BINARY DECIMAL TENS OF SECONDS TIME FROM I-CTR-2 (COUNTER) AND J2 CLOCK.

⑱ **(I-COM-8) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF MINUTES TIME FROM I-CTR-3 (COUNTER) AND J2 CLOCK.

⑲ **(I-COM-9) COMPARATOR:**

COMPARES BINARY DECIMAL TENS OF MINUTES TIME FROM I-CTR-4 (COUNTER) AND J2 CLOCK.

⑳ **(I-COM-10) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF HOURS TIME FROM I-CTR-5 (COUNTER) AND J2 CLOCK.

㉑ **(I-CCC-3) J3 CLOCK/J2 CLOCK COMPARATOR:**

COMPARES J3 CLOCK SIGNALS AND J2 CLOCK SIGNALS TO SEE IF THEY AGREE. OUTPUT SIGNALS FROM THIS COMPARATOR CIRCUIT ARE APPLIED TO CLOCK FAILURE DETECTOR (I-CFD-1). ONE OF THE FOLLOWING SIGNALS ARE OUTPUT FROM THIS COMPARATOR CIRCUIT:

1. J3 CLOCK = J2 CLOCK
2. J3 CLOCK > J2 CLOCK
3. J3 CLOCK < J2 CLOCK

SHEETS 3 AND 5 OF THIS FIGURE CONTAIN ADDITIONAL CIRCUITRY FOR THIS COMPARATOR CIRCUIT.

㉒ **(I-COM-11) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF SECONDS TIME FROM J3 CLOCK AND J2 CLOCK.

㉓ **(I-COM-12) COMPARATOR:**

COMPARES BINARY DECIMAL TENS OF SECONDS TIME FROM J3 CLOCK AND J2 CLOCK.

㉔ **(I-COM-13) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF MINUTES TIME FROM J3 CLOCK AND J2 CLOCK.

㉕ **(I-COM-14) COMPARATOR:**

COMPARES BINARY DECIMAL TENS OF MINUTES TIME FROM J3 CLOCK AND J2 CLOCK.

㉖ **(I-COM-15) COMPARATOR:**

COMPARES BINARY DECIMAL UNITS OF HOURS TIME FROM J3 CLOCK AND J2 CLOCK.

㉗ **(I-CSM-1) CLOCK/SWITCH MULTIPLEXER:**

SELECTS EITHER J3 CLOCK OR J2 CLOCK TIME INPUTS FOR LOADING OF COUNTERS AND PROVIDES TIME DATA TO I-TDM-1 (TIME/DAY MULTIPLEXER).

㉘ **(I-MUX-1) MULTIPLEXER:**

SELECTS UNITS OF SECONDS TIME INPUT FROM EITHER J3 CLOCK OR J2 CLOCK.

㉙ **(I-MUX-2) MULTIPLEXER:**

SELECTS TENS OF SECONDS TIME INPUT FROM EITHER J3 CLOCK OR J2 CLOCK.

㉚ **(I-MUX-3) MULTIPLEXER:**

SELECTS UNITS OF MINUTES TIME INPUT FROM EITHER J3 CLOCK OR J2 CLOCK.

㉛ **(I-MUX-4) MULTIPLEXER:**

SELECTS TENS OF MINUTES TIME INPUT FROM EITHER J3 CLOCK OR J2 CLOCK.

㉜ **(I-MUX-5) MULTIPLEXER:**

SELECTS UNITS OF HOURS TIME INPUT FROM EITHER J3 CLOCK OR J2 CLOCK.

㉝ **(N-LRS-1) LOAD RESISTORS:**

PROVIDES REQUIRED 100 OHM LOAD FOR TIME DATA INPUTS FROM FSDPS CODED TIME SOURCE (J2 INPUTS).

Figure 2-3. CTL Interface Blocked Schematic Diagram and Keyed Text (Sheet 2 of 13)

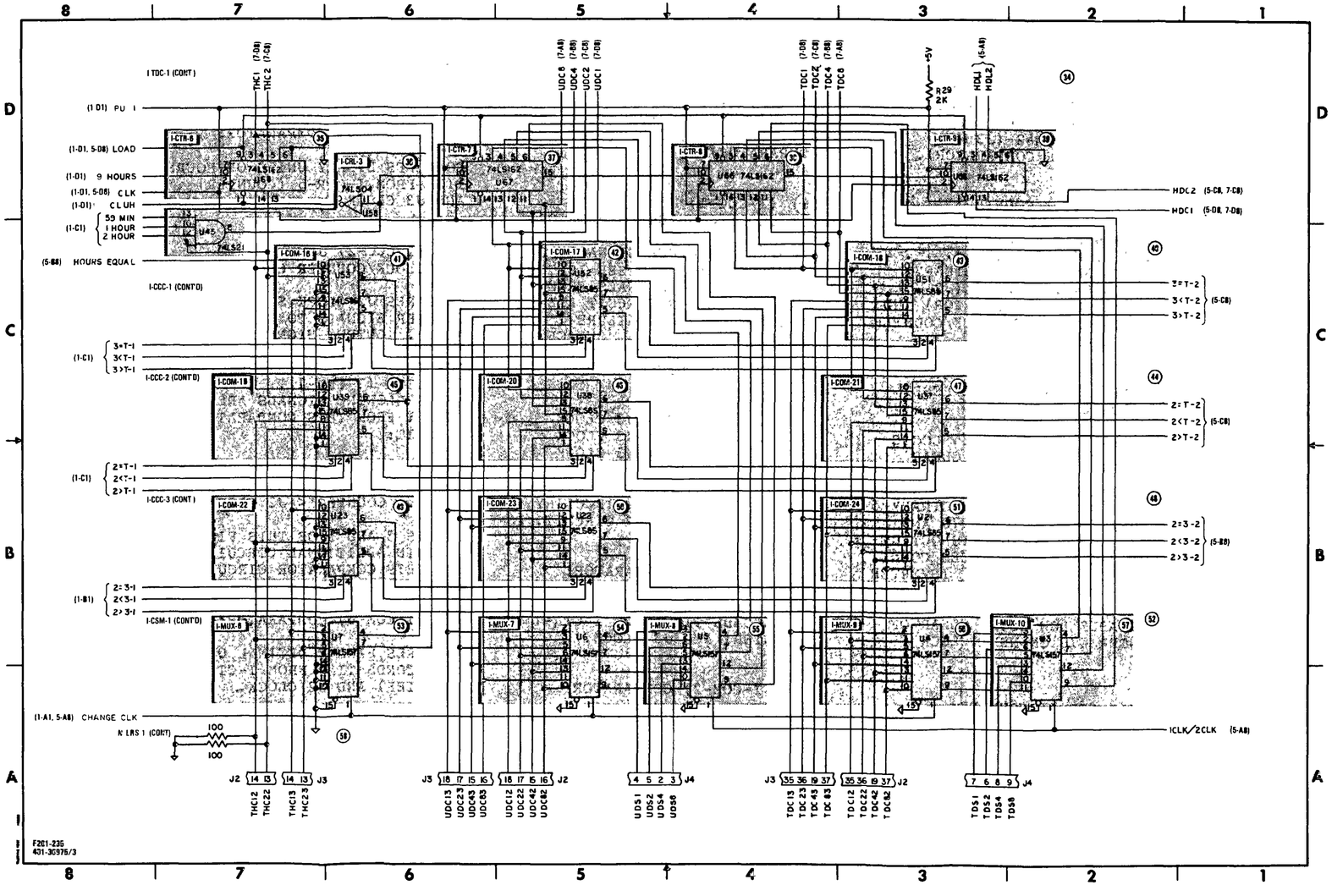


Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 3 of 13)

(34) (I-TDC-1 CONT.) TIME/DAY COUNTER:

REFER TO SHEET 2 FOR DESCRIPTION OF THIS CIRCUIT.

(35) (I-CTR-6) COUNTER:

COUNTS 2-BIT BINARY DECIMAL TENS OF HOURS TIME (0, 1, 2) AND OUTPUTS BINARY TIME TO U39, I-COM-19 (J2 CLOCK/COUNTER COMPARATOR) AND U53, I-COM-16 (J3 CLOCK/COUNTER COMPARATOR). NINE HOURS INPUT TO PIN 10 ENABLES COUNTER TO CHANGE OUTPUT WITH CLOCK PULSE.

(36) (I-CRL-3) COUNTER RESET LOGIC:

U45 PIN 8 GOES TO LOGIC HIGH LEVEL WHEN THE FOLLOWING CONDITIONS ARE MET:

1. 59 MIN SIGNAL FROM I-CRL-2 IS HIGH.
2. 1 HOUR SIGNAL FROM I-CTR-5 IS HIGH.
3. 2 HOUR SIGNAL FROM I-CTR-5 IS HIGH.
4. TENS OF HOURS SIGNAL FROM I-CTR-6 IS HIGH.

HIGH OUTPUT FROM U45 PIN 8 IS OUTPUT EVERY 24 HOURS AND ENABLES I-CTR-7 (U67). IT IS INVERTED BY U58 TO PROVIDE CLEAR INPUT FOR U68 AND U85.

(37) (I-CTR-7) COUNTER:

COUNTS 4-BIT BINARY DECIMAL UNITS OF DAYS. EACH TIME U45 PIN 8 OF I-CSL-3 OUTPUTS HIGH LOGIC LEVEL (EVERY 24 HOURS) COUNT OF U67 IS INCREMENTED BY ONE. U67 IS INITIALLY LOADED OR COUNT CHANGED BY CAUSING PIN 9 (LOAD INPUT) TO GO LOW AND LOADING OUTPUT OF I-MUX-8 (MULTIPLEXER) WHICH CONTAINS UNITS OF DAYS COUNT FROM EITHER J2 CLOCK OR J3 CLOCK. OUTPUT OF COUNTER IS OUTPUT TO U38, I-COM-20 (J2 CLOCK/COUNTER COMPARATOR) AND U52, I-COM-17 (J3 CLOCK/COUNTER COMPARATOR).

(38) (I-CTR-8) COUNTER:

COUNTS 4-BIT BINARY DECIMAL TENS OF DAYS. U66 IS ENABLED TO COUNT WHEN HIGH LOGIC LEVEL IS RECEIVED AT PIN 10 FROM U67 CARRYOUT (PIN 15) SIGNIFYING THAT UNITS OF DAYS COUNT HAS REACHED NINE. U66 IS INITIALLY LOADED OR COUNT CHANGED BY CAUSING PIN 9 (LOAD INPUT) TO GO LOW AND LOADING OUTPUT OF I-MUX-10 (MULTIPLEXER) WHICH CONTAINS TENS OF DAYS COUNT FROM SWITCH S4. OUTPUT OF COUNTER IS OUTPUT TO U37, I-COM-21, (J2 CLOCK/COUNTER COMPARATOR) AND U51, I-COM-18 (J3 CLOCK/COUNTER COMPARATOR).

(39) (I-CTR-9) COUNTER:

COUNTS 2-BIT BINARY DECIMAL HUNDREDS OF DAYS. U65 IS ENABLED TO COUNT WHEN HIGH LOGIC LEVEL IS RECEIVED AT PIN 10 FROM U66 CARRY OUT (PIN 15) SIGNIFYING THAT TENS OF DAYS COUNT HAS REACHED NINE. U65 IS INITIALLY LOADED OR COUNT CHANGED BY CAUSING PIN 9 (LOAD INPUT) TO GO LOW AND LOADING OUTPUT OF I-MUX-12 (MULTIPLEXER) WHICH CONTAINS HUNDREDS OF DAYS COUNT FROM SWITCH S4. OUTPUT OF COUNTER IS OUTPUT TO U36, I-COM-26 (J2 CLOCK/COUNTER COMPARATOR) AND U50, I-COM-25 (J3 CLOCK/COUNTER COMPARATOR).

(40) (I-CCC-1) J3 CLOCK/COUNTER COMPARATORS (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 9 ON SHEET 1 OF THIS ILLUSTRATION.

(41) (I-COM-16) COMPARATOR:

COMPARES BINARY DECIMAL TENS OF HOURS TIME FROM J-CTR-6 (COUNTER) AND J3 CLOCK.

(42) (I-COM-17) COMPARATOR:

COMPARES BINARY DECIMAL UNITS OF DAYS COUNT FROM I-CTR-7 (COUNTER) AND J3 CLOCK.

(43) (I-COM-18) COMPARATOR:

COMPARES BINARY DECIMAL TENS OF DAYS COUNT FROM I-CTR-8 (COUNTER) AND J3 CLOCK.

(44) (I-CCC-2) J2 CLOCK/COUNTER COMPARATORS (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 15 ON SHEET 1 OF THIS ILLUSTRATION.

(45) (I-COM-19) COMPARATOR:

COMPARES BINARY DECIMAL TENS OF HOURS TIME FROM I-CTR-6 (COUNTER) AND J2 CLOCK.

(46) (I-COM-20) COMPARATOR:

COMPARES BINARY DECIMAL UNITS OF DAYS COUNT FROM I-CTR-7 (COUNTER) AND J2 CLOCK.

(47) (I-COM-21) COMPARATOR:

COMPARES BINARY DECIMAL TENS OF DAYS COUNT FROM I-CTR-8 (COUNTER) AND J2 CLOCK.

(48) (I-CCC-3) J2 CLOCK/J3 CLOCK COMPARATORS (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 21 ON SHEET 1 OF THIS ILLUSTRATION.

(49) (I-COM-22) COMPARATOR:

COMPARES BINARY DECIMAL TENS OF HOURS TIME FROM J2 CLOCK AND J3 CLOCK.

(50) (I-COM-23) COMPARATOR:

COMPARES BINARY DECIMAL UNITS OF DAYS COUNT FROM J2 CLOCK AND J3 CLOCK.

(51) (I-COM-24) COMPARATOR:

COMPARES BINARY DECIMAL TENS OF DAYS COUNT FROM J2 CLOCK AND J3 CLOCK.

(52) (I-CSM-1) CLOCK/SWITCH MULTIPLEXER (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 27 ON SHEET 1 OF THIS ILLUSTRATION.

(53) (I-MUX-6) MULTIPLEXER:

SELECT TENS OF HOURS TIME INPUT FROM EITHER J2 CLOCK OR J3 CLOCK.

(54) (I-MUX-7) MULTIPLEXER:

SELECTS UNITS OF DAYS COUNT FROM EITHER J2 CLOCK OR J3 CLOCK. NEITHER J2 CLOCK NOR J3 CLOCK CONTAINS UNITS OF DAYS COUNT IN MODEL 1 SYSTEM.

(55) (I-MUX-8) MULTIPLEXER:

SELECTS UNITS OF DAYS COUNT FROM EITHER SWITCH S4 OR I-MUX-7 (MULTIPLEXER) OUTPUT.

(56) (I-MUX-9) MULTIPLEXER:

SELECTS TENS OF DAYS COUNT FROM EITHER J2 CLOCK OR J3 CLOCK.

(57) (I-MUX-10) MULTIPLEXER:

SELECTS TENS OF DAYS COUNT FROM EITHER SWITCH S4 OR I-MUX-9 (MULTIPLEXER) OUTPUT.

(58) (N-LRS-1) LOAD RESISTORS (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 33 OF THIS ILLUSTRATION.

Figure 2-3. CTC Interface Blocked Schematic Diagram and Keyed Text (Sheet 4 of 13)

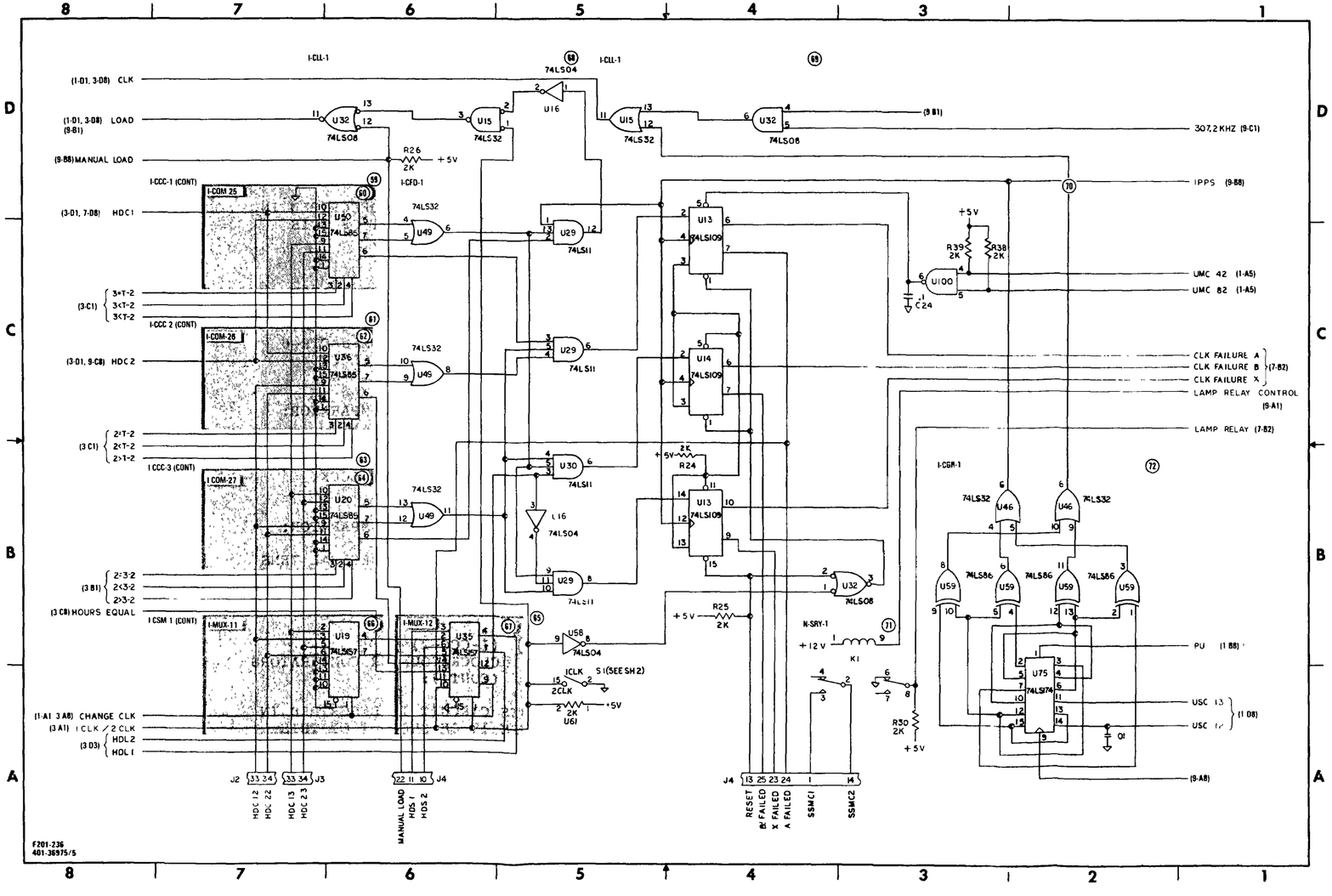


Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 5 of 13)

(59) (I-CCC-1) J3 CLOCK/COUNTER COMPARATORS (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 9 ON SHEET 1 OF THIS ILLUSTRATION.

(60) (I-COM-25) COMPARATOR:

COMPARES BINARY HUNDREDS OF DAYS COUNT FROM I-CTR-9 AND J3 CLOCK. OUTPUTS J3 CLOCK = COUNTER OR J3 CLOCK ≠ COUNTER SIGNALS TO I-CFD-1 (CLOCK FAILURE DETECTOR).

(61) (I-CCC-2) J2 CLOCK/COUNTER COMPARATORS (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 15 ON SHEET 1 OF THIS ILLUSTRATION.

(62) (I-COM-26) COMPARATOR:

COMPARES BINARY HUNDREDS OF DAYS COUNT FROM I-CTR-9 AND J2 CLOCK. OUTPUTS J2 CLOCK = COUNTER OR J2 CLOCK ≠ COUNTER SIGNALS TO I-CFD-1 (CLOCK FAILURE DETECTOR).

(63) (I-CCC-3) J2 CLOCK/J3 CLOCK COMPARATORS (CONT.):

THIS CIRCUIT IS DESCRIBED IN ITEM 21 ON SHEET 1 OF THIS ILLUSTRATION.

(64) (I-COM-27) COMPARATOR:

COMPARES BINARY DECIMAL HUNDREDS OF DAYS COUNT FROM J2 CLOCK AND J3 CLOCK. OUTPUTS J2 CLOCK = J3 CLOCK OR J2 CLOCK ≠ J3 SIGNALS TO I-CFD-1 (CLOCK FAILURE DETECTOR).

(65) (I-CSM-1) CLOCK/SWITCH MULTIPLEXER:

THIS CIRCUIT IS DESCRIBED IN ITEM 27 ON SHEET 1 OF THIS ILLUSTRATION.

(66) (I-MUX-11) MULTIPLEXER:

SELECTS BINARY DECIMAL HUNDREDS OF DAYS COUNT FROM EITHER J2 CLOCK OR J3 CLOCK.

(67) (I-MUX-12) MULTIPLEXER:

SELECTS BINARY DECIMAL HUNDREDS OF DAYS COUNT FROM SWITCH S4 AND OUTPUTS SIGNALS AS HUNDREDS OF DAYS LOGIC TO I-CTR-9 (COUNTER).

(68) (I-CLL-1) COUNTER LOAD LOGIC:

PROVIDES LOGIC LOW SIGNAL TO ENABLE LOADING OF I-TDC-1 (TIME/DAY COUNTER) WITH J2 CLOCK INPUT AND S4 SWITCH. THIS LOAD SIGNAL IS MANUALLY ENABLED BY /MANUAL LOAD INPUT SIGNAL FROM ENTER SWITCH OR AUTOMATICALLY ENABLED WHEN J2 CLOCK = J3 CLOCK AND CLOCK COUNTER.

(69) (I-CCL-1) COUNTER CLOCK LOGIC:

PROVIDES I-TDC-1 (TIME/DAY CLOCK) WITH CLOCK PULSES WHEN COUNTER IS NOT IN LOAD MODE. PROVIDES 307.2 KHZ INPUT IN LOAD MODE.

(70) (I-CFD-1) CLOCK FAILURE DETECTOR:

PROVIDES CLOCK FAILURES A, B, AND X OUTPUTS TO CLOCK FAILURE INDICATORS. CLOCK FAILURE A INDICATES THAT J2 CLOCK IS NOT ACCURATE. U13 PIN 6 OUTPUTS CLOCK FAILURE A WHEN THE FOLLOWING CONDITIONS ARE MET:

1. J3 CLOCK = CLOCK
2. J3 CLOCK ≠ J2 CLOCK
3. J2 CLOCK ≠ COUNTER

CLOCK FAILURE B INDICATES THAT J3 CLOCK IS NOT ACCURATE. U14 PIN 5 OUTPUTS CLOCK FAILURE B WHEN THE FOLLOWING CONDITIONS ARE MET:

1. J2 CLOCK ≠ J3 COUNTER
2. J3 CLOCK ≠ COUNTER
3. J2 CLOCK = COUNTER

CLOCK FAILURE X INDICATES THAT J2 CLOCK, J3 CLOCK, AND/OR COUNTER IS NOT ACCURATE. U13 PIN 10 OUTPUTS CLOCK FAILURE X WHEN THE FOLLOWING CONDITIONS ARE MET:

1. J2 CLOCK ≠ COUNTER
2. J3 CLOCK ≠ COUNTER
3. J2 CLOCK ≠ J3 CLOCK

(71) (N-SRY-1) SMMC RELAY:

ACTIVATES AND DEACTIVATES SMMC LAMP ON TANDEM COMPUTER.

(72) (I-CGR-1) CLOCK GENERATOR:

GENERATES TWO 1 PPS CLOCK SIGNALS FOR USE WITH I-CFD-1 (CLOCK FAILURE DETECTOR) AND I-CCL-1 (COUNTER CLOCK LOGIC). THESE TWO CLOCK SIGNALS ARE DELAYED IN TIME SO COUNTER CAN BE CLOCKED AND A CHECK CAN BE MADE TO SEE IF FAILURE HAS OCCURRED.

Figure 2-3. CCC Interface Blocked Schematic Diagram and Keyed Text (Sheet 6 of 13)

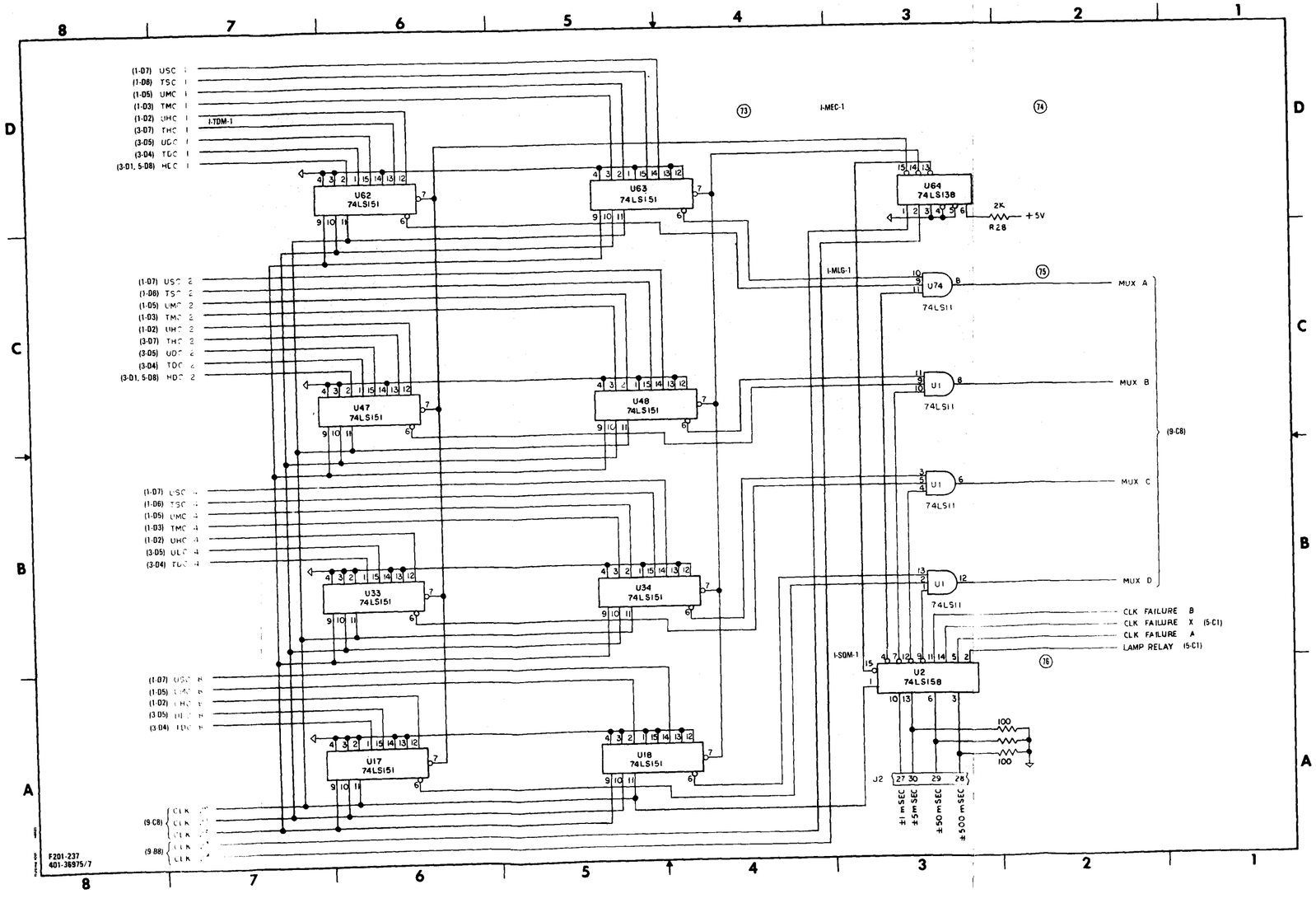


Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 7 of 13)

(73) (I-TDM-1) TIME/DAY MULTIPLEXER:

MULTIPLEXES TIME/DAY BINARY DECIMAL INPUT DATA RECEIVED FROM COMPARATORS AND COUNTERS. U62 AND U63 ARE USED TO MULTIPLEX BIT 1 OF TIME/DAY DATA. U47 AND U48 ARE USED TO MULTIPLEX BIT 2 OF TIME/DAY DATA; U33 AND U34 ARE USED TO MULTIPLEX BIT 4; AND U17 AND U18 ARE USED TO MULTIPLEX BIT 8. OUTPUTS OF MULTIPLEXER ARE SELECTED BY STATE OF CLK 2^0 - CLK 2^2 (CLOCK) SIGNALS. THESE CLOCK SIGNALS ARE APPLIED TO DATA SELECT INPUTS (PINS 9, 10, AND 11) OF EACH MULTIPLEXER (74LS151) WITHIN I-TDM-1. EACH MULTIPLEXER IS SEQUENTIALLY SELECTED BY I-MEC-1 (MULTIPLEXER ENABLE CIRCUIT). SELECTED MULTIPLEXER CHIP OUTPUTS TIME/DAY DATA TO I-MLG-1 (MULTIPLEXER LOGIC).

(74) (I-MEC-1) MULTIPLEXER ENABLE CIRCUIT:

SELECTS AND ENABLES APPROPRIATE MULTIPLEXER CHIP IN I-TDM-1 (TIME/DAY MULTIPLEXER) OR I-SQM-1 (STATUS/QUALITY MULTIPLEXER) WHEN CLOCKED BY CLK 2^3 AND CLK 2^4 (CLOCK).

(75) (I-MLG-1) MULTIPLEXER LOGIC:

CONTAINS FOUR LOGIC AND GATES TO OUTPUT MULTIPLEXED TIME/DAY DATA FOR EACH OF FOUR MULTIPLEXER CHANNELS (BITS 2, 4, AND 8). DATA PLACED ON MUX A-D CHANNELS CAN BE ONE OF THE FOLLOWING:

1. TIME/DAY DATA
2. QUALITY DATA
3. STATUS DATA

(76) (I-SQM-1) STATUS/QUALITY MULTIPLEXER:

SELECTS BETWEEN STATUS AND QUALITY DATA AND OUTPUTS SELECTED DATA TO I-MLG-1 (MULTIPLEXER LOGIC).

Figure 2-3. CIC Interface Blocked Schematic Diagram and Keyed Text (Sheet 8 of 13)

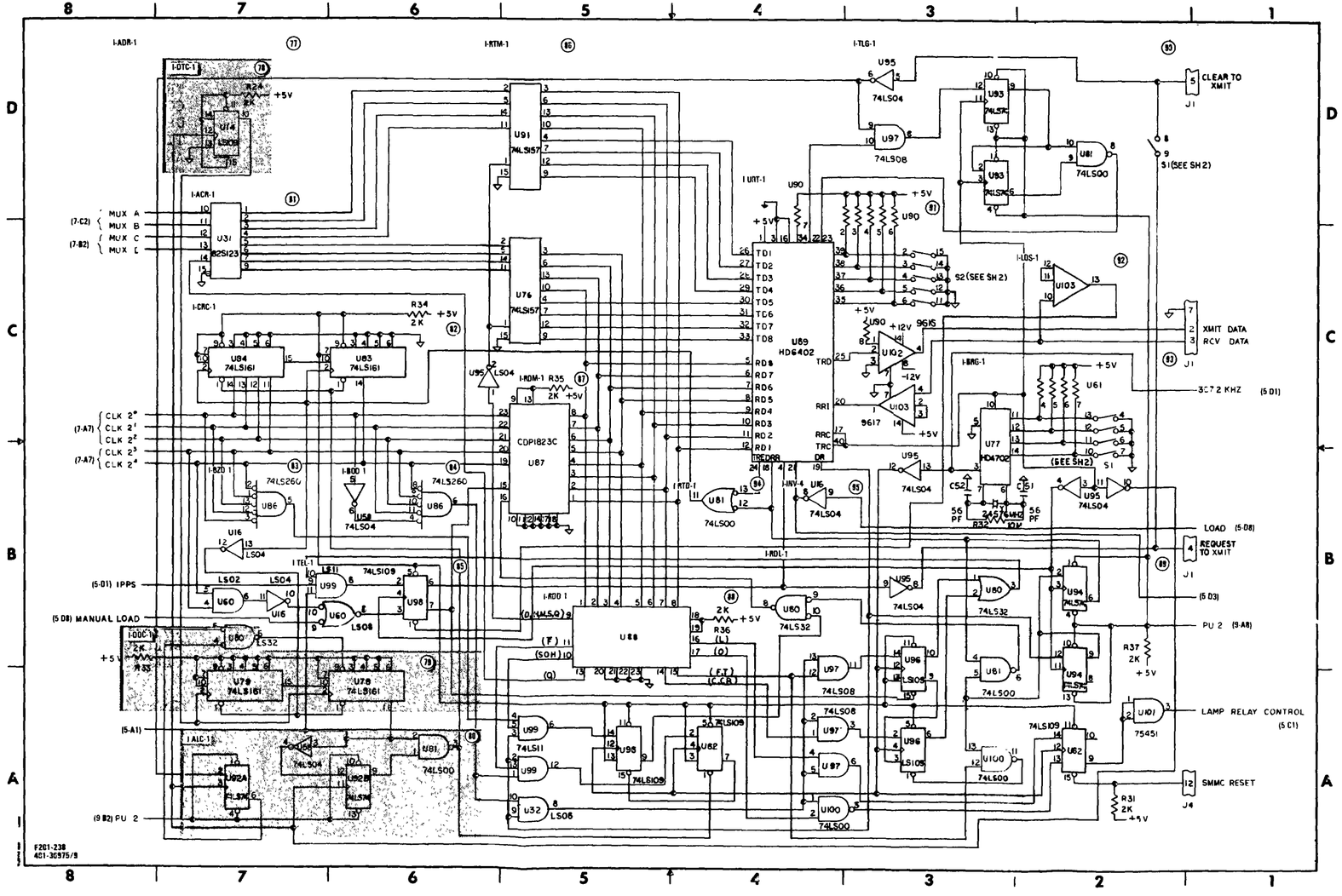


Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 9 of 13)

(77) (I-ADR-1) ACTIVITY DETECTOR:

DETECTS EITHER ACTIVITY OR NON-ACTIVITY OF I-URT-1 (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER). ACTIVITY IS PRESENT WHEN DATA IS BEING RECEIVED OR TRANSMITTED BY I-URT-1. DIVIDES 16X BAUD BY 512 FOR 750 HZ CLOCK TO I-CGR-1.

(78) (I-DTC-1) DIVIDE-BY-TWO COUNTER:

DIVIDES 16X BAUD SIGNAL FROM I-BRG-1 (BAUD RATE GENERATOR) BY TWO FOR USE AS CLOCK PULSE FOR I-DOC-1 (DIVIDE BY 128 COUNTER).

(79) (I-DOC-1) DIVIDE BY 128 COUNTER:

DIVIDES 8X BAUD SIGNAL FROM I-DTC-1 (DIVIDE BY TWO COUNTER). U80 PIN 8 CLEARS COUNTER WHEN ACTIVITY IS DETECTED. EACH TIME COUNTER IS CLEARED BEFORE REACHING COUNT OF 128 UNLESS THERE IS NO ACTIVITY. WHEN THERE IS NO ACTIVITY, COUNTER TIMES-OUT AND PIN 11 OF U78 GOES HIGH. U81 PIN 3 OUTPUTS LOGIC LOW TO I-CCR-1 (CHARACTER COUNTER) WHEN THERE IS NO ACTIVITY. THIS CLEARS CHARACTER COUNTER.

(80) (I-ALC-1) ACTIVITY LOGIC:

WHEN THERE IS ACTIVITY DETECTED BY I-DOC-1 (DIVIDE BY 128 COUNTER) U81 GOES LOW, CAUSING I-CCR-1 (CHARACTER COUNTER) TO RESET.

(81) (I-ACR-1) ASCII CODER:

CONVERTS BINARY DECIMAL TIME, DAY, STATUS, AND QUALITY DATA INTO 8-BIT ASCII DATA FOR OUTPUT TO COMPUTER. U88 PIN 13 IS AT HIGH LOGIC LEVEL FOR QUALITY DATA.

(82) (I-CRC-1) CHARACTER COUNTER:

DIVIDE-BY-24 COUNTER SERVES THE FOLLOWING FUNCTIONS:

1. SELECTS DESIRED INPUT DATA FOR I-TDM-1 (TIME/DAY MULTIPLEXER) USING CLK 2^0, 2^1, AND 2^2 CLOCK OUTPUTS.

2. SELECTS DESIRED MULTIPLEXER CHIP ON I-TDM-1 OR QUALITY MULTIPLEXER (I-QMX-1) BY PROVIDING CLK 2^3 AND CLK 2^4 CLOCK SIGNALS TO SELECT INPUTS OF I-MEC-1 (MULTIPLEXER ENABLE CIRCUIT).

3. ADDRESSES I-RDM-1 (RECEIVED DATA MEMORY) USING CLK 2^0 THROUGH CLK 2^4 CLOCK OUTPUTS.

4. CLK 2^3 AND CLK 2^4 CLOCK OUTPUTS ALLOW RESETTING OF I-TEL-1 (TRANSMIT ENABLE LOGIC).

5. CLOCK OUTPUTS ARE INPUT TO I-BZD-1 (BINARY ZERO DETECTOR) AND I-BOD-1 (BINARY ONE DETECTOR) TO DETECT WHEN BINARY ZERO AND ONE ARE OUTPUT BY I-CRC-1.

(83) (I-BZD-1) BINARY ZERO DETECTOR:

DETECTS BINARY ZERO OUTPUT FROM I-CRC-1 (CHARACTER COUNTER) AND OUTPUTS LOGIC HIGH WHEN ZERO IS DETECTED. LOGIC HIGH OUTPUT FROM U86 PIN 5 IS INPUT TO I-RDL-1 (RECEIVED DATA LOGIC). START OF HEADER (SOH) MUST BE FIRST CHARACTER RECEIVED (WHEN CLOCK OUTPUT FROM I-CRC-1 IS ZERO) OR I-RDL-1 WILL NOT ALLOW RECEPTION AND STORAGE OF DATA.

(84) (I-BOD-1) BINARY ONE DETECTOR:

DETECTS BINARY ONE OUTPUT FROM I-CRC-1 (CHARACTER COUNTER) AND OUTPUTS LOGIC HIGH WHEN ONE IS DETECTED. LOGIC HIGH OUTPUT FROM U86 PIN 6 IS INPUT TO I-RDL-1 (RECEIVED DATA LOGIC). FORMAT (/F) MUST BE SECOND CHARACTER RECEIVED (WHEN CLOCK OUTPUT FROM I-CRC-1 IS BINARY ONE) OR I-RDL-1 WILL NOT ALLOW RECEPTION AND STORAGE OF DATA.

(85) (I-TEL-1) TRANSMIT ENABLE LOGIC:

ENABLES TRANSMITTING OF DATA TO COMPUTER WHEN PIN 6 OF U98 IS AT HIGH LOGIC LEVEL. U98 IS RESET WHEN CLK 2^3 AND CLK 2^4 SIGNALS GO HIGH, OR /MANUAL LOAD SIGNAL IS INPUT TO U60 PIN 9, OR INPUT SIGNAL ACTIVITY IS DETECTED BY I-LDS-1 (U103, PIN 13).

(86) (I-RTM-1) RECEIVE/TRANSMIT MULTIPLEXER:

SELECTS EITHER STORED DATA FROM I-RDM-1 (RECEIVED DATA MEMORY) OR TIME, DAY, QUALITY, AND STATUS DATA FROM I-ACR-1 (ASCII CODER). OUTPUTS SELECTED DATA TO I-URT-1 (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER). OUTPUT OF I-RTM-1 IS SELECTED BY I-RDD-1 (RECEIVED DATA DECODER) U88, PIN 9.

(87) (I-RDM-1) RECEIVED DATA MEMORY:

PROVIDES RAM (RANDOM ACCESS MEMORY) TO STORE FORMAT INFORMATION FROM FSDPS COMPUTER IN RECEIVE MODE AND CONTROLS FORMAT OF TRANSMITTED DATA.

(88) (I-RDD-1) RECEIVED DATA DECODER:

DECODES DATA RECEIVED FROM COMPUTER AND OUTPUTS LOGIC HIGH LEVELS WHEN THE FOLLOWING DATA IS DETECTED:

1. D, H, M, S, Q - DAYS, HOURS, MINUTES, SECONDS, STATUS, QUALITY
2. /F - FORMAT
3. SOH - START OF HEADER
4. Q - QUALITY
5. L - LAMP ON
6. O - LAMP OFF
7. F, T - FORMAT, TIME ON REQUEST
8. C, CR - CONTINUOUS TIME, CARRIAGE RETURN

(89) (I-RDL-1) RECEIVED DATA LOGIC:

PROVIDES LOGIC CIRCUITS TO ACCEPT INPUTS FROM I-RDD-1 (RECEIVED DATA DECODER) AND PERFORM THE FOLLOWING FUNCTIONS:

1. ENSURE THAT SOH (START OF HEADER) IS FIRST CHARACTER RECEIVED FROM COMPUTER; IF NOT, DATA RECEPTION IS NOT ACTED UPON.

2. ENSURE THAT /F, F (FORMAT) IS SECOND CHARACTER RECEIVED FROM COMPUTER; IF NOT THEN DATA RECEPTION IS NOT ACTED UPON.

3. ACTIVATES LAMP (SMMC) RELAY K1 WHEN L SIGNAL APPEARS ON PIN 16 OF U88.

4. DEACTIVATES LAMP (SMMC) RELAY K1 WHEN O SIGNAL APPEARS ON PIN 17 OF U88.

5. ENABLES RESETTING OF I-TEL-1 (TRANSMIT ENABLE LOGIC) WHEN DATA IS READY TO TRANSMIT).

(90) (I-TLG-1) TRANSMIT LOGIC:

DETECTS WHEN I-URT-1 (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER) IS READY TO STORE DATA FOR TRANSMISSION AND ENABLES DATA TO BE STORED IN BUFFER WITHIN I-URT-1.

(91) (I-URT-1) UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER:

RECEIVES SERIAL START BITS, DATA, PARITY BIT, AND STOP BITS FROM COMPUTER AND CONVERTS SERIAL DATA INTO PARALLEL DATA FOR USE WITHIN CODED TIME SOURCE INTERFACE. CONVERTS PARALLEL DATA WITHIN CODED TIME SOURCE INTERFACE INTO SERIAL DATA FOR TRANSMISSION TO COMPUTER.

(92) (I-LDS-1) LINE DRIVERS:

U102 CONVERTS OUTGOING DATA AT TTL LOGIC LEVELS INTO RS-232-C COMPATIBLE SIGNAL LEVELS. U103 CONVERTS INCOMING RS-232-C SIGNAL LEVELS INTO TTL COMPATIBLE LOGIC LEVELS. U103 IS USED TO RESET U98 IN I-TEL-1 (TRANSMIT ENABLE) WHEN RECEIVED DATA IS DETECTED.

(93) (I-BRG-1) BAUD RATE GENERATOR:

PROVIDES I-URT-1 (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER) WITH RECEIVE AND TRANSMIT CLOCK AT FREQUENCY OF 16 X BAUD RATE (16 X 2400). ALSO PROVIDES 307.2 KHZ CLOCK SIGNAL FOR USE IN I-RDL-1 (RECEIVED DATA LOGIC).

(94) (I-RTD-1) RECEIVE/TRANSMIT DETECTOR:

PROVIDES CLOCK PULSE TO I-CRC-1 (CHARACTER CLOCK) WHEN I-URT-1 (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER) IS READY TO RECEIVE OR TRANSMIT NEXT CHARACTER.

(95) (I-INV-4) INVERTER:

INVERTS LOAD SIGNAL SO THAT WHEN CODED TIME SOURCE INTERFACE IS INITIALLY LOADED WITH CORRECT TIME, I-URT-1 (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER) WILL BE INITIALLY RESET (/LOAD).

Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 10 of 13)

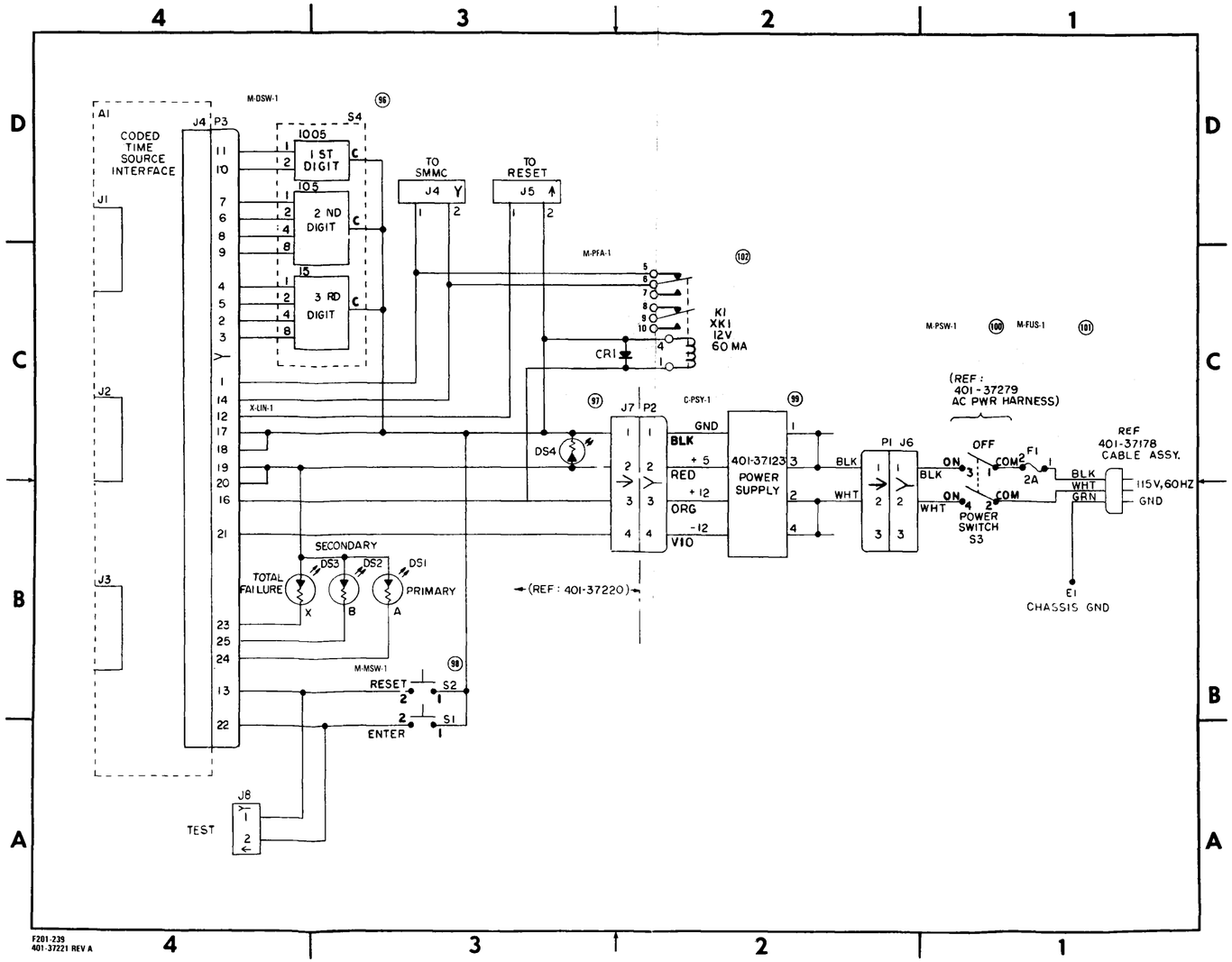


Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 11 of 13)

(96) (M-DSW-1) DAYS SWITCH:

THUMBWHEEL SWITCHES LOCATED ON FRONT PANEL OF CODED TIME SOURCE INTERFACE. ALLOWS SELECTION OF FIRST, SECOND, AND THIRD DIGIT OF DAY OF YEAR (JULIAN DATE).

(97) (X-LIN-1) LED INDICATORS:

DS1, WHEN LIT, INDICATES A J2 CODED TIME SOURCE CLOCK FAILURE (FAILURE B). DS2, WHEN LIT, INDICATES A J3 CODED TIME SOURCE CLOCK FAILURE (FAILURE B). DS3, WHEN LIT, INDICATES A TOTAL FAILURE (FAILURE X).

(98) (M-MSW-1) MOMENTARY SWITCHES:

RESET PUSH BUTTON SWITCH RESETS FAILURE INDICATOR LEDS (DS1, 2, AND 3) TO OFF STATE WHEN PRESSED. ENTER PUSHBUTTON SWITCH ALLOWS DAY COUNT IN M-DSW-1 (DAY SWITCH) TO BE LOADED INTO COUNTER WHEN PRESSED.

(99) (C-PSY-1) POWER SUPPLY:

PROVIDES +5VDC, +15VDC, AND -15VDC FROM 115 VAC FOR USE BY CODED TIME SOURCE INTERFACE.

(100) (M-PSW-1) POWER SWITCH:

PROVIDES 115 VAC TO C-PSY-1 (POWER SUPPLY) WHEN IN ON POSITION.

(101) (M-FUS-1) FUSE:

PROVIDES PROTECTION FOR CODED TIME SOURCE INTERFACE BY REMOVING 115 VAC WHEN CURRENT REQUIREMENT OVER 2 AMPS IS DETECTED.

(102) (M-PFA-1) POWER FAILURE ALARM:

RELAY K1 ESTABLISHES CONTACT CLOSURE ON TWO SMMC LINES TO SIGNIFY ALARM CONDITION WHEN POWER SUPPLY C-PSY-1 IS INOPERATIVE. WHEN C-PSY-1 IS OPERATIVE, K1 IS ENERGIZED AND OPENS SMMC LINES. DIODE CR1 PROVIDES TRANSIENT PROTECTION FOR RELAY K1.

Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 12 of 13)

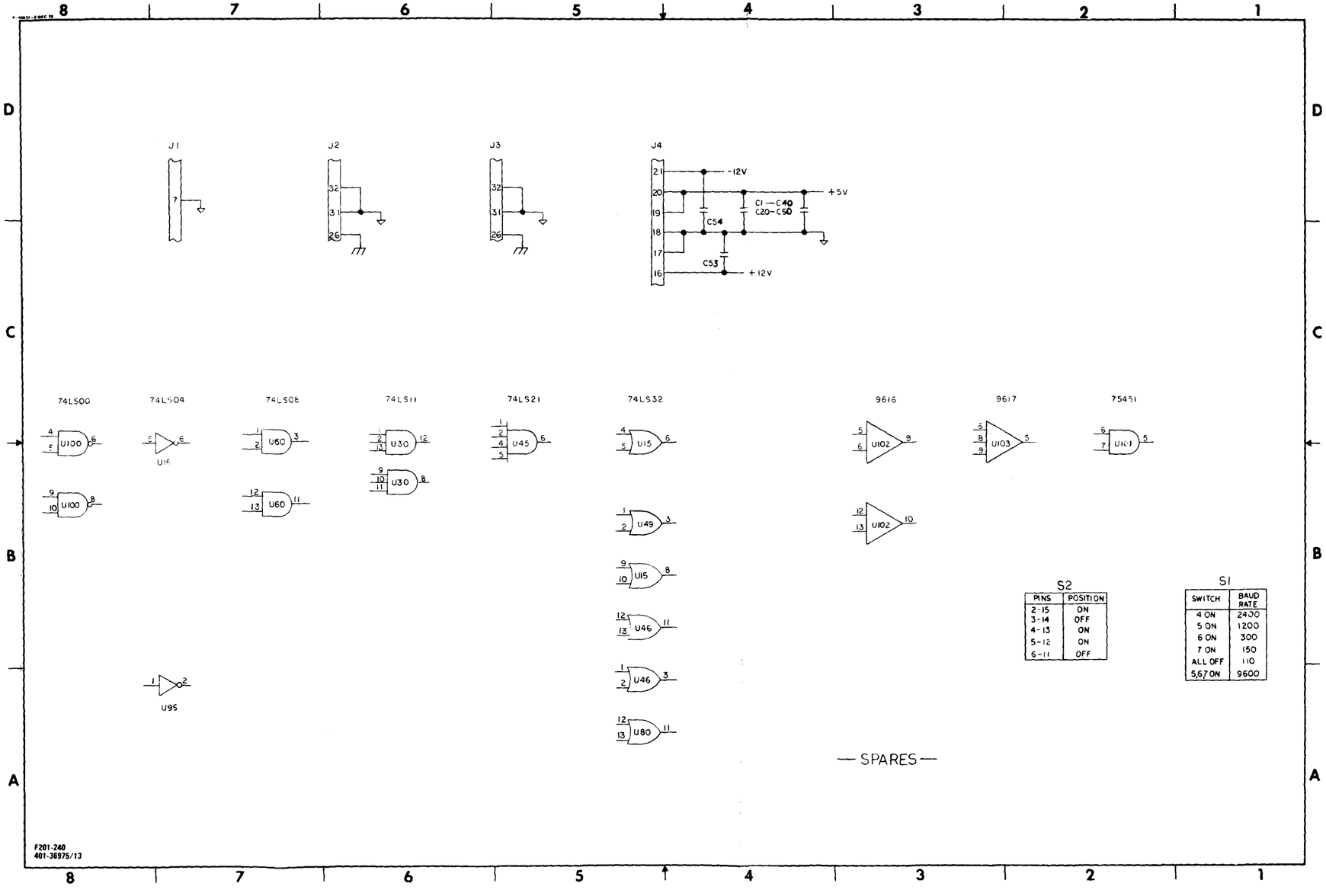


Figure 2-3. CTS Interface Blocked Schematic Diagram and Keyed Text (Sheet 13 of 13)

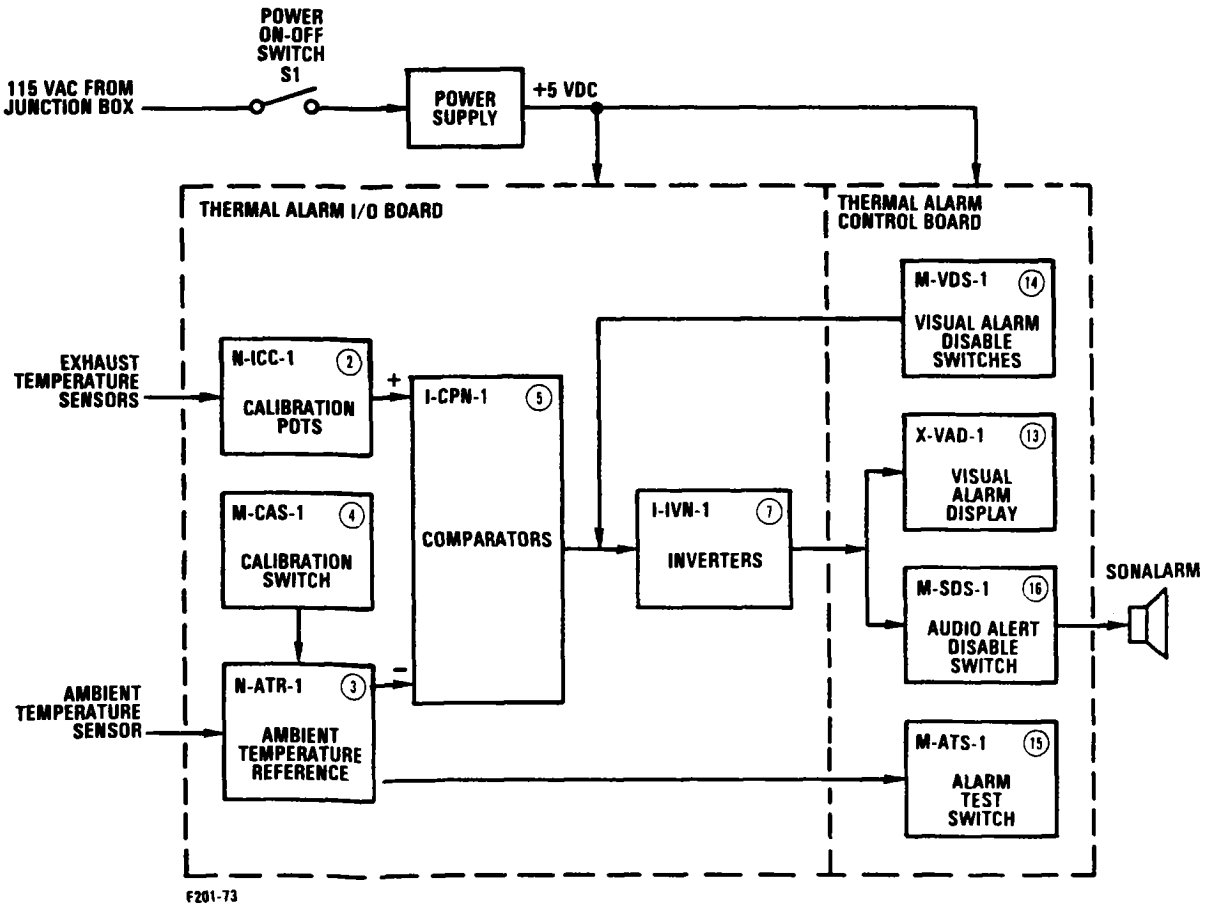


Figure 2-4. Thermal Alarm Unit Simplified Block Diagram

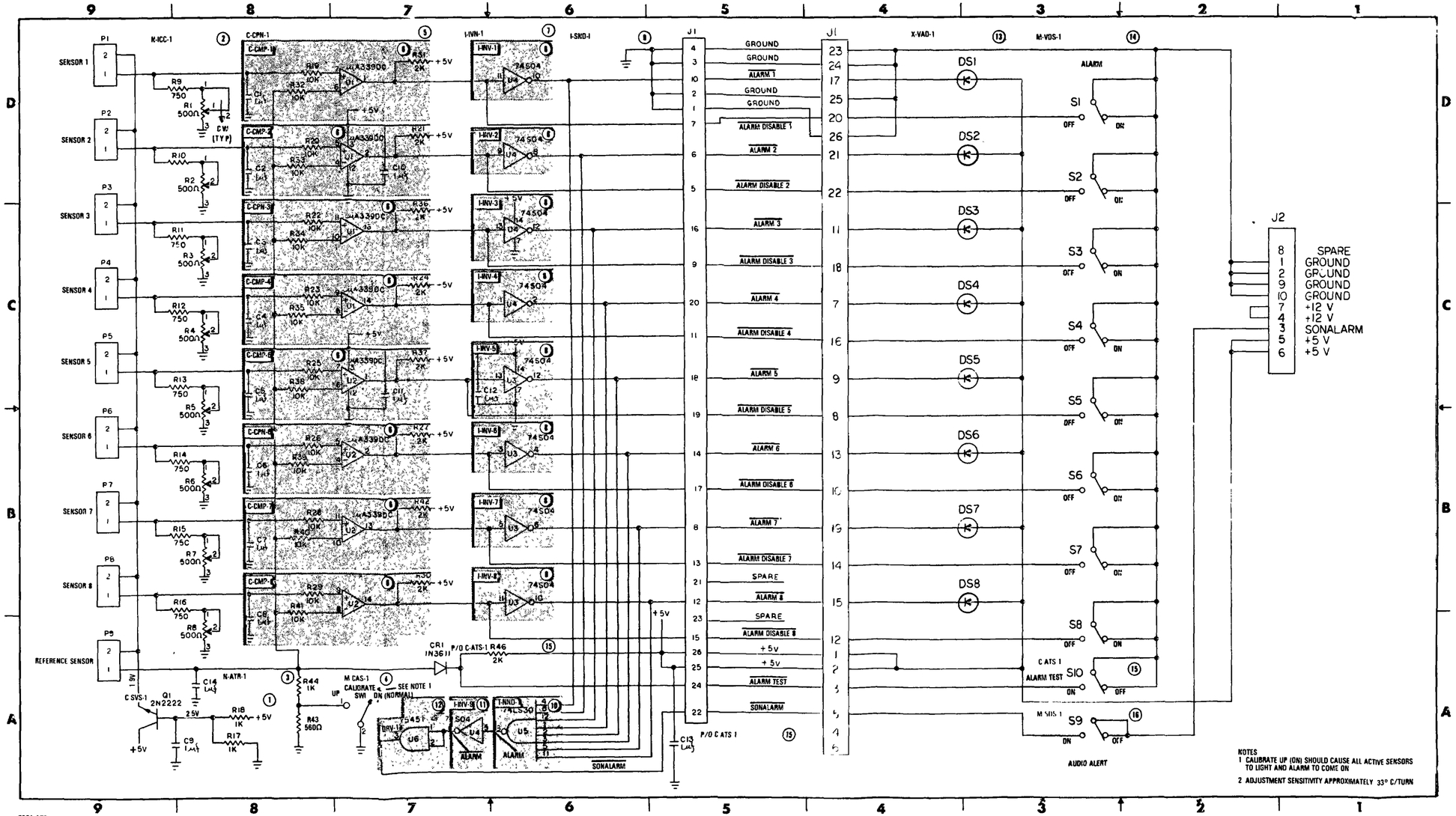


Figure 2-5. Thermal Alarm Unit Blocked Schematic Diagram and Keyed Text (Sheet 1 of 2)

(1) (C-SVS-1) SENSOR VOLTAGE SUPPLY:

C-SVS-1 CONSISTS OF RESISTORS R17, R18, CAPACITOR C9, AND TRANSITOR Q1. THESE COMPONENTS ARE CONFIGURED AS EMITTER FOLLOWER TO PROVIDE A 2.0 VDC SUPPLY VOLTAGE TO EXTERNALLY CONNECTED THERMISTORS (P1 THRU P9, PIN 2).

(2) (N-ICC-1) INPUT CALIBRATION CIRCUIT:

N-ICC-1 CONSISTS OF FIXED RESISTORS R9 THRU R16, AND POTENTIOMETERS R1 THRU R8, WHICH WORK IN CONJUNCTION WITH CALIBRATION SWITCH SW1 (M-CAS-1) TO PROVIDE MEANS OF ADJUSTING EXHAUST VOLTAGE INPUTS (P1 THRU P8, PIN 1). WHEN SWITCH SW1 (M-CAS-1) IS SET TO ON POSITION AND EXHAUST SENSORS ARE EXPOSED TO AMBIENT TEMPERATURES, POTENTIOMETERS R1 THRU R8 MAY BE ADJUSTED TO TRIGGER RESPECTIVE VISUAL ALARM INDICATORS (LEDS) IN X-VAD-1 (VISUAL ALARM DISPLAY) AND SIMULTANEOUSLY TRIGGER SONALARM.

(3) (N-ATR-1) AMBIENT TEMPERATURE REFERENCE:

N-ATR-1 CONSISTS OF FILTER CAPACITOR C14 AND RESISTORS R43 and R44. AMBIENT TEMPERATURE INPUT AT P9, PIN 1, IS FILTERED BY CAPACITOR C14, AND "DROPPED" ACROSS RESISTORS R43, R44. REFERENCE VOLTAGE ACROSS R43, R44 IS APPLIED TO THE NEGATIVE INPUTS OF COMPARATORS I-CMP-1 THRU I-CMP-8.

(4) (M-CAS-1) CALIBRATION SWITCH:

M-CAS-1 CONSISTS OF SWITCH SW1. WHEN SWITCH SW1 IS SET TO ON POSITION RESISTOR R43 (N-ATR-1) IS BYPASSED, CHANGING AMBIENT TEMPERATURE REFERENCE VOLTAGES APPLIED TO I-CMP-1 THRU I-CMP-8. THIS PERMITS POTENTIOMETERS IN N-ICC-1 (INPUT CALIBRATION CIRCUIT) TO BE ADJUSTED IN MANNER DESCRIBED IN 2. AFTER N-ICC-1 POTENTIOMETERS ARE ADJUSTED, SWITCH SW1 IS DE-ACTIVATED, RETURNING RESISTOR R43 TO CIRCUIT, AND RESTORING NORMAL AMBIENT TEMPERATURE REFERENCE VOLTAGE.

(5) (C-CPN-1) COMPARATOR NETWORK:

C-CPN-1 CONSISTS OF COMPARATORS C-CMP-1 THRU C-CMP-8 AND THEIR ASSOCIATED COMPONENTS. C-CPN-1 PROVIDES MEANS OF COMPARING THE AMBIENT TEMPERATURE, MONITORED BY THERMISTOR CONNECTED AT P9, WITH INDIVIDUAL EXHAUST TEMPERATURES, MONITORED BY THERMISTORS CONNECTED AT P1 THRU P8.

(6) (C-CMP-1 THRU C-CMP-8) COMPARATORS:

C-CMP-1 THRU C-CMP-8 FUNCTION IDENTICALLY. FOR PURPOSES OF DISCUSSION, AND TO ELIMINATE REDUNDANCY, ONLY C-CMP-2 IS DESCRIBED.

C-CMP-2 CONSISTS OF FILTER CAPACITOR C2, SERIES COUPLED INPUT RESISTORS R20 (POSITIVE EXHAUST TEMPERATURE INPUT) AND R33 (NEGATIVE AMBIENT TEMPERATURE REFERENCE INPUT), COMPARATOR U1, PINS 2, 3, 4, 5 AND 12, FILTER CAPACITOR C10, AND OUTPUT LOADING RESISTOR R21. EXHAUST TEMPERATURE SIGNAL FROM N-ICC-1 (P2, PIN 1) IS FILTERED BY CAPACITOR C2 AND APPLIED TO PIN 5 OF COMPARATOR U1 VIA RESISTOR R20. AMBIENT TEMPERATURE REFERENCE VOLTAGE FROM N-ATR-1 (AMBIENT TEMPERATURE REFERENCE) IS APPLIED TO PIN 4 OF U1 VIA RESISTOR R33. COMPARATOR U1 COMPARES TWO INPUTS, AND WHEN AN EXHAUST TEMPERATURE VARIATION OF GREATER THAN 12 ± 2 DEGREES CENTIGRADE (AS COMPARED WITH AMBIENT TEMPERATURE) OCCURS, HIGH OUTPUT SIGNAL FROM U1, PIN 2 IS APPLIED TO I-INV-2. FILTER CAPACITOR C10 IS CONNECTED BETWEEN POSITIVE SUPPLY INPUT TO U1 (PIN 3) AND GROUND (PIN 12) AND THUS PROVIDES OVERALL FILTERING FOR ALL U1 COMPARATORS.

(7) (I-IVN-1) INVERTER NETWORK:

I-IVN-1 CONSISTS OF INVERTERS I-INV-1 THRU I-INV-8 (U3 AND U4).

(8) (I-INV-1 THRU I-INV-8) INVERTERS:

I-INV-1 THRU I-INV-8 FUNCTION IDENTICALLY. FOR PURPOSES OF DISCUSSION AND TO ELIMINATE REDUNDANCY, ONLY I-INV-2 IS DESCRIBED.

HIGH ALARM SIGNAL OUTPUT FROM I-CMP-2 IS INVERTED BY I-INV-2, AND LOW OUTPUT FROM I-INV-2 IS APPLIED TO DS2 (X-VAD-1), ILLUMINATING LED. GROUND APPLIED TO U4, PIN 9 FROM SWITCH S2 (M-VDS-1) BEING ACTIVATED, IS INVERTED, RESULTING IN HIGH OUTPUT FROM U4, PIN 8, EXTINGUISHING LED DS2. OUTPUT FROM U4, PIN 8 IS ALSO APPLIED TO I-SND-1 (SONALARM DETECTION CIRCUIT).

(9) (I-SND-1) SONALARM DETECTION CIRCUIT:

I-SND-1 CONSISTS OF I-NND-1, I-INV-9, AND I-DRV-1.

(10) (I-NND-1) NAND GATE:

I-NND-1, NAND GATE U5, ACCEPTS OUTPUTS FROM I-INV-1 THRU I-INV-8. PRESENCE OF ANY LOW (ALARM SIGNAL) AT INPUT OF U5 RESULTS IN HIGH OUTPUT FROM U5, PIN 8 APPLIED TO I-INV-9.

(11) (I-INV-9) INVERTER:

I-INV-9 INVERTS OUTPUT OF I-NND-1 AND APPLIES OUTPUT TO I-DRV-1.

(12) (I-DRV-1) DRIVER:

I-DRV-1 (U6) OUTPUTS ACTIVE LOW LOGIC LEVEL TO M-SDS-1 (SONALARM DISABLE SWITCH) AND, IF SWITCH IS IN OFF POSITION, SONALARM IS ACTIVATED. I-DRV-1 OUTPUTS HIGH LOGIC LEVEL WHEN SONALARM IS NOT DESIRED.

(13) (X-VAD-1) VISUAL ALARM DISPLAY:

X-VAD-1 CONSISTS OF LEDS DS1 THRU DS8. A LOW OUTPUT FROM I-INV-1 THRU I-INV-8 LIGHTS RESPECTIVE LED, PROVIDING VISUAL INDICATION OF ALARM CONDITION.

(14) (M-VDS-1) VISUAL ALARM DISABLE SWITCHES:

M-VDS-1 CONSISTS OF SWITCHES S1 THRU S8. SETTING ANY OR ALL SWITCHES TO ON POSITION APPLIES GROUND TO RESPECTIVE INVERTER (I-INV-1 THRU I-INV-8) AND DISABLES (EXTINGUISHES) CORRESPONDING LED (DS1 THRU DS8).

(15) (C-ATS-1) ALARM TEST SWITCH:

C-ATS-1 CONSISTS OF SWITCH S10, RESISTOR R46, FILTER CAPACITOR C13, AND DIODE CR1. SETTING SWITCH S10 TO ON POSITION PLACES GROUND, VIA DIODE CR1, AT AMBIENT TEMPERATURE INPUTS TO I-CMP-1 THRU I-CMP-8, EFFECTIVELY BYPASSSING RESISTORS R43 AND R44. THIS GROUND POTENTIAL CREATES ALARM SIGNALS FROM ALL COMPARATORS, ILLUMINATING ALL LEDS IN X-VAD-1 AND ACTIVATING SONALARM SIGNAL TO M-SDS-1.

(16) (M-SDS-1) SONALARM DISABLE SWITCH:

M-SDS-1 CONSISTS OF SWITCH S9. SWITCH S9, WHEN SET TO ON POSITION, PROHIBITS PASSAGE OF SONALARM SIGNAL TO SONALARM CONNECTED AT J2, PIN 3. WHEN SET TO OFF POSITION, SWITCH S9 ENABLES THRUPUT OF SONALARM SIGNAL.

Figure 2-5. Thermal Alarm Unit Blocked Schematic Diagram and Keyed Text (Sheet 2 of 2)

2.1.1.1.3.1 Thermal Alarm Unit I/O Circuit Card. - The thermal alarm unit I/O circuit card has the following two types of externally supplied inputs:

1) eight EXHAUST TEMPERATURE SENSOR inputs from thermal sensors located within AFSS and FSDPS equipment racks equipped with a blower assembly.

2) AMBIENT TEMPERATURE SENSOR input which provides a reference thermal input based on room temperature.

The EXHAUST TEMPERATURE SENSOR input can be adjusted using Calibration Potentiometers R1-R8 located within the Input Calibration Circuit (N-ICC-1). The calibration switch input to the Ambient Temperature Reference circuit (N-ATR-1) works in conjunction with the calibration potentiometers to provide a means of optimizing the detection of temperature variations exceeding the 12 ± 2° C fluctuation specified in design parameters. Calibrated EXHAUST and AMBIENT TEMPERATURE SENSOR signals are input to Comparators (I-CPN-1) which detect temperature variations exceeding specified limits. When variation limits are exceeded, the respective comparator(s) provide(s) an output alarm signal to the thermal alarm unit control circuit card via Inverters (I-INV-1).

2.1.1.1.3.2 Thermal Alarm Unit Control Circuit Card. - Alarm signals from the thermal alarm unit I/O circuit card are input to the Visual Alarm Display (X-VAD-1) consisting of eight LEDs. These alarm signals are also input to the AUDIO ALERT DISABLE ON/OFF Switch (M-SDS-1). Respective LEDs in the visual alarm display are lighted when an alarm condition is present. Similarly, the presence of an alarm condition on any of the EXHAUST TEMPERATURE SENSOR lines is applied to the AUDIO ALERT DISABLE ON/OFF Switch. When the AUDIO ALERT DISABLE ON/OFF Switch is set to the ON position, the alarm signal is output to a sonalarm externally connected to the thermal alarm unit control circuit card. Individual alarm conditions may be inhibited from providing both a visual and/or audible alarm condition by setting the respective ALARM DISABLE ON/OFF Switch and/or the AUDIO ALERT DISABLE ON/OFF Switch to the OFF position. The ALARM TEST ON/OFF Switch effectively disables the AMBIENT TEMPERATURE SENSOR input; thus enabling all visual alarm signals (LEDs) and the sonalarm (provided that the AUDIO ALERT DISABLE Switch is set to the OFF position).

Figure 2-5 provides a blocked schematic diagram with keyed text describing the operation of the thermal alarm unit.

2.1.1.1.4 Digital Patch Panel. - Consult the manual listed in table 1-4 for the theory of operation of the Digital Patch Panel, 157-002C-00.

2.1.1.1.5 Disk Drive. - Consult the manual listed in table 1-4 for the theory of operation of the RL01-AK/RL02-AK Disk Drive.

2.1.1.1.6 Circuit Breaker AC Junction Box. - The Circuit Breaker AC Junction Box, 401-37231-01, is used in racks where primary AC power enters the equipment. The circuit breaker AC junction box has the capability to connect or disconnect AC power to or from the following:

1) communications switching rack,
2) communications equipment rack,
3) COTC processor rack, and
4) utility outlets on above three racks.

A wiring diagram for the Circuit Breaker AC Junction Box is shown in figure 10-8.

2.1.1.2 Communications Equipment Rack. - The communications equipment rack in the FSDPS contains a maximum of seven RM-8E Modem Enclosures with modem equipment and a Plain AC Junction Box, 401-37231-03.

2.1.1.2.1 RM-8E Modem Enclosure. - The RM-8E Modem Enclosure contains the following circuit cards in the communications equipment rack:

1) Modem Card, RM-9600,
2) Modem Card, RM-208,
3) Modem Card, RM-9600E FP,
4) Answer/Originate Card, RM-A/O,
5) Manual Call Unit, RM-800, and
6) Modem Power Supplies.

Consult the manual listed in table 1-4 for the theory of operation of the RM-8E modem equipment.

2.1.1.2.2 Plain AC Junction Box. - The Plain AC Junction Box, 401-37231-03, distributes AC power to the modem power supplies. It also provides AC power to the fan AC junction box in the COTC processor rack.

A wiring diagram for the plain AC junction box is shown in figure 10-10.

2.1.1.3 COTC Processor Rack. - The following paragraphs provide the theory of operation for the equipment provided in the COTC processor rack.

2.1.1.3.1 Analog Patch Panel. - Consult the manual listed in table 1-4 for the theory of operation of the Analog Patch Panel, 153-020-12VF-M1.

2.1.1.3.2 COTC Processor Card Cage. - The COTC Processor Card Cage, 401-42600-J1, contains the circuit cards which comprise one communications processor and one position processor.

2.1.1.3.2.1 Communications Processor. - The communications processor establishes handshakes to interface incoming data to the LSI-11/23 bus (Q-BUS). The communications processor performs cyclic redundancy checks as required by the ADCCP (Advanced Data Communications Control Procedure) protocol, and directs alphanumeric products to the selected processor. The communications processor is redundant in the AFSS. The redundant processor equipment is automatically switched into the system when a fault develops in the primary system equipment.

Incoming data from the FSDPS is received from the modems by the multiplexer interface assembly where it is applied to the multiplexer circuit card which provides the necessary interface between the LSI-11/23 bus and the communications equipment (patch panels and modems). After being multiplexed, incoming data is placed on the communications processor's internal Q-BUS. The data on the Q-BUS is routed by the LSI-11/23 to either the multiplexer circuit card or to a position processor via the interprocessor bus. The interprocessor communications is a multidrop system utilizing parallel direct memory access (DMA) channels. Processor communication selection is handled on a daisy chain priority-interrupt protocol.

Each LSI-11/23 processing subsystem includes a system module circuit card (KPV11-B). This circuit card combines the functions of real time clock, bus termination, and power fail and restart circuitry.

The communications architecture is structured around a control/data or A bus and an input/output (I/O) bus. DMA (direct memory access) data transfer is interlocked so that data is transferred from the communications processor to the position processor receiver CPU. The position processor is identified by decoding three identifier bits in the control register. The communications processor generates all required protocol, such as: bus handshaking, bus time-out, interrupt request, and interrupt vectoring. The communications processor has a self-contained bootstrap loader. External interrupts are initiated by:

1) a flag condition initiated by an interrupt request from the position processor,

2) an external power failure or shift-down, and

3) a predefined bus error or word-count zero condition.

The DMA interface supports two basic types of interrupts (internal and external) and contains separate enable logic for each type. An external interrupt is an interrupt that is generated by a flag from the interprocessor buffer located within the Multi-Processor Linking System, HEX/IPB-11. An internal interrupt is the result of either the byte counter reaching a zero condition or if there is sufficient delay in the response of an address to permit the bus time-out counter to cycle. Either one of these interrupts will set an interrupt request flip-flop then generate a BUS INTERRUPT REQUEST signal.

The BUS INTERRUPT REQUEST signal remains in effect until a BUS REQUEST GRANT signal is initiated by the interrupt service routine. The BUS REQUEST GRANT signal resets the bus request flip-flop until another interrupt request is received.

The DMA transfer request occurs at the interprocessor buffer. The DMA interface, however, determines the size and in what direction the transfer goes. The interprocessor buffer is merely the transfer medium. The interprocessor buffer makes a DMA transfer request. For example, the communications processor latches the data read from its memory, then makes a DMA request of the receiving position processor. Then, the communications processor makes the latched data available for it to write into its memory. When the position processor has completed its operation, the interprocessor buffer reinitiates the cycle. This process is repeated until the communications processor fails to respond to a DMA request. This usually happens because the byte count has been exhausted.

The byte count is monitored by a special purpose register called the byte count register. The byte count register (located on the DMA interface) is loaded with the complement of the number of bytes to be transferred, prior to a DMA transfer. Each time a word is transferred, this register is incremented by two. When the ultimate count of 177777 (octal) is obtained, further DMA transfer is inhibited. An interrupt is generated provided that the interrupt system is enabled.

The disk subsystem consists of a RLV12 Disk Controller and a RL01-AK or RL02-AK Disk Drive. The disk controller monitors and reports hardware error and status information for both the disk controller and the disk drive. The RL01-AK storage capacity is approximately 5.2 megabytes, while the RL02-AK storage capacity is approximately 10.4 megabytes. Average access time is 60 to 65 milliseconds. The RL01-AK/RL02-AK also includes closed-loop track following which eliminates all calibration requirements. The RL01-AK/RL02-AK system is direct-memory-accessed.

2.1.1.3.2.2 Position Processor - The position processor receives and transmits data over the interprocessor bus using the DMA Controller. The received data from the communications

processor is processed by the LSI-11/23 Microcomputer System which selects the appropriate A/N on-the-fly (OTF) processor circuit card. The A/N OTF processor circuit card contains pico processors (EPPs) which control the output of data to appropriate CRT monitors. The A/N quad cache circuit card provides memory locations for input data to be displayed on CRT monitors. The position processor is redundant in the AFSS; the redundant processor equipment is automatically switched into the system when a fault develops in the primary system equipment.

2.1.1.3.3 LSI-11 Processor Circuit Card, KDF11-AA. - Consult the manual listed in table 1-4 for the theory of operation of the KDF11-AA circuit card.

2.1.1.3.4 64K Word RAM Memory/Parity Circuit Card, MSV11-C. - Consult the manual listed in table 1-4 for the theory of operation of the MSV11-C circuit card.

2.1.1.3.5 System Module Circuit Card, KPV11-B. - Consult the manual listed in table 1-4 for the theory of operation of the the KPV11-B circuit card.

2.1.1.3.6 Disk Controller Circuit Card, RLV12. - Consult the manual listed in table 1-4 for the theory of operation of the RLV12 circuit card.

2.1.1.3.7 DMA Controller Circuit Card, DMA-QB. - Consult the manual listed in table 1-4 for the theory of operation of the DMA-QB circuit card.

2.1.1.3.8 Eight-Channel Serial I/O Circuit Card, 8S. - Consult the manual listed in table 1-4 for the theory of operation of the 8S circuit card.

2.1.1.3.9 Multi-Processor Linking System, HEX/IPB-L11. - Consult the manual listed in table 1-4 for the theory of operation of the HEX/IPB-L11 circuit cards.

2.1.1.3.10 Multiplexer Circuit Card. - The Multiplexer Circuit Card, 401-36993-03, is an intelligent, multi-protocol, four-channel serial communication device used in the M1FC FSAS to provide an interface between the LSI-11/23 Processor and external peripherals. The multiplexer has an 8085 microprocessor which permits the multiplexer to relieve the LSI-11/23 of routine tasks that do not require system level decisions.

Data transfers between the multiplexer and LSI-11 are direct memory access (DMA) transfers initiated and controlled by the 8085 microprocessor.

The four serial communications channels serving peripherals are full duplex RS-449 ports capable of asynchronous, bit synchronous and byte synchronous communications. Each channel can be clocked internally or externally.

Figure 2-6 is an intermediate logic diagram of the multiplexer. Each block on the intermediate logic diagram contains a circuit identifier code in the upper left-hand corner and a circled keyed text reference number in the upper right-hand corner of the block. These identifier codes and keyed text reference numbers refer to the blocked schematic diagrams provided in figure 2-7.

The multiplexer is divided into two major functional areas: the local processor and the Q-Bus controller (QBC).

The local processor consists of the following:

I-LPR-1	Local Processor
I-LMM-1	Local Microprocessor Memory
I-TCS-1	Timer-Counters
I-DDY-1	Diagnostic Display
I-PIO-1	Parallel Input/Output Logic
I-SCR-1, 2	Serial Input/Output Controllers
I-LDR-1, 2, 3, 4	Line Drivers/Receivers
I-BEP-1	Bus Exchange Port
I-EAP-1	Extended Address Port
I-QCP-1	Q-Bus Controller Command Port.

I-LPR-1 is an 8085 eight-bit parallel microprocessor. I-LPR-1 divides a crystal oscillator input of 9.8304 MHz by two to derive an operating frequency of 4.9152 MHz used for timing by various functions on the multiplexer. The I-LPR-1 operating sequence begins with an instruction fetch from memory. The 16-bit address of the next instruction is placed on the address bus, selecting one of a possible 65,536 locations in memory. Read and write control lines determine the transaction to be performed. After the address has been latched, the address/data bus function changes, and data is passed between I-LPR-1 and memory or I/O device. When a transfer of data is complete, I-LPR-1 informs the LSI-11 processor by means of an interrupt. Interrupt vectors are programmable and vary depending on the event completed. All transactions are timed to ensure completion within predetermined time limits, and thus prevent bus "hangups".

The multiplexer uses two 8K x 8 EPROMs and four 2K x 8 RAMs to provide storage for firmware, message data and CPU variables. The EPROMs store firmware instructions used by I-LPR-1. The lower 32K bytes of memory are reserved for memory devices (RAM, EPROM) and the upper 32K bytes are reserved for I/O ports. Thus, either an input/output instruction or a memory move instruction can be selected when moving data to/from the I/O ports. Two of the RAMs

mapped into the upper 32K bytes of memory are multi-function devices containing 256 bytes of RAM, typically reserved for a program stack.

Timer-Counters are contained in three integrated circuits and serve two purposes. One timer-counter is a processor controlled variable length event timer. The remaining timer-counters generate clock signals to operate the four serial I/O channels at the various standard communication baud rates. Thus, channel operation is programmable by I-LPR-1 and the channel configuration can be down loaded by the LSI-11 Processor.

The diagnostic display provides a visual indication of multiplexer's performance by means of eight red LEDs and one green LED. These LEDs display error codes indicating conditions occurring during self-test, upon initialization, or during normal operation. The green LED illuminated indicates normal operation, and when extinguished, indicates catastrophic failure in the multiplexer. A list of error codes is provided in table 2-1.

Six parallel I/O ports contained in two integrated circuits are used on the multiplexer board. Three of the ports are programmed as output ports from I-LPR-1. The remaining three ports are input ports to I-LPR-1. The majority of signals are control/status lines for the four RS-449 channels. One output line from I-PIO-1 (TEST GO) operates the green LED in I-DDY-1. The balance of lines are used to control the QBC and to receive status information from the QBC.

Two multi-protocol serial controllers (MPSCs) are used to provide control for the four serial I/O ports. Each MPSC contains two full duplex channel controllers (each operating independently), an interrupt controller, sync logic and cylic redundancy check (CRC) logic. The MPSCs can accommodate:

HDLC Private Lines (9600 bps, Full Duplex)
HDLC Switched Lines (4800 bps, Full Duplex)
Asynchronous Switched Lines (1200 bps, Full Duplex)
Asynchronous Printers (9600 bps, Half Duplex).

Line drivers/receivers servicing the four serial I/O channels provide TTL to RS-423 and RS-423 to TTL conversion for interface with external devices. RS-423 lines are unbalanced. They require a pair of wires for each circuit, grounded at the generator and terminated at the associated receiver.

Data that must be moved between the QBC and I-LPR-1 is temporarily stored in the bus exchange port. The bus exchange port is a dual port,16-byte register array. Data from I-LPR-1 is written into or read from the bus exchange port in byte format. The QBC moves data to/from the bus exchange port in either word or byte format. Data may be read from any register and may be written to different registers simultaneously from either port. Handshaking between the QBC and I-LPR-1 prohibits simultaneous attempts to write to the same register. The bus exchange port registers include the

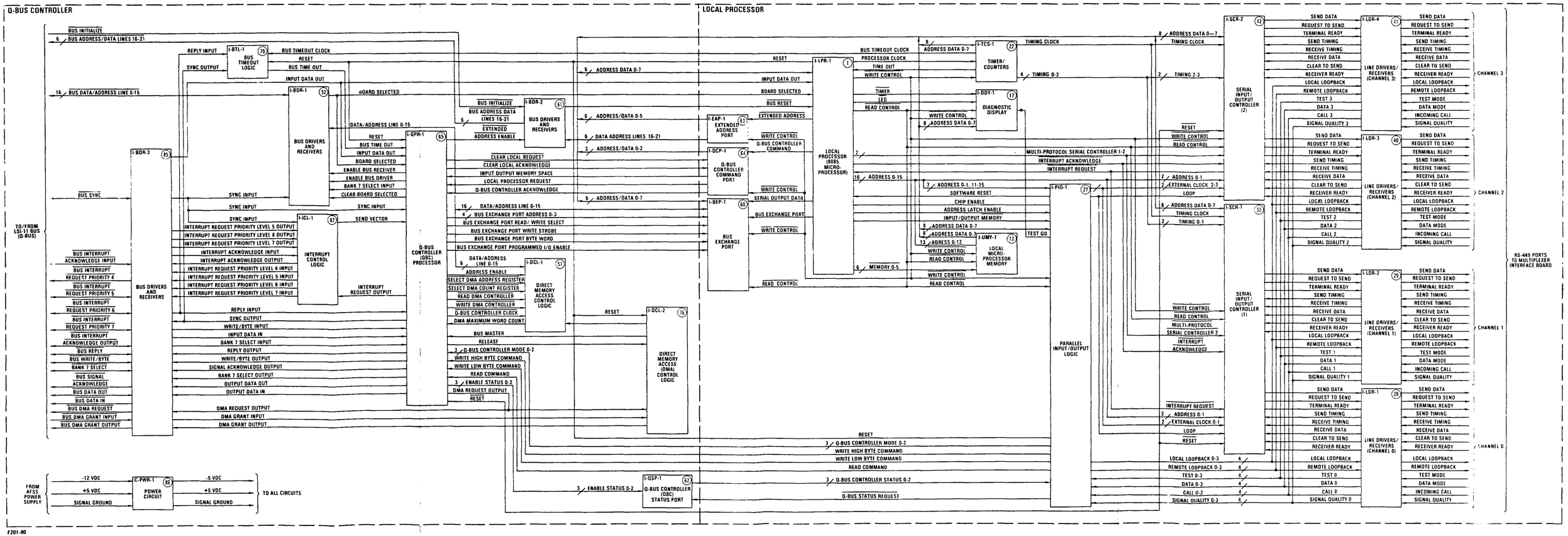


Figure 2-6. Multiplexer Circuit Board Intermediate Logic Diagram

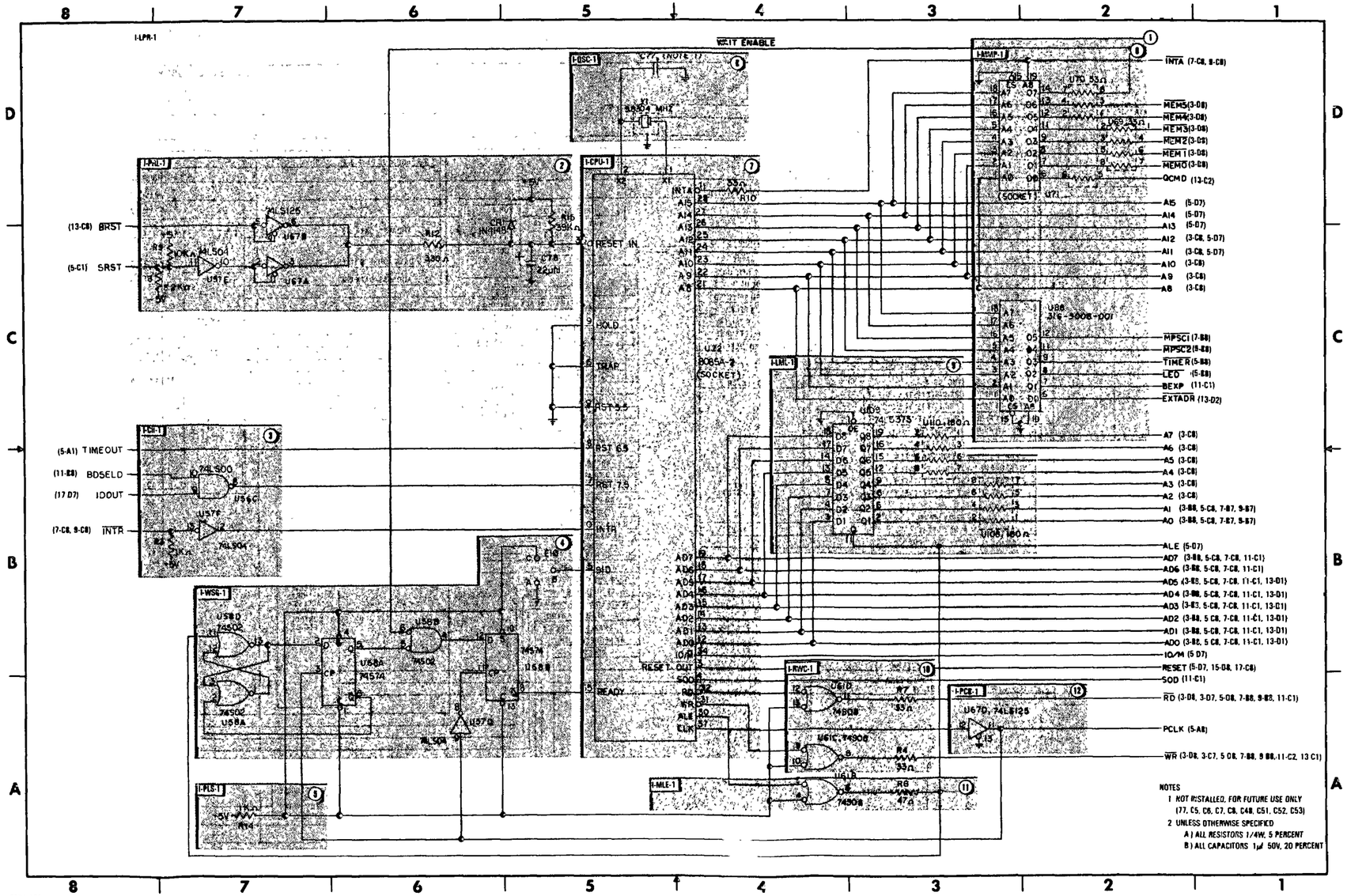


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 1 of 25)

(1) (I-LPR-1) LOCAL PROCESSOR:

INITIATES AND CONTROLS ALL DATA TRANSFERS BETWEEN MULTIPLEXER AND LSI 11/23 MICROCOMPUTER THROUGH DIRECT MEMORY ACCESS (DMA) TRANSFERS. CONTROLS ALL SERIAL CHANNEL OPERATION WITH EXTERNAL DEVICES THROUGH FOUR RS-449 SERIAL CHANNELS.

(2) (I-PRL-1) PROCESSOR RESET LOGIC:

CAUSES RESET CONDITION OF I-CPU-1, CAUSING I-CPU-1 TO BEGIN INSTRUCTION EXECUTION AT ADDRESS LOCATION ZERO WHEN (1) /BRST (BUS RESET) IS AT LOW LOGIC LEVEL, (2) SRST (SOFTWARE RESET) IS AT HIGH LOGIC LEVEL, OR (3) DC POWER IS INITIATED. CAPACITOR C8 PROVIDES CHARGE TIME DURING INITIAL DC POWER APPLICATION TO ALLOW I-CPU-1 TO ENTER RESET STATE. RESISTOR R12 LIMITS DISCHARGE CURRENT OF C8 TO PROTECT U67. RESISTORS R8 AND R9 FORM VOLTAGE DIVIDER WHICH MAINTAINS LOGIC LOW STATE AT INPUT OF U57E DURING TIME PRIOR TO SOFTWARE RESET (PARALLEL INPUT/OUTPUT IN OUTPUT MODE). INVERTER U57F AND THREE-STATE BUFFERS U67A AND B ESTABLISH CORRECT ACTIVE LOW LOGIC RESET IN SIGNALS TO I-CPU-1.

(3) (I-CII-1) CPU INTERRUPT INTERFACE:

ESTABLISHES RESTART INTERRUPTS AND INTERRUPT REQUEST SIGNAL TO I-CPU-1. U56C PROVIDES POSITIVE LOGIC LEVEL TO RESTART 7.5 INTERRUPT INPUT OF I-CPU-1 UNLESS BOTH BDSELD (BOARD SELECTED) AND IDOUT (INPUT-DATA OUT) SIGNALS ARE AT POSITIVE LOGIC LEVEL. INVERTER U57F PROVIDES POSITIVE LOGIC LEVEL TO THE INTERRUPT INPUT OF I-CPU-1. /INTR (/INTERRUPT) SIGNAL IS AT ACTIVE LOW LEVEL. RESISTOR R3 SERVES AS PULL UP RESISTOR TO KEEP INPUT TO U57F AT HIGH LEVEL UNTIL ACTIVATED WITH LOW LOGIC LEVEL.

(4) (I-WSG-1) WAIT STATE GENERATOR:

OUTPUTS READY SIGNAL TO I-CPU-1 TO ACKNOWLEDGE THAT BUS TRANSACTION IS COMPLETE AND EXECUTION OF THE INSTRUCTION SHOULD CONTINUE. U58D PIN 13 IS OUTPUT OF SET/RESET LATCH COMPOSED OF U58A AND D. THE SET/RESET LATCH IS SET BY ALE (ADDRESS LATCH ENABLE) SIGNAL FROM I-MLE-1, U61B PIN 6. WHEN SET/RESET LATCH IS SET, A LOW IS APPLIED TO U68A PIN 2 AND Q OUTPUT (U68A) GOES TO LOW LOGIC LEVEL. A WAIT/ENABLE SIGNAL IS GENERATED BY I-MCE-1, U71 PIN 14 IS APPLIED TO U58B PIN 6 IF WAIT STATE IS DESIRED. U58B PIN 4 GOES TO LOGIC LOW LEVEL, CAUSING U68B PIN 8 TO GO LOW, INHIBITING READY INPUT OF I-CPU-1. WHEN WAIT /ENABLE IS INACTIVE, OR AT LOGIC HIGH, READY SIGNAL TO I-CPU-1 IS ACTIVE. INVERTER U57 PROVIDES INVERTED PCLK (PROCESSOR CLOCK) SIGNAL TO CLOCK WAIT STATE.

(5) (I-PLS-1) POSITIVE LOGIC SUPPLY:

PROVIDES POSITIVE LOGIC LEVEL FOR USE BY I-WSG-1 AND I-RWC-1.

(6) (I-OSC-1) OSCILLATOR:

PROVIDES A 9.8304 MHZ SIGNAL FOR USE BY I-CPU-1. CAPACITOR C98 PROVIDES START-UP STABILITY.

(7) (I-CPU-1) CENTRAL PROCESSING UNIT:

PROVIDES 8-BIT PARALLEL PROCESSING. CONTROLS Q BUS CONTROLLER (QBC) VIA CONTROL PORTS. DIVIDES 9.8304 MHZ SIGNAL FROM I-OSC-1 BY TWO TO PROVIDE OPERATING FREQUENCY OF 4.9152 MHZ.

(8) (I-MMP-1) MEMORY MAPPING PROMS:

PROGRAMMABLE READ ONLY MEMORY WHICH ENABLES MULTIPLEXER MEMORY CHIPS. U71 DECODES ADDRESSES A8 - A15 FROM I-CPU-1 AND SELECTS A MEMORY DEVICE FROM I-UMY-1 WITH /MEM0 - /MEM5 (/MEMORY0 - /MEMORY5) OUTPUTS. QCMD (Q-BUS COMMAND) SIGNAL ENABLES I-QCP-1. U88 DECODES ADDRESSES A8 - A15 FROM I-CPU-1. /MPSC1 AND /MPSC2 (MULTI-PROTOCOL SERIAL CONTROLLER 1 AND 2) SIGNALS ENABLE I-MSC-1 AND I-MSC-2. /TIMER SIGNAL SELECTS I-CTR-1. /LED SIGNAL ENABLES ERROR CODE REGISTER (I-ECR-1) AND PRODUCES DIAGNOSTIC DISPLAY. BEXP (BUS EXCHANGE PORT) ENABLES I-BEP-1 WHEN /WR (/WRITE CONTROL) OR /RD (/READ CONTROL) IS ACTIVE LOW. /EXTADR (EXTENDED ADDRESS) ENABLES I-EAP-1 (EXTENDED ADDRESS PORT). RESISTOR NETWORKS U69 AND U70 MATCH THE OUTPUT IMPEDANCE OF U71 WITH LINE IMPEDANCE.

(9) (I-LML-1) LOWER BYTE MEMORY LATCH:

LATCHES LOWER 8-BITS OF MEMORY ADDRESS AND SENDS ADDRESS VIA LOCAL BUS TO DEVICE SELECTED BY I-MMP-1. RESISTOR NETWORKS U108 AND U110 MATCH OUTPUT IMPEDANCE OF U109 WITH LINE IMPEDANCE.

(10) (I-RWC-1) READ/WRITE CONTROL LOGIC:

INFORMS MEMORY OR I/O DEVICE THAT READ OR WRITE OPERATION IS DESIRED. U61D AND C ACT AS BUFFERS FOR /RD (/READ) AND /WR (/WRITE) SIGNALS. RESISTORS R7 AND R4 PROVIDE IMPEDANCE MATCHING.

(11) (I-MLE-1) MEMORY LATCH ENABLE:

ESTABLISHES ALE (ADDRESS LATCH ENABLE) SIGNAL FROM I-CPU-1 TO ENSURE MEMORY ADDRESS LATCHING OF I-LML-1 AND I-PIO-1. U61D BUFFERS ALE SIGNAL AND R6 PROVIDES IMPEDANCE MATCHING.

(12) (I-PCB-1) PROCESSOR CLOCK BUFFER:

U67 BUFFERS CLOCK SIGNAL FROM I-CPU-1 AND OUTPUTS PCLK (PROCESSOR CLOCK) SIGNAL. PCLK IS USED FOR TIMING BY VARIOUS FUNCTIONS ON MULTIPLEXER BOARD.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 2 of 25)

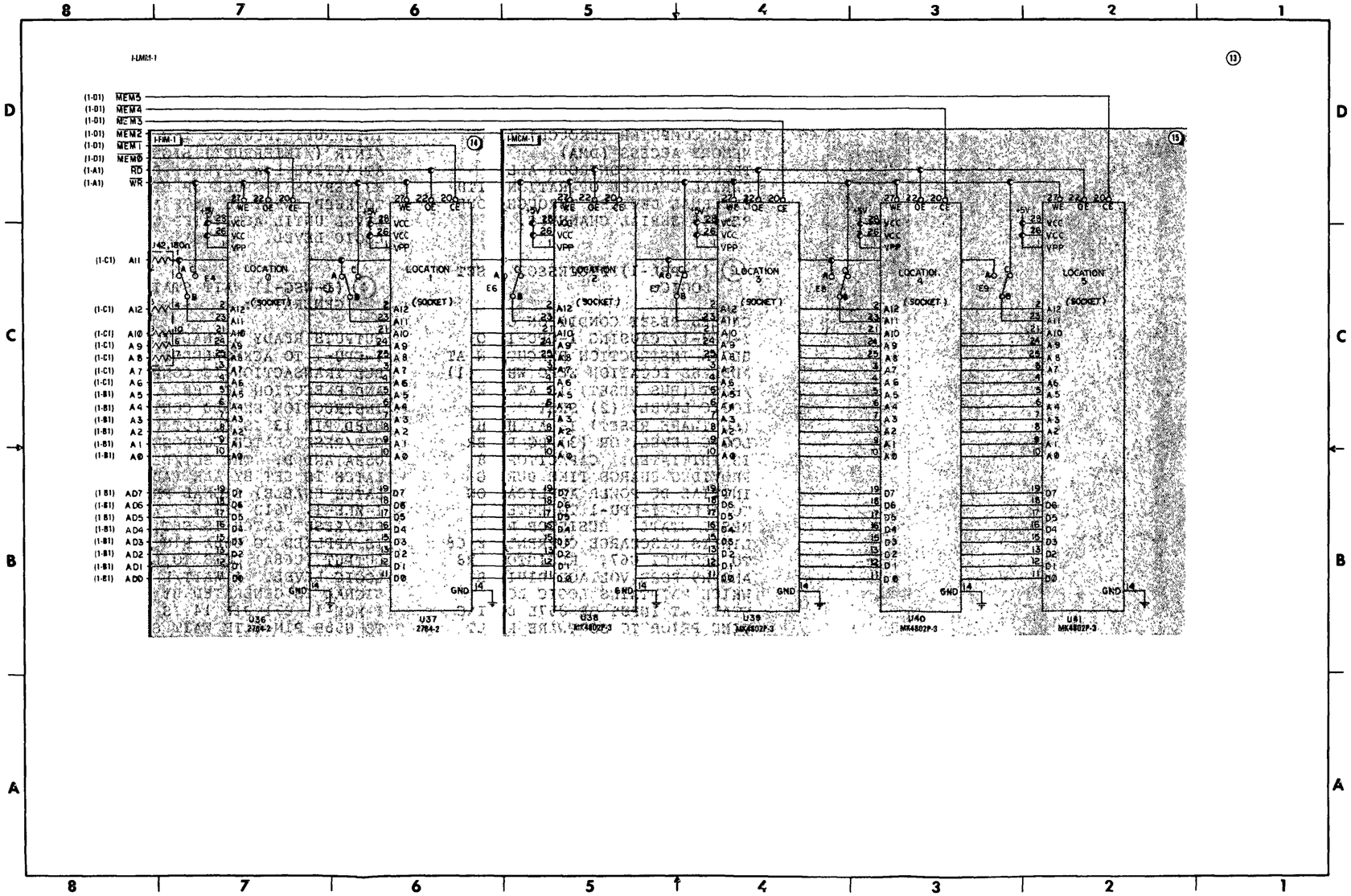


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 3 of 25)

(13) (I-LMM-1) LOCAL MICROCOMPUTER MEMORY:

CONTAINS TWO E-PROMS (I-FIM-1, U36, U37) AND FOUR 2K X 8 RAM DEVICES (I-MCM-1, U38 THROUGH U41) USED TO STORE FIRMWARE INSTRUCTIONS, MESSAGE DATA, AND CPU VARIABLES.

(14) (I-FIM-1) FIRMWARE INSTRUCTION MEMORY:

U36, U37 ARE 2764-2 E-PROMS USED TO STORE FIRMWARE INSTRUCTIONS USED BY I-CPU-1. /MEM0 OR /MEM1 SIGNALS FROM I-MMP-1, U71, SELECT EITHER U36 OR U37, RESPECTIVELY, FOR INSTRUCTION FETCHES. /RD SIGNAL FROM I-RWC-1 ENABLES EPROM TO OUTPUT DATA ONTO BUS WHEN PIN 20 IS AT ACTIVE LOW. STRAPPING OPTIONS E-4 AND E-5 ARE STRAPPED FROM A TO B TO ACCOMMODATE 2764-2 DEVICES USED IN THIS CONFIGURATION.

RESISTOR NETWORK U42 PROVIDES IMPEDENCE MATCHING TO MINIMIZE RINGING AND NEGATIVE UNDERSHOOT. U36 IS ADDRESSABLE FROM 0000H THROUGH 1FFFH. U37 IS ADDRESSABLE FROM 2000H THROUGH 3FFFH. INSTRUCTIONS ARE ADDRESSED ON INPUTS A0-A12 AND OUTPUT ON D0-D7.

(15) (I-MCM-1) MESSAGE DATA AND CPU VARIABLES MEMORY:

U38 THROUGH U41 ARE MK4802P-1, 2K X 8 RAM DEVICES USED TO STORE MESSAGE DATA AND CPU VARIABLES. /MEM2 THROUGH /MEM5 SIGNALS FROM I-MMP-1, U71, SELECT U38 THROUGH U41, RESPECTIVELY, AT PIN 20, CHIP ENABLE (CE). READ OR WRITE OPERATIONS ARE INDICATED BY THE STATES OF /RD OR /WR SIGNALS FROM I-REWC-1. STRAPPING OPTIONS E6 THROUGH E9 ARE STRAPPED FROM B TO C TO ACCOMMODATE MK4802P-1 DEVICES USED IN THIS CONFIGURATION. MEMORY ADDRESSING IS AS FOLLOWS:

DEVICE LOCATION	MEMORY ADDRESS
U38	4000-47FF
U39	4800-4FFF
U40	5000-57FF
U41	5800-5FFF

INPUT OF ADDRESSING IS VIA A0-A12 AND DATA I/O IS VIA D0-D7.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 4 of 25)

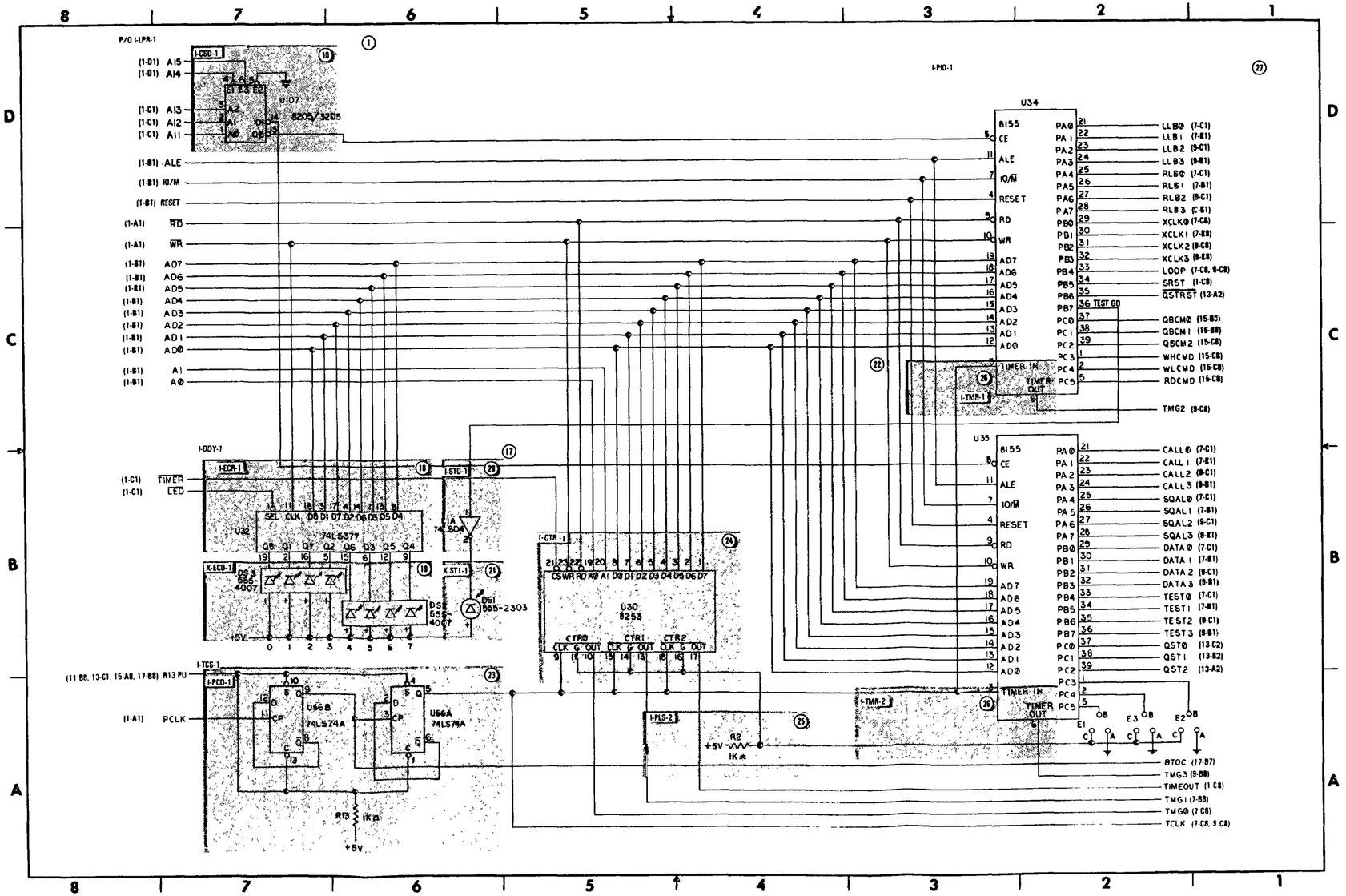


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 5 of 25)

(16) (I-CSD-1) CHIP SELECT DECODER (PART OF I-LPR-1):

U107 IS HIGH SPEED DECODER WHICH DECODES ADDRESS BITS A11 THROUGH A15 FROM I-CPU-1 TO ENABLE EITHER U34 OR U35 (PARALLEL INPUT/OUTPUT STACK RAMS).

(17) (I-DDY-1) DIAGNOSTIC DISPLAY:

I-DDY-1 CONSISTS OF ERROR CODE REGISTER (I-ECR-1, U32), ERROR CODE DISPLAY (X-ECD-1, DS2 & DS3), SELF TEST DRIVER (I-STD-1, U1) AND SELF-TEST INDICATOR (X-STI-1, DS1). I-DDY-1 INDICATES SUCCESSFUL EXECUTION OF POWER-ON SELF TEST, DISPLAYS ERROR CODES, AND PROVIDES INDICATION OF MUX CATASTROPHIC FAILURE.

(18) (I-ECR-1) ERROR CODE REGISTER:

REGISTER U32 STORES ERROR CODES FROM I-CPU-1, AND PROVIDES DRIVE FOR ILLUMINATING X-ECD-1 LEDS. U32 IS ENABLED BY /LED SIGNAL FROM I-MMP-1, AND RECEIVES ADDRESS/DATA BITS AD0-AD7 FROM I-CPU-1, INDICATING STATUS TO DISPLAY. /WR INPUT FROM I-MMP-1 WRITES DATA INTO U32. OUTPUTS Q1 - Q8 ARE APPLIED TO X-ECD-1.

(19) (X-ECD-1) ERROR CODE DISPLAY:

DS2 AND DS3 FORM COMBINED BANK OF EIGHT RED LEDS FOR DISPLAYING BINARY CODED ERROR INDICATIONS. ERROR CODES MAY BE FOUND BY REFERENCING TABLE 2-1. U32 OUTPUTS SIGNALS TO PROVIDE LOGIC ZERO (LOW) REQUIRED TO ILLUMINATE LED.

(20) (I-STD-1) SELF-TEST DRIVER:

U1 INVERTS PB7 OUTPUT FROM I-PIO-1, U34, AND PROVIDES DRIVE TO ILLUMINATE X-STI-1 (DS1). SIGNAL PB7 IS ENABLED AFTER SUCCESSFUL COMPLETION OF SELF-TEST, AND REMAINS ENABLED WHILE MUX IS OPERATING NORMALLY (I.E., NOT EXPERIENCING CATASTROPHIC FAILURE).

(21) (X-STI-1) SELF-TEST INDICATOR:

DS1 IS GREEN LED ILLUMINATED UPON SUCCESSFUL COMPLETION OF SELF TEST. DS1 MAY REMAIN ILLUMINATED WHILE ERROR CODES ARE DISPLAYED BY RED LEDS (DS2 AND DS3). I-STD-1 PROVIDES INPUT FOR DS1.

(22) (I-TCS-1) TIMER-COUNTERS:

I-TCS-1 CONSISTS OF PROCESSOR CLOCK DIVIDER (I-PCD-1), COUNTER (I-CTR-1), POSITIVE LOGIC SUPPLY (I-PLS-2), AND TWO TIMERS IN I-PIO-1, U34, U35 (I-TMR-1, I-TMR-2). I-TCS-1 GENERATES CLOCKS FOR FOUR SERIAL I/O CHANNELS AND ALSO SERVES AS PROCESSOR CONTROLLED VARIABLE LENGTH EVENT TIMER.

(23) (I-PCD-1) PROCESSOR CLOCK DIVIDER:

I-PCD-1 IS A FLIP-FLOP (U66A & B), CONFIGURED TO DIVIDE 4.9152 MHZ PCLK SIGNAL FROM I-CPU-1 BY FOUR TO PROVIDE 1.2288 MHZ CLOCK (U66A, PIN5) INPUT TO I-CTR-1, I-TMR-1 AND I-TMR-2. U66B, PIN 9 OUTPUT IS 2.4576 MHZ SIGNAL, BTOC, USED AS TIME-BASE INPUT TO BUS TIME-OUT LOGIC (I-BTL-1). RESISTOR R13 STRAPS THE CLEAR (C) AND SET (S) INPUTS TO U66TO LOGIC HIGH (1) AND PROVIDES SIGNAL R13 PU OUTPUT TO BOARD SELECT LOGIC (I-BSL-1), Q-BUS CONTROLLER CONTROL PORT (I-QCP-1), Q-BUS CONTROLLER PROCESSOR (I-QPR-1), DMA CONTROL LOGIC (I-DCL-1), BUS TIMEOUT LOGIC (I-BTL-1), AND INTERRUPT CONTROL LOGIC (I-ICL-1).

(24) (I-CTR-1) COUNTER:

U30 IS A PROGRAMMABLE INTERVAL TIMER WITH THREE INDEPENDENT 16-BIT COUNTERS, CAPABLE OF OPERATING IN DIFFERENT MODES TO GENERATE CLOCK SIGNALS FOR SERIAL I/O CHANNELS 0 AND 1 (I-SCR-1). U30 IS ENABLED BY /TIMER SIGNAL FROM I-MMP-1 APPLIED TO CHIP SELECT (CS) INPUT PIN 21. A0 AND A1 INPUTS FROM I-CPU-1 ADDRESS SPECIFIC U30 COUNTER (CTR0, CTR1 OR CTR2). SIGNAL /WR FROM I-CPU-1 PERMITS U30 TO WRITE MODE INFORMATION DATA OR TO LOAD COUNTERS FROM DATA AVAILABLE ON DATA LINES AD0-AD7. SIGNAL /RD FROM I-CPU-1 ALLOWS COUNTER VALUES FROM U30 TO BE READ FROM DATA LINES AD0-AD7 BY I-CPU-1. U30 COUNTERS ARE CLOCKED BY 1.2288 MHZ (TCLK) SIGNAL FROM I-TCS-1. CTR0 AND CTR1 OUTPUTS (TMG0, TMG1) ARE PROGRAMMABLE SQUARE WAVE SIGNALS AT VARYING FREQUENCIES, USED TO CLOCK SERIAL I/O CHANNELS 0 AND 1. CTR-2 OUTPUT (TIMEOUT) OPERATES AS ONE-SHOT TRIGGERED BY I-CPU-1, SET TO COUNT SPECIFIED NUMBER OF INPUT CLOCKS, EACH 814 NANOSECONDS IN LENGTH, VARYING IN NUMBER BETWEEN 1 AND 65,535, TO PROVIDE EVENT TIMING FROM 814 NANOSECONDS TO 53.3 MILLISECONDS. CTR-2 SETS TIMEOUT SIGNAL UPON COMPLETION OF PROGRAMMED COUNT, INTERRUPTING I-CPU-1, INDICATING EXPIRATION OF DELAY PERIOD.

(25) (I-PLS-2) POSITIVE LOGIC SUPPLY:

RESISTOR R2 STRAPS LOGIC ONE (HIGH) TO GATE (G) INPUTS OF U30 TO ENABLE COUNTING BY I-CTR-1.

(26) (I-TMR-1,2) TIMERS:

TCLK OUTPUT FROM I-TCS-1 IS APPLIED TO TIMER IN INPUTS TO I-PIO-1, U34 AND U35, PIN 3. U34, U35, PIN 6 OUTPUT TMG-2 AND TMG-3 ARE PROGRAMMABLE SQUARE WAVE VARIABLE FREQUENCY SIGNALS USED TO CLOCK SERIAL I/O CHANNELS 2 AND 3, RESPECTIVELY.

(27) (I-PIO-1) PARALLEL I/O LOGIC:

U34, U35 EACH CONTAIN 22 I/O LINES (PA0-PA7, PB0-PB7, PC0-PC5). U34 I/O LINES ARE OUTPUTS AND U35 I/O LINES ARE INPUTS. MAJORITY OF I/O SIGNALS PROVIDE INTERFACE TO RS-449 CONTROL LINES FOR THE FOUR SERIAL I/O CHANNELS. U34 OUTPUTS PC0-PC5 AND U35 INPUTS PC0-PC2 ARE CONTROL PORT I/O SIGNALS FOR QBC (I-QPR-1) INTERFACE. CHIP ENABLE (CE) SIGNALS FROM I-CSD-1 SELECT EITHER U34 OR U35. U34 AND U35 ARE MULTI-FUNCTION DEVICES EACH CONTAINING THREE I/O PORTS (PA, PB, PC), PROGRAMMABLE TIMER-COUNTERS (I-TMR-1,2) AND 256 BYTES OF RAM. SIGNALS ALE, /IO/M, RESET /RD, /WR, AD0 AND AD1 FROM I-LPR-1 ARE DECODED BY U34, U35 TO DETERMINE FUNCTION BEING ACCESSED. RAM IS AVAILABLE FOR GENERAL PURPOSE USE BY LSI-11 PROCESSOR, BUT USUALLY SERVES AS STACK (FIRST-IN, LAST OUT REGISTER) FOR THE I-CPU-1, WHICH CONTROLS ADDRESSING. XCLK OUTPUTS FROM U34 CONTROL ONBOARD OR EXTERNAL TIMING FOR FOUR SERIAL I/O CHANNELS. STRAPPING OPTIONS E1, 2 AND 3 ARE NOT USED IN THIS CONFIGURATION.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 6 of 25)

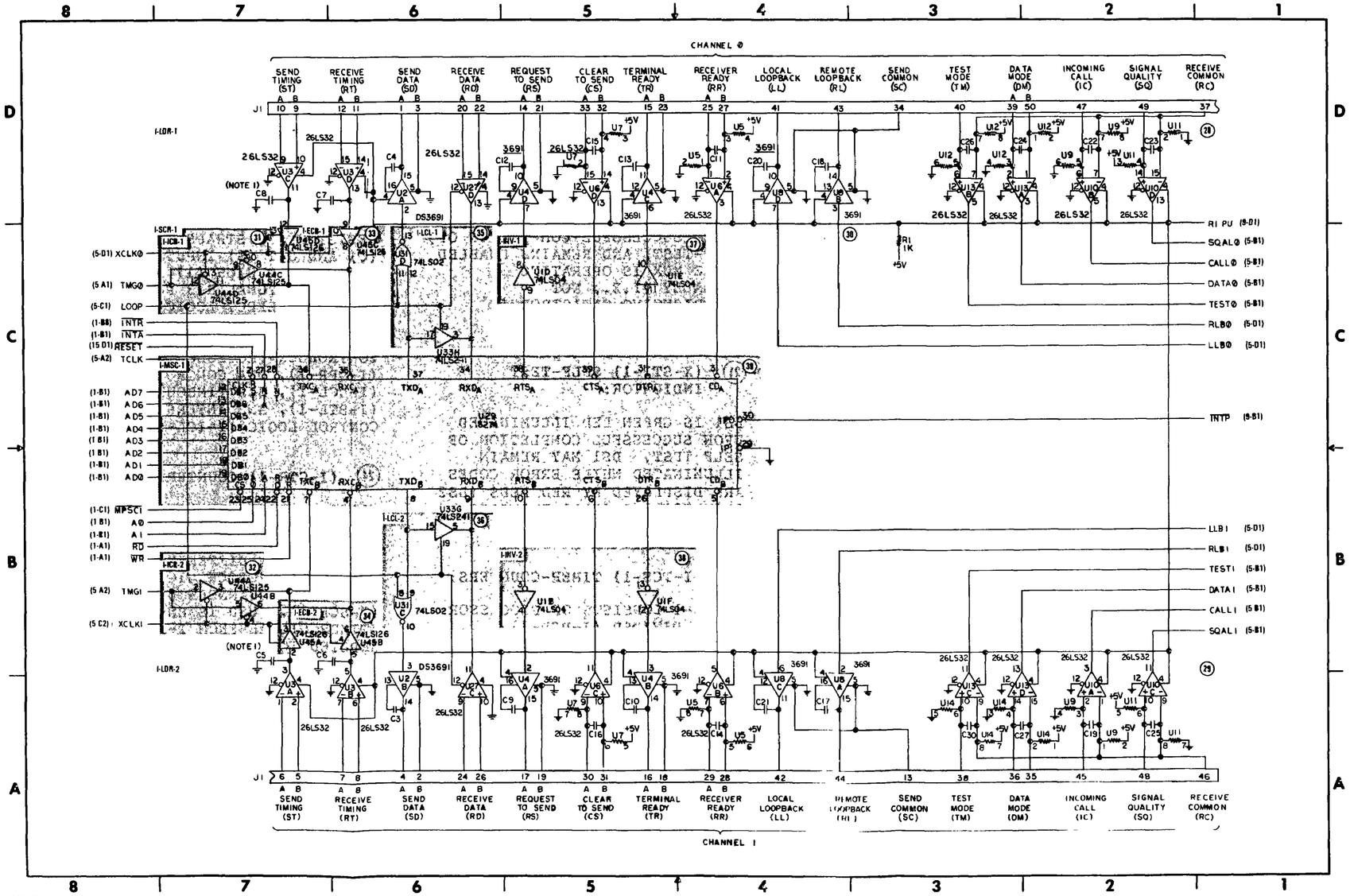


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 7 of 25)

(28) (I-LDR-1) LINE DRIVERS/RECEIVERS:

I-LDR-1 CONSISTS OF CHANNEL 0 I/O LINES AND LINE DRIVERS/RECEIVERS U2A; U3C,D: U4C,D; U6A,D; U8B,D; U10B,D; U13A,B AND U27D. LINE DRIVERS CONVERT TTL LEVEL SIGNALS TO RS423 LEVELS FOR OUTPUT TO EXTERNAL DEVICES. LINE RECEIVERS CONVERT RS423 LEVEL SIGNALS TO TTL LEVELS FOR INPUT TO I-SCR-1. A SIGNALS TO/FROM I-LDR-1 ARE NON-RETURN TO ZERO (NRZ) +5 VDC AND -5 VDC, TYPICALLY. B (TRANSMIT OR RECEIVE COMMON) SIGNALS TO/FROM I-LDR-1 ARE RETURNS, APPROXIMATELY 0 VDC. SIGNALS TO/FROM U8, U10, AND U13 ARE TEST SIGNALS USED TO CHECK LOCAL AND REMOTE LOOPBACK BETWEEN THE MUX AND EXTERNAL CHANNEL DEVICES. CAPACITORS C4, C12, C13, C18 AND C20 PROVIDE RISE TIME CONTROL FOR OUTPUT SIGNALS. CAPACITOR C15, RESISTOR U7, PINS 1, 2, 3 AND 4 FORM "FAIL-SAFE" INPUT NETWORK CAUSING OUTPUT OF U6D TO BE INACTIVE WHEN INPUT CABLE IS DISCONNECTED, ONE OF TWO INPUTS TO U6D (PINS 14 OR 15) ARE OPENED, OR WHEN POWER IS REMOVED FROM EQUIPMENT SUPPLYING INPUT SIGNAL. OTHER FAIL-SAFE NETWORKS INCLUDE:

RESISTOR/PINS	CAPACITOR
U5, 1 THROUGH 4	C11
U12, 5 THROUGH 8	C26
U12, 1 THROUGH 4	C24
U9, 5 THROUGH 8	C22
U11, 1 THROUGH 4	C23

RESISTOR R1 IS PULL-UP RESISTOR PROVIDING POSITIVE LOGIC INPUTS TO LINE DRIVERS/RECEIVERS.

(29) (I-LDR-2) LINE DRIVERS/RECEIVERS:

I-LDR-2 CAPACITOR AND COMPONENT PIN NUMBERS DIFFER FROM I-LDR-1, BUT I-LDR-1 AND I-LDR-2 ARE FUNCTIONALLY IDENTICAL. SEE 28 FOR FUNCTIONAL DESCRIPTION.

(30) (I-SCR-1) SERIAL INPUT/OUTPUT CONTROLLER:

I-SCR-1 CONSISTS OF TWO INTERNAL CLOCK BUFFERS (I-ICB-1,2), TWO EXTERNAL CLOCK BUFFERS (I-LCL-1,2), TWO INVERTER CIRCUITS (I-INV-1,2) AND MULTI-PROTOCOL SERIAL CONTROLLER (I-MSC-1). I-MSC-1 CONTAINS TWO FULL DUPLEX CHANNEL CONTROLLERS (EACH OPERATING INDEPENDENTLY), INTERRUPT CONTROLLER, SYNC AND CYCLIC REDUNDENCY (CRC) LOGIC. REGISTERS IN I-MSC-1 MAY BE CONFIGURED TO PERMIT SYNCHRONOUS, BYTE SYNCHRONOUS AND BIT SYNCHRONOUS MODES OF OPERATION. MOST REGISTERS ARE ACCESSIBLE ONLY DURING INITIALIZATION, AND ARE WRITTEN TO IN PREDEFINED ORDER. I-MSC-1 MAY BE CONFIGURED TO INTERFACE WITH LINE PRINTERS, WITH HDLC COMMUNICATION CHANNELS, OR OTHER COMMUNICATION PROTOCOLS, AS REQUIRED. DAISY-CHAIN INTERRUPT SCHEME IS USED BETWEEN I-MPS-1 AND I-MPS-2 TO PERMIT AUTOMATIC INTERRUPT PRIORITY RESOLUTION DURING THE INTERRUPT ACKNOWLEDGE CYCLE. CHANNELS 0 AND 1 HAVE PRIORITY OVER CHANNELS 2 AND 3. I-MPS-1 GENERATES INTERRUPTS TO I-CPU-1 TO INDICATE STATUS EVENTS, SUCH AS RECEIPT OF CRC ERRORS.

(31) (I-ICB-1) INTERNAL CLOCK BUFFER:

I-ICB-1 CONSISTS OF U44C AND D. SELECTION OF INTERNAL VERSUS EXTERNAL CLOCK IS CONTROLLED BY XCLK0 FROM I-PIO-1. XCLK0 LOW DISABLES EXTERNAL CLOCKS FROM U3C AND D PINS 11 AND 13, AND ENABLES U44. TMG0 IS PROGRAMMABLE INTERNAL TIMING CLOCK FROM I-CTR-1 INPUT VIA U44 TO THE TXC_A AND RXC_A (PINS 36,35) INPUTS OF I-MSC-1.

(32) (I-ICB-2) INTERNAL CLOCK BUFFER:

I-ICB-2 IS FUNCTIONALLY IDENTICAL TO I-ICB-1. I-ICB-2 CONTROLS INTERNAL TIMING FOR CHANNEL 1, CONSISTS OF U44A AND B AND HAS XCLK1 AND TMG1 INPUTS CORRESPONDING TO XCLK0 AND TMG0 SIGNALS THAT PERTAIN TO CHANNEL 0 OPERATION.

(33) (I-ECB-1) EXTERNAL CLOCK BUFFER:

I-ECB-1 CONSISTS OF U45C AND D. XCLK0 FROM I-P10-1, WHEN HIGH, ENABLES U45, AND PERMITS EXTERNAL TIMING INPUTS FROM U3C AND D TO BE APPLIED TO I-MSC-1, U29, PINS 35 AND 36.

(34) (I-ECB-2) EXTERNAL CLOCK BUFFER:

I-ECB-2 IS FUNCTIONALLY IDENTICAL TO I-ECB-1. I-ECB-2 CONSISTS OF U45A AND B AND IS ENABLED BY XCLK1.

(35) (I-LCL-1) LOOPBACK CONTROL LOGIC:

I-LCL-1 CONSISTS OF U31D AND U33 H. WHEN THE LOOP SIGNAL IS HIGH, U33H IS ENABLED, U27 D IS DISABLED, AND TXD_A (U29, PIN 37) WILL BE LOOPED BACK TO RXD_A (U29, PIN 34). WHEN LOOP IS LOW, U33H IS DISABLED, U31D IS ENABLED, AND TXD_A IS OUTPUT TO I-LDR-1.

(36) (I-LCL-2) LOOPBACK CONTROL LOGIC:

I-LCL-2 CONSISTS OF U31C AND U33G. I-LCL-2 IS FUNCTIONALLY IDENTICAL TO I-LCL-1.

(37) (I-INV-1) INVERTER:

I-INV-1 CONSISTS OF U1D AND E. I-INV-1 INVERTS ACTIVE (LOW LEVEL) RTS_A (REQUEST TO SEND) AND DTR_A (DATA TERMINAL READY) SIGNALS FROM I-MSC-1 TO ON CONDITION (+5 VDC) FOR OUTPUT TO I-LDR-1.

(38) (I-INV-2) INVERTER:

I-INV-2 CONSISTS OF U1B AND F AND IS FUNCTIONALLY IDENTICAL TO I-INV-1 RELATIVE TO CHANNEL 1 OPERATION.

(39) (I-MSC-1) MULTI-PROTOCOL/ SERIAL CONTROLLER:

I-MSC-1 CONSISTS OF U29, MULTI-PROTOCOL SERIAL CONTROLLER WITH TWO SERIAL I/O CHANNELS, 0 AND 1. I-MSC-1 APPEARS AS SERIES OF PORTS TO I-CPU-1. INTERNAL (LOCAL BUS) SIGNALS INCLUDE ADDRESS/DATA BITS AD0-AD7 TO/FROM BI-DIRECTIONAL THREE STATE LINES DB0-DB7.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 8 of 25)

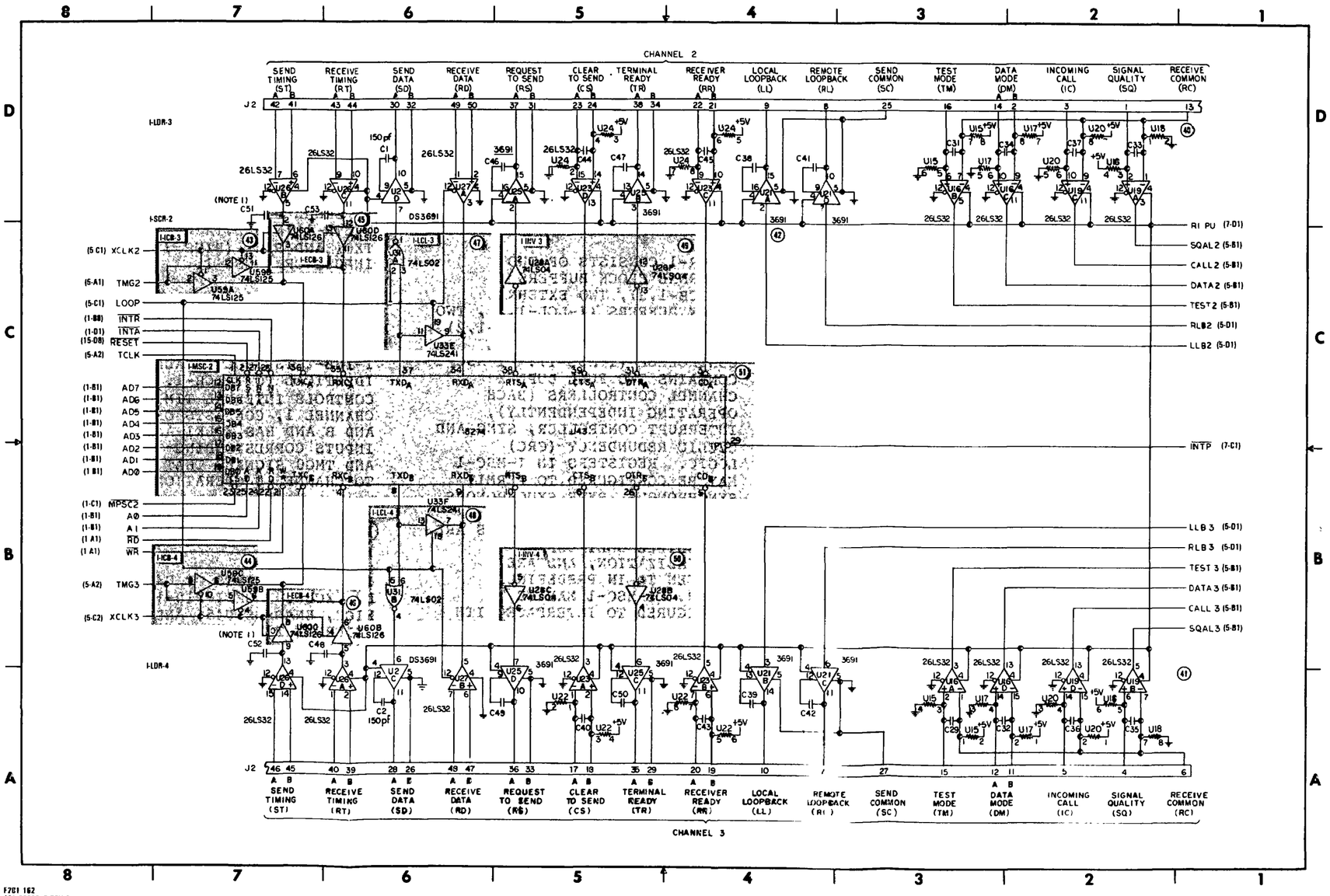


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 9 of 25)

(40) (I-LDR-3) LINE DRIVERS/RECEIVERS:

I-LDR-3 CONSISTS OF CHANNEL 2 I/O LINES AND LINE DRIVERS/RECEIVERS U2D; U16B,C; U19A,C; U21A,D; U23C,D; U25A,B; U26B,C; AND U27A. LINE DRIVERS CONVERT TTL LEVEL SIGNALS TO RS423 LEVELS FOR OUTPUT TO EXTERNAL DEVICES. LINE RECEIVERS CONVERT RS423 LEVEL SIGNALS TO TTL LEVELS FOR INPUT TO I-SCR-2. A SIGNALS TO/FROM I-LDR-3 ARE NON-RETURN TO ZERO (NRZ) +5 VDC AND -5 VDC, TYPICALLY. B (TRANSMIT OR RECEIVE COMMON) SIGNALS TO/FROM I-LDR-1 ARE RETURNS, APPROXIMATELY 0 VDC. SIGNALS TO/FROM U16, U19 AND U20 ARE TEST SIGNALS USED TO CHECK LOCAL AND REMOTE LOOPBACK BETWEEN MUX AND EXTERNAL CHANNEL DEVICES. CAPACITORS C1, C46, C47, C38 AND C41 PROVIDE RISE TIME CONTROL FOR OUTPUT SIGNALS. CAPACITORS C51 AND C53 ARE FOR NOISE REMOVAL. CAPACITOR C44, RESISTOR U24, PINS 1 AND 2, AND RESISTOR U24, PINS 3 AND 4 FORM A FAIL-SAFE INPUT NETWORK CAUSING THE OUTPUT OF U23D PIN 13 TO BE INACTIVE WHEN INPUT CABLE IS DISCONNECTED, ONE OF TWO INPUTS TO U23 (PINS 14 OR 15) ARE OPENED, OR WHEN POWER IS REMOVED FROM EQUIPMENT SUPPLYING INPUT SIGNAL. OTHER FAIL-SAFE NETWORKS INCLUDE:

RESISTOR/PINS	CAPACITOR
U5, 1 THROUGH 4	C11
U12, 5 THROUGH 8	C26
U12, 1 THROUGH 4	C24
U9, 5 THROUGH 8	C22
U11, 1 THROUGH 4	C23

RESISTOR R1 IS A PULL-UP REGISTOR PROVIDING POSITIVE LOGIC INPUTS TO LINE DRIVERS/RECEIVERS.

(41) (I-LDR-4) LINE DRIVERS/RECEIVERS:

I-LDR-4 CAPACITOR AND COMPONENT PIN NUMBERS DIFFER FROM I-LDR-3, BUT I-LDR-3 AND I-LDR-4 ARE FUNCTIONALLY IDENTICAL. SEE 40 FOR FUNCTIONAL DESCRIPTION.

(42) (I-SCR-2) SERIAL INPUT/OUTPUT CONTROLLER:

I-SCR-2 CONSISTS OF TWO INTERNAL CLOCK BUFFERS (I-ICB-3,4), TWO EXTERNAL CLOCK BUFFERS (I-ECB-3,4), TWO INVERTER CIRCUITS (I-INV-3,4) AND MULTIPROTOCOL SERIAL CONTROLLER (I-MSC-2). I-MSC-2 CONTAINS TWO FULL DUPLEX CHANNEL CONTROLLERS (EACH OPERATING INDEPENDENTLY), INTERRUPT CONTROLLER, SYNC AND CYCLIC REDUNDANCY (CRC) LOGIC. REGISTERS IN I-MSC-2 MAY BE CONFIGURED TO OPERATE ASYNCHRONOUS, BYTE SYNCHRONOUS AND BIT SYNCHRONOUS MODES OF OPERATION. MOST REGISTERS ARE ACCESSIBLE ONLY DURING INITIALIZATION, AND ARE WRITTEN TO IN PRE-DEFINED ORDER. I-MSC-2 MAY BE CONFIGURED TO INTERFACE WITH LINE PRINTERS, WITH HDLC COMMUNICATION CHANNELS, OR OTHER COMMUNICATION PROTOCOLS, AS REQUIRED. DAISY-CHAIN INTERRUPT SCHEME IS USED BETWEEN I-MPS-1 AND I-MPS-2 TO PERMIT AUTOMATIC INTERRUPT PRIORITY RESOLUTION DURING INTERRUPT ACKNOWLEDGE CYCLE. CHANNELS 0 AND 1 HAVE PRIORITY OVER CHANNELS 2 AND 3. I-MPS-2 GENERATES INTERRUPTS TO I-CPV-1 TO INDICATE STATUS EVENTS, SUCH AS RECEIPT OF CRC ERRORS.

(43) (I-ICB-3) INTERNAL CLOCK BUFFER:

I-ICB-3 CONSISTS OF U59A AND D. SELECTION OF INTERNAL VERSUS EXTERNAL CLOCK IS CONTROLLED BY THE XCLK 2 SIGNAL FROM I-PIO-1. XCLK LOW DISABLES EXTERNAL CLOCKS FROM U26B AND C PINS 5 AND 11, AND ENABLES U59. TMG2 IS PROGRAMMABLE INTERNAL TIMING CLOCK FROM I-CTR-1 INPUT VIA U59 TO THE TXC_A AND RXC_A (PINS 36, 35) INPUTS OF I-MSC-2.

(44) (I-ICB-4) INTERNAL CLOCK BUFFER:

I-ICB-4 IS FUNCTIONALLY IDENTICAL TO I-ICB-3. I-ICB-4 CONTROLS INTERNAL TIMING FOR CHANNEL 3, CONSISTS OF U59B AND C, AND HAS XCLK3 AND TMG3 INPUTS CORRESPONDING TO XCLK2 AND TMG2 SIGNALS THAT PERTAIN TO CHANNEL 2 OPERATION.

(45) (I-ECB-3) EXTERNAL CLOCK BUFFER:

I-ECB-3 CONSISTS OF U60A AND D. XCLK 2 FROM I-P10-1, WHEN HIGH ENABLES U60, AND PERMITS EXTERNAL TIMING INPUTS FROM U26B AND C TO BE APPLIED TO I-MSC-2, U43, PINS 35 and 36.

(46) (I-ECB-4) EXTERNAL CLOCK BUFFER:

I-ECB-4 IS FUNCTIONALLY IDENTICAL TO I-ECB-3. I-ECB-4 CONSISTS OF U60B AND C, AND IS ENABLED BY XCLK3.

(47) (I-LCL-3) LOOPBACK CONTROL LOGIC:

I-LCL-3 CONSISTS OF U31A AND U33E. WHEN LOOP SIGNAL IS HIGH, U33E IS ENABLED, U27 IS DISABLED, AND TXD_A (U43, PIN 37) WILL BE LOOPED BACK TO RXD_A (U43, PIN 34). WHEN LOOP IS LOW, U33E IS DISABLED, U31 IS ENABLED, AND TXD_A IS OUTPUT TO I-LDR-3.

(48) (I-LCL-4) LOOPBACK CONTROL LOGIC:

I-LCL-4 CONSISTS OF U31B AND U33F. I-LCL-4 IS FUNCTIONALLY IDENTICAL TO I-LCL-3.

(49) (I-INV-3) INVERTER:

I-INV-3 CONSISTS OF U28A AND F I-INV-3 INVERTS ACTIVE (LOW LEVEL) RTS_A (REQUEST TO SEND) AND DRT_A (DATA TERMINAL READY) SIGNALS FROM I-MSC-2 TO ON CONDITION (+5VDC) FOR OUTPUT TO I-LDR-3.

(50) (I-INV-4) INVERTER:
I-INV-4 CONSISTS OF U28B AND C AND IS FUNCTIONALLY IDENTICAL TO I-INV-3 RELATIVE TO CHANNEL 2 OPERATION.

(51) (I-MSC-2) MULTI-PROTOCOL SERIAL CONTROLLER:

I-MSC-2 CONSISTS OF U43, A MULTI-PROTOCOL SERIAL CONTROLLER WITH TWO SERIAL I/O CHANNELS, 2 AND 3. I-MSC-2 APPEARS AS SERIES OF PORTS TO I-CPU-1. INTERNAL (LOCAL BUS) SIGNALS INCLUDE ADDRESS/DATA BITS AD0-AD7 TO/FROM BI-DIRECTIONAL THREE STATE LINES DB0-DB7.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 10 of 25)

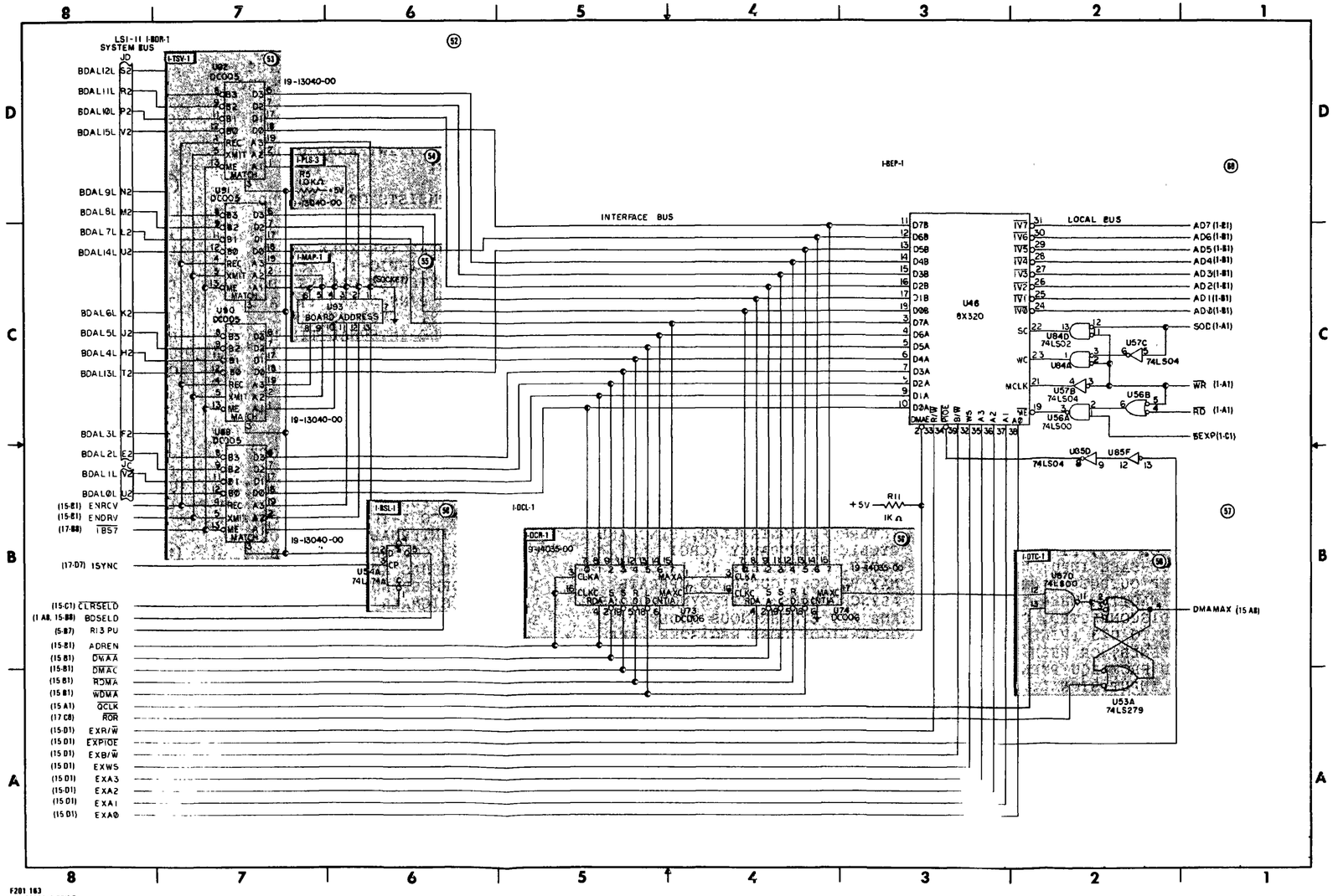


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 11 of 25)

(52) (I-BDR-1) BUS DRIVERS/RECEIVERS:

I-BDR-1 CONSISTS OF TRANSCEIVERS U89 THRU U92 (I-TSV-1), POSITIVE LOGIC SUPPLY (I-PLS-3), MULTIPLEXER ADDRESS PLUG (I-MAP-1) AND BOARD SELECT LOGIC (I-BSL-1). I-BDR-1 PROVIDES ELECTRICAL INTERFACE BETWEEN LSI-11 BUS AND MUX LOGIC, AND BUFFERS BUS SIGNALS TO MEET BUS LOADING SPECIFICATIONS. I-BDR-1 ALSO PROVIDES MUX BOARD ADDRESSING (SELECT) LOGIC.

(53) (I-TSV-1) TRANSCEIVERS:

I-TSV-1 CONSISTS OF FOUR DC005 ICS (U89 THROUGH U92). SYSTEM BUS SIDE CONSISTS OF B0-B3 INPUT/OUTPUT LINES AND INTERFACE BUS SIDE CONSISTS OF D0-D3 INPUT/OUTPUT LINES. ENDRV (ENABLE DRIVER FROM QBC PROCESSOR) SET HIGH ENABLES DATA FROM INTERFACE BUS TO SYSTEM BUS. ENRCV (ENABLE RECEIVE FROM QBC PROCESSOR) SET HIGH ENABLES DATA FROM SYSTEM BUS TO INTERFACE BUS. ENDRV, ENRCV LOW DISABLES DRIVERS. DC005 INTERNAL CIRCUITRY COMPARES B1-B3 INPUTS WITH A1-A3 INPUTS FROM I-MAP-1 FOR MATCH. WHEN MATCH WITH ALL FOUR TRANCEIVERS OCCURS, I-PLS-3 AND I-BSL-1 INTERACT TO INDICATE THAT MUX BOARD (AND CSR) IS SELECTED. MATCH OUTPUT FROM U89-U92 IS ENABLED WHEN B1-B3 COMPARE WITH A1-A3 AND ME (MATCH ENABLE) IS LOW. ME IS CONTROLLED BY IBS7 SIGNAL, ACTIVE WHEN LSI-11 IS BUS MASTER. ADDRESS IS PLACED ON BUS AND BBS7L IS SET ACTIVE, FOLLOWED BY BSYNCL (SEE I-BDR-3) CAUSING ISYNC TO GO ACTIVE.

(54) (I-PLS-3) POSITIVE LOGIC SUPPLY:

I-PLS-3 CONSISTS OF RESISTOR R5 CONNECTED TO MATCH OUTPUTS OF U89 THRU U92 AND TO D INPUT OF FLIP-FLOP U54A (I-BSL-1). WHEN I-TSV-1 MATCH OCCURS, RESISTOR R5 PULLS THE D INPUT TO U54A HIGH.

(55) (I-MAP-1) MULTIPLEXER ADDRESS PLUG:

I-MAP-1 CONSISTS OF U93, HARD-WIRED OPTION PLUG WHICH GROUNDS A INPUTS TO I-TSV-1 FOR LOGICAL ONE (1) AND PROVIDES OPEN WHEN COMPARISON WITH ZERO IS REQUIRED. OPTIONS USED IN THIS CONFIGURATION ARE OPTION 1 (ONE MUX BOARD USED) WITH PINS 1,2,3,5,6 AND 7 GROUNDED AND OPTION 2, (2 MUX BOARDS USED) WITH PINS 1,2,3,5,6,7 AND 13 GROUNDED.

(56) (I-BSL-1) BOARD SELECT LOGIC:

CONSISTS OF FLIP-FLOP U54A. ISYNC, ACTIVE WHEN LSI-11 IS ADDRESSING I/O PAGE OF MEMORY, CLOCKS MATCH STATE OF U89-U92 INTO U54A, CAUSING BDSELD (BOARD SELECTED) TO GO HIGH WHEN ADDRESS SPECIFIED BY I-MAP-1 (U93) IS DETECTED. BDSLED IS OUTPUT TO QBC STATUS MULTIPLEXER (I-SMX-1) AND TO I-CPU-1. AFTER BDSELD IS DETECTED, QBC PROCESSOR SETS CLRSELD (CLEAR SELECTED), RESETTING U54A IN PREPARATION FOR NEXT CSR ADDRESS. SIGNAL R13 PU APPLIES CONSTANT POSITIVE LOGIC INPUT TO SET SIDE OF FLIP-FLOP U54A.

(57) (I-DCL-1) DMA CONTROL LOGIC:

I-DCL-1 CONSISTS OF DMA CONTROL REGISTERS (I-DCR-1) AND DMA COMPLETE LOGIC (I-DTC-1). DMA LOGIC CAN PERFORM FOUR TYPES OF TRANSFERS, INCLUDING READ FROM DATA MEMORY, WRITE TO DATA MEMORY, READ FROM I/O PAGE OF MEMORY, OR WRITE TO I/O PAGE OF MEMORY.

(58) (I-DCR-1) DMA CONTROL REGISTERS:

I-DCR-1 CONSISTS OF REGISTERS U73 AND U74. TWO 8-BIT DC006 ICS ARE CONNECTED TO FORM TWO 16-BIT REGISTERS. ONE REGISTER IS USED TO COUNT NUMBER OF WORDS TRANSFERRED AND ONE TO CONTAIN THE LSI-II MEMORY ADDRESS FOR CURRENT DMA TRANSACTION. ADDRESS/DATA LINES TO/FROM INTERFACE BUS ARE ON PINS 7 THRU 15, EXCLUDING PIN 10. REMAINING PINS ARE CONTROL LINES.

MAXA/MAXC OUTPUTS FROM U73 TO U74 PROVIDE CLOCKS TO U74 WHEN CONTENTS OF RESPECTIVE REGISTER REACHES MAXIMUM COUNT OF 255. MAXC OUTPUT FROM U74 IS ACTIVE WHEN DMA COUNT REGISTERS IN BOTH U73 AND U74 REACH MAXIMUM (65,536). All PROGRAMMED READ/WRITE OPERATIONS ARE BETWEEN I-DCR-1 AND I-BEP-1. DATA CANNOT BE MOVED BETWEEN I-DCR-1 AND SYSTEM BUS UNDER CONTROL OF BUS MASTER.

(59) (I-DTC-1) DMA COMPLETE LOGIC:

I-DTC-1 CONSISTS OF GATE U87D AND LATCH U53A. ACTIVE MAXC OUTPUT FROM U74 AND /QCLK ARE APPLIED TO U87D, PINS 12 AND 13, RESPECTIVELY. U87D ENSURES THAT U53A IS NOT SET TO ACTIVE STATE BY DECODE GLITCHES POSSIBLY PRESENT ON MAXC OUTPUT OF U74 DURING COUNTER TRANSITIONS. DMAMAX OUTPUT OF LATCH U53A IS ACTIVE WHEN DMA TRANSACTION IS COMPLETE. WHEN DMAMAX IS DETECTED BY QBC PROCESSOR, QBC PROCESSOR SETS RELEASE SIGNAL, WHICH COMBINES WITH RESET (NOT SHOWN ON THIS SHEET) TO PROVIDE /ROR INPUT TO PIN 1 OF U53A. /ROR ACTIVE CAUSES LATCH U53A TO RESET TO QUIESCENT STATE UNTIL MAXC FROM U74 IS AGAIN DETECTED.

(60) (I-BEP-1) BUS EXCHANGE PORT:

I-BEP-1 CONSISTS OF U46 (AN 8X320 DUAL PORT 16-BYTE REGISTER ARRAY), GATES U84A AND D, U56A AND B, AND INVERTERS U57B AND C, U85F AND D. THE PRIMARY PORT OF U46 SERVES INTERFACE BUS AND CONSISTS OF I/O LINES D0A-D7A AND D0B-D7B. SECONDARY PORT SERVES LOCAL BUS AND CONSISTS OF I/O LINES IV0-IV7. SIMULTANEOUS ACCESS TO PRIMARY AND SECONDARY PORTS IS POSSIBLE, EXCEPT FOR WRITE TO SAME REGISTER. GATE U84D ENABLES SC WHEN SOD IS LOW AND /WR IS APPLIED. GATE U84A ENABLES WC WHEN SOD IS HIGH AND /WR IS APPLIED. /WR IS INVERTED BY U57B TO ENABLE MCLK. U56B AND U56A COMBINE TO ENABLE /ME WHEN BEXP AND /RD OR /WR ARE ACTIVE. U85D AND F PROVIDE SLIGHT DELAY IN /PIOE SIGNAL TO ELIMINATE BUS CONTENTION.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 12 of 25)

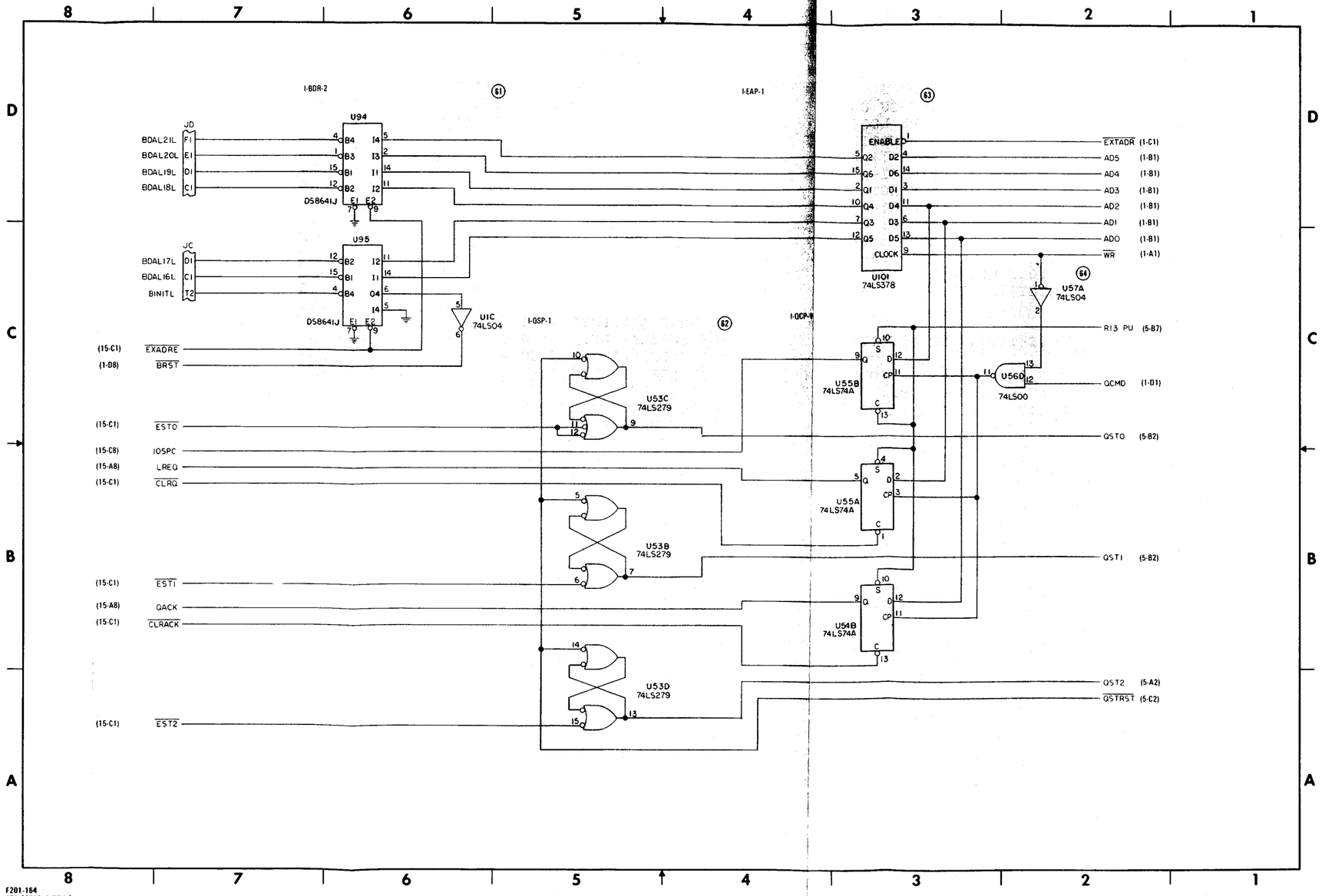


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 13 of 25)

(61) (I-BDR-2) BUS DRIVERS/RECEIVERS:

I-BDR-2 CONSISTS OF EXTENDED ADDRESS LINE DRIVERS U94, U95 AND INVERTER U1C. U94 AND U95 INVERTER INPUTS ARE EXTENDED ADDRESS LINES CONTAINING UPPER SIX BITS OF LSI-11 ADDRESS. INPUTS ARE FROM I-CPU-12 VIA I-EAP-1. OUTPUTS FROM U94, U95 TO THE SYSTEM BUS ARE ADDRESS SIGNALS BDAL16L THRU BDAL21L. U94 AND U95 ARE ENABLED BY SIGNAL /EXADRE (EXTENDED ADDRESS ENABLE). SIGNAL BINTL (BUS INITIALIZE) THE LSI-11 TO U95 SETS THE /BRST OUTPUT VIA U1C INVERTER TO I-CPU-1.

(62) (I-QSP-1) Q-BUS CONTROLLER STATUS PORT:

I-QSP-1 CONSISTS OF LATCHES U53B, C AND D WHICH REFLECT THE OUTCOME OF PARTICULAR OPERATION. SIGNAL /QSTRST IS RESET SIGNAL TO THREE LATCHES, ASSERTED WHEN I-CPU-1 READS NON-ZERO STATUS (QST0, QST1, QST2) SECOND TIME, INDICATING COMPLETION OF OPERATION. EST0, EST1 AND EST2 ARE LATCH INPUTS FROM I-OSR-1. LOW ON ANY EST INPUT WILL SET RESPECTIVE LATCH OUTPUT (QST0, QST1, QST2) HIGH.

(63) (I-EAP-1) EXTENDED ADDRESS PORT:

I-EAP-1 CONSISTS OF 8-BIT HIGH SPEED PARALLEL EXTENDED ADDRESS REGISTER U101. ADDRESS/DATA LINES AD0-AD5 ARE INPUT TO U101 FROM I-CPU-1. SIGNAL /WR PROVIDES CLOCK INPUT AND /EXTAPR ENABLES REGISTER. Q1-Q6 ARE OUTPUT LINES TO LSI-11 VIA I-BDR-2. ADDRESS DATA LINES AD0-AD2 ARE ALSO APPLIED TO I-QCP-1, ALONG WITH SIGNAL /WR.

(64) (I-QCP-1) Q-BUS CONTROLLER COMMAND PORT:

I-QCP-1 CONSISTS OF FLIP-FLOPS U54B AND U55A, B, AND GATES U56D AND U57A. SIGNAL /WR FROM I-CPU-1 IS INVERTED BY U57A AND APPLIED TO PIN 13 OF GATE U56D. SIGNAL QCMD ENABLES CLOCK INPUT TO FLIP-FLOPS. R13PU PROVIDES POSITIVE LOGIC INPUT TO SET AND CLEAR INPUTS TO U55B, AND TO SET INPUTS TO U55A AND U54B. AD0 THRU AD2 ARE D INPUTS TO U54B, U55A AND U55B, RESPECTIVELY. Q OUTPUT OF U54B (QACK) INDICATES THAT THE QBC PROCESSOR MAY TRANSFER THE NEXT FOUR DATA WORDS TO/FROM LSI-11 MEMORY. WHEN QACK IS SAMPLED, QBC PROCESSOR ASSERTS CLRACK, WHICH IS APPLIED TO CLEAR INPUT OF U54B, RESETTING FLIP-FLOP. Q OUTPUT OF U55A (LREQ) IS OUTPUT TO QBC PROCESSOR. WHEN LREQ IS SAMPLED, QBC PROCESSOR BEGINS SAMPLING OTHER CONTROL SIGNALS TO DETERMINE PROCESS REQUIRED. QBC PROCESSOR SETS /CLRQ, WHICH IS APPLIED TO CLEAR INPUT TO U55A, RESETTING FLIP-FLOP IN PREPARATION FOR NEXT REQUEST. IOSPC (I/O SPACE) OUTPUT FROM U55B TO QBC PROCESSOR INDICATES LSI-11 BUS TRANSACTION IN PROGRESS IS IN I/O PAGE MEMORY. IOSPC IS NOT RESET AFTER BEING SAMPLED.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 14 of 25)

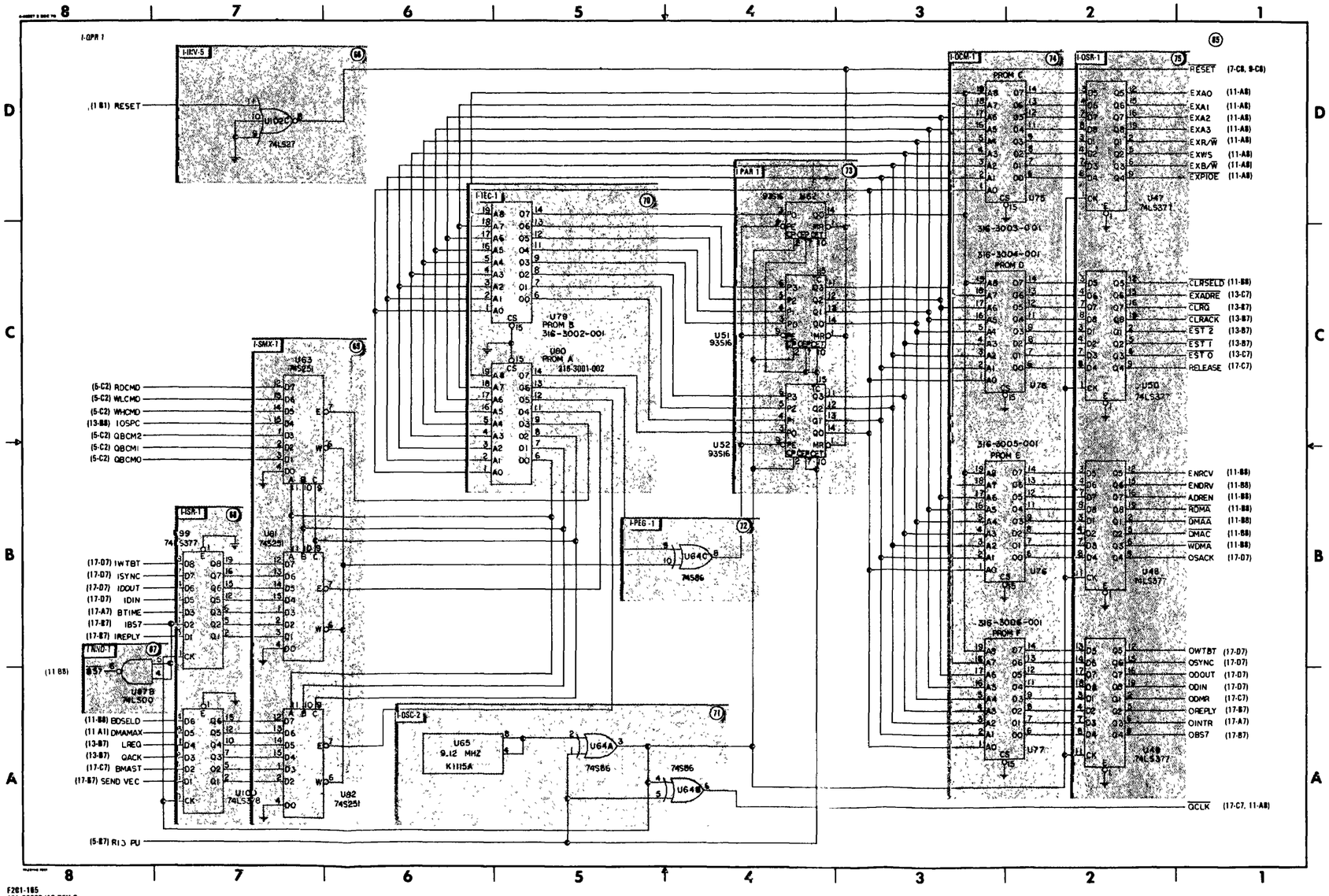


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 15 of 25)

(65) (I-QPR-1) Q-BUS CONTROLLER PROCESSOR:

I-QPR-1 CONSISTS OF THE FOLLOWING:

I-INV-5	INVERTER
I-NND-1	NAND GATE
I-ISR-1	INPUT STABILITY REGISTER
I-SMX-1	STATUS MULTIPLEXERS
I-IEC-1	INSTRUCTION EXECUTION CONTROL
I-OSC-2	OSCILLATOR
I-PEG-1	PROCESSOR ADDRESS REGISTER ENABLE GATE
I-PAR-1	PROCESSOR ADDRESS REGISTER
I-OCM-1	OUTPUT CONTROL MEMORY
I-OSR-1	OUTPUT STABILITY REGISTER

I-QPR-1 CONTROLS ALL QBC FUNCTIONS THROUGH PROM PROGRAM EXECUTION.

(66) (I-INV-5) INVERTER:

I-INV-5 CONSISTS OF U102C WHICH INVERTS RESET FOR APPLICATION TO I-PAR-1, I-MSC-1 AND I-MSC-2. QBC STARTS EXECUTING INSTRUCTIONS AT PROM ADDRESS ZERO (0) EACH TIME I-CPU-1 IS RESET.

(67) (I-NND-1) NAND GATE:

I-NND-1 CONSISTS OF U87B, CONFIGURED AS INVERTER, USED TO INVERT IBS7 (MASTER ENABLE SIGNAL FOR I-TSV-1).

(68) (I-ISR-1) INPUT STABILITY REGISTERS:

I-ISR-1 CONSISTS OF U99 AND U100, USED TO PROVIDE INPUT STABILITY FOR LSI-11 AND QBC CONTROL SIGNALS. CLOCK INPUT FOR U97 AND U100 IS PROVIDED BY I-OSC-2.

(69) (I-SMX-1) STATUS MULTIPLEXERS:

I-SMX-1 CONSISTS OF STATUS MUX U63, U81 AND U82. STATUS MUX U63 INPUTS ARE CONTROL SIGNALS FROM I-CPU-1. STATUS INPUTS TO U81 AND U82 ARE FROM LSI-11 (TO U82) AND QBC INTERNAL CIRCUITS (TO U82) VIA I-ISR-1. QBC PROCESSOR SAMPLES STATE OF U63 INPUT TO DETERMINE OPERATION REQUESTED BY ICPU-1. U63, U81 AND U82 ARE ENABLED BY PIN 7 SIGNALS FROM I-IEC-1. INPUT SIGNALS (D0-D7) TO BE SAMPLED ARE SELECTED BY U63, U81 AND U82 PIN 9, 10 AND 11 INPUTS FROM I-IEC-1. STATUS OUPUTS (PIN 6, U63, U81, U82) ARE APPLIED TO I-PEG-1.

(70) (I-IEC-1) INSTRUCTION EXECUTION CONTROL:

I-IEC-1 CONSISTS OF U79 (PROM B) AND U80 (PROM A). I-IEC-1 CONTROLS FLOW OF INSTRUCTION EXECUTION AND OUTPUT OF STATUS MULTIPLEXERS (I-SMX-1). NINE I-IEC-1 OUTPUTS PROVIDE JUMP ADDRESS TO I-PAR-1. SIX OUTPUTS TO I-SMX-1 CONTROL SELECTION OF STATUS TO BE MONITORED. ONE OUTPUT TO I-PEG-1 CONTROLS POLARITY OF STATUS APPLIED TO I-PAR-1.

(71) (I-OSC-2) OSCILLATOR:

I-OSC-2 CONSISTS OF U65 AND U64A AND B. I-OSC-2 PROVIDES 9.12MHZ (109 NANOSECONDS) CLOCK FOR QBC. U64A AND B ARE CONFIGURED AS INVERTING BUFFERS.

(72) (I-PEG-1) PROCESSOR ADDRESS REGISTER ENABLE GATE:

I-PEG-1 CONSISTS OF U64C WHICH CONTROLS POLARITY OF STATUS INPUT TO I-PAR-1. WHEN OUTPUT OF I-IEC-1, PIN 13 (TO U64C, PIN 9) IS LOW, OUTPUT TO I-PAR-1 IS NOT INVERTED AND REFLECTS INPUT WHICH APPEARS ON PIN 10 OF U64.

(73) (I-PAR-1) PROCESSOR ADDRESS REGISTER:

I-PAR-1 CONSISTS OF U62, U51 AND U52. ADDRESS INPUTS FROM I-IEC-1 ARE CONTROLLED BY PE INPUT FROM I-PEG-1. WHEN PE IS LOW, NEW ADDRESS IS LOADED INTO I-PAR-1 AT NEXT RISING EDGE OF CLOCK AT PIN 2. WHEN PE IS HIGH, ADDRESS IS INCREMENTED ON NEXT CLOCK PULSE. LOADING NEW ADDRESS CONTROLS JUMPS TO NEW ADDRESS, OR INCREMENTING TO NEXT ADDRESS CONTROLS EXECUTION OF NEXT SEQUENTIAL INSTRUCTION BY THE QBC PROCESSOR. Q0-Q3 OUTPUTS FROM I-PAR-1 PROVIDE ADDRESS INPUTS TO I-OCM-1 AND I-IEC-1. RESET FROM I-INV-5 RESETS I-PAR-1 TO ADDRESS ZERO.

(74) (I-OCM-1) OUTPUT CONTROL MEMORY:

I-OCM-1 CONSISTS OF PROMS U75 THRU U78. I-OCM-1 GENERATES 32 SIGNALS REQUIRED TO CONTROL QBC OPERATIONS. ADDRESS INPUTS ARE FROM I-PAR-1. OUTPUTS ARE TO I-OSR-1.

(75) (I-OSR-1) OUTPUT STABILITY REGISTERS:

I-OSR-1 CONSISTS OF REGISTERS U47 THRU U50 WHICH STABILIZE OUTPUTS OF I-OCM-1. I-OSR-1 OUTPUTS ARE CLOCKED SUCH THAT CONTROL SIGNALS ARE APPLIED TO DEVICES ONE QBC CLOCK TIME LATER THAN WHEN GENERATED BY I-OCM-1.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 16 of 25)

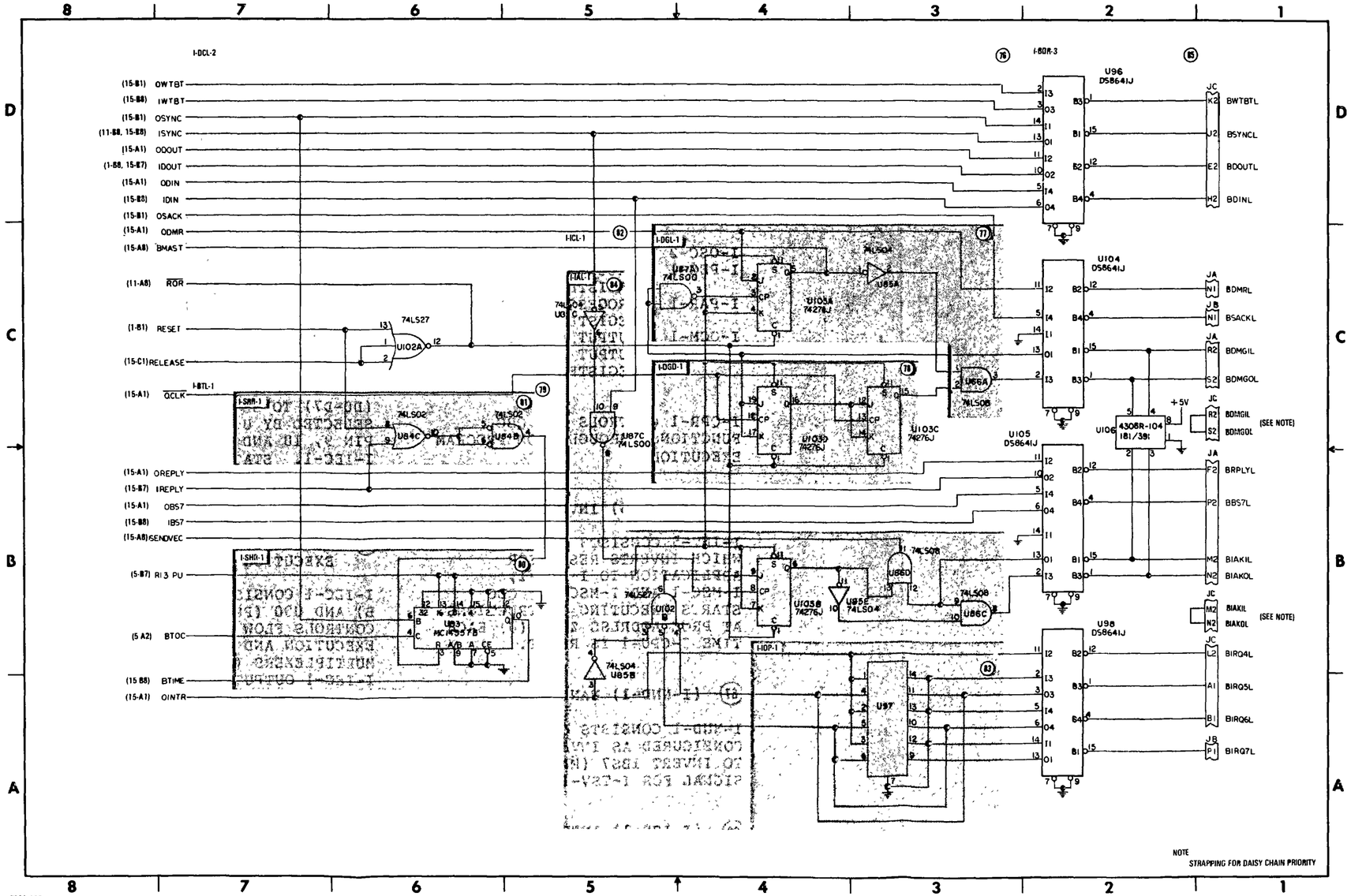


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 17 of 25)

(76) I-DCL-2) DMA CONTROL LOGIC:

I-DCL-2 CONSISTS OF GATE U102, DMA GRANT LOGIC (I-DGL-1), AND DMA GRANT DELAY (I-DGD-1). I-DCL-2 GAINS CONTROL OF LSI-11 SYSTEM BUS WHEN COMMANDED BY QBC PROCESSOR. COMMAND OF SYSTEM BUS IS REQUIRED FOR DMA TRANSFER OF FOUR WORDS OR LESS (USING DMA REGISTER ADDRESS) AND FOR I/O PROGRAMMED TRANSFER OF A WORD OR BYTE (USING ADDRESS OF REGISTER IN I-BEP-1). SIGNALS RESET AND RELEASE ARE INPUT TO GATE U102, RESULTING IN ROR SIGNAL OUTPUT TO I-DTC-1. U102 ALSO FURNISHES CLEAR INPUTS TO FLIP-FLOPS IN I-DGL-1, I-DGD-1, and I-ICL-1.

(77) (I-DGL-1) DMA GRANT LOGIC:

I-DGL-1 CONSISTS OF GATES U85A, U86A AND U87A, AND FLIP-FLOP U103A. DMA GRANT TO SYSTEM BUS IS BASED ON DAISY-CHAIN PRICRITY. BUS ACCESS BY HIGHEST-PRIORITY DEVICE IS RESULT OF QBC PROCESSOR-GENERATED ODMR (OUTPUT DMA REQUEST) SIGNAL WITH BDMGOL (BUS DMA GRANT OUT LOW) RESPONSE FROM LSI-11 SYSTEM. IF HIGHER PRIORITY MUX HAS NO DMA REQUEST PENDING, BDMGOL IS APPLIED TO NEXT LOWER-PRIORITY DEVICE AS BDMGIL (BUS DMA GRANT IN LOW). WHEN DMA REQUEST IS PENDING, HIGHER-PRIORITY DEVICE INHIBITS BDMGOL OUTPUT TO NEXT LOWER-PRIORITY MUX. HIGH INPUT TO U87A INVERTS BDMGIL AND APPLIES OUTPUT TO CLOCK INPUT OF FLIP-FLOP U103A. ODMR ACTIVE AT J INPUT OF U103A TOGGLES FLIP-FLOP, RESULTING IN BMAST (BUS MASTER) OUTPUT, WHICH INDICATES MUX IS MASTER OF LSI-11 SYSTEM BUS. BMAST IS INVERTED BY U85A AND APPLIED TO GATE U86A. BMAST ACTIVE INHIBITS GATE U86A AND SUBSEQUENT BDMGOL OUTPUT FROM I-BDR-3. THE K INPUT TO U103A IS POSITIVE, PROVIDED BY R13PU. THE C (RESET) INPUT TO U103A IS ROR FROM GATE U102A.

(78) (I-DGD-1) DMA GRANT DELAY:

I-DGD-1 CONSISTS OF U103C AND D. BDMG1L IS APPLIED TO J AND K INPUTS OF U103D. QCLK PROVIDES CLOCK INPUT TO U103 C AND D, CLOCKING Q OUTPUT OF U103D TO J AND K INPUTS OF U103C. ON FOLLOWING NEGATIVE TRANSITION OF QCLK, Q OUTPUT OF U103C IS APPLIED TO GATE U86A. IF BMAST IS INACTIVE, OUTPUT OF U86A, APPLIED TO I-BDR-3, ENABLES BDMGOL OUTPUT APPLIED TO NEXT LOWER-PRIORITY DEVICE. SIGNAL /ROR PROVIDES THE RESET INPUTS TO U103C AND D. SET INPUTS TO U103C AND D ARE POSITIVE, PROVIDED BY R13PU.

(79) (I-BTL-1) BUS TIMEOUT LOGIC:

I-BTL-1 CONSISTS OF SHIFT REGISTER (I-SHR-1) AND SHIFT REGISTER RESET LOGIC (I-SRR-1). I-BTL-1 IS ACTIVATED WHEN QBC PROCESSOR ASSERTS BSYNCL INDICATING START OF BUS TRANSACTION. I-BTL-1 ACTS AS ALARM WHEN ADDRESSED DEVICE FAILS TO RESPOND.

(80) (I-SHR-1) SHIFT REGISTER:

I-SHR-1 CONSISTS OF SHIFT REGISTER U83. U83 IS VARIABLE LENGTH DEVICE CONFIGURED FOR LENGTH OF 25 STAGES. SIGNAL OSYNC IS CONNECTED TO DATA INPUT OF U83. BTOC (BUS TIMEOUT CLOCK) IS CLOCK INPUT TO U83 AND HAS PERIOD OF 407 NANOSECONDS. U83 OUTPUT BTIME (BUS TIMEOUT) OCCURS 25 CLOCKS AFTER OSYNC IS APPLIED, PROVIDING DELAY OF APPROXIMATELY 10 MICRO-SECONDS. UNDER NORMAL OPERATING CONDITIONS, BRPLYL IS RETURNED FROM ADDRESSED DEVICE BEFORE BTIME IS OUTPUT FROM U83. (IF QBC PROCESSOR DETECTS BTIME HIGH, QBC PROCESSOR RELINQUISHES CONTROL OF SYSTEM BUS AND NOTIFIES I-CPU-1 THAT BUS TIMEOUT ERROR HAS OCCURRED). RESET INPUT TO U83 (PIN 3) IS FROM I-SRR-1.

(81) (I-SRR-1) SHIFT REGISTER RESET LOGIC:

I-SRR-1 CONSISTS OF U84C AND B. IREPLY OR RESET ARE INPUT VIA U84C AND B TO I-SHR-1 TO RESET ALL 25 STAGES OF U83 TO ZERO.

(82) (I-ICL-1) INTERRUPT CONTROL LOGIC:

I-ICL-1 CONSISTS OF INTERRUPT OPTION PLUG (I-IOP-1) AND INTERRUPT ACKNOWLEDGE LOGIC (I-IAL-1). I-ICL-1 PROVIDES DIRECT COMMUNICATIONS WITH LSI-11 PROCESSOR FOR INTERRUPT REQUESTS AND RESPONSE.

(83) (I-IOP-1) INTERRUPT OPTION PLUG:

I-IOP-1 CONSISTS OF U97 STRAPPABLE PLUG-IN, OPTIONALLY CONFIGURED TO SERVICE VARYING PRIORITY LEVELS. INTERRUPT LEVEL FOUR IS OPTION USED IN SYSTEM AND IS STRAPPED AS SHOWN. BUS PROTOCOL DICTATES THAT LEVEL SEVEN DEVICES ASSERT BOTH LEVEL SIX AND LEVEL SEVEN INTERRUPT REQUESTS (BIRQ6L, BIRQ7L), SO ONLY LEVEL FIVE AND SIX INTERRUPT REQUESTS ARE MONITORED. U97 OUTPUTS (PINS 12, 13, AND 14) CORRESPONDING TO LEVEL 5, 6 AND 7 INTERRUPT REQUEST INPUTS TO I-BDR-3, (U98) ARE GROUNDED, PROHIBITING OUTPUT OF LEVEL 5, 6 AND 7 INTERRUPT REQUESTS. LEVEL 5 INTERRUPT REQUESTS FROM I-BDR-3 U98 TO U97 ARE INPUT AT PIN 11, WHICH IS EXTERNALLY CONNECTED TO U97 PIN 4. LEVEL 6 INTERRUPT REQUESTS FROM I-BDR-3 (U98) TO U97 ARE INPUT TO U97, PIN 10, WHICH IS EXTERNALLY CONNECTED TO U97, PINS 5 AND 6.

(84) (I-IAL-1) INTERRUPT ACKNOWLEDGE LOGIC:

I-IAL-1 CONSISTS OF GATES U85B, C, E, U86C, D, U87C AND U102B, AND FLIP-FLOP U103B. WHEN I-CPU-1 COMMANDS QBC PROCESSOR TO SEND INTERRUPT, QBC PROCESSOR ASSERTS OINTR, APPLIED TO U85B AND TO I-BDR-3, U98, RESULTING IN BIRQ4L OUTPUT TO LSI-11 PROCESSOR. AFTER EXECUTION OF CURRENT INSTRUCTION, AND UPON DETECTION OF BIRQ4L, LSI-11 PROCESSOR ASSERTS BDINL (I-BDR-3, U96). BDINL RESULTS IN IDIN TO U87C, PIN 9 BEING SET. LSI-11 PROCESSOR ALSO DISABLES BSYNCL (I-BDR-3, U96) CAUSING ISYNC TO U85C TO BE LOW. U85C INVERTS ISYNC, PROVIDING HIGH INPUT TO U87C. HIGH TO LOW TRANSITION OUTPUT FROM U87C IS INPUT TO U103B. J INPUT TO U103B IS FUNCTION OF U102B. LEVEL 5, 6 OR 7 INTERRUPT REQUESTS FROM I-IOP-1 TO U102B, PINS 4 AND 5, DISABLING U102B OUTPUT. ACTIVE OINTR SIGNAL, INVERTED BY U85B AND INPUT TO U102B, PIN 3, WITHOUT LEVEL 5, 6 OR 7 INTERRUPTS PRESENT AT PINS 4, OR 5 OF U102B, ENABLING OUTPUT OF U102B, PIN 6. ENABLED OUTPUT OF U102B IS APPLIED TO J INPUT OF U103D. RESULTING HIGH Q OUTPUT FROM U103D ENABLES GATE U86D. ACTIVE BIAKIL SIGNAL FROM I-BDR-3 IS APPLIED TO GATE U86D, RESULTING IN SENDVEC OUTPUT. WHEN MUX BOARD HAS NO INTERRUPT REQUEST PENDING, Q OUTPUT FROM U103D IS LOW, INVERTED BY U85E, ENABLING U86C, WHICH PROVIDES OUTPUT (BIAKOL) TO I-BDR-3, WHEN BIAKIL IS ACTIVE. BIAKOL IS DAISY-CHAINED TO NEXT LOWER-PRIORITY DEVICE, INPUT AS BIAKIL AT OTHER MUX BOARD.

(85) (I-BDR-3) BUS DRIVERS AND RECEIVERS:

I-BDR-3 CONSISTS OF TRANSCEIVERS U96, U98, U104 AND U105 AND RESISTOR NETWORK U106. TRANSCEIVERS PROVIDE NECESSARY INTERFACE BETWEEN QBC LOGIC AND LSI-11 SYSTEM BUS. RESISTOR NETWORK U106 PROVIDES TERMINATION FOR GRANT AND INTERRUPT ACKNOWLEDGE SIGNALS.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 18 of 25)

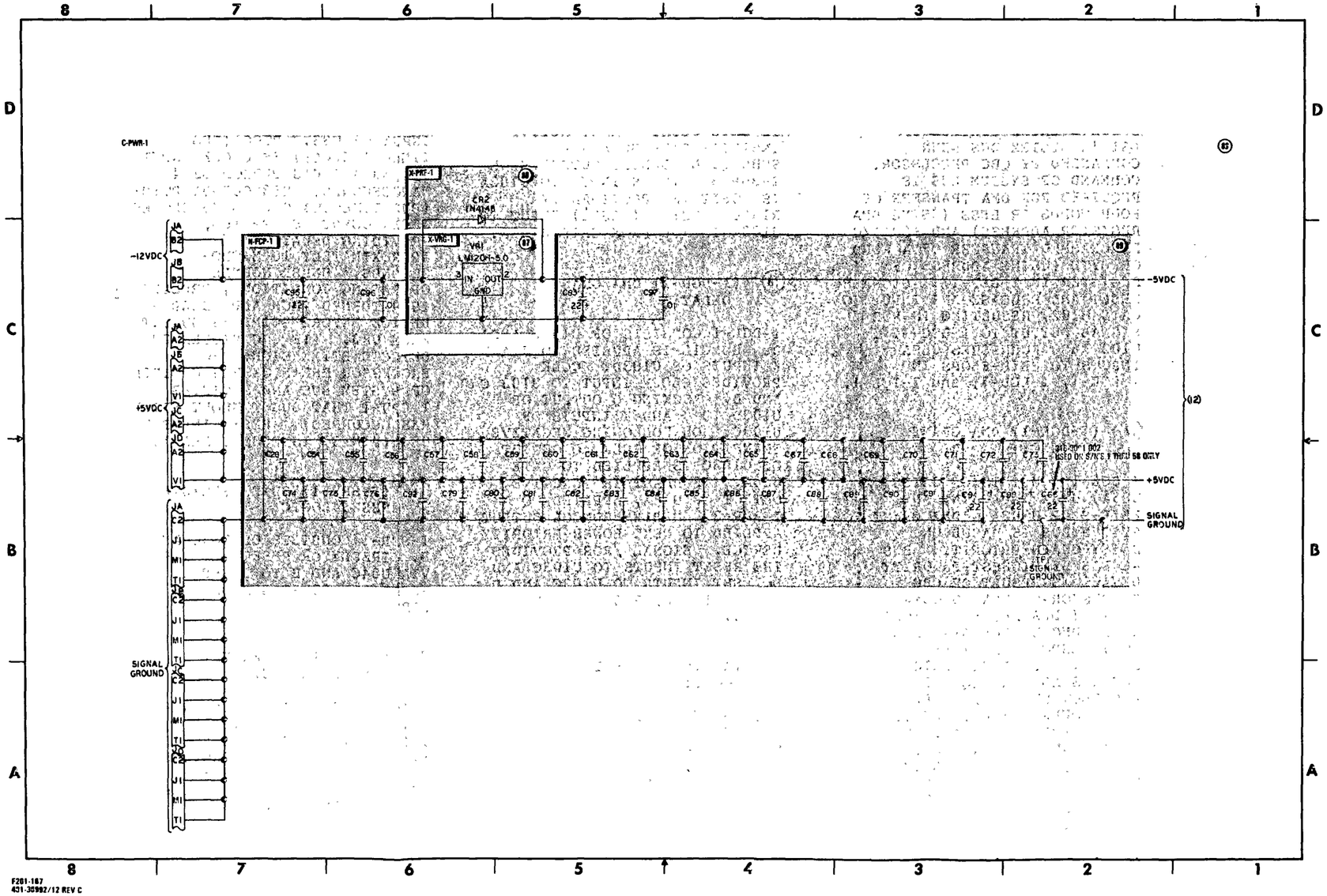


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 19 of 25)

(86) **(C-PWR-1) POWER CIRCUIT:**

I-PWR-1 CONSISTS OF VOLTAGE REGULATOR (X-VRG-1), PROTECTION RECTIFIER (X-PRF-1) AND FILTER CAPACITORS (N-FCP-1).

(87) **(X-VRG-1) VOLTAGE REGULATOR:**

X-VRG-1 CONVERTS -12 VDC INPUT TO -5 VDC USED PRIMARILY BY I-LDR-1 THRU I-LDR-4.

(88) **(X-PRF-1) PROTECTION RECTIFIER:**

X-PRF-1 CONSISTS OF DIODE CR2, WHICH PROVIDES PROTECTION FOR X-VRG-1 IF IMPROPER VOLTAGE IS ACCIDENTALLY CONNECTED OR -12 VDC POWER SUPPLY FAILS.

(89) **(N-FCP-1) FILTER CAPACITORS:**

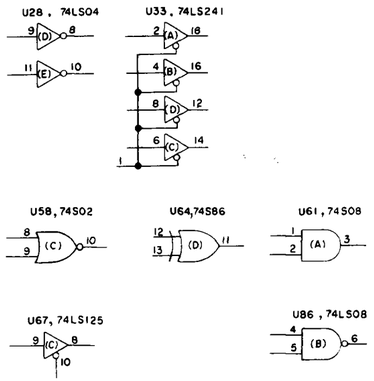
N-FCP-1 CONSISTS OF TWO 22 MICROFARAD AND TWO .1 MICROFARAD CAPACITORS IN -5 VDC NETWORK, AND THREE 22 MICROFARAD AND THIRTY-SEVEN .1 MICROFARAD CAPACITORS IN +5 VDC NETWORK. 22 MICROFARAD CAPACITORS HAVE RELATIVELY SLOW RESPONSE TIMES BUT CAN SUPPLY LARGE CURRENTS. .01 MICROFARAD CAPACITORS HAVE FAST RESPONSE TIMES AND SUPPLY A LIMITED AMOUNT OF CURRENT.

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 20 of 25)

POWER AND GROUND DISTRIBUTION TABLE

DEVICE	GROUND PIN	+5V PIN	-12V PIN	-5V PIN	REF DES
74LS00	7	14			U56, U87
74LS02	7	14			U31, U84
74S02	7	14			U58
74LS04	7	14			U1, U28, U57, U85
74LS08	7	14			U86
74S08	7	14			U61
74LS27	7	14			U102
74LS74A	7	14			U54, U55, U66
74S74	7	14			U68
74S86	7	14			U64
74LS125	7	14			U44, U59, U67
74LS126	7	14			U45, U60
74LS241	10	20			U33
74S251	8	16			U63, U81, U82
74276	10	20			U103
74LS373	10	20			U109
74LS377	10	20			U32, U47, U48, U49, U50, U99
74LS378	8	16			U100, U101
8085A-2	20	40			U72
8155-2	20	40			U34, U35
8253-5	12	24			U30
8274	20	40			U29, U43
26LS32	8	16			U3, U6, U10, U13, U16, U19, U23, U26, U27
3691	5	1		8	U2, U4, U8, U21, U25
8641	8	16			U94, U95, U96, U98, U104, U105
8X32C	20,1	40			U46
19-13C40-00	10	20			U89, U90, U91, U92
19-14035-00	10	20			U73, U74
K1115A	7	14			U65
14557B	8	16			U83
93S16	8	16			U51, U52, U62
MEMORY SOCKET	14	1,26,28			U36, U37, U38, U39, U40, U41
LM120H-5.0	1		3		VR1
74LS279	8	16			U53
3205	8	16			U107
MP18	CASE				Y1
316-XXXX-001	10	20			U71, U75—U80, U88

SPARES



F201-168
401-38992/2 REV C

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 21 of 25)

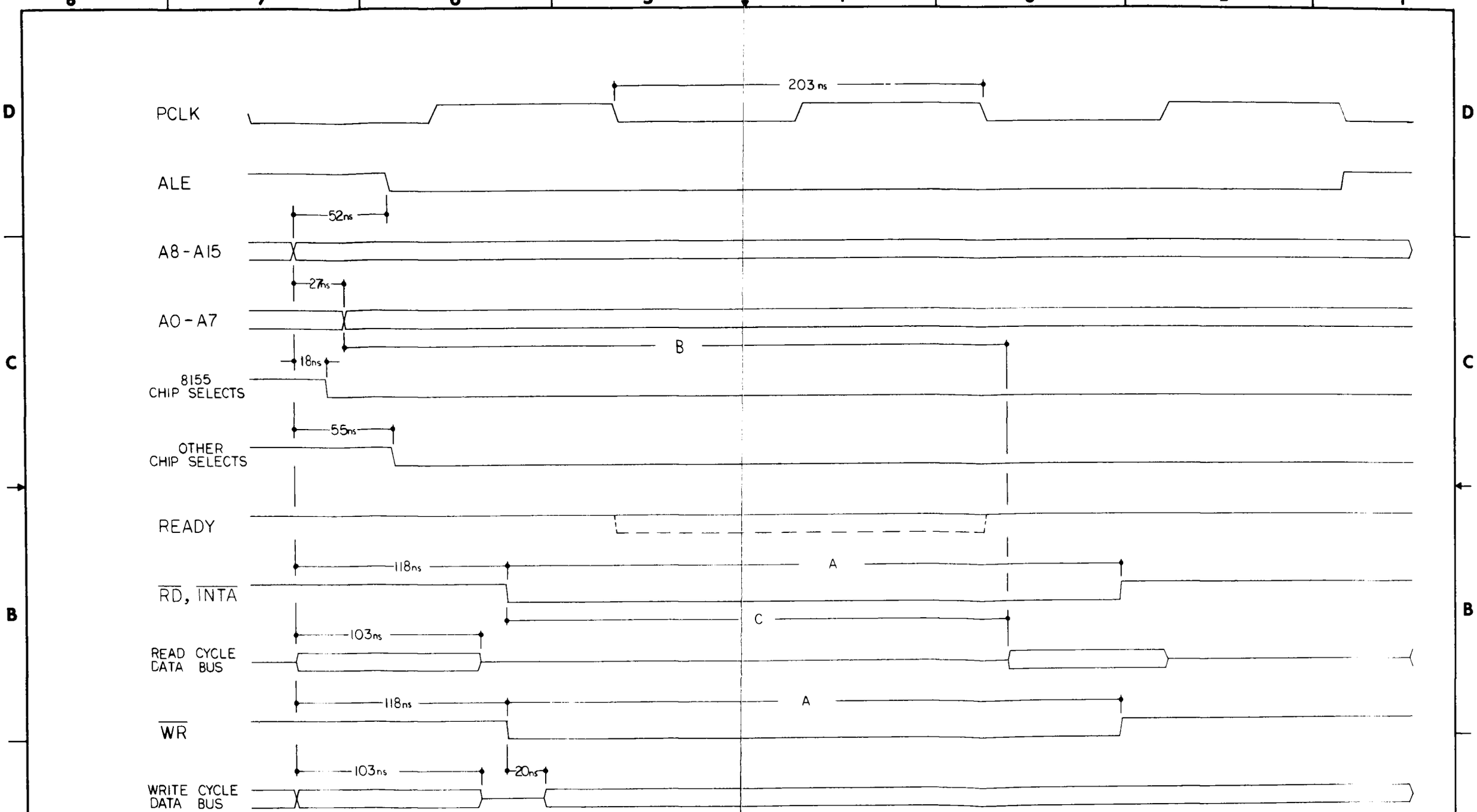


TABLE II

DEVICE	A	B	C
2764 - 2	235ns	200 ns	70 ns
MK4802P -3	235ns	200ns	100 ns
8155 -2	235ns	348ns	258 ns
8253 -5	438ns	330ns	200ns
8274	438ns	200ns	200ns

F201-169
401-36992/13 REV C

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 22 of 25)

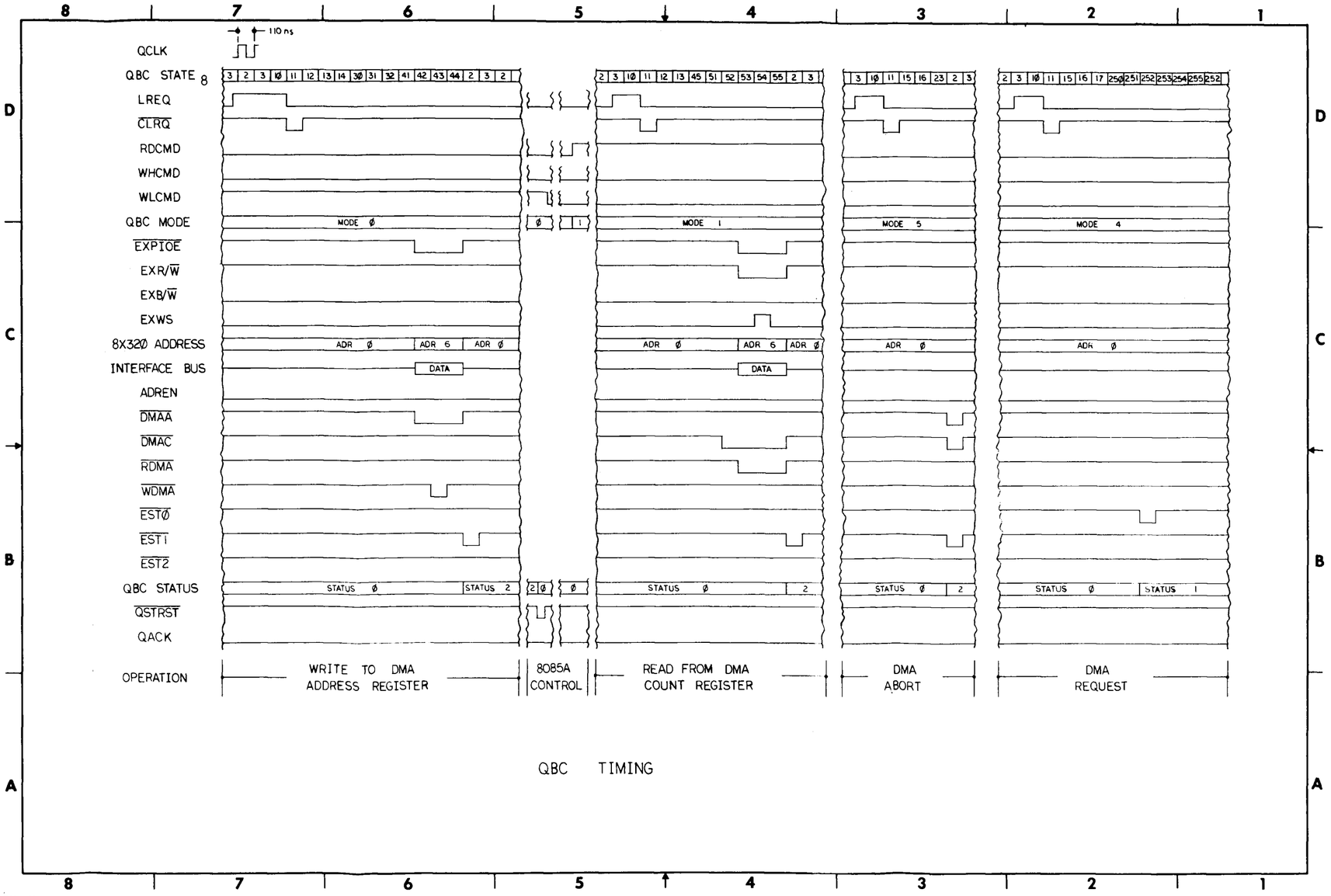
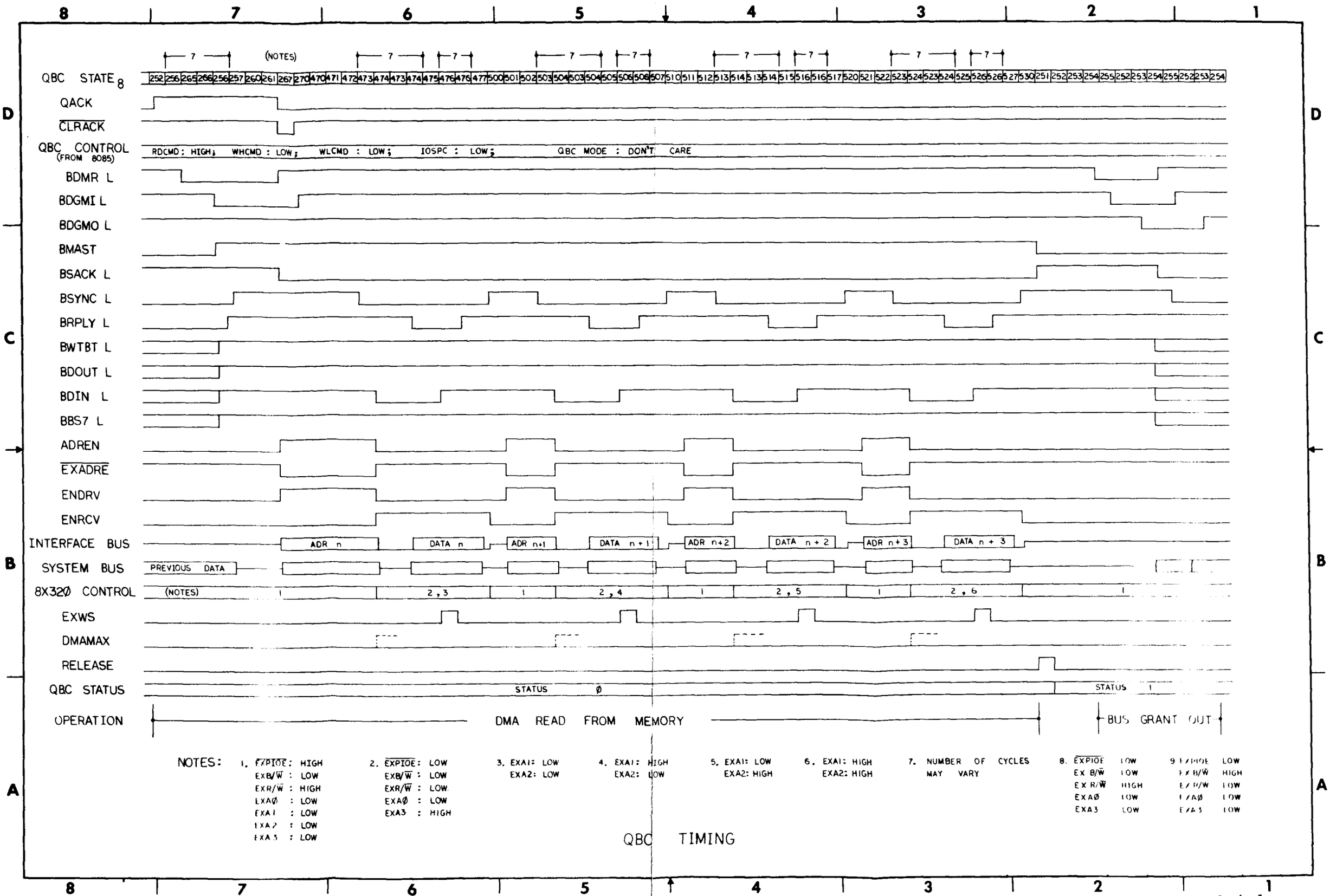


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 23 of 25)



F201-171
401-36992/15 REV C

Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 24 of 25)

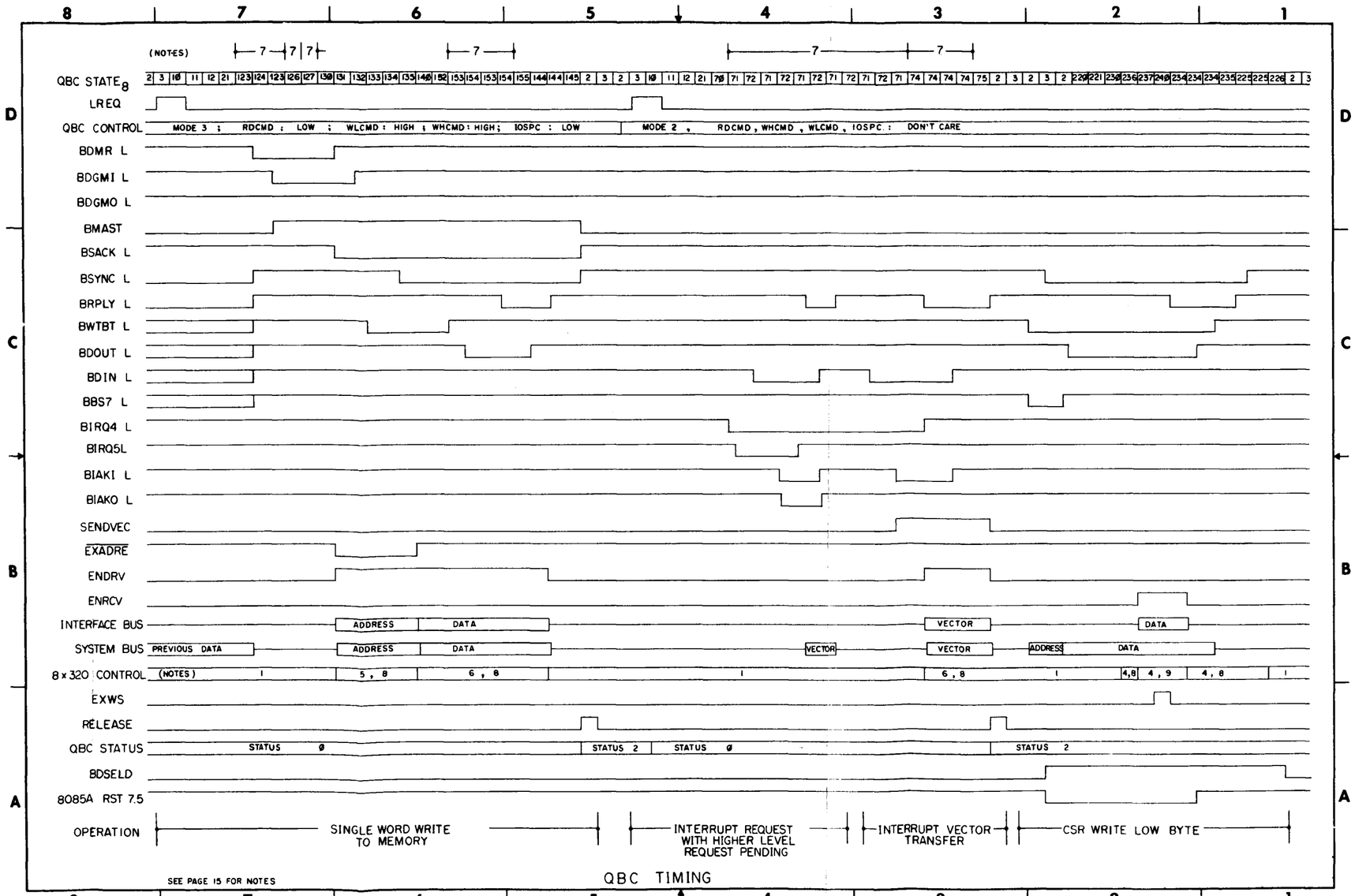


Figure 2-7. Multiplexer Blocked Schematic Diagram and Keyed Text (Sheet 25 of 25)

Table 2-1. Multiplexer Error Codes

CODE	DEFINITION
00000010	PROM 0 CHECKSUM ERROR
00000011	PROM 1 CHECKSUM ERROR
00000100	ILLEGAL RST 4
00000101	ILLEGAL RST 5
00000110	ILLEGAL RST 6
00000111	ILLEGAL RST 7
00001000	
00001001	8155A (STACK) RAM DATA LINE TIED LOW
00001010	8155A (STACK) RAM DATA LINE TIED HIGH
00001011	8155A (STACK) RAM DATA LINES TIED TOGETHER
00001100	8155A (STACK) RAM MULTIPLE DECODE PASS 1
00001101	8155A (STACK) RAM MULTIPLE DECODE PASS 2
00001110	8155A COUNTER SLOW
00001111	8155A COUNTER FAST
00010000	
00010001	8155B RAM DATA LINE TIED LOW
00010010	8155B RAM DATA LINE TIED HIGH
00010011	8155B RAM DATA LINES TIED TOGETHER
00010100	8155B RAM MULTIPLE DECODE PASS 1
00010101	8155B RAM MULTIPLE DECODE PASS 2
00010110	8155B COUNTER SLOW
00010111	8155B COUNTER FAST
00011000	
00011001	BUFFER RAM DATA LINE TIED LOW
00011010	BUFFER RAM DATA LINE TIED HIGH
00011011	BUFFER RAM DATA LINES TIED TOGETHER
00011100	BUFFER RAM MULTIPLE DECODE PASS 1
00011101	BUFFER RAM MULTIPLE DECODE PASS 2
00011110	ILLEGAL TRAP INTERRUPT
00011111	ILLEGAL RST 5.5 INTERRUPT
00100000	COUNTER 0 SLOW
00100001	COUNTER 0 FAST
00100010	COUNTER 1 SLOW
00100011	COUNTER 1 FAST
00100100	COUNTER 2 SLOW
00100101	COUNTER 2 FAST

Table 2-1. Multiplexer Error Codes (Continued)

CODE	DEFINITION
00100110	QBC: NO RESPONSE
00100111	QBC: BUS TIME-OUT
00101000	QBC: NEGATIVE ACKNOWLEDGE
00101001	QBC: INVALID CODE
00101010	DMA: IMPROPER STATE FOR "REQUEST NEXT FOUR WORDS"
00101011	DMA: IMPROPER STATE FOR "ACKNOWLEDGE"
00101100	DMA: IMPROPER STATE FOR "DMA OPERATION COMPLETE"
00101101	DMA: IMPROPER NEXT STATE FOR "PIO COMPLETE"
00101110	DMA: IMPROPER NEXT STATE FOR "INTERRUPT COMPLETE"
00101111	LSI-11/23 BUS TIME-OUT
00110000	INTERRUPT QUEUE OVERFLOW
00110001	PIO QUEUE OVERFLOW
00110010	DMA QUEUE OVERFLOW
00110011	DEFERRED TASK QUEUE OVERFLOW
00110100	WAITING FOR RST 6.5
00110101	NO READ OR WRITE SET FOR DMA TRANSACTION
00110110	
00110111	
	DMA ADDRESS REGISTER FAILURES:
00111000	INVALID QBC RESPONSE TO LOW BYTE WRITE
00111001	LOW BYTE ERROR
00111010	HIGH BYTE ERROR
00111011	
	DMA WORD COUNT REGISTER FAILURES:
00111100	INVALID QBC RESPONSE TO WRITE
00111101	LOW BYTE ERROR
00111110	HIGH BYTE ERROR
00111111	
	DMA ABORT FAILURES
01000000	INVALID QBC RESPONSE TO DMA ADDRESS REG WRITE
01000001	INVALID QBC RESPONSE TO DMA WORD COUNT REG WRITE
01000010	INVALID QBC RESPONSE TO DMA ABORT COMMAND
01000011	DMA ADDRESS REGISTER READ ERROR
01000100	DMA WORD COUNT REGISTER READ ERROR
01001000	CHANNEL LOOPBACK FAILURE

control-status register (CSR) which provides exchange of control-status information between I-LPR-1 and the LSI-11 Processor, under QBC control.

The extended address port provides I-LPR-1 control of LSI-11 data/address lines 16 thru 21. Extended address lines provide multiplexer compatibility with Digital Equipment systems having up to 4M bytes of memory.

The Q-Bus controller control port provides I-LPR-1 direct control over QBC operations. I-LPR-1 initiates command signals, asserts a request monitored by the QBC processor, enabling the transfer of data to or from the LSI-11 memory.

The Q-Bus controller is a set of logic that allows data transfer between the local 8085A processor and the LSI-11 Bus (Q-Bus). The Q-Bus controller consists of the following:

I-QPR-1	Q-Bus Controller Processor
I-BDR-1, 2, 3	Bus Drivers and Receivers
I-DCL-1, 2	DMA Control Logic
I-BTL-1	Bus Time-out Logic
I-ICL-1	Interrupt Control Logic
I-QSP-1	Q-Bus Controller Status Port.

The QBC processor is a hardware sequencer which generates control signals, samples status information, and branches or makes decisions based on status. All Q-bus controller logic is under direct control of the QBC processor. The QBC processor has a PROM 512 words long with each word being 48 bits wide. QBC logic is controlled by 32 of the 48 PROM lines (bits). Operation of the QBC processor is controlled by 16 of the 48 PROM lines. These 16 lines permit the QBC processor to select the status input, sample control polarity of the status input, and set up a jump address when the status input indicates a jump.

The QBC processor has 21 status inputs which, when sampled, control the execution of the program. Two of the status inputs allow the QBC processor to either unconditionally increment or unconditionally jump to a new address. Six of the QBC processor status inputs are control signals from the 8085 microprocessor. These control signals are listed in table 2-2.

The QBC microcode has instructions built in that return a negative acknowledge status to I-CPU-1 in the event that a local request is issued without the appropriate control ports being set up.

Bus drivers and receivers provide the required electrical interface between the LSI-11 bus and multiplexer logic. All bus signals are buffered to ensure that bus loading specifications are met. Data bus buffers also provide the capability to detect CSR addressing by the LSI-11 Processor. Based on the state of the bus control signals from the LSI-11, the QBC controls the reading of data from or the writing of data into the CSR.

Table 2-2. Multiplexer QBC Control Signals

WHCMD	WRITE HIGH BYTE COMMAND Enables the QBC to write only the high byte of data during a programmed I/O data transfer, or to write both the high and the low bytes during a DMA operation. It also enables DMA address register write or DMA word count register write.
WLCMD	WRITE LOW BYTE COMMAND Enables the QBC to write only the low byte of data during a programmed I/O data transfer or to write both the high and low bytes during a DMA operation. It also enables DMA address register write or DMA word count register write.
RDCMD	READ COMMAND Enables the QBC to read a word (both high and low bytes) of data during a programmed I/O data transfer, a DMA operation, DMA address register read, or a DMA word-count register read.
IOSPC	I/O SPACE Specifies that an LSI-11 bus operation is to an address in the LSI-11 I/O page of memory. If IOSPC is not set, the operation will be to an address in the non-I/O portion of memory.
LREQ	LOCAL REQUEST Indicates to the QBC that I-CPU-1 is requesting the QBC to begin an operation. The operation to be performed is defined by the QBC mode that I-CPU-1 has previously written into the QBC control port. The QBC resets this bit after the local request has been recognized.
QACK	QBC ACKNOWLEDGE Indicates to the QBC during a DMA write operation that I-CPU-1 has placed data into the bus exchange port, and that the QBC may request use of the bus to transfer that data. The QACK signal indicates to the QBC during a DMA read operation that the QBC may request use of the LSI-11 bus to read data from LSI-11 memory and place it into the bus exchange port. The QBC resets this bit after QACK has been recognized.

Table 2-3. Multiplexer QBC Modes

Mode	Function	QBCM2	QBCM1	QBCM0
0	DMA Address Register	Low	Low	Low
1	DMA Word Count Register	Low	Low	High
2	Interrupt Sequence	Low	High	Low
3	Q-Bus Transaction	Low	High	High
4	DMA Operation Request	High	Low	Low
5	DMA Operation Abort	High	Low	High
6	(Invalid Mode)	High	High	Low
7	(Invalid Mode)	High	High	High

During idle periods, the QBC processor runs an executive program which continuously samples the LREQ signal. When LREQ changes to the active state the QBC processor begins testing other control inputs to determine what type of operation is required. The possible QBC modes are listed in table 2-3.

DMA Control Logic performs four types of transfers, which are: read from data memory, write to data memory, read from I/O page of memory, and write to I/O page of memory. DMA control logic is divided into two categories: I-DCL-2, which provides for bus acquisition and I-DCL-1, which provides data transfer control.

I-DCL-2, controlled by the QBC processor, issues a request for the Q-Bus from the LSI-11. The LSI-11 Processor responds with a grant signal. I-DCL-2 then assumes control of the Q-Bus as "Bus Master" for the duration of the DMA transaction. Upon completion of the DMA transaction, I-DCL-2 releases control of the Q-Bus and is reset to await the next request. If the LSI-11 issues a grant signal and I-DCL-2 has no request pending, the grant signal is passed on to the next lower priority multiplexer to provide a daisy chain priority scheme.

I-DCL-1 has two registers which control DMA transfers between the multiplexer and LSI-11 memory. These registers provide the address of memory locations to be referenced for each transaction in the DMA sequence, and a count of the number of words transferred. Register values are loaded by I-CPU-1 before the DMA transaction is started. After each 16-bit word is transferred, the address and word counts are automatically incremented. When the count register reaches its maximum count, the QBC processor is notified and the DMA operation is terminated. The length of DMA transfers is limited to the 512 to 1000 word range based on the

amount of available RAM. Actual DMA transfers are much shorter. DMA transactions are broken into a series of up to four word transfers. After each four word transfer, the QBC relinquishes control of the Q-Bus to allow the LSI-11 processor to continue program execution and to refresh memory. I-CPU-1 uses this interim time to load the next four words into I-BEP-1, or to read the last four words from I-BEP-1 in preparation for the next transaction sequence.

A programmed I/O transfer differs from the normal DMA operation in that only one read or write bus transaction is performed rather than multiple data transfers. Also, the programmed I/O transfer may be either a word or byte operation. The address for a programmed I/O transfer is obtained from a register in I-BEP-1 rather than from I-DCL-1.

Data registers for programmed transfers are programmed I/O data registers in I-BEP-1. Separation of the programmed I/O and DMA registers permits initiation of a programmed I/O transfer before a previously tasked DMA operation is completed.

The bus time-out logic is enabled for all QBC controlled data transfers to the Q-Bus. If a data word or byte transfer is not completed in less than 10 microseconds, the bus time-out logic generates a BUS TIME-OUT signal to I-QPR-1 indicating that a bus error exists. The QBC then sets the bus time-out status to I-CPU-1 via I-TCS-1, aborts the current bus transaction, and relinquishes control of the Q-Bus. When a bus time-out condition occurs during a DMA operation, the remainder of the DMA transaction is automatically aborted. Usually, a bus time-out is the result of an attempt to transfer data to an address where no device exists, such as in the case of a memory board temporarily removed from the system.

I-CPU-1 can command the QBC to perform an interrupt cycle to the LSI-11; this causes the LSI-11 to suspend current program execution and begin executing an interrupt service routine. Typically, the interrupt cycle is initiated at the end of a DMA transfer, or when an error has been detected by the multiplexer. I-CPU-1 writes the address at which the LSI-11 is to begin executing instructions (the interrupt vector) to I-BEP-1 prior to issuing the interrupt command to the QBC. I-ICL-1 is configured in interrupt level four, which is the lowest priority level defined in the Q-Bus specification. When I-CPU-1 asserts the interrupt command, the QBC enables the interrupt request output to I-ICL-1. I-ICL-1 monitors the higher priority interrupt lines; if no higher priority interrupt is pending, and if the BUS INTERRUPT ACKNOWLEDGE signal is input to I-BDR-3, the QBC places the interrupt vector on the Q-Bus. When the LSI-11 receives the interrupt vector and responds with an interrupt acknowledge, the QBC terminates the interrupt by removing the interrupt vector from the Q-Bus, then signals I-CPU-1 with an acknowledge status.

In the event of an error, or when a QBC operation is complete, the QBC processor sets bits in I-QSP-1. I-CPU-1 reads I-QSP-1 bits to

determine results of a QBC operation. Two reads are performed to avoid the possibility of the first read occurring while the QBC is writing status to the port. I-CPU-1 resets the status port to zero after the status is read. Possible status codes read by I-CPU-1 are listed in table 2-4. Error codes are listed in table 2-5.

Figure 2-7 provides a blocked schematic diagram with keyed text describing the operation of the multiplexer circuit card. Timing diagrams for the multiplexer circuit card are included in figure 2-7.

2.1.1.3.11 Power Control Module. - The Power Control Module, 401-36719, performs the following five basic functions:

1) provides on/off control and fusing for 115 VAC between an AC junction box and power supply assembly,

2) provides 24 VAC output to the system module circuit card for power-up/power-failure sensing and orderly sequencing (-01 and -02 types),

3) provides switch selectable HALT or REBOOT commands to the LSI-11 Processor,

4) provides a visual indication of the LSI-11 RUN mode status, and

5) provides a visual indication of the +5 VDC power supply assembly operation.

Figure 2-8 provides an intermediate logic diagram of the power control module.

As shown in figure 2-8, 115 VAC from the AC junction box is input to C-PIO-1 which provides in-line fuses and an ON/OFF switch. When the switch is in the ON position, 115 VAC is output to the power supply assembly and to N-PFR-1.

The 115 VAC output from C-PIO-1 is applied to a step-down transformer in N-PFR-1 and the resulting 24 VAC is output to the System Module Circuit Card, KPV11-B.

M-HRB-1 contains a momentary two position switch that outputs either a HALT or REBOOT signal to the LSI-11, depending on the switch position.

The SRUNL signal from the KPV11-B is applied to I-RNC-1. I-RNC-1 provides a visual indication of the LSI-11 RUN mode status.

The +5 VDC and +5 VDC SENSE inputs to I-DCO-1 are compared to detect the presence of current in the power bus. This presence signifies proper operation of the power supply assembly. An LED is illuminated during normal operation.

Figure 2-9 provides a blocked schematic diagram with keyed text describing the operation of the power control module.

Table 2-4. Multiplexer QBC Status Codes

Status	Function	QST2	QST1	QST0
0	Quiescent	Low	Low	Low
1	Request Next Four Words	Low	Low	High
2	Acknowledge	Low	High	Low
3	Negative Acknowledge	Low	High	High
4	DMA Operation Complete	High	Low	Low
5	Bus Time-out	High	Low	High
6	(Invalid Status)	High	High	Low
7	(Invalid Status)	High	High	High

Table 2-5. Multiplexer Channel 0 Error Codes:

10000000	INVALID CHANNEL CONFIGURATION CODE RECEIVED
10000001	
10000010	INVALID RX STATUS INTERRUPT
10000011	INVALID TX STATUS INTERRUPT
10000100	RX QUEUE OVERFLOW
10000101	RX BUFFER OVERFLOW
10000110	TX QUEUE OVERFLOW
10000111	TX BUFFER OVERFLOW
10001000	RX ERROR ON LOOPBACK
10001001	TX ERROR ON LOOPBACK
10001010	WAITING FOR SYNC

Error Codes for Channels 1, 2 and 3 will be identical to those of Channel 0 with the exception of Bits 5 and 6:

Channel 1	X 0 1 X X X X X
Channel 2	X 1 0 X X X X X
Channel 3	X 1 1 X X X X X

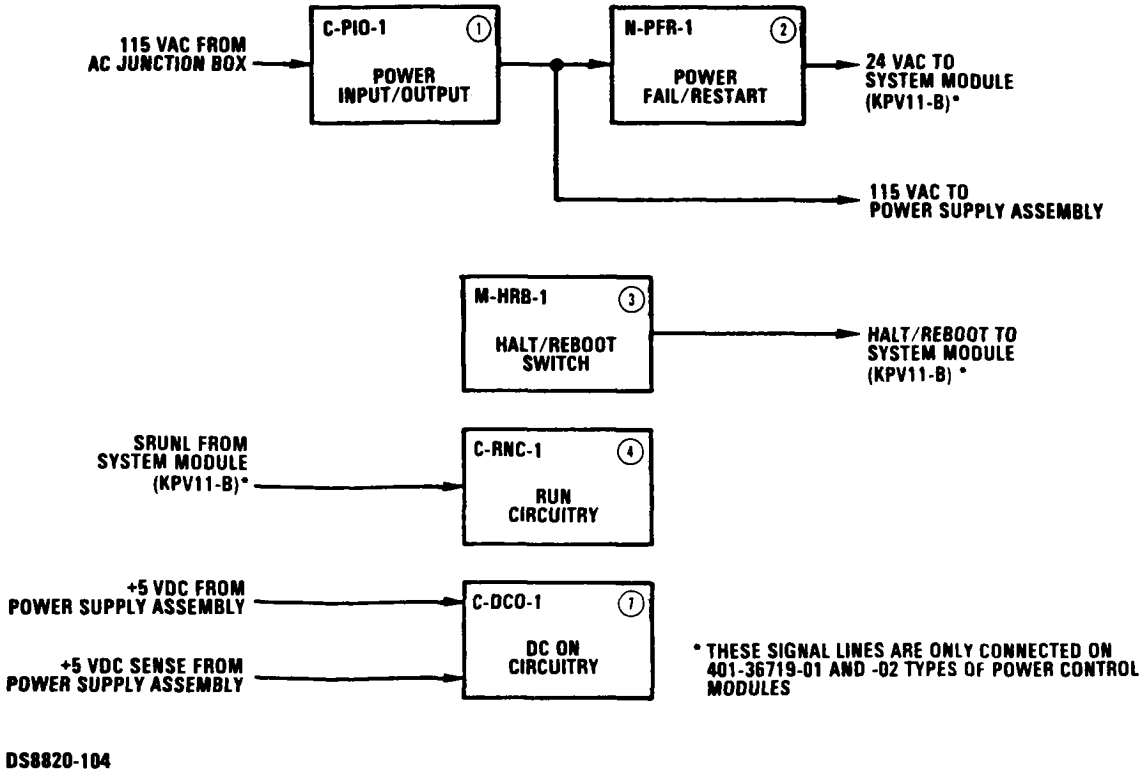


Figure 2-8. Power Control Module Intermediate Logic Diagram

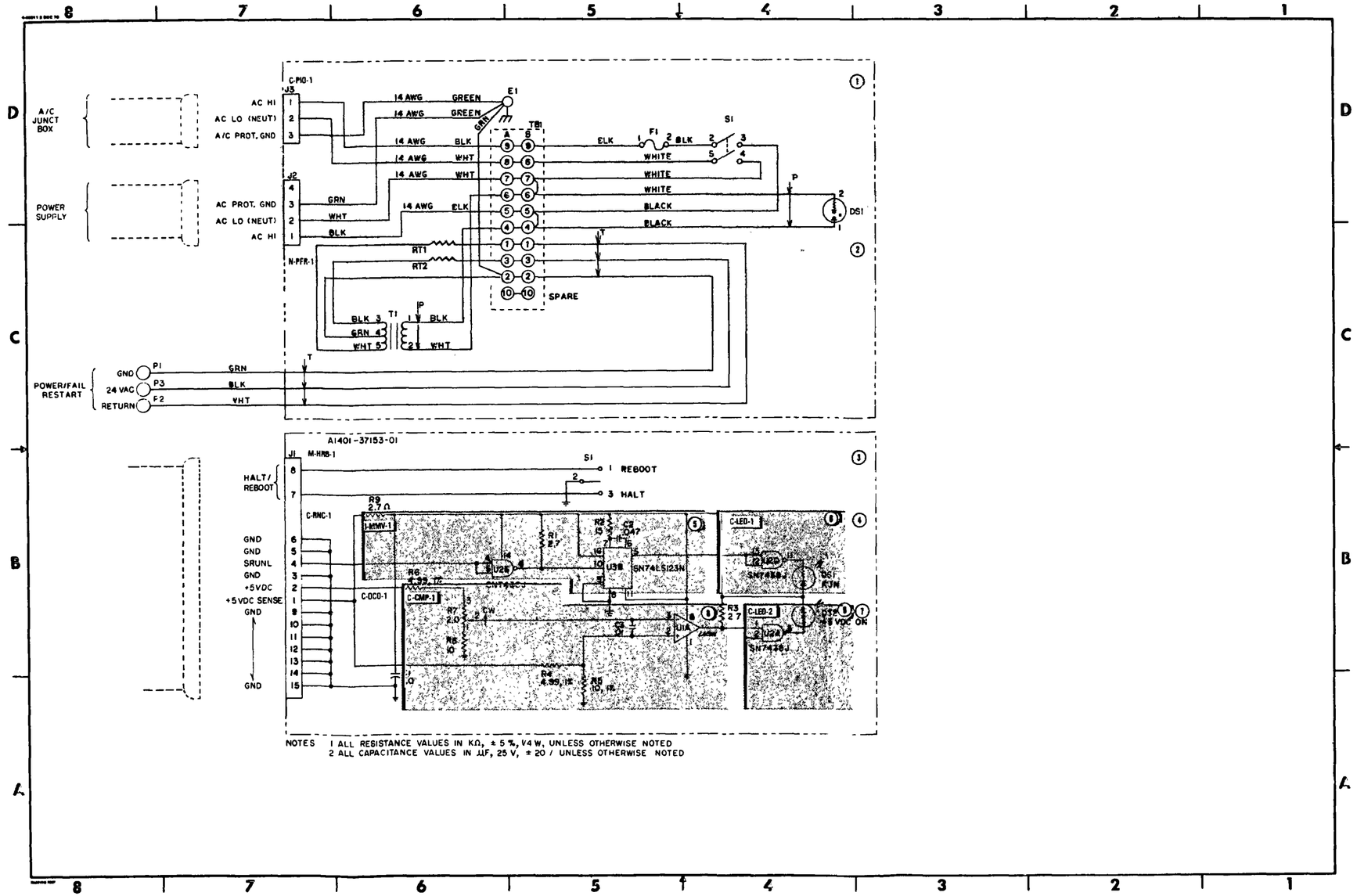


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Figure 2-9. Power Control Module Blocked Schematic Diagram and Keyed Text (Sheet 1 of 2)

① (C-PIO-1) POWER INPUT/ OUTPUT:

C-PIO-1 RECEIVES 115 VAC FROM THE AC JUNCTION BOX, INPUT VIA JACK J3 AND CONNECTED TO TERMINAL BOARD TB1. AC HI AND LO ARE FUSED BY F1 AND F2, RESPECTIVELY. SETTING SWITCH S1 ON PERMITS RETURN OF 115 VAC VIA TB1 TO BE OUTPUT VIA JACK J2 TO CHASSIS POWER SUPPLY. STRAPPING ON TB1 PROVIDES ILLUMINATION OF LAMP DS1 AND 115 VAC OUTPUT TO N-PFR-1 (POWER/FAIL RESTART) WHEN SWITCH S1 IS IN ON POSITION.

② (N-PFR-1) POWER/FAIL RESTART:

N-PFR-1 CONSISTS OF 115 VAC FROM C-PIO-1 (POWER INPUT/OUTPUT) APPLIED VIA TB1 TO THE PRIMARY SIDE OF TRANSFORMER T1. THE 24 VAC OUTPUT FROM THE SECONDARY OF TRANSFORMER TI IS APPLIED VIA TB1 AS AN OUTPUT (VIA P1 THRU P3) TO POWER FAIL-RESTART BOARD (KPV11-B). THE 24 VAC OUTPUT FROM N-PFR-1 PERMITS KPV11-B TO WARN OF POWER FAILURE AND PROVIDE AN ORDERLY POWER UP/POWER DOWN SEQUENCE.

③ (M-HRB-1) HALT/REBOOT CIRCUITRY:

M-HRB-1 CONSISTS OF MOMENTARY, TWO POSITION ON/OFF SWITCH, S1. SWITCH S1 PROVIDES A HALT OR REBOOT COMMAND TO LSI-11 WHEN PLACED IN EITHER HALT OR REBOOT POSITION.

④ (I-RNC-1) RUN CIRCUITRY:

I-RNC-1 PROVIDES AN INDICATION OF A RUN CONDITION FROM LSI-11. I-RNC-1 CONSISTS OF I-MMV-1(MONOSTABLE MULTIVIBRATOR) AND X-LED-1 (RUN INDICATOR).

⑤ (I-MMV-1) MONOSTABLE MULTIVIBRATOR:

I-MMV-1 PRIMARILY CONSISTS OF INVERTER U2B AND MONOSTABLE MULTIVIBRATOR U3B. RESISTOR R9 AND CAPACITOR C1 (NOT SHOWN AS PART OF I-MMV-1) ISOLATES THE PRINTED CIRCUIT BOARD FROM THE POWER SUPPLY. INVERTER U2B INVERTS SRUNL SIGNAL FROM LSI-11/23 FOR INPUT TO U2B. RESISTOR R1 IS AN OUTPUT LOADING RESISTOR. MONOSTABLE MULTIVIBRATOR U3B INCREASES PULSE DURATION OF SRUNL SIGNAL BASED ON RC TIME CONSTANT PROVIDED BY RESISTOR R2 AND CAPACITOR C2. THE OUTPUT FROM U3B IS APPLIED TO X-LED-1.

⑥ (X-LED-1) RUN INDICATOR:

X-LED-1 CONSISTS OF INVERTER U2D AND LED DS1. U2D INVERTS OUTPUT OF I-MMV-1 AND APPLIES IT TO DS1. WHEN LSI-11/23 IS IN THE RUN MODE, DS1 IS ILLUMINATED.

⑦ (I-DCO-1) DC ON CIRCUITRY:

I-DCO-1 CONSISTS OF I-CMP-1 AND X-LED 2, WHICH COMBINE TO PROVIDE AN INDICATION THAT EXTERNAL +5 VDC POWER SUPPLY IS FUNCTIONING PROPERLY.

⑧ (I-CMP-1) COMPARATOR CIRCUIT:

I-CMP-1 COMPARES +5VDC OUTPUT FROM CHASSIS POWER SUPPLY WITH THE +5 VDC SENSE SIGNAL REPRESENTING THE VOLTAGE DROP ACROSS AN EXTERNALLY CONNECTED POWER BUS. POWER SUPPLY FAILURE CAUSES AN IMBALANCE MEASURED BY COMPARATOR U1A, RESULTING IN DS2 (X-LED-2) BEING EXTINGUISHED. THE +5 VDC INPUT TO U1A IS APPLIED ACROSS RESISTOR R6, POTENTIOMETER R7 AND RESISTOR R8. THE +5 VDC SENSE INPUT TO UIA IS APPLIED ACROSS RESISTORS R4 AND R5, WHICH EQUAL RESISTORS R6 AND R8. POTENTIOMETER R7 IS ADJUSTED TO EQUAL THE RESISTANCE OFFERED BY THE EXTERNALLY CONNECTED POWER BUS (VOLTAGE DROP ACROSS THE POWER BUS). CAPACITOR C3 ISOLATES THE INPUTS TO UIA. RESISTOR R3 IS AN OUTPUT LOADING RESISTOR. A LOW OUTPUT FROM U1A REPRESENTS A BALANCED CONDITION AND A HIGH OUTPUT REPRESENTS AN IMBALANCE. THE OUTPUT OF U1A IS APPLIED TO X-LED-2.

⑨ (X-LED-2) +5 VDC ON INDICATOR:

A LOW OUTPUT FROM I-CMP-1 IS INVERTED BY INVERTER U2A, ILLUMINATING LED DS2. A HIGH OUTPUT FROM I-CMP-1 REPRESENTS POWER SUPPLY FAILURE (NO CURRENT THROUGH THE EXTERNALLY CONNECTED POWER BUS) AND IS INVERTED BY U2A, EXTINGUISHING DS2.

Figure 2-9. Power Control Module Blocked Schematic Diagram and Keyed Text (Sheet 2 of 2)

2.1.1.3.12 Multiplexer Interface Assembly. - The Multiplexer Interface Assembly, 401-37170-04, interfaces the Multiplexer Circuit Card, 401-36993-03, with modems and eight-channel serial I/O circuit card channels via the digital patch panel. The schematic diagram of the multiplexer interface assembly is shown in figure 10-50.

2.1.1.3.13 Alphanumeric (A/N) On-The-Fly (OTF) Processor Circuit Card. - An intermediate logic diagram of the E-Systems A/N OTF processor is shown in figure 2-10. Each block on the intermediate logic diagram contains a circuit identifier code in the upper left-hand corner and a circled keyed text reference number in the upper right-hand corner of the block. These identifier codes and keyed text reference numbers refer to the blocked schematic diagrams provided in figure 2-12.

Data is input to and output from the A/N OTF processor via the LSI-11/23 bus. DATA/ADDRESS LINE 00-15 bits are input to the Data/Address Buffer (I-DAB-1). The contents of these 16 bits are described in table 2-6. The DATA/ADDRESS LINE bits are output to an Address Decoder (I-ADR-1) and a Control Status Register (I-CSR-1).

The address decoder contains PROM (programmable read only memory) that decodes the DATA/ADDRESS LINE 00-17 signals. The decoder determines if this particular A/N OTF processor is selected by the LSI-11/23 and initiates the selection of a particular A/N quad cache memory circuit card.

The Control Status Register (CSR) selects the desired CRT display with UNIT NUMBER 00-07 output signals. The CSR also outputs BOARD SELECT and /BOARD SELECT signals when it is determined that this particular A/N OTF processor circuit card has been selected.

The A/N OTF processor circuit card contains three individual E-Systems pico processors (EPPs): the mode pico processor, horizontal pico processor, and vertical pico processor. The mode pico processor outputs control signals (refresh, retrace, non-refresh), CACHE MEMORY READ, and WRITE CONTROL signals for use within the A/N OTF processor circuit card. The horizontal pico processor establishes and outputs CACHE ADDRESS 00-11 data bits that logically define which vertical base line address (0, 80, 160, etc.) is currently addressed. Refer to figure 2-11 for horizontal and vertical character positions on the CRT monitor.

The Refresh Control Buffer (I-RCB-1) and the Unit and Read/Write Control Buffer (I-UCB-1) output control signals to the A/N quad cache memory circuit card. They receive a /SELECT UNIT signal from A/N quad cache memory circuit card which informs the A/N OTF processor circuit card that a CRT monitor has been selected.

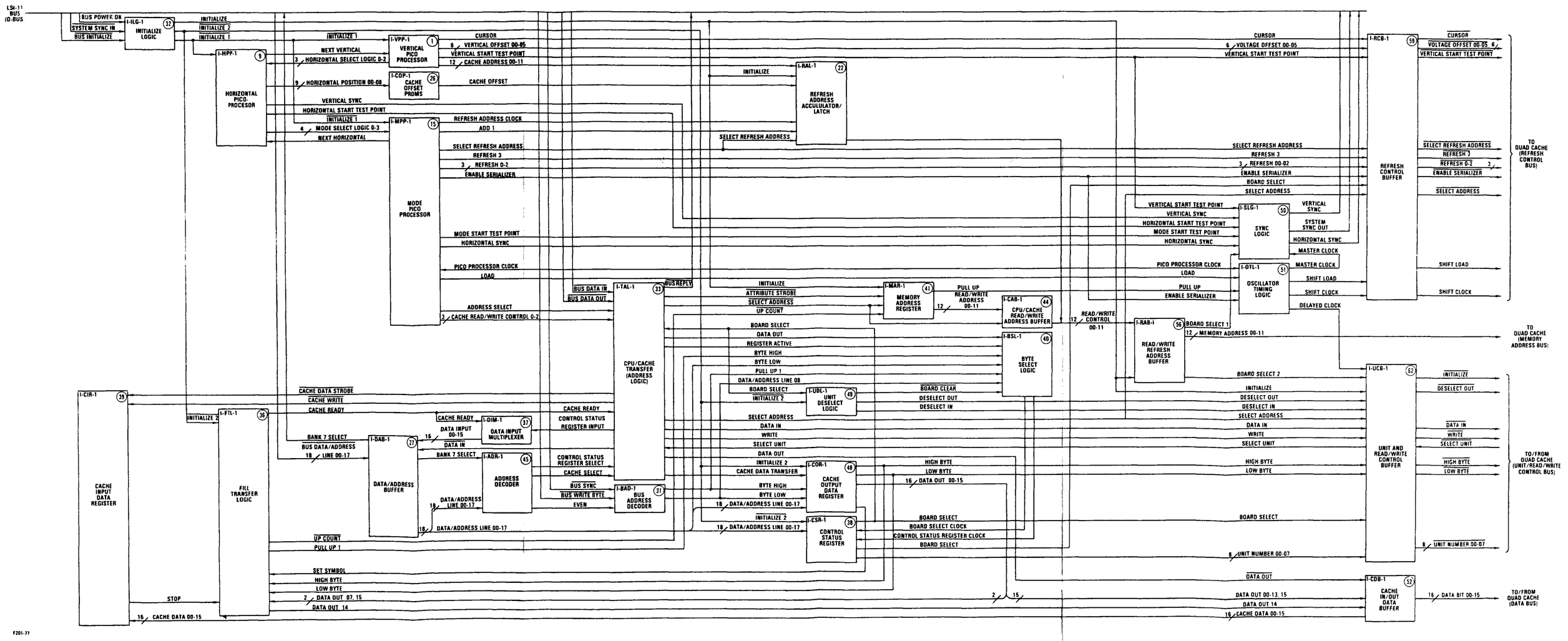

Figure 2-10. A/N OTF Processor Circuit Board Intermediate Logic Diagram

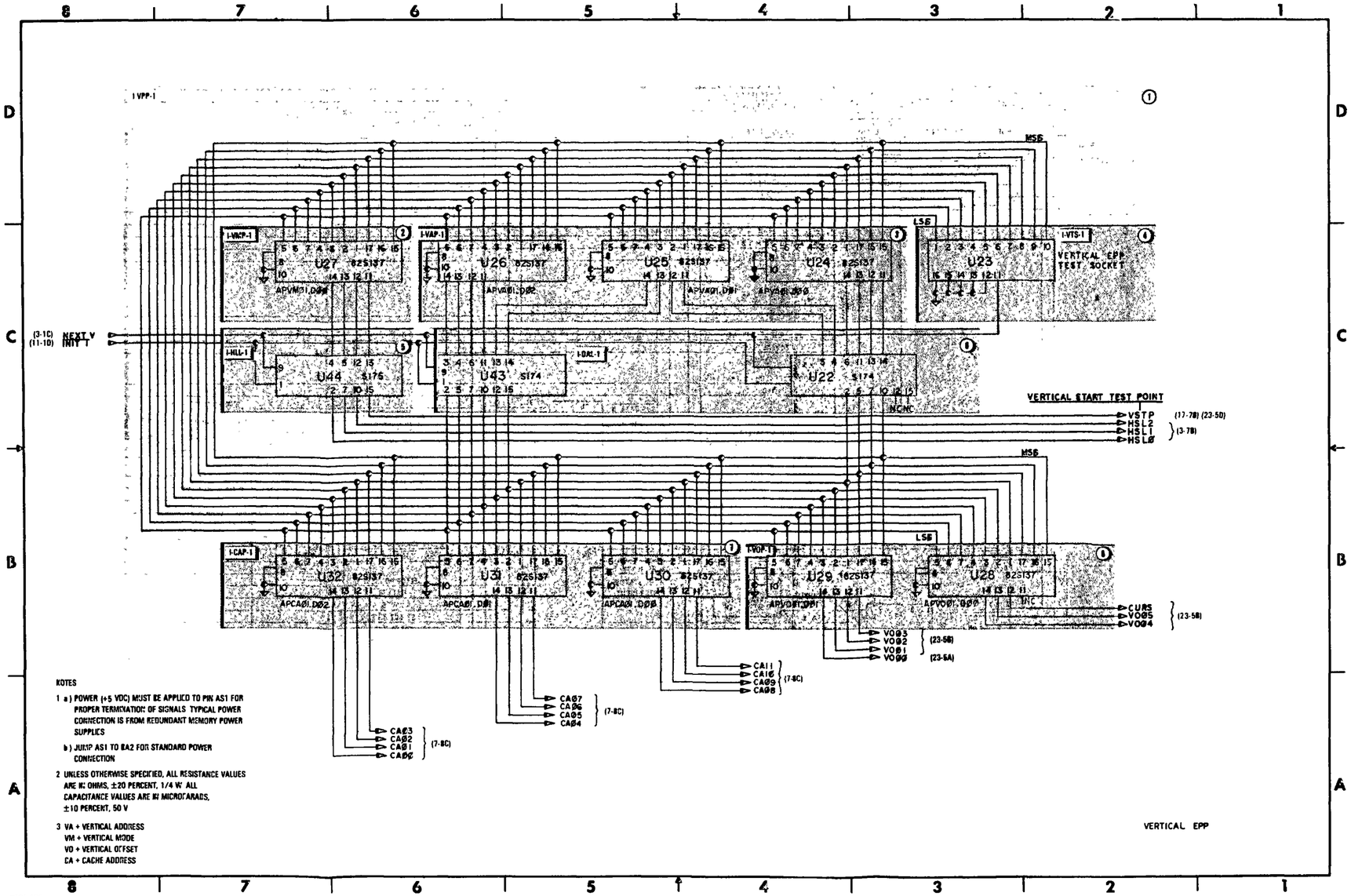

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 1 of 27)

① (I-VPP-1) VERTICAL PICO PROCESSOR:

(1) ESTABLISHES AND OUTPUTS CACHE ADDRESS DATA BITS (CA00-CA11) THAT LOGICALLY DEFINE WHICH VERTICAL BASE LINE ADDRESS (0, 80, 160, 240, ETC.) IS CURRENTLY ADDRESSED.

(2) ESTABLISHES AND OUTPUTS VERTICAL OFFSET DATA BITS TO ALLOW REFRESHING OF 20 DOT MATRIX CHARACTER LINES WHICH FORM ONE COMPLETE LINE OF CHARACTERS ON CRT MONITOR.

(3) ESTABLISHES AND OUTPUTS HORIZONTAL SELECT LOGIC SIGNALS (HSL0-2) WHICH SELECTS TYPE OF HORIZONTAL LINE (REFRESH, NON-REFRESH, RETRACE, ETC.) ADDRESSED BY I-VPP-1.

(4) ESTABLISHES AND OUTPUTS VSTP (VERTICAL START TEST POINT) SIGNAL TO SIGNIFY BEGINNING OF FRAME.

② (I-VMP-1) VERTICAL MODE PROM:

RECEIVES 10-BIT VERTICAL ADDRESS DATA AND OUTPUTS DECODED 4-BIT DATA TO I-HLL-1 (HORIZONTAL LINE LATCH). LATCHED DATA SELECTS TYPE OF HORIZONTAL LINE DESIRED (REFRESH, NON-REFRESH, VERTICAL SYNC, ETC.). U27 IS A 1K X 4 BIT PROM (PROGRAMMABLE READ-ONLY MEMORY).

③ (I-VAP-1) VERTICAL ADDRESS PROM:

OUTPUTS 10-BIT VERTICAL ADDRESSES WHICH REPRESENT ONE OF 525 LINES MAKING UP SCREEN OF CRT MONITOR. U24, U25, AND U26 ARE EACH 1K X 4 BIT PROMS. PROMS ARE INITIALIZED BY /INIT 1 (/INITIALIZE 1) SIGNAL AND ADDRESS LINE 525 DOWN TO LINE 1 (ODD-NUMBERED LINES) AND ARE THEN RESYNCHRONIZED FOR EVEN-NUMBERED LINES (INTERLACED SCANNING).

④ (I-VTS-1) VERTICAL EPP TEST SOCKET:

PROVIDES A SOCKET FOR CONNECTOR HOOK-UP OR DIRECT PROBING OF 10-BIT VERTICAL ADDRESS FOR TEST PURPOSES.

⑤ (I-HLL-1) HORIZONTAL LINE LATCH:

LATCHES 4-BIT DECODED DATA FROM I-VMP-1 (VERTICAL MODE PROM) CONTAINING HORIZONTAL SELECT LOGIC (HSL0-2) AND VERTICAL START TEST POINT (VSTP). THIS 4-BIT DATA SELECTS THE TYPE OF HORIZONTAL LINE DESIRED (REFRESH, NON-REFRESH, VERTICAL SYNC, ETC.). VSTP SIGNAL IS OUTPUT AT BEGINNING OF EACH NEW FRAME. LATCH IS CLEARED BY /INIT 1 (/INITIALIZE 1) SIGNAL AND IS CLOCKED BY NEXT V (NEXT VERTICAL) SIGNAL.

⑥ (I-DAL-1) DISPLAY ADDRESS LATCH:

LATCHES CRT MONITOR ADDRESS FROM I-VAP-1 (VERTICAL ADDRESS PROM) CONTAINING BASE LINE ADDRESS (VERTICAL LINE LOCATION OF 24 VERTICAL LINES OF CRT MONITOR) AND VERTICAL OFFSET (DOT MATRIX LINES, OF WHICH THERE ARE 20 PER BASE LINE ADDRESS). OUTPUTS ADDRESS TO VERTICAL ADDRESS BUS. LATCHES U22 AND U43 ARE CLEARED BY /INIT 1 (/INITIALIZE 1) SIGNAL AND ARE CLOCKED BY NEXT V (NEXT VERTICAL) SIGNAL.

⑦ (I-CAP-1) CACHE ADDRESS PROM:

DECODES VERTICAL ADDRESS BUS AND OUTPUTS 12-BIT CACHE ADDRESS (CA00-11) WHICH IS BASE LINE ADDRESS (VERTICAL LINE OF 24 ON CRT MONITOR CONSISTING OF 20 DOT MATRIX LINES). U30, U31 AND U32 ARE 1K X 4 BIT PROMS.

⑧ (I-VOP-1) VERTICAL OFFSET PROM:

DECODES VERTICAL ADDRESS BUS AND OUTPUTS 6-BIT VERTICAL OFFSET DATA (VO00-05) AND CURS (CURSOR) SIGNAL. VERTICAL OFFSET DATA SELECTS ONE OF 20 DOT MATRIX LINES WHICH MAKE UP LINE OF CHARACTERS. CURSOR SIGNAL IS ALWAYS OUTPUT DURING LINE 13 OF DOT MATRIX LINES TO ENABLE CURSOR TO BE PLACED THERE IF DESIRED. U28 AND U29 ARE 1K X 4 BIT PROMS.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 2 of 27)

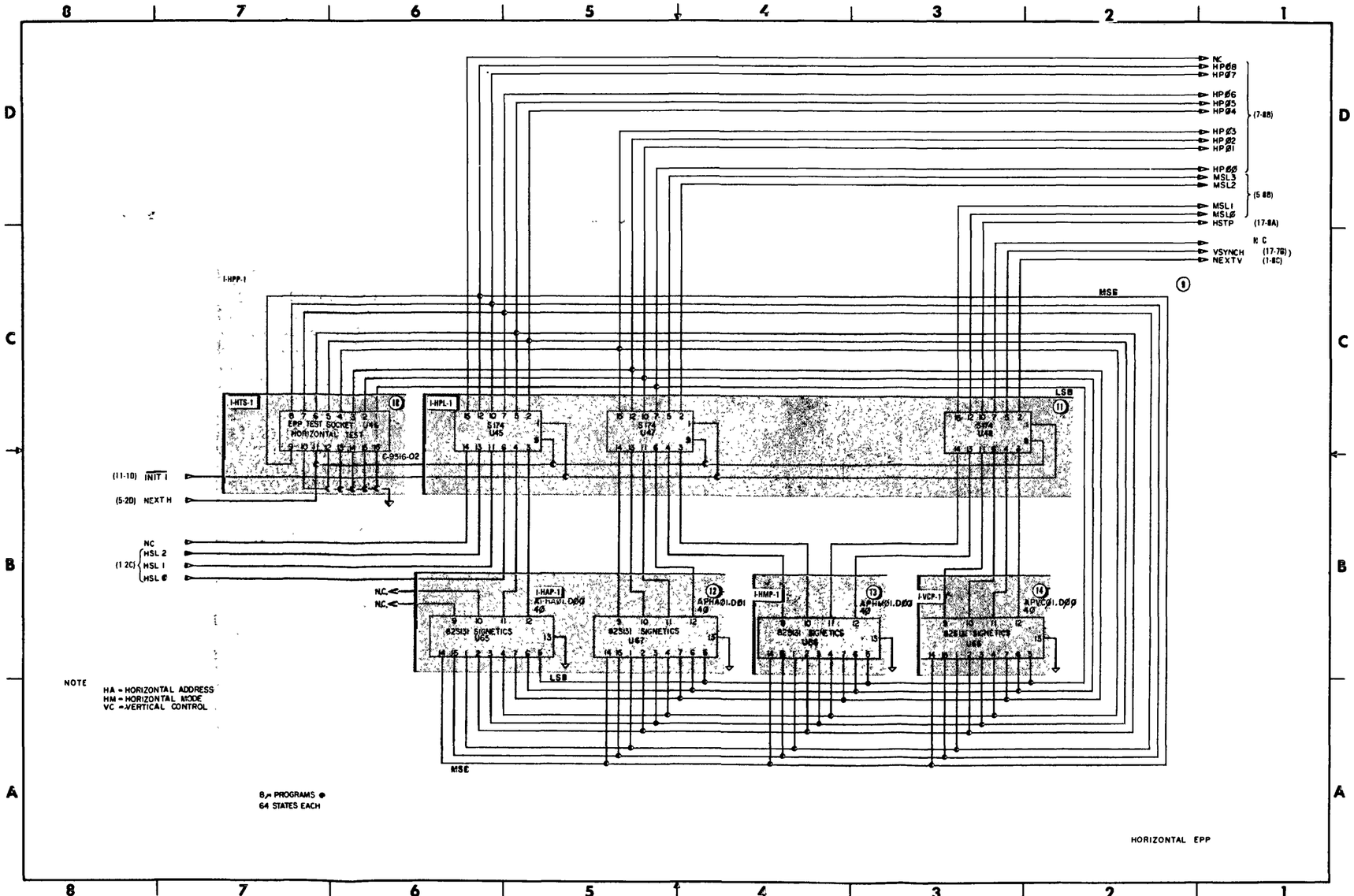

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 3 of 27)

(9) (I-HPP-1) HORIZONTAL PICO PROCESSOR:

(1) ESTABLISHES AND OUTPUTS HORIZONTAL POSITION DATA (HP00-08) FOR 80 CHARACTERS OF EACH LINE.

(2) ESTABLISHES AND OUTPUTS MODE SELECT LOGIC SIGNALS (MSL0-3) WHICH INFORM MODE PICO PROCESSOR (I-MPP-1) WHICH OPERATIONAL MODE IS DESIRED.

(3) ESTABLISHES AND OUTPUTS HSTP (HORIZONTAL START TEST POINT) WHICH IS USED FOR SYSTEM SYNCHRONIZATION.

(4) ESTABLISHES AND OUTPUTS V SYNCH (VERTICAL SYNC) SIGNAL WHICH IS USED FOR CRT MONITOR SYNCHRONIZATION.

(5) ESTABLISHES AND OUTPUTS NEXT V (NEXT VERTICAL) SIGNAL WHICH CLOCKS LATCHES ON VERTICAL PICO PROCESSOR (I-VPP-1).

(10) (I-HTS-1) HORIZONTAL EPP TEST SOCKET:

PROVIDES SOCKET FOR CONNECTOR HOOK-UP OR DIRECT PROBING OF 9-BIT HORIZONTAL ADDRESS FOR TEST PURPOSES.

(11) (I-HPL-1) HORIZONTAL PROCESSOR LATCHES:

LATCHES 9-BIT HORIZONTAL ADDRESS AND ALL OUTPUT SIGNALS FROM HORIZONTAL PROCESSOR. LATCHES ARE CLOCKED BY NEXT H (NEXT HORIZONTAL) SIGNAL FROM MODE PICO PROCESSOR (I-MPP-1).

(12) (I-HAP-1) HORIZONTAL ADDRESS PROMS:

DECODES SIX LEAST SIGNIFICANT BITS OF HORIZONTAL POSITION (HP00-05) AND OUTPUTS BITS TO LATCHES U45 AND U47 OF I-HPL-1. HORIZONTAL SELECT LOGIC SIGNALS (HSL0-2) ARE LATCHED BY U45 OF I-HPL-1 TO MAKE UP THREE MOST SIGNIFICANT BITS OF HORIZONTAL POSITION (HP06-08).

(13) (I-HMP-1) HORIZONTAL MODE PROM:

DECODES 4-BIT MODE SELECT LOGIC (MSL0-3) FROM 9-BIT HORIZONTAL ADDRESS. MSL0-3 IS LATCHED BY U47 AND U48 AND APPLIED TO MODE PICO PROCESSOR (I-MPP-1) TO SELECT DESIRED MODE OF OPERATION (REFRESH, NON-REFRESH, HORIZONTAL SYNC, ETC.).

(14) (I-VCP-1) VERTICAL CONTROL PROM:

DECODES HSTP (HORIZONTAL START TEST POINT), VSYNCH (VERTICAL SYNC) AND NEXTV (NEXT VERTICAL) SIGNALS FROM 9-BIT HORIZONTAL ADDRESS. HSTP IS OUTPUT ONCE PER LINE AND IS USED WITH VSTP (VERTICAL START TEST POINT) AND MSTP (MODE START TEST POINT) TO PROVIDE FRAME SYNCHRONIZATION. VSYNCH IS OUTPUT TO PROVIDE SYNCHRONIZATION FOR DISPLAYS. NEXTV IS OUTPUT TO PROVIDE CLOCK PULSE FOR LATCHES IN VERTICAL PICO PROCESSOR (I-VPP-1).

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 4 of 27)

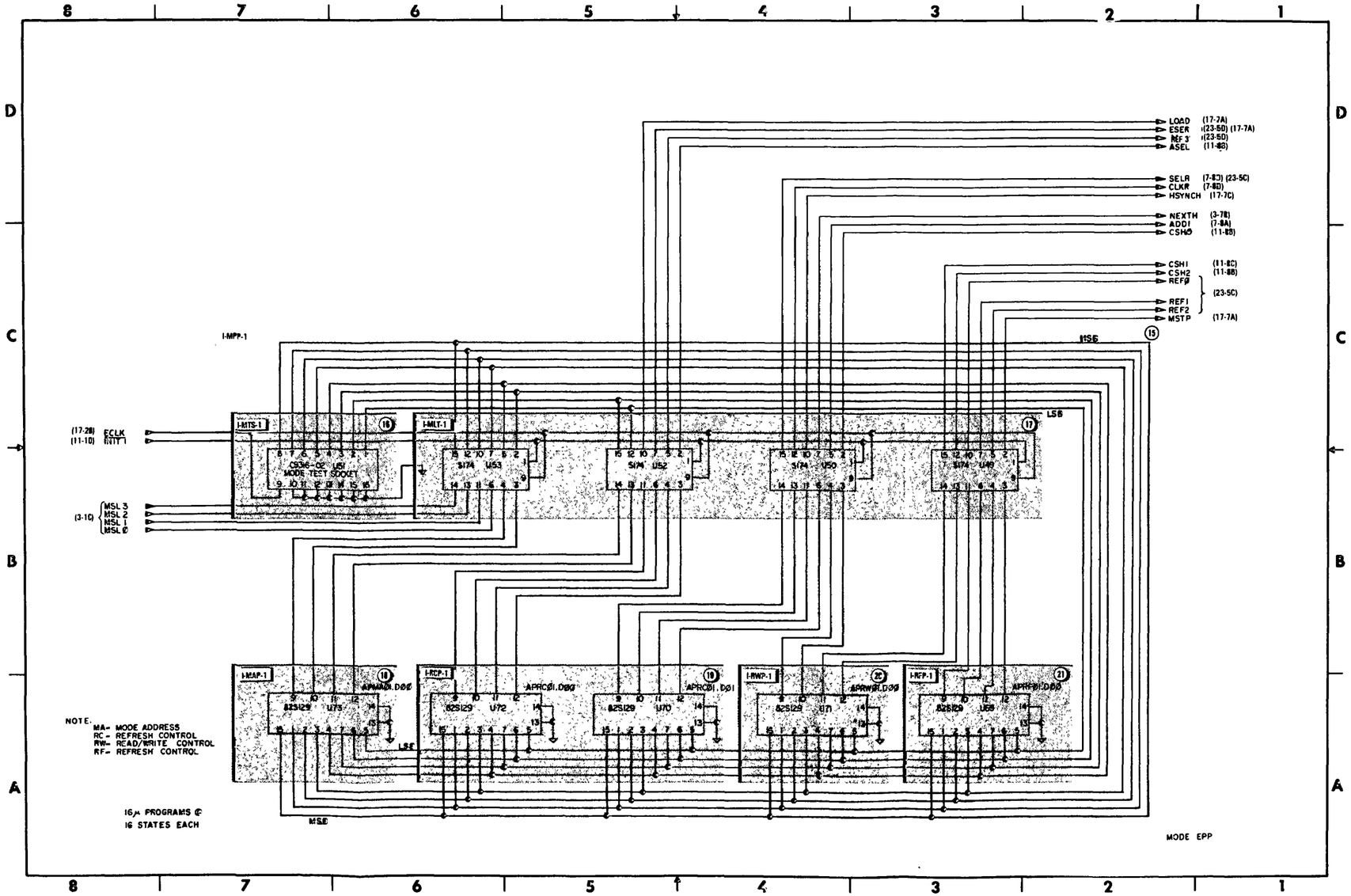

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Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 5 of 27)

(15) (I-MPP-1) MODE PICO PROCESSOR:

OUTPUTS REFRESH CONTROL SIGNALS AND CACHE READ/WRITE CONTROL SIGNALS FOR USE WITHIN OTF PROCESSOR AND QUAD CACHE. MODE SELECT LOGIC SIGNALS (MSL0-3) ARE INPUT TO I-MPP-1 FROM HORIZONTAL PICO PROCESSOR (I-HPP-1) TO INFORM MODE PICO PROCESSOR WHICH MODE OF OPERATION (REFRESH, NON-REFRESH, RETRACE, ETC.) IS DESIRED.

(16) (I-MTS-1) MODE TEST SOCKET:

PROVIDES SOCKET FOR CONNECTOR HOOK-UP OR DIRECT PROBING OF 8-BIT ADDRESS FOR TEST PURPOSES.

(17) (I-MLT-1) MODE LATCHES:

LATCHES REFRESH CONTROL SIGNALS, READ/WRITE CONTROL SIGNALS AND MODE ADDRESS WHEN CLOCKED BY ECLK (PICO PROCESSOR CLOCK). LATCHES ARE ALL CLEARED WHEN /INIT 1 SIGNAL IS APPLIED TO LATCHES IN ACTIVE LOW STATE.

(18) (I-MAP-1) MODE ADDRESS PROM:

OUTPUTS 4 LEAST SIGNIFICANT BITS OF MODE ADDRESS TO I-MLT-1 (MODE LATCHES). FOUR MOST SIGNIFICANT BITS OF MODE ADDRESS ARE INPUT FROM I-HPP-1 (HORIZONTAL PICO PROCESSOR) TO MODE LATCHES. FOUR LEAST SIGNIFICANT BITS PERFORM COUNTING OPERATION WHILE FOUR MOST SIGNIFICANT BITS SPECIFY MODE TYPE DESIRED.

(19) (I-RCP-1) READ CONTROL PROMS:

OUTPUTS 8-BITS OF READ CONTROL SIGNALS FOR REFRESH OPERATION TO I-MLT-1 (MODE LATCHES). PROMS U70 AND U72 MAKE UP I-RCP-1 AND ARE ADDRESSED BY 8-BIT MODE ADDRESS FROM I-MLT-1.

(20) I-RWP-1 (READ/WRITE CONTROL PROM):

OUTPUTS 4-BITS OF READ/WRITE CONTROL SIGNALS WHICH CONTROL READING OR WRITING OF DATA FROM OR TO LSI-11/23. U71 IS ADDRESSED BY 8-BIT MODE ADDRESS FROM I-MLT-1.

(21) (I-RFP-1) REFRESH CONTROL PROM:

OUTPUTS 4 BITS OF REFRESH CONTROL SIGNALS WHICH CONTROL REFRESH OPERATIONS. U69 IS ADDRESSED BY 8-BIT MODE ADDRESS FROM I-MLT-1.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 6 of 27)

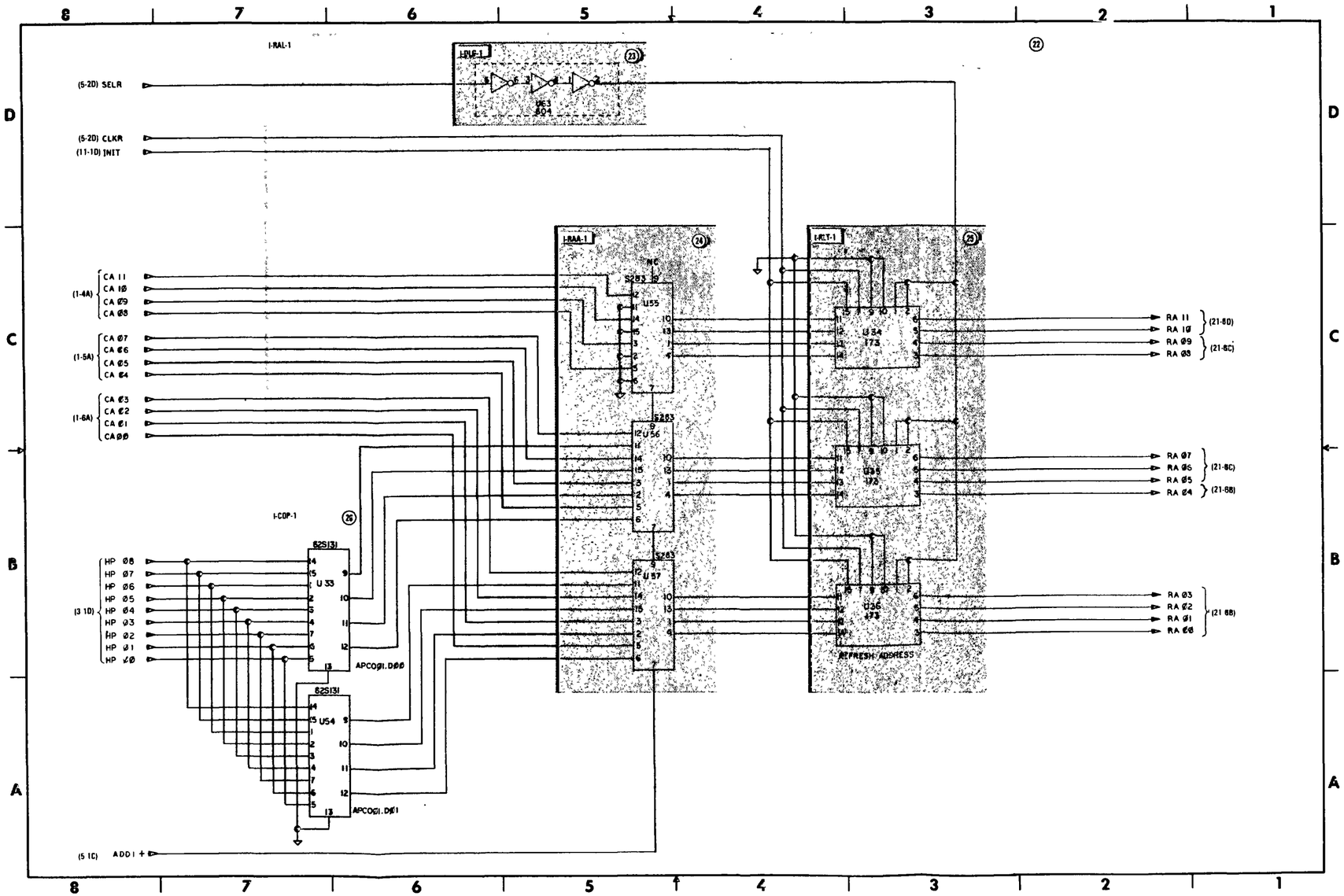

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Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 7 of 27)

(22) (I-RAL-1) REFRESH ADDRESS ACCUMULATOR/LATCH:

COMBINES 12-BIT CACHE ADDRESS (CA00-11) FROM VERTICAL PICO PROCESSOR WITH 8-BIT CACHE OFFSET FROM CACHE OFFSET PROM (I-COP-1) TO ESTABLISH REFRESH ADDRESS (RA00-11). REFRESH ADDRESS OUTPUT BY I-RAL-1 LATCHES CONTAINS 12 BITS OF DATA CONTAINING EXACT HORIZONTAL AND VERTICAL LINE COORDINATES OF CHARACTER BEING REFRESHED (0-79 HORIZONTAL; 0, 80, 160, ..., 1840 VERTICAL).

(23) (I-DLG-1) DELAY LOGIC:

PROVIDES APPROPRIATE DELAY FOR SELR (SELECT REFRESH ADDRESS) SIGNAL BY PROVIDING THREE INVERTERS IN SERIES.

(24) (I-RAA-1) REFRESH ADDRESS ACCUMULATOR:

ADDS VERTICAL AND HORIZONTAL LINE COORDINATES TO PRODUCE 12-BIT REFRESH ADDRESS. HORIZONTAL COORDINATES ARE ADDRESSED IN ODD NUMBERS FROM I-COP-1 SO THAT ADD 1 SIGNAL IS APPLIED TO I-RAA-1 TO SUPPLY EVEN HORIZONTAL ADDRESSES.

(25) (I-RLT-1) REFRESH ADDRESS LATCH:

LATCHES 12-BIT REFRESH ADDRESS FROM I-RAA-1 (REFRESH ADDRESS ACCUMULATOR). LATCHES ARE THREE-STATE AND THEIR OUTPUTS ARE ENABLED BY /SELR (/SELECT REFRESH ADDRESS) OUTPUT FROM I-DLG-1 (DELAY LOGIC) ON PINS 1 AND 2. NEW DATA IS LOADED INTO LATCH EACH TIME CLKR (REFRESH CLOCK PULSE) IS APPLIED TO PIN 7. LATCHES ARE CLEARED BY INITIALIZE (INIT) SIGNAL APPLIED AT PIN 15.

(26) (I-COP-1) CACHE OFFSET PROMS:

DECODE HORIZONTAL POSITION DATA (HP00-08) AND ESTABLISH 8-BIT HORIZONTAL CHARACTER ADDRESS FOR ODD-NUMBERED HORIZONTAL COORDINATES (1-79). THE EVEN ADDRESSES ARE THE SUM OF THE ODD ADDRESSES AND ADD1+.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 8 of 27)

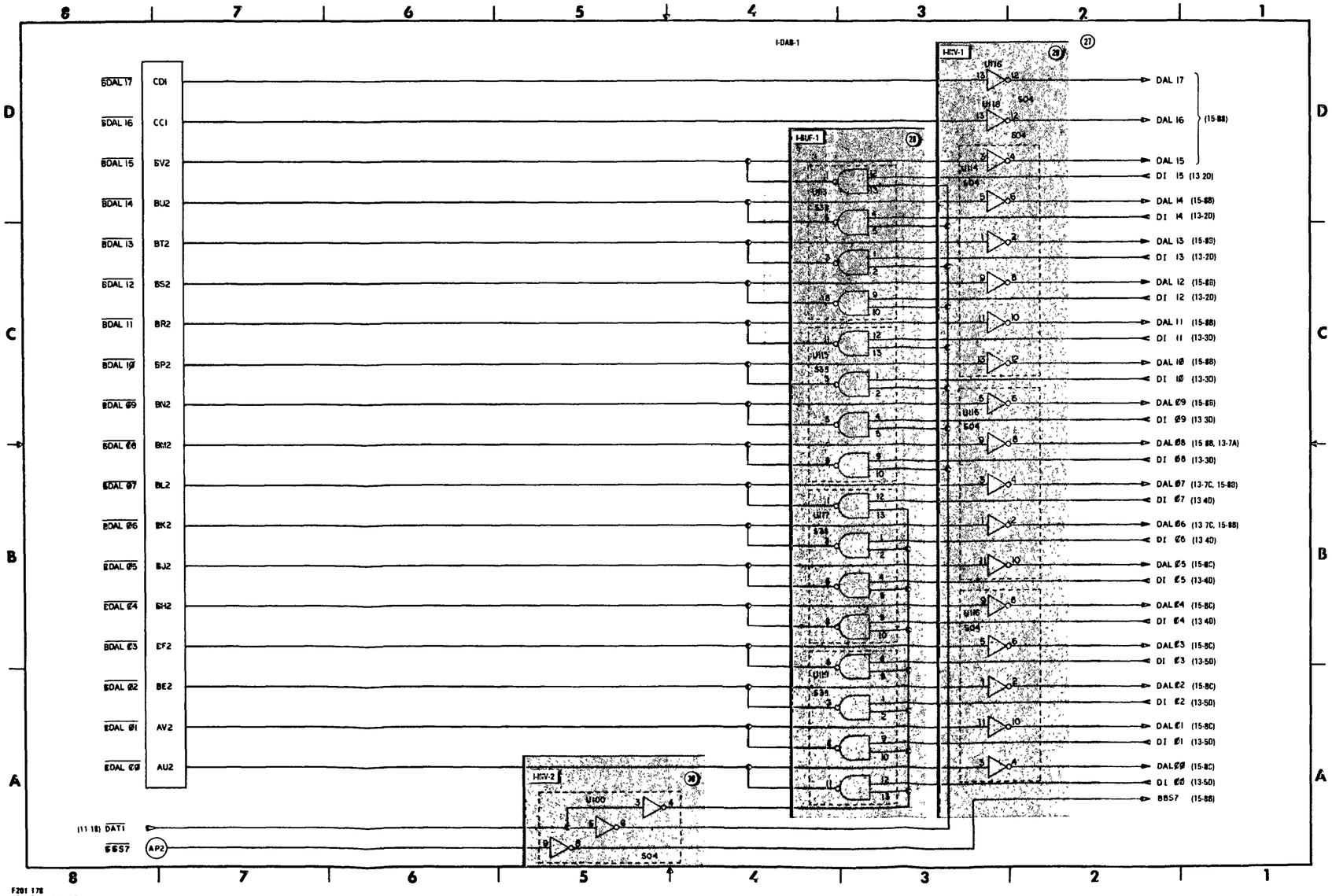


Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 9 of 27)

(27) (I-DAB-1) DATA/ADDRESS BUFFER:

(1) RECEIVES AND INVERTS 18-BIT DATA/ADDRESS LINES (DAL00-17) FROM LSI-11/23 BUS.

(2) OUTPUTS 16-BIT DATA INPUT (DI00-15) FROM OTF PROCESSOR TO LSI-11/23 BUS.

(28) (I-BUF-1) BUFFERS:

INVERTS AND BUFFERS DATA INPUTS (DI00-15) FROM OTF PROCESSOR TO LSI-11/23 BUS. /DATI (/DATA INPUT) SIGNAL IS INVERTED BY I-INV-2 TO ENABLE BUFFERS TO OUTPUT DATA WHEN DATA INPUT TO LSI-11/23 BUS IS DESIRED.

(29) (I-INV-1) INVERTERS:

INVERTS AND BUFFERS /BUS DATA/ADDRESS LINES (/BDAL00-17) FROM LSI-11/23 BUS TO OTF PROCESSOR.

(30) (I-INV-2) INVERTERS:

TWO INVERTERS ARE USED TO ESTABLISH DATA IN (DATI) SIGNAL TO ALLOW NAND GATES IN I-BUF-1 (BUFFERS) TO OUTPUT DATA. THIRD INVERTER IS USED TO INVERT /BUS BANK 7 SELECT SIGNAL (/BBS7) FROM LSI-11/23 BUS TO POSITIVE LOGIC LEVEL (BBS7).

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 10 of 27)

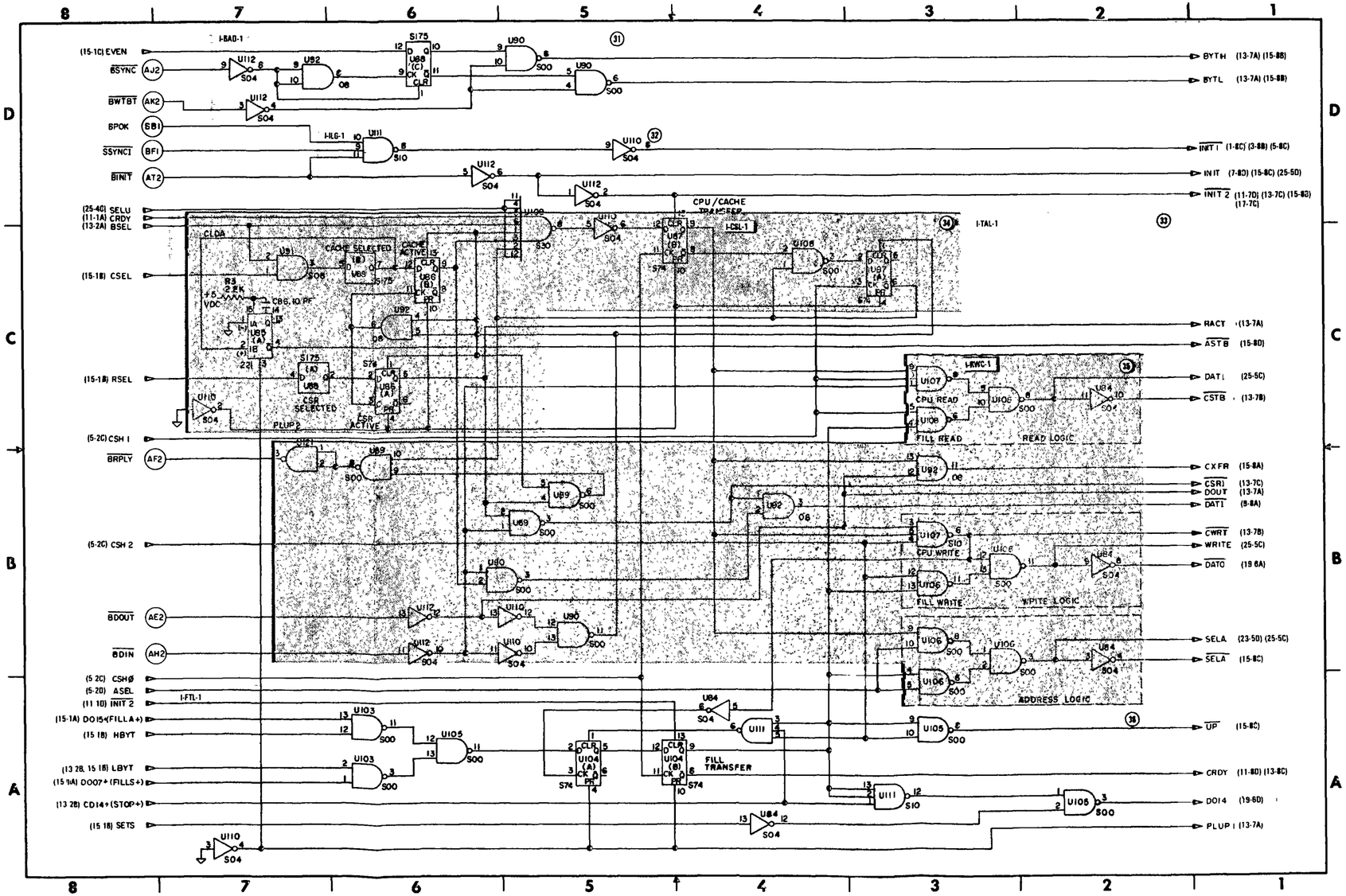


Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 11 of 27)

(31) (I-BAD-1) BUS ADDRESS DECODER:

DETERMINES WHETHER BUS ADDRESS FROM THE BUS MASTER IS (1) AN EVEN-NUMBERED WORD ADDRESS, (2) AN EVEN-NUMBERED LOW BYTE ADDRESS, OR (3) AN ODD-NUMBERED HIGH BYTE ADDRESS. EVEN SIGNAL TO D INPUT OF FLIP-FLOP U88 INDICATES LOW BYTE OR WORD ADDRESS WHEN IN ACTIVE HIGH STATE. WHEN EVEN SIGNAL IS AT LOGIC LOW, HIGH BYTE ADDRESS IS INDICATED. /BUS SYNC INDICATES THE BUS MASTER HAS PLACED ADDRESS ON BUS WHEN IN ACTIVE LOW STATE. INVERTER U112 PIN 8 INVERTS /BSYNC SIGNAL TO PROVIDE CLOCK CLEAR SIGNALS FOR FLIP-FLOP U88. U92 PROVIDES BUFFERED DELAY BETWEEN CLEAR AND CLOCK SIGNALS TO FLIP-FLOP U88. /BUS WRITE BYTE (/BWTBT) SIGNAL INDICATES LOW OR HIGH BYTE ADDRESS WHEN IN ACTIVE LOW STATE OR WORD ADDRESS WHEN IN HIGH STATE. NAND GATE U90 LOGICALLY DETERMINES WHETHER LOW BYTE ADDRESS, HIGH BYTE ADDRESS, OR WORD ADDRESS IS ON BUS. BOTH BYTH (BYTE HIGH) AND BYTL (BYTE LOW) SIGNALS ARE OUTPUT IN HIGH LOGIC STATE TO SIGNIFY WORD ADDRESS.

(32) (I-ILG-1) INITIALIZE LOGIC:

ESTABLISHES AND OUTPUTS INITIALIZE SIGNALS /INIT 1, INIT, AND /INIT 2. THESE SIGNALS ARE USED TO INITIALIZE COUNTERS, LATCHES, ETC. WITHIN OTF PROCESSOR. NAND GATE U111 PROVIDES LOGICAL OR FUNCTION FOR SIGNALS BPOK (BUS POWER OK), /SSYNCI (/SYSTEM SYNC INPUT), AND /BINIT (/BUS INITIALIZE). WHEN AC POWER IS LOST (/BPOK), SYSTEM SYNC FROM OTF PROCESSOR IS OUTPUT (/SSYNCI), OR BUS IS MANUALLY INITIALIZED FROM LSI- 11/23 (/BINIT), /INITIALIZE 1 SIGNAL IS OUTPUT TO INITIALIZE PICO PROCESSORS. /BINIT SIGNAL ALSO OUTPUTS INITIALIZE 1 AND /INITIALIZE 2 SIGNALS TO INITIALIZE CIRCUITS ON OTF PROCESSOR OTHER THAN PICO PROCESSORS.

(33) (I-TAL-1) CPU/CACHE TRANSFER ADDRESS LOGIC:

(1) PROVIDES LOGIC TO SELECT CONTROL STATUS REGISTER (CSR) AND CACHE MEMORY ASSOCIATED WITH OTF PROCESSOR WHEN ADDRESSED BY LSI-11/23.

(2) PROVIDES READ/WRITE CONTROL WITH HANDSHAKING BETWEEN OTF PROCESSOR AND LSI-11/23.

(34) (I-CSL-1) CACHE/CSR SELECT LOGIC:

SELECTS CONTROL STATUS REGISTER AND CACHE MEMORY FOR OTF PROCESSOR WHEN ADDRESSED BY LSI-11/23 AND ESTABLISHES A CPU/CSR OR CPU/CACHE TRANSFER OF DATA. CPU/CACHE TRANSFER OF DATA IS ALLOWED WHEN EVERY INPUT TO NAND GATE U109 IS AT HIGH LOGIC LEVEL. THESE HIGH INPUTS INCLUDE THE FOLLOWING:

(1) SELU (SELECT UNIT) - INDICATES THAT UNIT (CRT MONITOR) HAS BEEN SELECTED.

(2) CRDY (CACHE READY) - INDICATES THAT CACHE MEMORY IS READY TO ACCEPT DATA.

(3) BSEL (BOARD SELECT) - OTF PROCESSOR HAS BEEN ADDRESSED BY LSI-11/23.

(4) /B DOUT (/BUS DATA OUT) OR /BDIN (/BUS DATA IN) IS IN ACTIVE LOW STATE INDICATING THAT DATA IS READY FOR INPUT FROM LSI-11/23.

(5) CACHE MEMORY HAS BEEN SELECTED AND ACTIVATED.

(6) CPU/CACHE TRANSFER CIRCUIT IS READY TO ACCEPT DATA.

A REGISTER ACTIVE (RACT) SIGNAL IS OUTPUT FROM U86 PIN 5 (CSR ACTIVE REGISTER) TO INDICATE TO OTHER CIRCUITS WITHIN OTF PROCESSOR THAT CSR HAS BEEN SELECTED AND IS IN USE. /ADDRESS STROBE (/ASTB) SIGNAL IS OUTPUT FROM U85 PIN 4 TO ALLOW ADDRESSES FROM LSI-11/23 TO BE SENT TO CACHE MEMORY DURING CPU/CACHE TRANSFERS.

(35) (I-RWC-1) READ/WRITE CONTROL LOGIC:

ESTABLISHES SIGNALS TO PROVIDE READING, WRITING, AND ADDRESSING OF DATA TO AND FROM LSI-11/23. /BDOUT (/BUS DATA OUT) IS INPUT FROM BUS MASTER TO INFORM OTF PROCESSOR THAT DATA IS AVAILABLE ON LSI-11/23 BUS FOR INPUT TO OTF PROCESSOR. /BDIN (/BUS DATA IN) IS INPUT FROM BUS MASTER TO INFORM OTF PROCESSOR THAT BUS MASTER IS READY TO ACCEPT DATA FROM OTF PROCESSOR. /BDOUT AND /BDIN ARE LOGICALLY COMBINED BY U110, U112, AND U90 TO FORM CONTROL SIGNAL THAT PREPARES SELECTED OTF PROCESSOR FOR CPU/CACHE DATA TRANSFER.

CACHE 0-2 (CSH0-2) SIGNALS PROVIDE SYNCHRONIZATION BETWEEN LSI-11/23 BUS TIMING AND OTF PROCESSOR TIMING (OTF SELECT, READ, AND WRITE TIMING). /SELECT ADDRESS (/SELA) OUTPUT AT PIN 4 OF U84 IS SENT TO QUAD CACHE TO ENABLE SELECTION OF RAM (RANDOM ACCESS MEMORY) FOR PARTICULAR ADDRESSED DISPLAY.

(36) (I-FTL-1) FILL TRANSFER LOGIC:

CREATES CONTROL SIGNALS TO ALLOW FILL OPERATION TO BE PERFORMED ON CRT MONITOR. /INIT 2 (/INITIALIZE 2) SIGNAL IS INPUT TO I-FTL-1 TO CREATE INITIALIZATION OF FILL FUNCTION. FILL TRANSFER IS ESTABLISHED AT PIN 9 OF U104 WHEN ONE OF FOLLOWING IS PRESENT:

(1) DO 15 (DATA OUT 15), ALSO REFERRED TO AS FILL ATTRIBUTE, IS AT LOGIC HIGH AND HBYT (HIGH BYTE) IS AT LOGIC HIGH.

(2) DO 07, ALSO REFERRED TO AS FILL SYMBOL, IS AT LOGIC HIGH AND LBYT (LOW BYTE) IS AT LOGIC HIGH.

CD14 (CACHE DATA 14), ALSO REFERRED TO AS STOP BIT, IS INPUT TO I-FTL-1 (FILL TRANSFER LOGIC) TO HALT FILL OPERATION. SET STOP (SETS) IS INPUT TO U84 PIN 13 FROM LSI-11/23 TO WRITE THE STOP BIT IN CACHE MEMORY. /UP (/UP COUNT) IS OUTPUT TO INCREMENT CPU/CACHE READ/WRITE ADDRESS COUNTER (I-CAC-1) FOR ADDRESSING DURING FILL OPERATIONS. CACHE READY (CRDY) IS OUTPUT FOR PURPOSE OF INFORMING OTF PROCESSOR AND LSI-11/23 THAT FILL OPERATION HAS BEEN COMPLETED AND CACHE MEMORY IS READY TO RECEIVE DATA. DATA OUT 14 (DO14) IS STOP BIT WHICH IS SENT TO QUAD CACHE MEMORY. DO14 IS WRITTEN TO THE QUAD CACHE MEMORY DURING A CPU/CACHE TRANSFER OR WHEN THE STOP BIT IS ENCOUNTERED DURING THE READ CYCLE OF A FILL. U110 PIN 4 PROVIDES A HIGH LOGIC LEVEL FOR USE WITHIN OTF PROCESSOR.

Figure 2-12. A/H OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 12 of 27)

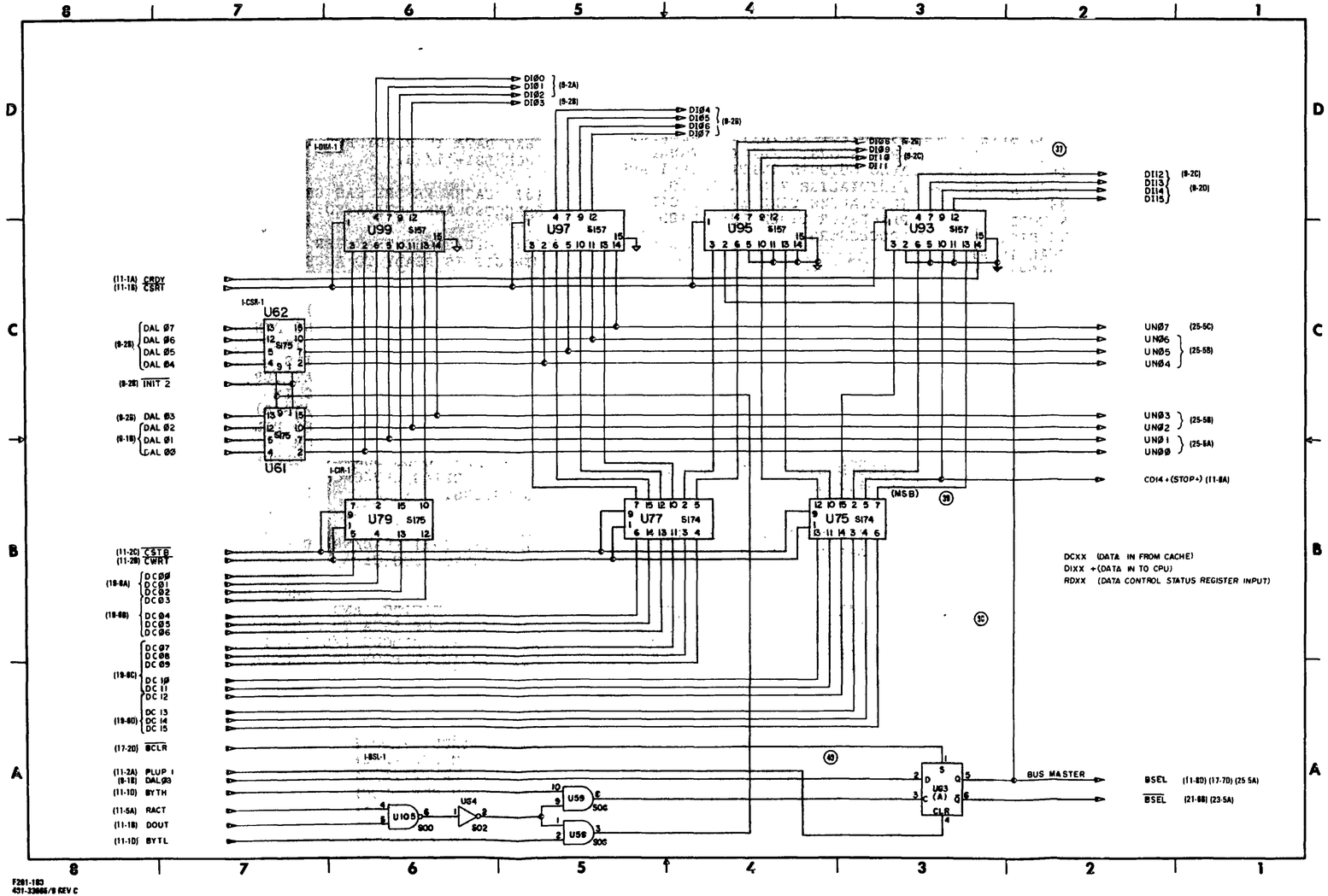


Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 13 of 27)

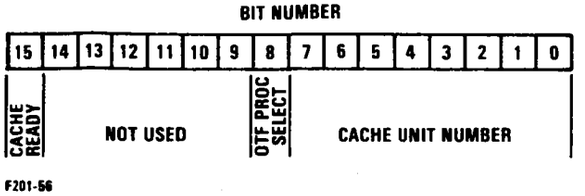
(37) (I-DIM-1)DATA INPUT MULTIPLEXER:

PROVIDES BUS MASTER WITH 16-DATA BITS WHICH CONTAIN EITHER: (1) CACHE DATA OUTPUT FROM I-CIR-I (CACHE INPUT DATA REGISTER) OR (2) UNIT NUMBER (CRT MONITOR SELECTED), BOARD SELECT BIT, AND CACHE READY BIT FROM I-CSR-1 (CONTROL STATUS REGISTER). THE TYPE OF DATA SELECTED FOR OUTPUT BY THE MULTIPLEXER IS CONTROLLED BY CSRI (CONTROL STATUS REGISTER INPUT) SIGNAL TO PIN1 OF U93, U95, U97, AND U99. WHEN CSRI IS AT A HIGH LOGIC LEVEL, DATA IS SELECTED FROM I-CIR-1. WHEN CSRI IS AT A LOW LOGIC LEVEL, DATA IS SELECTED FROM I-CSR-1.

(38) (I-CSR-1) CONTROL STATUS REGISTER:

OUTPUTS 10-BITS OF DATA IN FORMAT SHOWN BELOW:

CONTROL STATUS REGISTER (CSR) FORMAT



BITS 0-7 OF CONTROL STATUS REGISTER ARE OUTPUT FROM U61 AND U62 LATCHES AND ARE LABELED UN00-07 (UNIT NUMBER 00-07). THESE 8-BITS SPECIFY DISPLAY UNIT DESIRED BY LSI-11/23. BIT 8 IS OUTPUT FROM U83A PIN 5 AND IS LABELED BSEL (BOARD SELECT). THIS SIGNAL ALLOWS SELECTION OF APPROPRIATE OTF PROCESSOR BY LSI-11/23. BIT-15 IS OUTPUT FROM I-FTL-1, U104 (B) PIN 8 AND IS LABELED CRDY (CACHE READY). CRDY IS USED TO ALLOW DATA TRANSFERS FROM LSI-11/23 TO CACHE MEMORY.

(39) (I-CIR-1) CACHE INPUT DATA REGISTER:

OUTPUTS 16-BITS OF CACHE DATA (DC 00-15) TO I-DIM-1 (DATA INPUT MULTIPLEXER) FOR OUTPUT TO LSI-11/23. REGISTERS U75, U77, AND U79 ARE CLEARED WITH /CWRT (/CACHE WRITE) SIGNAL FROM I-TAL-1 (TRANSFER ADDRESS LOGIC). REGISTERS ARE CLOCKED WITH /CSTB (/CACHE STROBE) SIGNAL FROM I-TAL-1.

(40) (I-BSL-1) BYTE SELECT LOGIC:

PROVIDES CLOCK PULSES FOR I-CSR-1 (CONTROL STATUS REGISTER). ONE CLOCK PULSE IS INPUT TO PIN 9 OF U61 AND U62 ALLOWING INPUT OF UNIT NUMBER. THE OTHER CLOCK PULSE IS APPLIED TO PIN3 OF U83(A) AND ALLOWS THE OTF BOARD TO BE SELECTED OR DESELECTED. OUTPUT OF BSEL (BOARD SELECT) SIGNAL OCCURS WHEN DAL08) (DATA/ADDRESS LINE 08) IS AT HIGH LOGIC LEVEL. U59 PIN 3 OUTPUTS CLOCK PULSE FOR REGISTERS CONTAINING UNIT NUMBER. THIS CLOCK OUTPUT CAN ONLY GO TO HIGH LOGIC LEVEL WHEN FOLLOWING SIGNALS ARE HIGH:

(1) RACT (CSR REGISTER ACTIVE)
(2) DOUT (DATA OUT)
(3) BYTL (BYTE LOW)

WORD ADDRESS OR LOW BYTE ADDRESS WITH RACT AND DOUT HIGH WILL CAUSE UNIT NUMBER TO BE LATCHED INTO I-CSR-1. U59 PIN 8 OUTPUTS CLOCK PULSE FOR BOARD SELECT (BSEL) AND /BOARD SELECT (/BSEL) SIGNAL OUTPUT FROM U83(A). THIS CLOCK OUTPUT CAN ONLY GO TO HIGH LOGIC LEVEL WHEN THE FOLLOWING SIGNALS ARE HIGH:

(1) RACT (CSR REGISTER ACTIVE)
(2) DOUT (DATA OUT)
(3) BYTH (BYTE HIGH)

OTF PROCESSOR BOARD CAN ONLY BE SELECTED WHEN HIGH LOGIC CLOCK PULSE IS INPUT TO U83(A) AND PIN 2 OF U83(A) GOES HIGH (DAL08).

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 14 of 27)

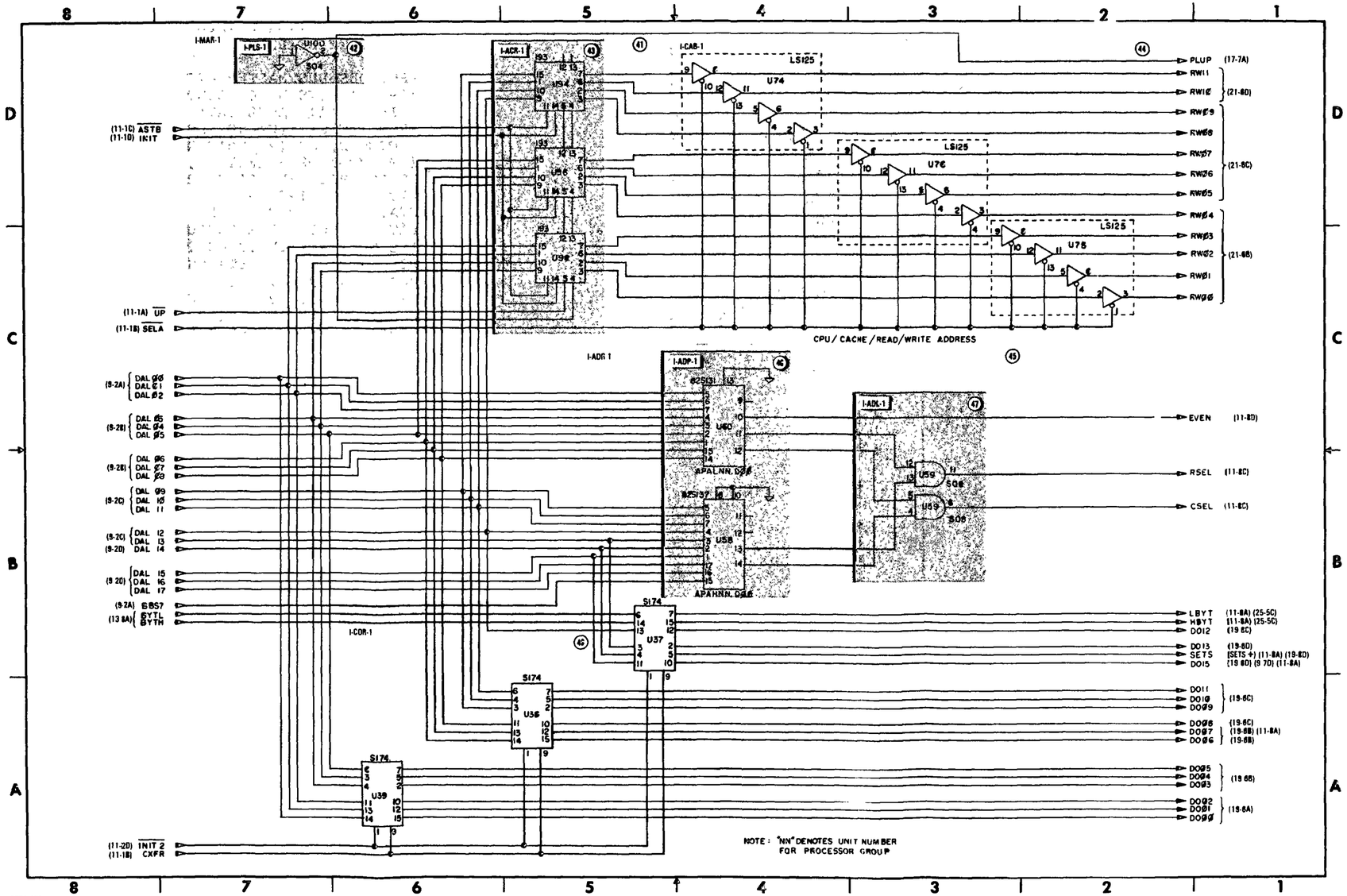


Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 15 of 27)

(41) (I-MAR-1) MEMORY ADDRESS REGISTER:

OUTPUTS 12-BIT READ/WRITE ADDRESS FROM LSI-11/23 TO SELECTED QUAD CACHE.

(42) (I-PLS-1) POSITIVE LOGIC SUPPLY:

PROVIDES CONSTANT HIGH LEVEL LOGIC SUPPLY BY USING INVERTER U100 TO INVERT COMMON SIGNAL.

(43) (I-ACR-1) ADDRESS COUNTER/REGISTER:

DURING FILL OPERATION THIS CIRCUIT IS USED TO INCREMENT ADDRESSES FROM INITIAL START ADDRESS FROM LSI-11/23 UNTIL STOP BIT IS ENCOUNTERED. DURING NON-FILL OPERATION, THIS CIRCUIT IS USED AS REGISTER TO OUTPUT 12-BIT READ/WRITE ADDRESS TO QUAD CACHE FROM BUS MASTER. /ASTB (/ADDRESS STROBE) IS INPUT AS CLOCK PULSE TO LOAD A NEW READ/WRITE ADDRESS. THAT ADDRESS IS THEN OUTPUT TO I-ABF-1 (ADDRESS BUFFERS). /UP (/UP COUNT) IS A CLOCK TO INCREMENT THE ADDRESS COUNTER DURING FILL OPERATION.

(44) (I-CAB-1) CACHE READ/WRITE ADDRESS BUFFERS:

BUFFERS 12-BIT READ/WRITE ADDRESS FROM LSI-11/23 TO QUAD CACHE BY USING THREE-STATE BUFFERS. READ/WRITE 00-11 (RW00-11) DATA CAN ONLY BE OUTPUT TO QUAD CACHE WHEN /SELA (/SELECT ADDRESS) SIGNAL IS AT ACTIVE LOW LEVEL, ENABLING THREE-STATE BUFFERS.

(45) (I-ADR-1) ADDRESS DECODER:

DECODES 18-BIT DATA/ADDRESS LINES (DAL00-17) AND BBS7, AND OUTPUTS EVEN, RSEL, AND CSEL SIGNALS. EVEN OUTPUT IS USED TO SIGNIFY THAT ADDRESS INPUT IS EITHER LOW BYTE OR WORD ADDRESS WHEN AT HIGH LOGIC LEVEL, OR HIGH BYTE ADDRESS WHEN AT LOW LOGIC LEVEL. RSEL (CSR SELECT), WHEN AT HIGH LOGIC LEVEL, SELECTS THE CONTROL STATUS REGISTER ON PARTICULAR OTF PROCESSOR. CSEL (CACHE SELECT), WHEN AT HIGH LOGIC LEVEL, SIGNIFIES THAT QUAD CACHE IS BEING ACCESSED.

(46) (I-ADP-1) ADDRESS DECODER PROMS:

DECODES 18-BIT DATA/ADDRESS LINES (DAL00-17) AND OUTPUTS PROGRAMMED DATA FOR EACH ADDRESS. U60 IS UNIQUE FOR EACH OTF PROCESSOR AND SELECTS OTF PROCESSOR WHEN PARTICULAR ADDRESS IS INPUT TO PROM U60.

(47) (I-ADL-1) ADDRESS DECODER LOGIC:

ACCEPTS 4-BIT INPUT FROM PROMS U58 AND U60 OF I-ADP-1 (ADDRESS DECODER PROMS) AND LOGICALLY ENABLES OR DISABLES CSR AND CACHE MEMORY TO BE SELECTED.

(48) (I-COR-1) CACHE OUTPUT DATA REGISTER:

OUTPUTS 16-BIT DATA (DAL00-15), LBYT (LOW BYTE), AND HBYT (HIGH BYTE) SIGNALS TO SELECTED QUAD CACHE. /INIT 2 (/INITIALIZE 2) SIGNAL IS USED TO CLEAR REGISTER. CXFR (CACHE TRANSFER) SIGNAL IS USED TO CLOCK REGISTERS AND STORE DATA TO BE WRITTEN FROM BUS MASTER TO ADDRESSED CACHE MEMORY LOCATIONS.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 16 of 27)

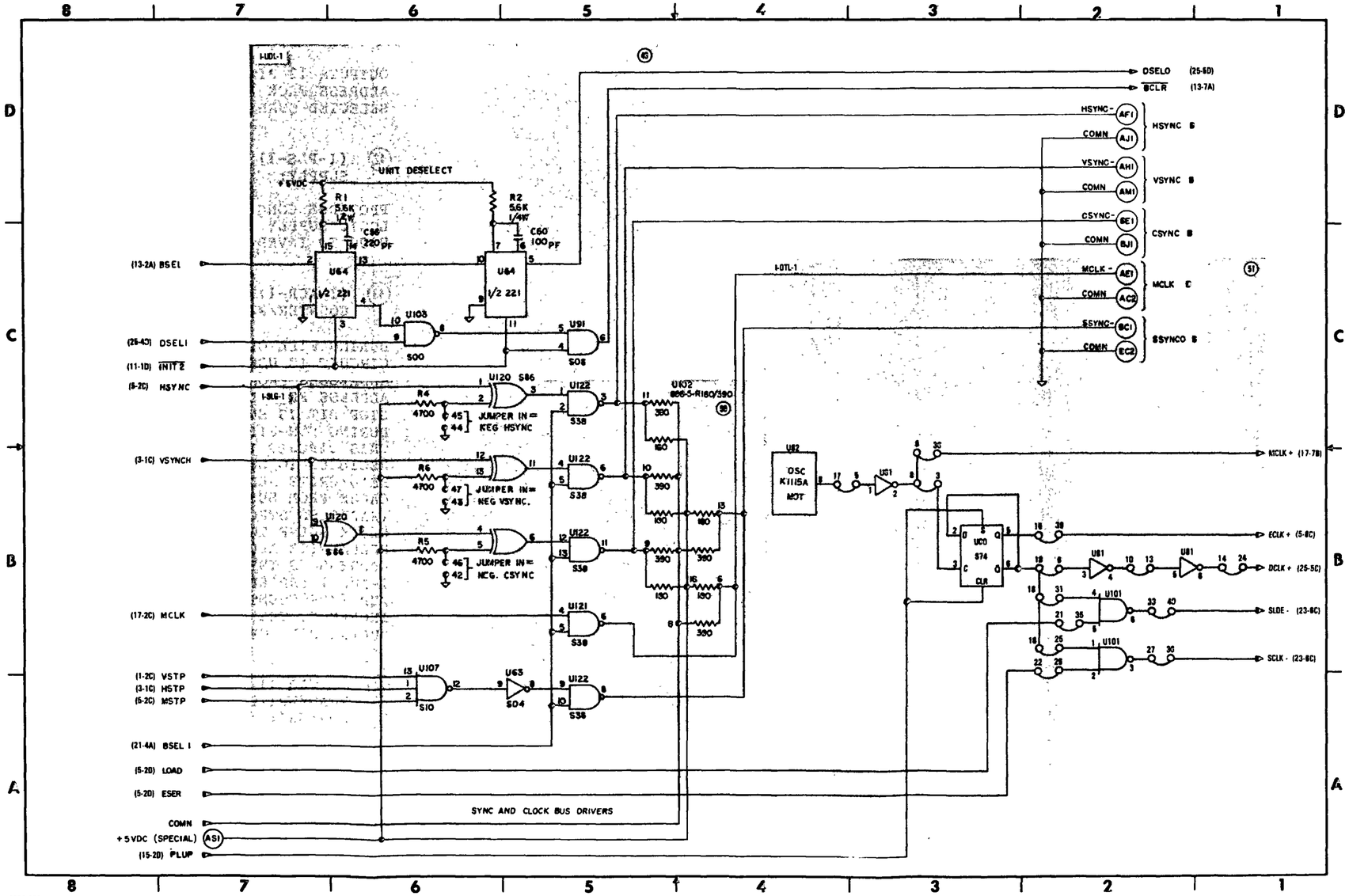


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Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 17 of 27)

(49) (I-UDL-1) UNIT DESELECT LOGIC:

PROVIDES DSELO (DESELECT OUT) AND BCLR (BOARD CLEAR) SIGNALS TO ENSURE THAT ONLY ONE OTF PROCESSOR ON THE ALPHANUMERICS BUS IS SELECTED BY LSI-11/23. U64 PROVIDES TWO MONOSTABLE MULTIVIBRATORS WHICH PROVIDE PULSES WHEN OTF PROCESSOR IS SELECTED WHICH PREVENT BOARD FROM BEING DESELECTED. DSELI (DESELECT IN) IS INPUT ALONG WITH /Q (PIN 4) OUTPUT OF U64 AND DSELI IS AT HIGH LEVEL. LOW OUTPUT AT PIN 8 OF U103 WILL CAUSE U91 PIN 6 TO OUTPUT LOW LOGIC LEVEL LABELED /BCLR (/BOARD CLEAR) WHICH WILL DESELECT OTF PROCESSOR. BCLR IS OUTPUT WHEN PIN 6 OF U91 IS A LOW LEVEL CAUSED BY EITHER A LOW LEVEL INITIALIZE 2 (INIT2) SIGNAL OR A LOW LEVEL OUTPUT FROM U103 PIN8. DESELO (DESELECT OUT) IS OUTPUT BY U64 PIN 5 AND SERVES TO DESELECT ALL OTF PROCESSORS EXCEPT ONE DESIRED.

(50) (I-SLG-1) SYNC LOGIC:

PROVIDES HORIZONTAL SYNC (HSYNC B) AND VERTICAL SYNC (VSYNC B) FOR USE BY CRT MONITOR FOR SYNCHRONIZATION PURPOSES. PROVIDES SYSTEM SYNC OUT (SSYNCO B) WHICH IS CONNECTED TO EACH OTF PROCESSOR. JUMPERS ARE INSTALLED BETWEEN POINTS 44 AND 45, 43 AND 47, AND 42 AND 46. C SYNC B (COMPOSITE SYNC) AND MCLK B (MASTER CLCOK) OUTPUT SIGNALS ARE NOT USED IN MODEL 1 SYSTEM. HYSNC (HORIZONTAL SYNC) IS APPLIED TO PIN 1 OF EXCLUSIVE-OR GATE U120 AND, BECAUSE PIN 2 IS ALWAYS AT LOGIC LOW, PIN 3 OF U120 IS ALWAYS BUFFERED REPLICA OF HSYNC. HYSNC IS THEN INPUT TO PIN 1 OF U122 WHERE LOGICALLY COMBINED WITH BSEL 1 (BOARD SELECT 1) BY U122. WHEN OTF PROCESSOR IS SELECTED AND BSEL 1 IS LOGIC HIGH LEVEL, HSYNC IS INVERTED TO PROVIDE NEGATIVE HORIZONTAL SYNC OUTPUT (HYSNC B). VSYNCH (VERTICAL SYNC) IS INPUT TO I-SLG-1 IN SAME MANNER AS HSYNC AND IS OUTPUT AS NEGATIVE VERTICAL SYNC (VSYNC B). VSTP (VERTICAL START TEST POINT), HSTP (HORIZONTAL START TEST POINT), AND MSTP (MODE START TEST POINT) ARE INPUT TO U107 TO PROVIDE SYSTEM SYNC OUT (SSYNCO B) SIGNAL WHEN EACH OF THE THREE SIGNALS IS AT LOGIC HIGH. SYSTEM SYNC SIGNAL IS USED TO KEEP ALL OTF PROCESSORS IN MODEL 1 SYSTEM IN SYNCHRONIZATION.

(51) (I-OTL-1) OSCILLATOR TIMING LOGIC:

PROVIDES THE FOLLOWING TIMING SIGNALS FROM 32.76 MHZ OSCILLATOR (U82) FOR USE WITHIN OTF PROCESSOR:

(1) MCLK (MASTER CLOCK)
(2) DCLK (DELAYED CLOCK)
(3) ECLK (PICO PROCESSOR CLOCK)
(4) SCLK (SHIFT CLOCK)
(5) SLDE (SHIFT LOAD)

STRAPPING OPTIONS ARE WIRED AS SHOWN ON BLOCKED SCHEMATIC DIAGRAM.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 18 of 27)

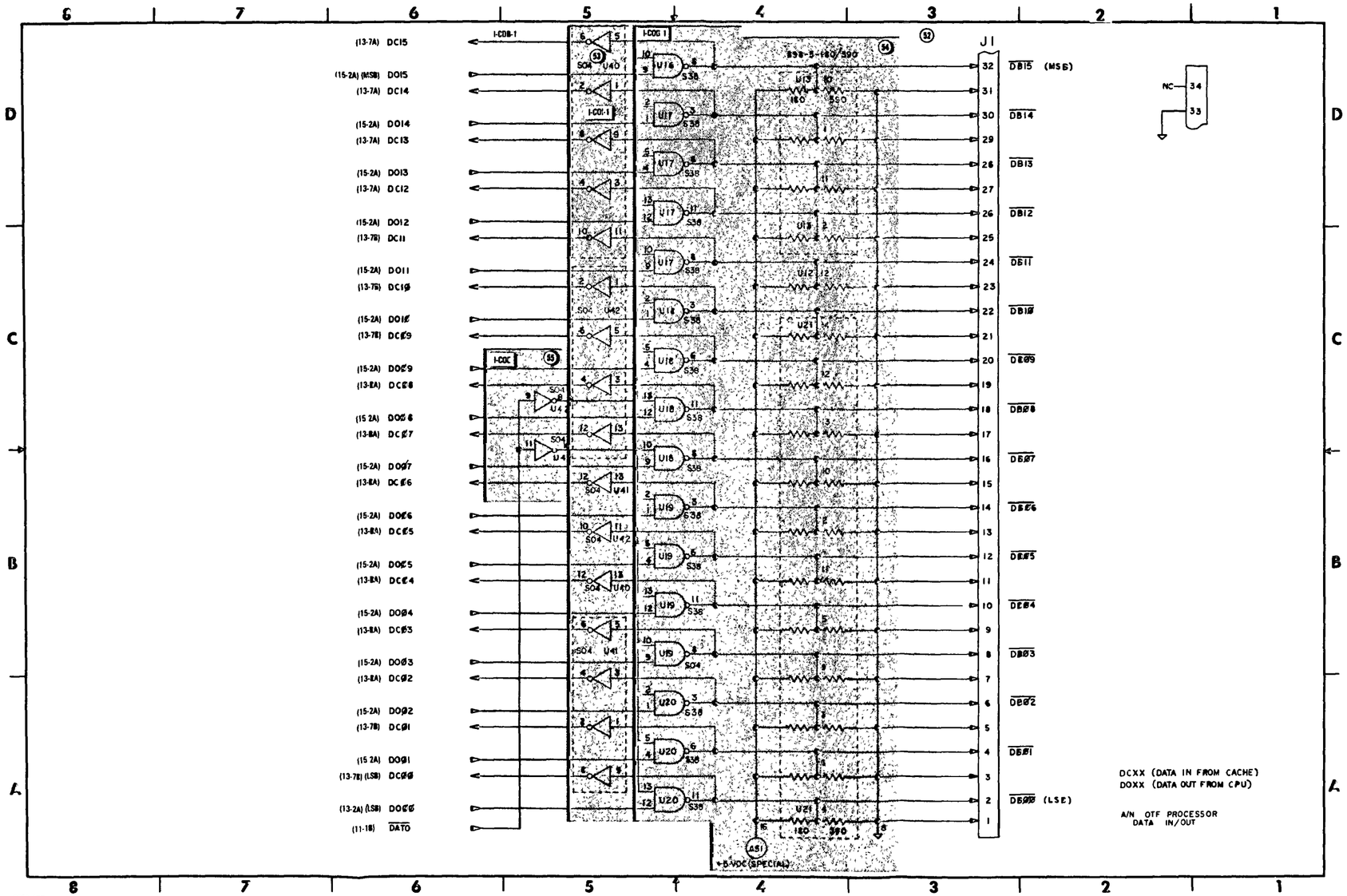

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Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 19 of 27)

(52) (I-CDB-1) CACHE IN/OUT DATA BUFFER:

ALLOWS DATA TO BE TRANSFERRED FROM LSI-11/23 TO QUAD CACHE OR FROM QUAD CACHE TO LSI-11/23.

(53) (I-COI-1) CACHE OUTPUT INVERTERS:

ACCEPTS 16-BIT DATA OUTPUT FROM QUAD CACHE (DB 00-15). INVERTS AND BUFFERS DATA BITS AND OUTPUTS DATA TO I-CIR-1 (CACHE INPUT DATA REGISTER) WHERE DATA IS MADE READY FOR OUTPUT TO LSI-11/23.

(54) (I-COB-1) CPU OUTPUT BUFFERS:

BUFFERS AND INVERTS 16-BIT DATA OUTPUT FROM LSI-11/23 WHEN ENABLED BY I-COE-1 (CPU OUTPUT ENABLE) CIRCUIT. OPEN COLLECTOR LOGIC IS USED SO OUTPUT IS DISABLED UNLESS I-COE-1 ENABLES IT. RESISTOR NETWORK TIED TO OUTPUTS OF NAND GATES IS USED TO PROVIDE CORRECT OUTPUT LOGIC LEVELS WITH OPEN COLLECTOR LOGIC, AND TO TERMINATE THE CABLES.

(55) (I-COE-1) CPU OUTPUT ENABLE:

ENABLES I-COB-1 (CPU OUTPUT BUFFERS) TO OUTPUT 16-BIT DATA FROM LSI-11/23 TO QUAD CACHE WHEN /DATO (/DATA OUTPUT) SIGNAL IS RECEIVED FROM I-RWC-1 (READ/WRITE CONTROL LOGIC) CIRCUIT.

Figure 2-12. A/H OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 20 of 27)

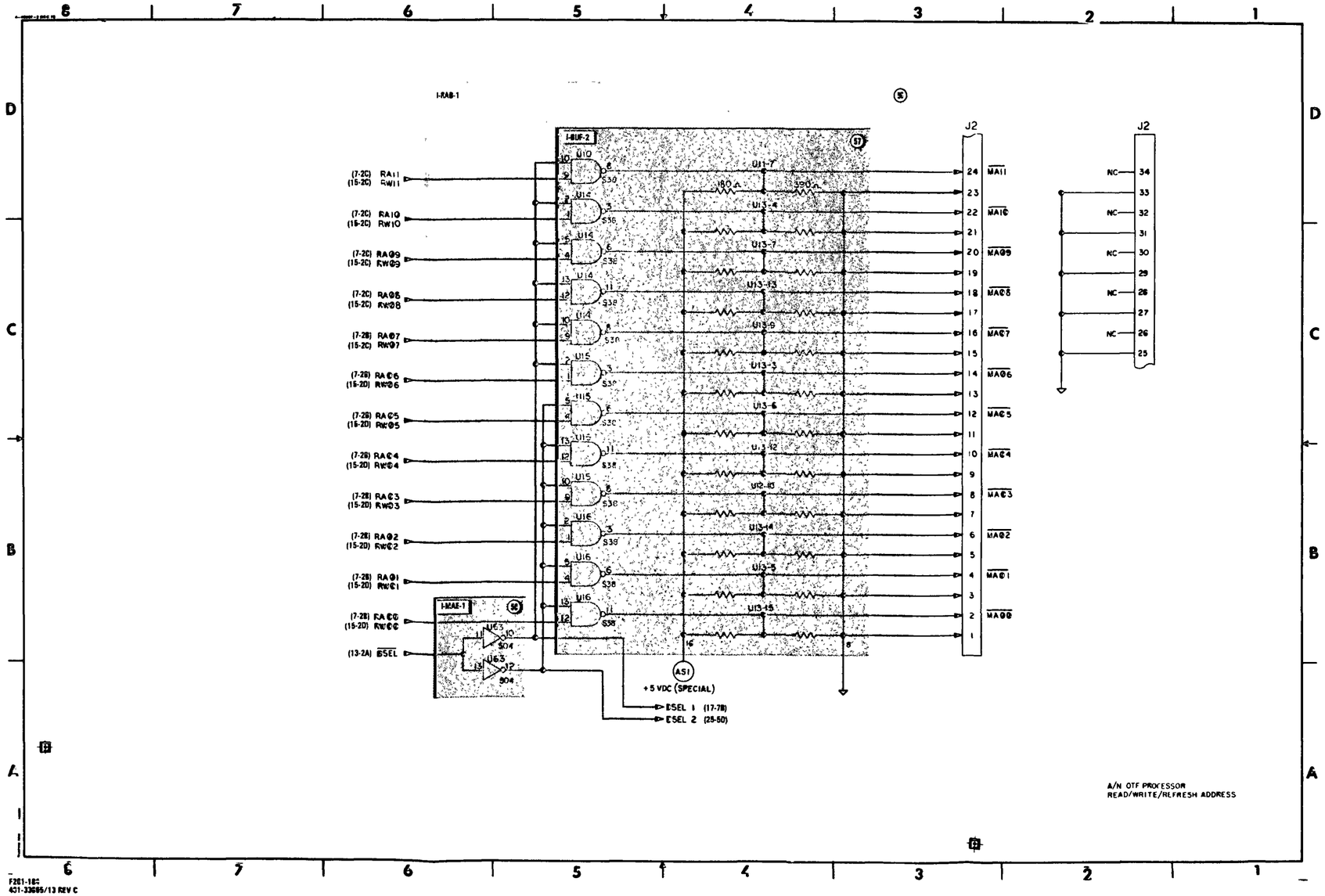

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 21 of 27)

(56) (I-RAB-1) READ/WRITE/REFRESH ADDRESS BUFFERS:

BUFFERS AND INVERTS ONE OF FOLLOWING TWO TYPES OF ADDRESSES FOR OUTPUT TO QUAD CACHE:

(1) RA00-RA11 (REFRESH ADDRESS) CONTAINS QUAD CACHE MEMORY LOCATION FOR EACH CHARACTER REFRESH. THIS 12-BIT ADDRESS IS INPUT FROM I-RAL-1 (REFRESH ADDRESS ACCUMULATOR/LATCH) WHEN REFRESH OPERATION IS DESIRED.

(2) RW00-RW11 (READ/WRITE ADDRESS) CONTAINS ADDRESS OF QUAD CACHE MEMORY READ OR WRITE LOCATION. THIS 12-BIT ADDRESS IS INPUT FROM I-CAB-1 (CACHE READ/WRITE ADDRESS BUFFERS) WHEN BUS MASTER DESIRES TO READ DATA FROM OR WRITE DATA INTO CACHE MEMORY LOCATIONS.

(57) (I-BUF-2) BUFFERS:

OPEN COLLECTOR BUFFERS WHICH INVERT AND BUFFER EITHER REFRESH ADDRESSES OR READ/WRITE ADDRESSES WHEN ENABLED BY I-MAE-1 (MEMORY ADDRESS ENABLE) CIRCUIT. RESISTOR NETWORK TIED TO OUTPUTS OF NAND GATES IS USED TO PROVIDE CORRECT OUTPUT LOGIC LEVELS WITH OPEN COLLECTOR LOGIC, AND TO TERMINATE THE CABLES.

(58) (I-MAE-1) MEMORY ADDRESS ENABLE:

ENABLES NAND GATES IN I-BUF-1 TO OUTPUT EITHER REFRESH OR READ/WRITE ADDRESSES TO QUAD CACHE WHEN /BSEL (/BOARD SELECT) IS INPUT FROM I-CSR-1 (CONTROL STATUS REGISTER). BSEL 1 (BOARD SELECT 1) AND BSEL 2 (BOARD SELECT 2) ARE ALSO OUTPUT TO ENABLE OTHER CIRCUITS WITHIN OTF PROCESSOR WHEN PROCESSOR IS SELECTED BY CONTROL STATUS REGISTER.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 22 of 27)

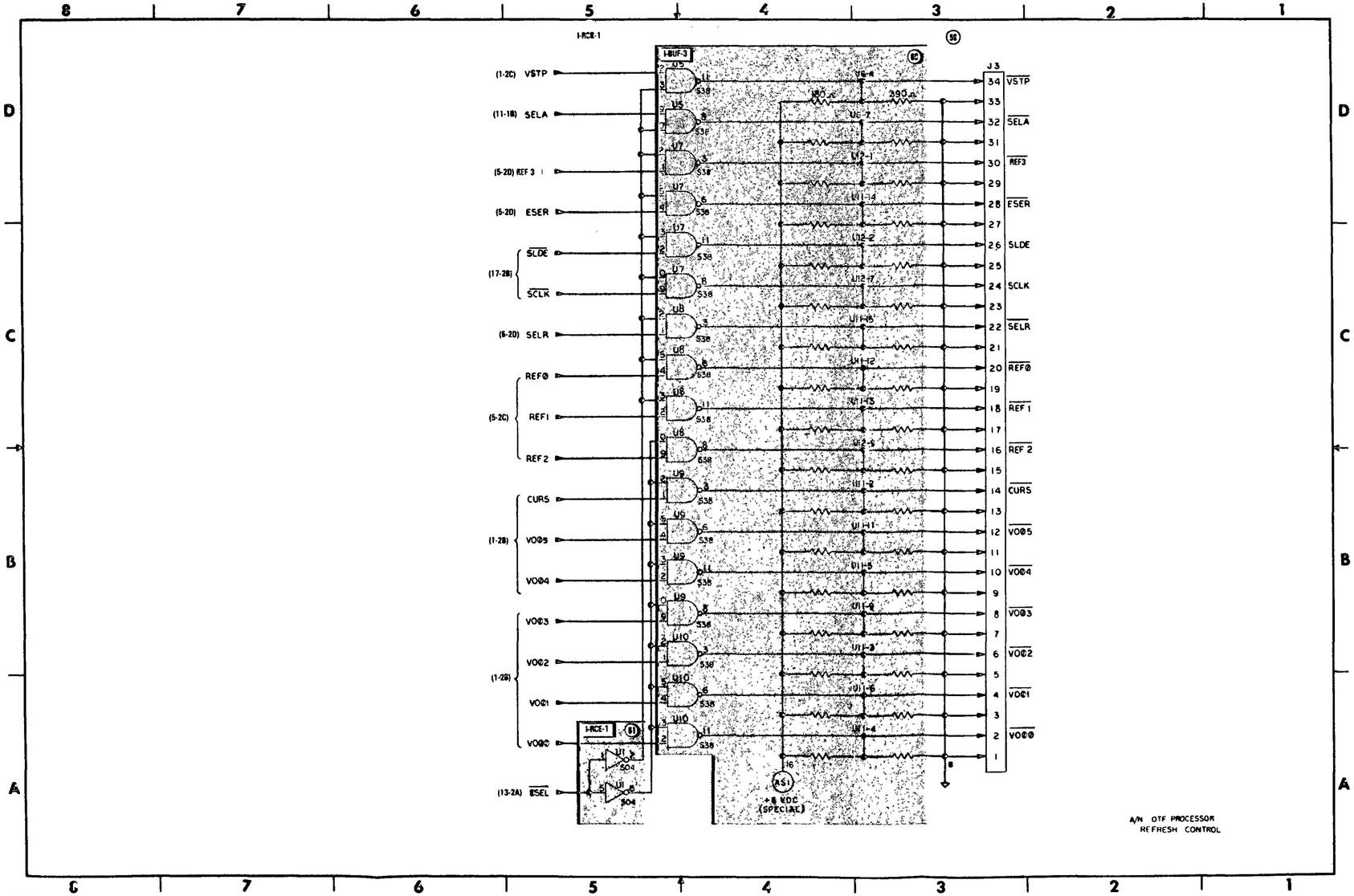

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 23 of 27)

(59) (I-RCB-1) REFRESH CONTROL BUFFER:

BUFFERS AND INVERTS FOLLOWING REFRESH CONTROL SIGNALS AND OUTPUTS SIGNALS TO QUAD CACHE WHEN ENABLED BY I-RCE-1 (REFRESH CONTROL ENABLE) CIRCUIT:

(1) VSTP (VERTICAL START TEST POINT)
(2) SELA (SELECT ADDRESS)
(3) REF 0-3 (REFRESH 0-3)
(4) ESER (ENABLE SERIALIZER)
(5) /SLDE (/SHIFT LOAD)
(6) /SCLK (/SHIFT CLOCK)
(7) SELR (SELECT REFRESH)
(8) CURS (CURSOR)
(9) VO00-05 (VERTICAL OFFSET 00-05)

(60) (I-BUF-2) BUFFERS:

OPEN COLLECTOR BUFFERS WHICH INVERT AND BUFFER REFRESH CONTROL SIGNALS FROM OTF PROCESSOR TO QUAD CACHE. NAND GATES ARE ENABLED BY I-RCE-1 (REFRESH CONTROL ENABLE) CIRCUIT.

(61) (I-RCE-1) REFRESH CONTROL ENABLE:

ENABLES I-RCB-1 (REFRESH CONTROL BUFFERS) TO OUTPUT REFRESH CONTROL SIGNALS FROM OTF PROCESSOR TO QUAD CACHE WHEN /BSEL (/BOARD SELECT) SIGNAL FROM I-CSR-1 (CONTROL STATUS REGISTER) IS AT LOGIC LOW LEVEL SIGNIFYING THAT OTF PROCESSOR HAS BEEN SELECTED.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 24 of 27)

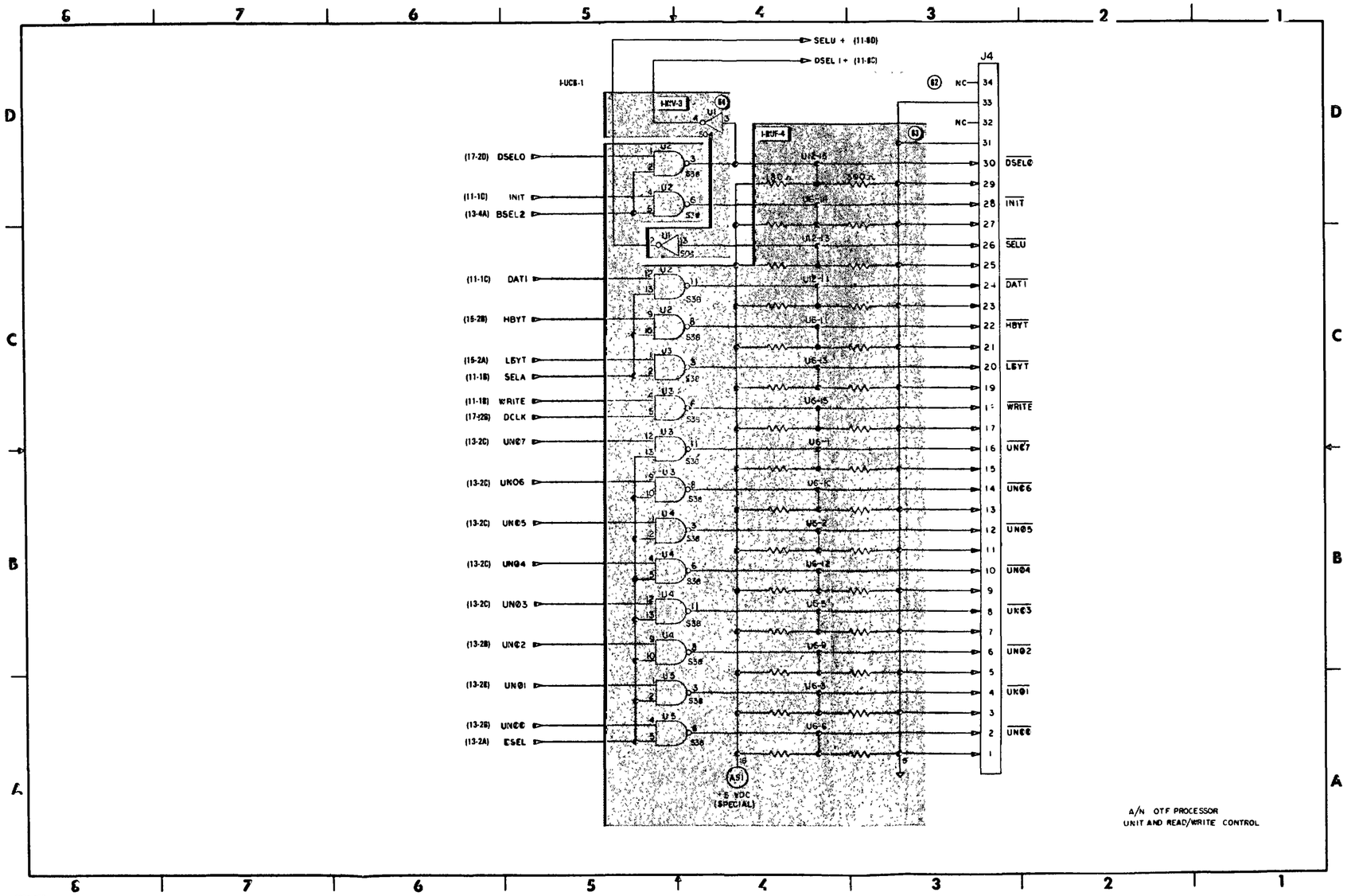

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 25 of 27)

(62) (I-UCB-1) UNIT AND READ/WRITE CONTROL BUFFER:

(1) BUFFERS AND INVERTS UNIT NUMBER DATA (UN00-07) FROM CONTROL STATUS REGISTER (I-CSR-1) AND OUTPUTS UNIT NUMBER DATA TO QUAD CACHE WHEN ENABLED BY BSEL (BOARD SELECT) SIGNAL FROM I-CSR-1.
(2) BUFFERS AND INVERTS DESELO (DESELECT OUT) AND INIT (INITIALIZE) WHEN BSEL 2 (BOARD SELECT 2) IS AT AN ACTIVE HIGH.
(3) BUFFERS AND INVERTS DATI (DATA IN), HBYT (HIGH BYTE), AND LBYT (LOW BYTE) WHEN ENABLED BY SELA (SELECT ADDRESS) SIGNAL FROM I-RWC-1 (READ/WRITE CONTROL LOGIC).
(4) BUFFERS AND INVERTS WRITE SIGNAL WHEN ENABLED BY DCLK (DELAYED CLOCK) SIGNAL FROM I-OTL-1 (OSCILLATOR TIMING LOGIC).

(63) (I-BUF-4) BUFFERS:

BUFFERS AND INVERTS UNIT AND READ/WRITE CONTROL SIGNALS FROM OTF PROCESSOR TO QUAD CACHE. ENABLE SIGNALS USED TO ENABLE OPEN COLLECTOR NAND GATES INCLUDE BSEL, DCLK, SELA, AND BSEL 2. RESISTOR NETWORK TIED TO OUTPUTS OF NAND GATES IS USED TO PROVIDE CORRECT OUTPUT LOGIC LEVELS WITH OPEN COLLECTOR LOGIC, AND TERMINATE CABLES.

(64) (I-INV-3) INVERTERS:

(1) INVERTS /DESELO (/DESELECT OUT) AND INPUTS DSELO (DESELECT OUT) TO OTF PROCESSOR TO PROVIDE DESELECTING OF OTF PROCESSOR WHEN NOT DESIRED FOR USE BY LSI-11/23.

(2) INVERTS /SELU (/SELECT UNIT) SIGNAL FROM QUAD CACHE WHICH INFORMS OTF PROCESSOR THAT UNIT NUMBER (CRT MONITOR) HAS BEEN ENABLED BY QUAD CACHE.

Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 26 of 27)

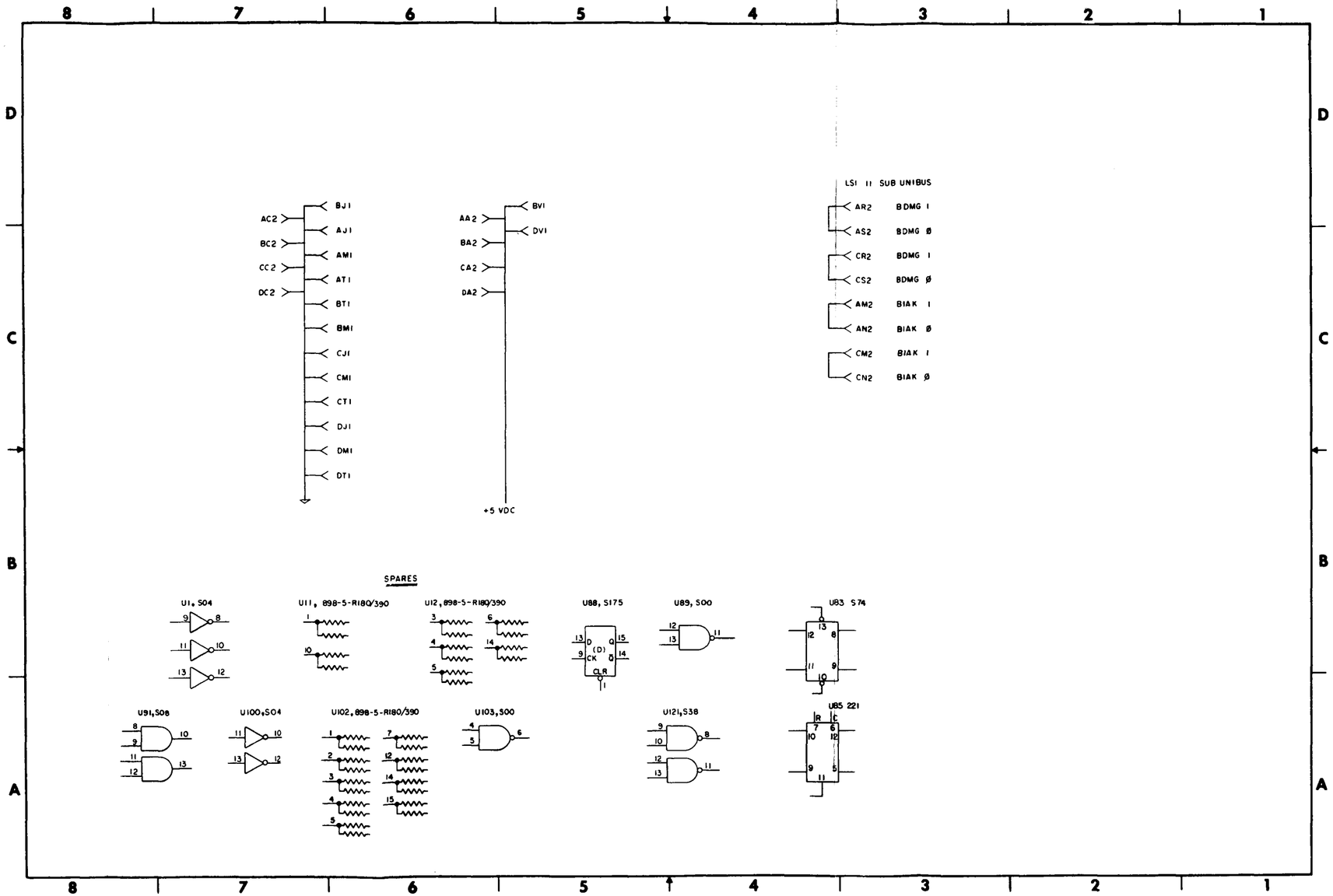

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Figure 2-12. A/N OTF Processor Blocked Schematic Diagram and Keyed Text (Sheet 27 of 27)

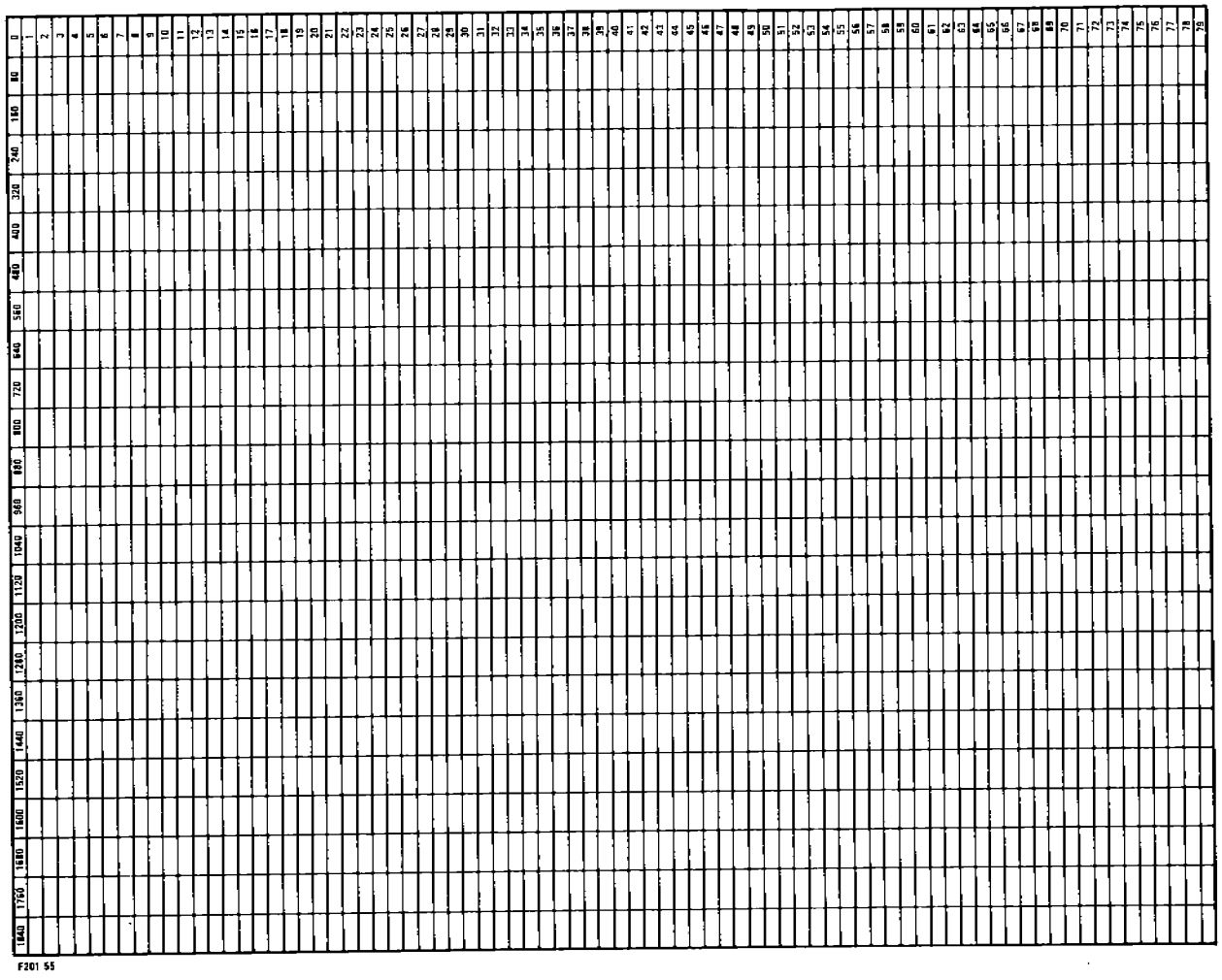

Figure 2-11. CRT Monitor Character Positions

Table 2-6. Data Bits Assignments

BIT NUMBER	PURPOSE
0 (low byte)	ASCII bit 0
1	ASCII bit 1
2	ASCII bit 2
3	ASCII bit 3
4	ASCII bit 4
5	ASCII bit 5
6	ASCII bit 6
7	Used to cause a symbol fill to take place. The symbol selected by bits 0 through 6 will be automatically written into low bank cache memory up to and including the location where an end of field (stop) bit is encountered.
8 (high-byte)	Used to emphasize the symbol presentation. If bit 8 = 1, the symbol will be emphasized.
9	Used to blink the symbol presentation. If bit 9 = 1, the symbol will blink.
10	Used to reverse the video presentation. If bit 10 = 1, the symbol will be presented with the symbol and background video reversed.
11	Used as a background control. If bit 11 = 1, half intensity is displayed.
12	Used as a cursor (underscore) control. If bit 12 = 1, the symbol position will be underscored.

Table 2-6. Data Bits Assignments (Continued)

BIT NUMBER	PURPOSE
13	Used as a switch for bits 8 through 10. If bit 13 = 0, video attributes will be written or read.
14	Used to fix an end of field. Used to stop a fill operation. If bit 14 = 1, the fill operation will stop.
15	Used to cause an attribute fill to take place. The attributes selected by bits 8 through 13 will be automatically written in the high byte cache memory up to and including the location where an end of field (stop) bit is encountered.

The Cache In/Out Data Buffer (I-CDB-1) outputs data to and receives data from the A/N quad cache memory circuit card. This data consists of symbol and attribute information (DATA BIT 00-15).

Figure 2-12 provides a blocked schematic diagram with keyed text describing the operation of the A/N OTF processor circuit card.

2.1.1.3.14 Alphanumeric (A/N) Quad Cache Memory Circuit Card.

An intermediate logic diagram for the A/N quad cache memory circuit card is shown in figure 2-13. Each block on the intermediate logic diagram contains a circuit identifier code in the upper left-hand corner and a circled, keyed text reference number in the upper right-hand corner of the block. These identifier codes and keyed text reference numbers refer to the blocked schematic diagrams given in figure 2-14.

The A/N quad cache memory circuit card receives 16 bits of data from the A/N OTF processor circuit card. Table 2-6 gives the assignments for each of these bits. These received data bits are applied to a data buffer and are output to various sections of the A/N quad cache circuit card as DATA OUT bits. DATA OUT 00-06 bits are applied to the cache memory low bank for storage of ASCII characters in RAM. DATA OUT 08-12 and 14 bits are applied to the cache memory high bank for storage of attributes in RAM. DATA OUT 07 and 15 bits are not connected on this card because the attribute and symbol fill operations are performed on the A/N OTF processor circuit card. DATA OUT inputs are sent back to the LSI-11/23 bus via the A/N quad cache memory circuit card as /MEMORY ADDRESS 00-11 bits. These bits are applied to both the low and high bank cache memories where the particular memory location for a symbol and its associated attributes are stored.

Control signals from the A/N OTF processor circuit card are applied to the Refresh Control Buffer (I-RCB-1) and the Unit Read/Write Control Buffer (I-UCB-1). These signals are routed throughout the board to control refresh operations and memory reads and writes.

UNIT NUMBER 00-07 signals are sent from the A/N OTF processor circuit card to the RAM select circuit on the A/N quad cache memory circuit card. The RAM select circuit uses a PROM (programmable read only memory) to decode the UNIT NUMBER 00-07 signals to determine which of up to eight CRT monitors is desired. A /SELECT MEMORY signal is output to the high and low bank cache memories if they correspond to the desired CRT monitors. This enables the cache memories. The MEMORY ADDRESS 12 and 13 signals are output by the PROM and associated logic circuits to select the desired area of RAM in the cache memories dedicated to the desired CRT monitor.

The cache memory low bank and high bank outputs stored ASCII character (symbol) data and attribute data to the Symbol/Attribute Latch (I-SAL-1). The symbol data is output to the Character PROM (I-CHP-1) as REFRESH DATA 00-06. The character PROM converts this

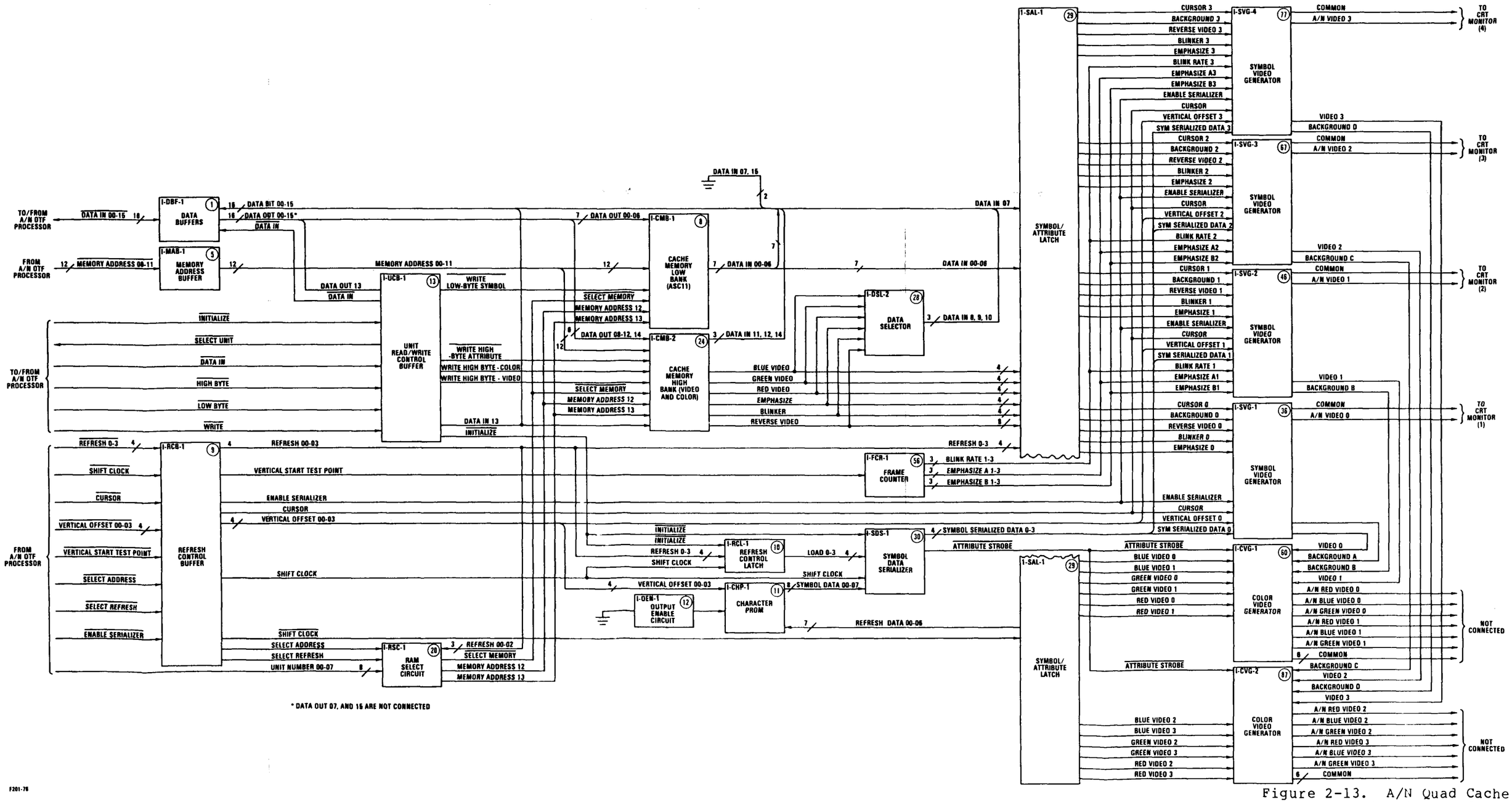

Figure 2-13. A/N Quad Cache Memory Circuit Board Intermediate Logic Diagram

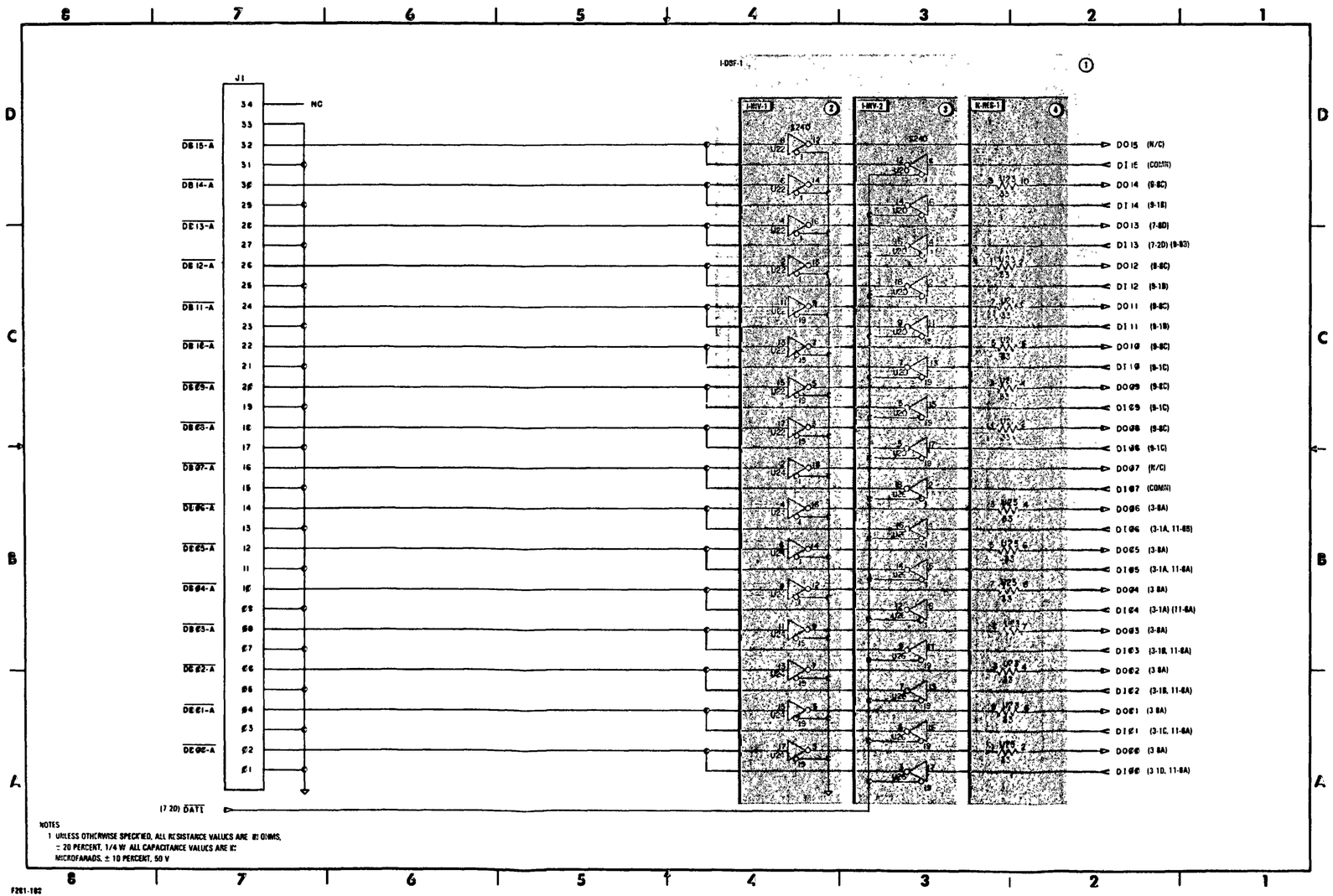

Figure 2-14. A/N Quad Cache Blocked Schematic Diagram and Keyed Text (Sheet 1 of 24)